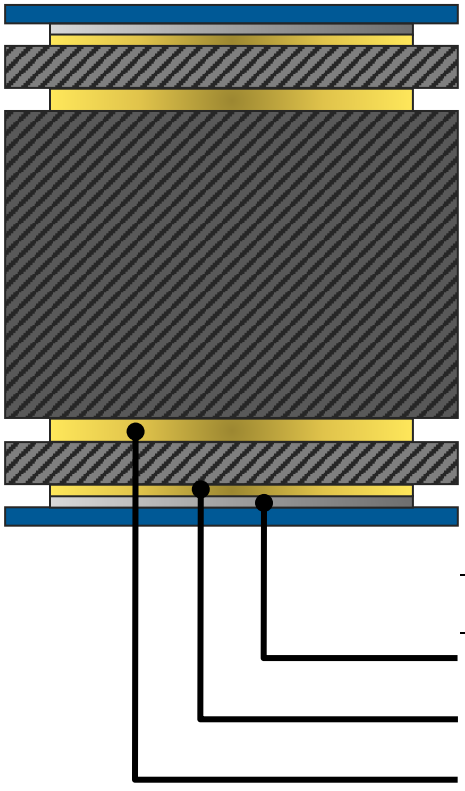
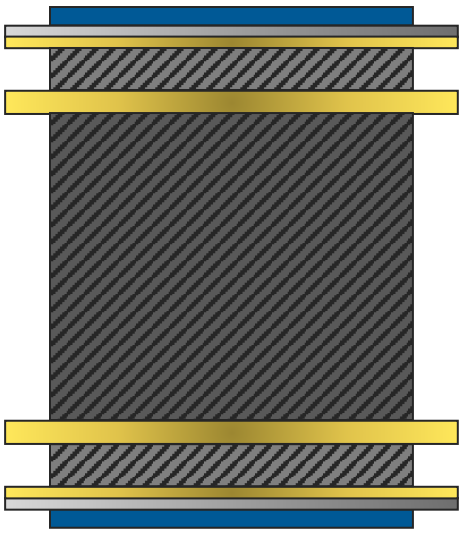
1 PCB Stackup

1.1 Stackup



Type	Material	Height [µm]	Dk	Df
Mask	–	15	3.5	–
Prepreg	FR-4	70	4.2	0.02
Core	FR-4	500	4.5	0.02
Prepreg	FR-4	70	4.2	0.02
Mask	–	15	3.5	–

Type	Material	Height [µm]	Weight [oz]
Finish	HASL-Pb Free	18	1/2
Cond	Cu	18	1/2
Cond	Cu	35	1



1.2 Layer Stack in Altium Designer 20

#	Name	Material	Type	Weight	Thickness	Dk	Df	Process
	Top Overlay		Overlay					
	Top Solder Mask	Solder Resist	Solder Mask		0.015mm	3.5		
	Top Surface Finish	Lead-Free	Surface Finish		0.018mm			HASL Lead-...
1	Top Layer		Signal	1/2oz	0.018mm			
	Top Prepreg	FR-4	Prepreg		0.07mm	4.2	0.02	
2	Mid-Layer 1		Signal	1oz	0.035mm			
	Core	FR-4	Core		0.488mm	4.5	0.02	
3	Mid-Layer 2		Signal	1oz	0.035mm			
	Bottom Prepreg	FR-4	Prepreg		0.07mm	4.2	0.02	
4	Bottom Layer		Signal	1/2oz	0.018mm			
	Bottom Surface Finish	Lead-Free	Surface Finish		0.018mm			HASL Lead-...
	Bottom Solder Mask	Solder Resist	Solder Mask		0.015mm	3.5		
	Bottom Overlay		Overlay					

Figure 1: The Layer Stack of the PCB in Altium Designer 20.

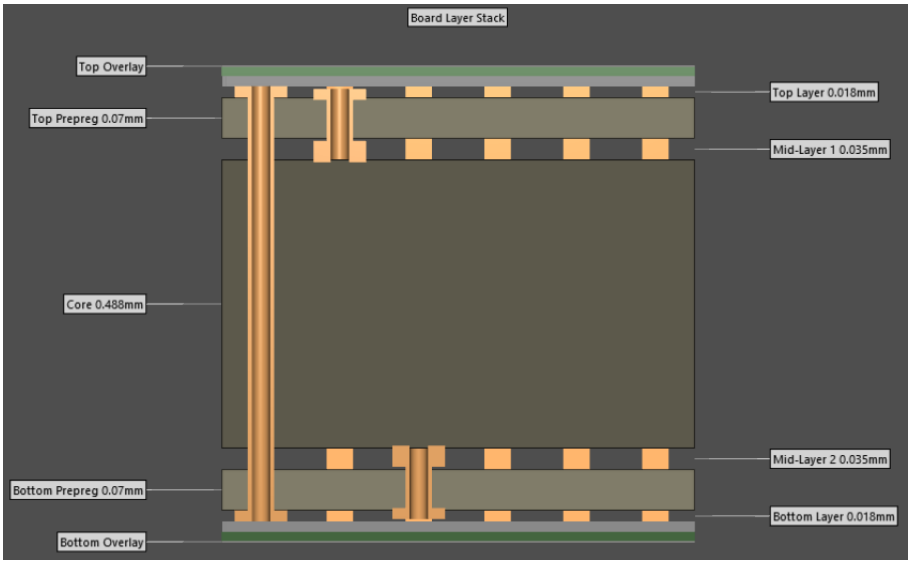


Figure 2: The Board Layer Stack, with real relative layer heights.

The total PCB thickness is approximately $0.8\ \mathrm{mm}$.

1.3 Impedance Calculations

The transmission lines in the RF front end are grounded coplanar waveguides (GCPWs), which require a bottom ground plane in addition to coplanar ground planes. Simulations of the transmission lines are necessary to obtain a characteristic impedance of

$$Z_0 = 50\ \Omega,$$

However, this is very challenging when embedding GCPWs on very small PCBs as the *nRF9160 Tracker*. It is important to have in mind that Z_0 is dispersive and depends on the effective permittivity $\varepsilon_{\mathrm{eff}}$, which satisfies

$$1 \leq \varepsilon_{\mathrm{eff}} \leq \varepsilon_r.$$

Only the upper layer pair is used in the nRF9160 Tracker, thus, the GCPWs for the LTE and the GPS circuitry only depend on the prepreg layer height and not the PCB core.

Altium Designer 20 can compute the characteristic impedance (in the Layer Stack Manager). It incorporates the solder mask layer and optionally, the surface finish layer in its calculation.

Free calculators like *AppCAD Design Assistant* or *Saturn PCB Toolkit* can also be used to calculate the characteristic line impedance Z_0, as well as the effective permittivity ε_{eff}. However, values from these calculators do not take surface finish and solder mask into account, unlike Altium Designer 20. A comparison of calculated transmission line values on the nRF9160 Tracker is presented in table 1, when the clearance, the dielectric thickness and the relative permittivity, respectively are:

$$S = 200\ \mu\text{m},$$
$$t = 70\ \mu\text{m},$$
$$\varepsilon_r = 4.2.$$

Table 1: Comparison of calculated transmission line values in Altium and AppCAD.

		Altium	AppCAD
Impedance	$Z_0\ [\Omega]$	50.0	51.0
Delay	$T_p\ [\text{ns/m}]$	6.08	5.46
Line Width	$W\ [\mu\text{m}]$	102	150

The AppCAD line width value of $W = 150\ \mu\text{m}$ is used in nRF9160 Tracker v0.1.2.