

1. Description

1.1. Project

Project Name	test2_10_2
Board Name	custom
Generated with:	STM32CubeMX 6.12.1
Date	10/02/2024

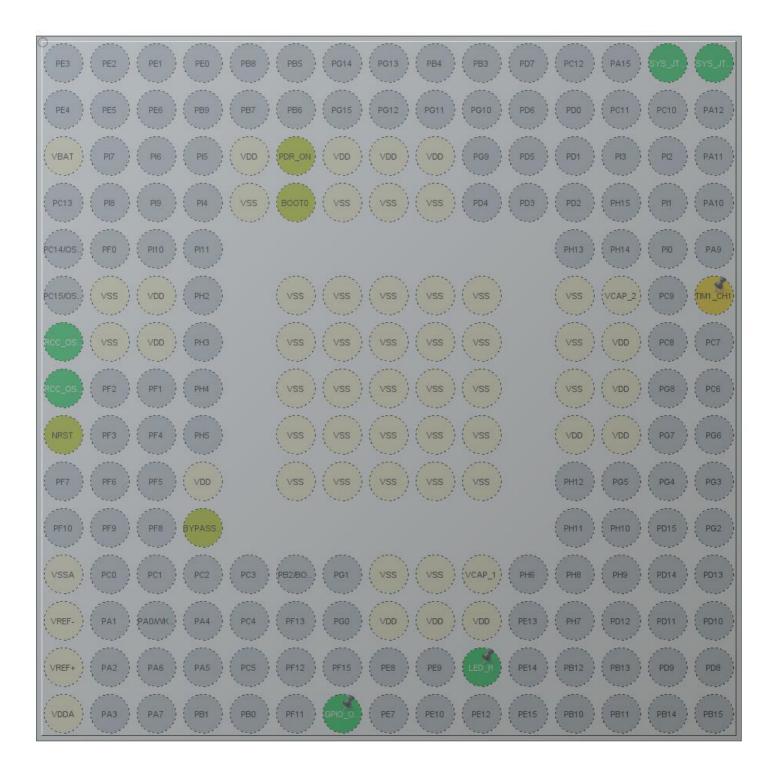
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F427IIHx
MCU Package	UFBGA176
MCU Pin number	201

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

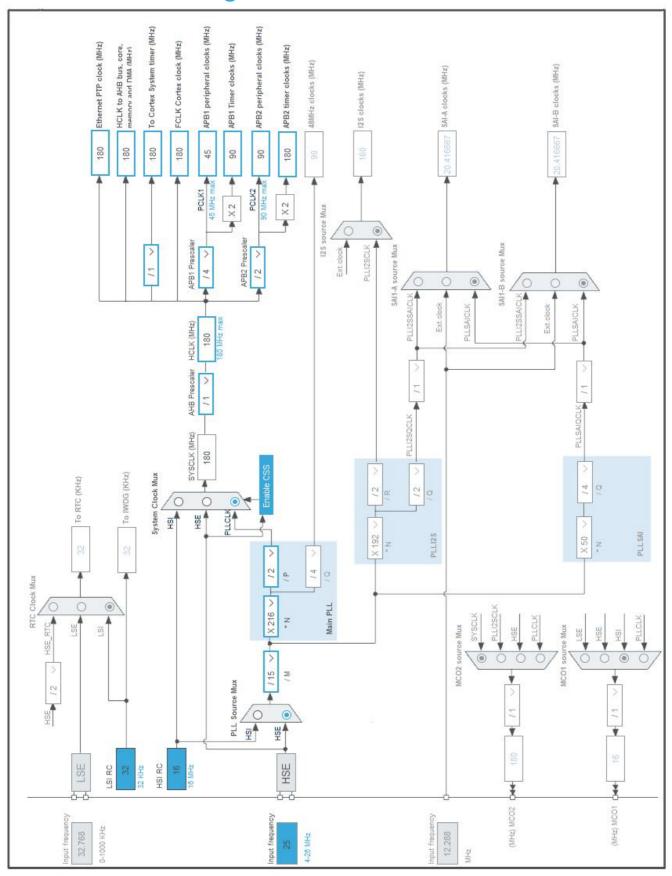
Pin Number	Pin Name	Pin Type	Alternate	Label
UFBGA176	(function after		Function(s)	
	reset)			
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
C1	VBAT	Power		
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDD	Power		
C9	VDD	Power		
D5	VSS	Power		
D6	воото	Boot		
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
F2	VSS	Power		
F3	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP_2	Power		
F15	PA8 *	I/O	TIM1_CH1	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H6	VSS	Power		
H7	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VSS	Power		
H13	VDD	Power		
J1	NRST	Reset		
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	VDD	Power		
J13	VDD	Power		
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
L4	BYPASS_REG	Reset		
M1	VSSA	Power		
M8	VSS	Power		
M9	VSS	Power		
M10	VCAP_1	Power		
N1	VREF-	Power		
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		
P1	VREF+	Power		
P10	PE11 **	I/O	GPIO_Output	LED_R
R1	VDDA	Power		
R7	PF14 **	I/O	GPIO_Output	

^{**} The pin is affected with an I/O function

^{*} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



Page 5

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
мси	STM32F427IIHx
Datasheet	DS9405_Rev9

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

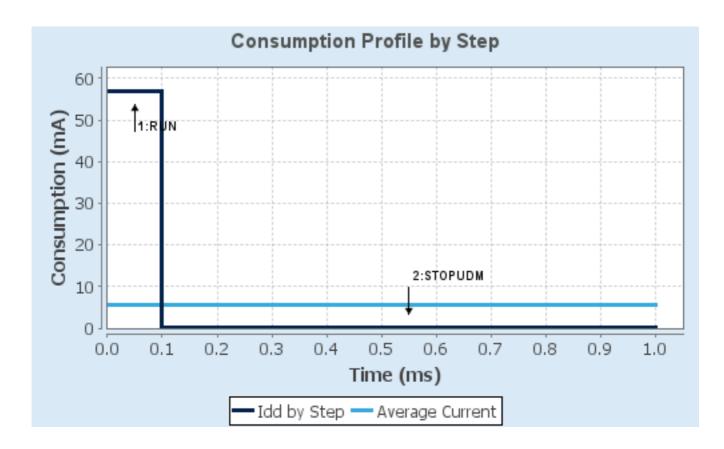
1.4. Sequence

C4am	Ct 4	Ct O
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.66	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	test2_10_2
Project Folder	D:\code\stm\test2_10_2
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name		
1	SystemClock_Config	RCC		
2	MX_GPIO_Init	GPIO		
3	MX TIM2 Init	TIM2		

3. Peripherals and Middlewares Configuration

3.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Power Over Drive Enabled

3.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.3. TIM2

Clock Source: Internal Clock

3.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Ur

Counter Period (AutoReload Register - 32 bits value) 4294967295
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

test2_	_10_	_2	Pro	ject
Configu	ıratio	on	Re	port

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0/OSC_I N	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
Single Mapped Signals	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_R
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	15	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
TIM2 global interrupt		unused			
FPU global interrupt		unused			

4.3.2. NVIC Code generation

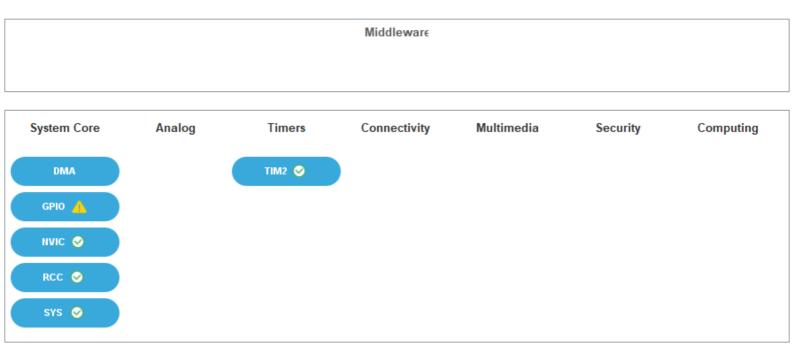
Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordering	Handlei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

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439_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f427-437_429-

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System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

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