

Diploma Thesis

**Software Defined
S-Band Ground Station Transceiver
for Satellite Communications**

under the supervision of

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*“Do not go where the path may lead,
go instead where there is no path and leave a trail.”*
Ralph Waldo Emerson

Abstract

Satellite communications meant, in the last few decades, a reliably outstanding technical advance in different fields such as physics, astrophysics, geography, electronics and communications. It became the most significant tool to ease human scientific research for both Earth and deep space, whereas it is still giving support to current commercial services.

The current project deals with the design and construction of a ground station at the Institute of Telecommunications at the Vienna University of Technology which should handle three different low Earth orbiting satellite missions: MOST, COROT and BRITE constellation. They are aimed at the research in the scientific areas of the physics, asteroseismology and communications. Communication is performed at S-band frequencies (2.00 - 2.45 GHz), UHF (435 - 438 MHz) and VHF (144 - 146 MHz).

This thesis is focused on the design and characterization of a front-end for this ground station by means of Software Defined Radio, using an USRP1 by Ettus as the main hardware component for up- and downconversion and analog-digital conversion. The digital output is treated by the software tool GNU Radio. Paying special attention to the hardware employed and the modulation and demodulation block's performance at the graphical software interface, a detailed study of the complete system is carried out and the fundamentals for the prospective adaptation procedure for both hardware and software blocks to the final project mission requirements, are consequently determined.

Resumen

En las últimas décadas, las comunicaciones por satélite han supuesto un gran avance técnico fiable en sectores como la física, astrofísica, geografía, electrónica y comunicaciones; llegando así a ser una herramienta importante que facilita el desarrollo científico tanto en la Tierra como en el espacio, a la vez que prestan otros servicios comerciales del día a día.

El proyecto que se está llevando a cabo, está centrado en el diseño y construcción de una estación terrestre en el Instituto de Telecomunicación de la Universidad Técnica de Viena, la cual soportará tres misiones de satélites LEO: MOST,

COROT y la constelación BRITE. Mediante enlaces en banda S (2.00 - 2.45 GHz), UHF (435 - 438 MHz) y VHF (144 - 146 MHz), el objetivo final de esta comunicación es la investigación científico-educacional en el área de la física, asteroseismología y de las comunicaciones.

Concretamente esta tesis se centra en el diseño y caracterización del terminal de dicha estación terrestre a través de Software Defined Radio, usando una USRP1 como hardware básico para la conversión en frecuencia y para la conversión analógico-digital. La salida digital es tratada a través de una herramienta software propiedad de GNU Radio. Prestando especial atención a los componentes del hardware y al funcionamiento de los bloques de modulación y demodulación en la interfaz gráfica del software empleado, se lleva a cabo un estudio detallado del sistema completo, determinando así, las bases fundamentales para el posterior proceso de adaptación tanto de software como hardware para así satisfacer los requisitos establecidos por los satélites de dicho proyecto.

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Chapter 1

Introduction

Since the Second World War II very different technologies were expanded, like missiles and microwaves. And the combination of both of them brought to life a new era, the era of a new form of communication, complementing the already existing ground radio-cabled networks, providing bigger ranges, capacities and access to areas that would not be possible by any other technology. Satellite communications era started with the launching of the Soviet Sputnik I, the first artificial satellite working on 20.005 and 40.002 MHz, on October 4, 1957. Then, in 1962, AT&T launched Telstar, the world's first true communications satellite. After that, innumerable satellites have been set into orbit supporting any kind of applications [1].

The use of satellites came up to fulfill the need of encountering difficulties due to the congestion and low reliability on long distance cable networks, such as transoceanic routes, and they also provide a more advantageous communication compared to the cabled links [2]:

- they support point-to-multipoint communication;
- they handle longer links without increasing the cost of the service;
- they reach remote areas where it would be impossible to supply any service with terrestrial routes and mobile terminals such as ships, aircrafts, etc;
- they offer bigger channel capacities.

Any satellite communication is divided into space and ground segment as it can be seen in Figure 1.1. The space segment is purely constituted by the artificial satellites which are categorized depending on the orbit they are set into. Depending on the altitude, they are classified into LEO¹ satellites, MEO² satellites, etc. Regarding the trajectory described, the classification is into elliptical inclined orbit, polar orbit or circular equatorial orbit. The last type of satellites also known as GEO³ satellites, have an equatorial orbit and their speed and direction make them to be stationary relative to the Earth. But not only satellites define the space segment, but also its on-board equipment and the telemetry, tracking and control system.

¹Low Earth Orbit

²Medium Earth Orbit

³Geostationary Earth Orbit

The Earth or ground segment consists of the ground terminals and its equipment such as antennas, electronics and links to the service terrestrial networks. They can be fixed ground stations or can be mobile devices.

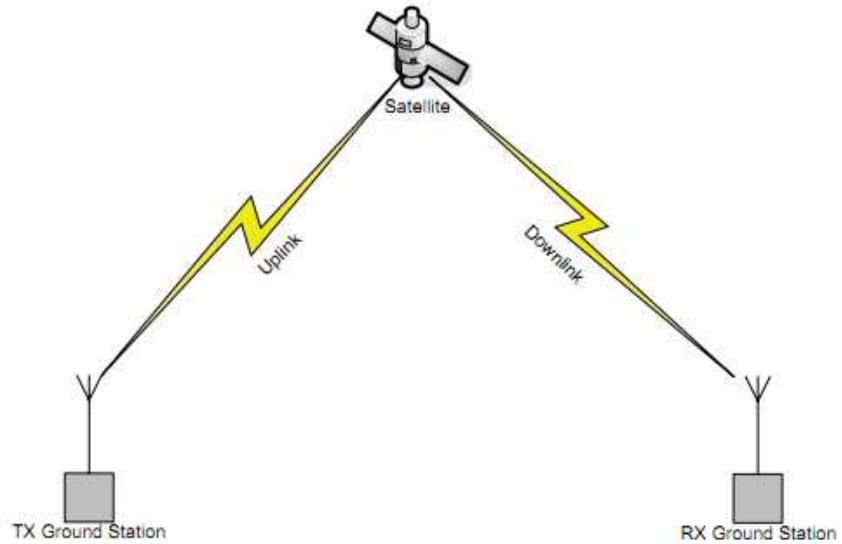


Figure 1.1: Satellite communications basic scenario [3].

This thesis describes a part of an ongoing project in satellite communications to build a ground station at the Institute of Telecommunication at the Vienna University of Technology, using a software defined radio basis. The predefined objective is to get to know the hardware in detail and get deep into the software performance of this front-end, so that a complete understanding of the system and the signal treatment can be reached and the future steps can be clarified, in order to set this front-end up and make it run for the missions considered in this project.

Hence, Chapter 2 describes the three different satellite missions – motivation of the project – with their own satellite segments parameters to which we want to finally adapt our system. The common ground segment and its main features is given in Chapter 3.

In Chapter 4, there is a detailed description of the hardware employed for the mixer, the different components on it and their functional contribution to the main goal. Meanwhile, the performance of the software running in the PC is analyzed in Chapter 5, paying special attention to the modulation and demodulation blocks.

In order to get a proper understanding of the signal behavior along the system, Chapter 6 describes the signal flow, followed by Chapter 7, where it comes to a detailed characterization of the whole system and the explanation to the encountered anomalies.

And finally, in Chapter 8, the conclusions are seen and, as a complementary

1 Introduction

work, the future steps and objectives are established, based on the research of this thesis, in order to follow up with this project and achieve the desired goals.

Chapter 2

MOST, COROT and BRITE

2.1 Missions and Motivation

Every satellite communication is held by two segments: the space segment and the Earth segment. The space segment is basically constituted by the artificial satellite constellations.

The space astronomy missions which give incentive to this project are handled in three different satellite constellations: MOST, COROT and BRITE.

MOST: Under the acronym MOST stands the project Microvariability and Oscillations of STars. It is a microsatellite space telescope mission led by the Canadian Space Agency.

The MOST satellite is a LEO satellite with an orbital period of 100 min, which handles the study of asteroseismology and its mission is to measure the brightness variations in the stars during a 60-day period, to find out the age of the stars and to discover exoplanets, in order to get to know the Universe's origin [4], [5].

Our ground station on the roof of the Electrical Engineering building of the Vienna University of Technology is planned to be one of the four ground stations working with this satellite, together with another ground station in Vienna placed at the Institute of Astronomy and two more in Canada (Vancouver and Toronto).

COROT: COnvection Rotation and planetary Transits is the name of a mission conducted by the CNES, Centre National d'Études Spatiales and ESA, European Space Agency.

Its mission consists of the search for exoplanets by detecting the stars' light fade out as the exoplanet cuts in front of the stars, and the calculation of the stars' mass, age and chemical composition by means of asteroseismology [6], [7].

The Earth segment is placed in different geographical areas around the world. Our Vienna ground station also works as a secondary station for COROT [4], [5].

BRITE: In order to explore massive luminous stars, which dominate the ecology of the Universe, by means of a precise differential photometry and

asteroseismology, the BRIght Target Explorer Constellation mission will be carried out.

A constellation of four nearly identical Austrian/Canadian LEO nanosatellites will allow a longer duty cycle of observation compared to the case of having just one satellite. These are grouped in pairs in which each satellite filters different spectral ranges, so that an spectral improvement is achieved. Different pairs of satellites are planned to be placed in different orbits [5]. It is to mention, that the first Austrian satellite TUGSAT-1/BRITE-Austria funded by the Austrian Space Program forms part of this mission [8], [9]. The communication with our ground station will be full duplex.

2.2 Project Basic Requirements

In this subsection, a list of the main parameters of the different satellite constellations which make up the space segment of this project is given [4], [5], [8], [9]. These parameters must be taken into account as requirements for our ground station design and configuration.

2.2.1 Frequency Ranges

The frequency requirements for all theses space missions which must be taken into account in our ground station are listed in Table 2.1. The three of them have an S-Band downlink, i.e. from 2.00 GHz to 2.45 GHz. Nevertheless, meanwhile MOST uplink works also at S-Band, BRITE uplink will be at UHF¹, i.e. from 435 MHz to 438 MHz.

Table 2.1: Uplink and downlink frequency values.

	MOST	COROT	BRITE	Unit
Uplink frequency f_{up}	2055	-	437	MHz
Downlink frequency f_{down}	2232	2280	2230	MHz

2.2.2 Equivalent Isotropically Radiated Power Values

The different satellite links require an specific power level for a proper communication. In Table 2.2, the power level is listed in terms of EIRP² power, i.e. as if the antenna was considered to be isotropical.

¹Ultra High Frequency

²Equivalent Isotropically Radiated Power

Table 2.2: Uplink and downlink power (EIRP) levels.

MOST _{uplink}	MOST _{downlink}	COROT	BRITE _{uplink}	BRITE _{downlink}	Unit
69.5	25	37.7	50	27	dBm
39.5	-5	7.7	20	-3	dBW
8912.5	0.32	5.85	100	0.5	W

2.2.3 Power Density

Another way to express the power requirements is as the power density. In contrast with the power level, which is the power radiated in the link bandwidth, the power density is the power per 1 Hz. These values are shown in Table 2.3.

Table 2.3: Uplink and downlink power densities.

	MOST	COROT	BRITE	Unit
Uplink EIRP P_{up}	-10.9		-25.4	dBW/Hz
Downlink EIRP P_{down}		-55.3	-60	dBW/Hz

2.2.4 Data Rate

The amount of data processed or conveyed per second for all the satellite links is shown in Table 2.4.

Table 2.4: Uplink and downlink data rates.

	MOST	COROT	BRITE	Unit
Uplink Rate R_{up}	9.6		4	kbps
Downlink Rate R_{down}	38.4	838.9	32 to 256	kbps

2.2.5 Modulation Standards

The information needs to be modulated in order to be transmitted. The modulation standards (Table 2.5) employed by the different satellite missions, which does not coincide in both uplink and downlink paths for the same satellite, can be a GFSK³, QPSK⁴ or BPSK⁵. The only difference between them lays in the parameter of the carrier signal which holds the information, i.e. the frequency for FSK⁶ or the phase for PSK⁷.

Table 2.5: Uplink and downlink modulation standards.

	MOST	COROT	BRITE
Uplink	GFSK		GFSK
Downlink	BPSK	QPSK	BPSK

2.2.6 Other Parameters

Other requirements of the three missions are the bandwidth BW and the bandwidth including the Doppler shift. In case of MOST, it uses also alternative frequencies for up- and downlink. The polarization can be linear (LP⁸) or circular, in this last case it can be right hand (RHCP⁹) or left hand circular polarization (LHCP¹⁰). All the parameters are shown in Table 2.6.

³Gaussian Frequency Shift Keying

⁴Quadrature Phase Shift Keying

⁵Binary Phase Shift Keying

⁶Frequency Shift Keying

⁷Phase Shift Keying

⁸Linear Polarization

⁹Right Handed Circular Polarization

¹⁰Left Handed Circular Polarization

Table 2.6: Other parameters of the satellite missions.

	BW ¹¹	BW + Doppler	Alternative Freq	Polarization
Unit	kHz	kHz	MHz	-
MOST _{up}	110		2045.9	RHCP
MOST _{down}			2231.6	RHCP
COROT	2000	270	-	RHCP&LHCP
BRITE _{upl}	35	35	-	LP
BRITE _{down}	500	500	-	LP

Chapter 3

Ground Station

A ground station can be defined as a group of components which performs an uplink and/or downlink path in order to establish a communication channel with a satellite. These components are basically an antenna, the element that radiates and receives the radio waves; the tracking and the rotator, that takes care of determining where the satellite is and helps the antenna to point towards it; a transmitter, which modulates, converts and amplifies the signal to be transmitted; the receiver, that takes the received signal from the satellite and demodulates it after amplifying it; and last but not least, the power supply to provide the power to make the other components work [3].

To establish a communication channel from a ground station to a satellite, information about the position and velocity of the satellite is required in order to design the ground station equipment and structure. Outgoing from the information about the MOST, COROT and BRITE missions in Chapter 2, the specifications for the needed ground station are defined [4].

This chapter will describe the Earth or ground segment of this satellite communication project.

3.1 Background Project

As a previous project, the Vienna Ground Station (VGS) was built to fulfill the MOST mission. This ground station uses separated antennas for uplink and downlink in order to mitigate crosstalk and to achieve an optimized downlink performance. At the downlink the signal is taken by a parabolic dish, while the uplink signal is radiated by a Yagi antenna group [4].

The core of the present project is located at the Institute of Telecommunications, Vienna University of Technology.

3.2 A Software Defined Ground Station

The general components of a ground station are shown in the Figure 3.1 [3].

Feeding Block [3]:

- Antenna: It sends the signal to the satellite and receives the one coming from the satellite. The antenna in our ground station is a 3.7 m dish.
- Duplexer: Element which allows to have a duplex communication using a single antenna.
- LNA¹ and power amplifier: The low-noise amplifier performs the amplification of weak received signals, and the power amplifier does the same with the transmitted signals in order to reach the power level necessary.

USRP:

- Downconverter and upconverter: These elements take care of shifting the frequency of the S-Band signal received to an IF² and viceversa for the transmitted signal. This function is done by the USRP³ (Figure 3.2), a computer-hosted hardware developed by Ettus for allowing general purpose computers to work out as a software radio, using a daughterboard (Figure 3.3) specifically design for a certain bandwidth connected to the motherboard (Figure 3.4). This element includes the digital-analog converters, ADC⁴ and DAC⁵. In general terms, it serves as digital baseband and IF section for our ground station. This device will be on greater detail in Chapter 4 [10], [11].

PC:

In contrast to other radio communication systems, this ground station is a Software Defined Radio Station, where most of the components (e.g modulator, demodulator, coder, decoder, etc.), instead of being implemented in hardware, they are performed by means of a software on a personal computer. The software development toolkit chosen for this project is GNU Radio which includes a user-friendly graphical interface called GRC⁶.

- Demodulator and modulator: To demodulate and modulate the signals at the intermediate frequency. It is usually performed by a modem.
- Decoder and coder: The coding and decoding of the signals is usually executed by a TNC⁷, a device which integrates the higher protocol layers, e.g. the AX.25 protocol [5].

The fact of using a certain open-source software instead of a dedicated TNC

²Intermediate Frequency

³Universal Software Radio Peripheral

⁴Analog-to-Digital Converter

⁵Digital-to-Analog Converter

⁶GNU Radio Companion

⁷Terminal Node Controller

Chapter 3 Ground Station

or a modem, and combined with the flexible hardware provided by Ettus permits a rapidly evolving platform for radio communication.

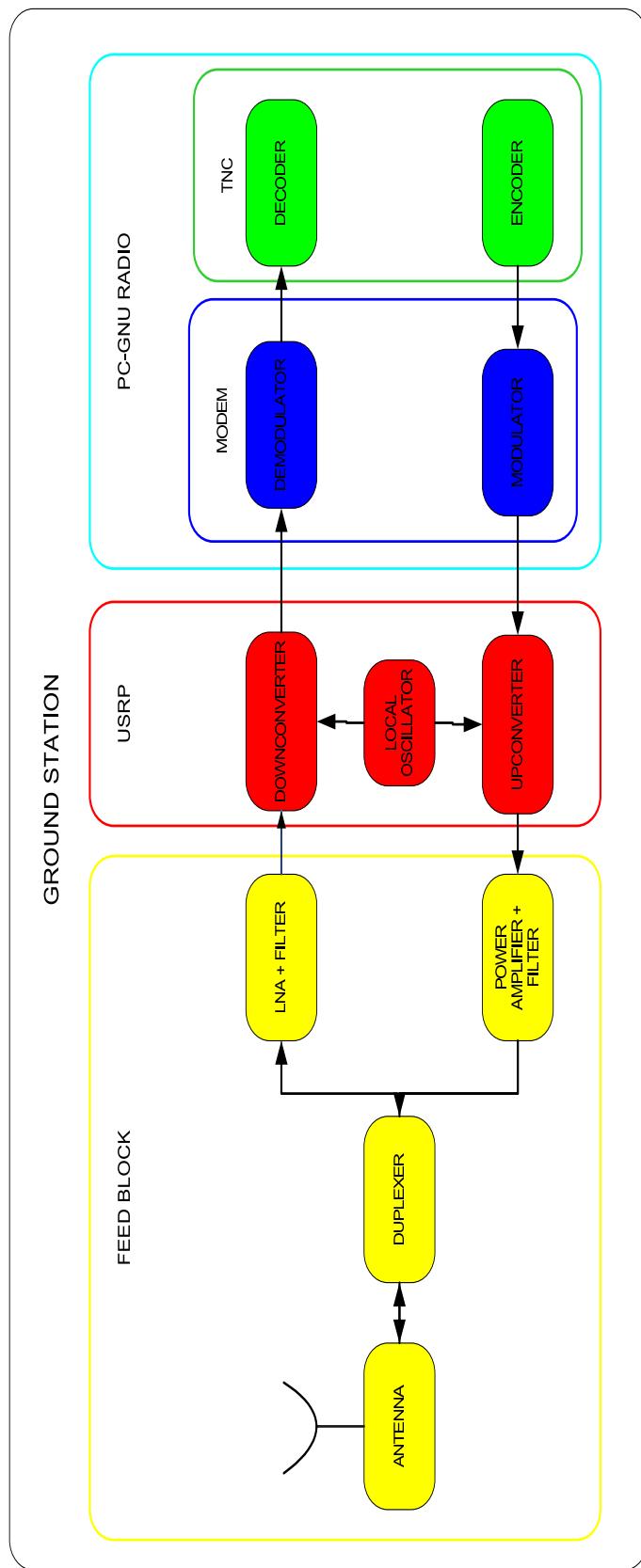


Figure 3.1: Ground station diagram.



Figure 3.2: Universal Software Radio Peripheral.

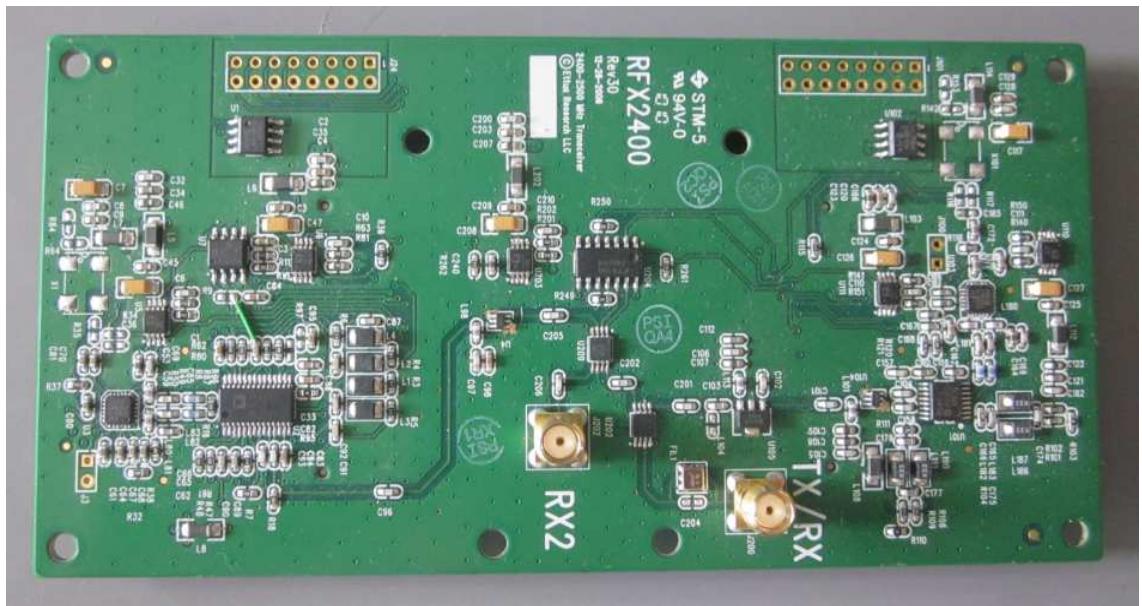


Figure 3.3: RFX2400 Daughterboard.

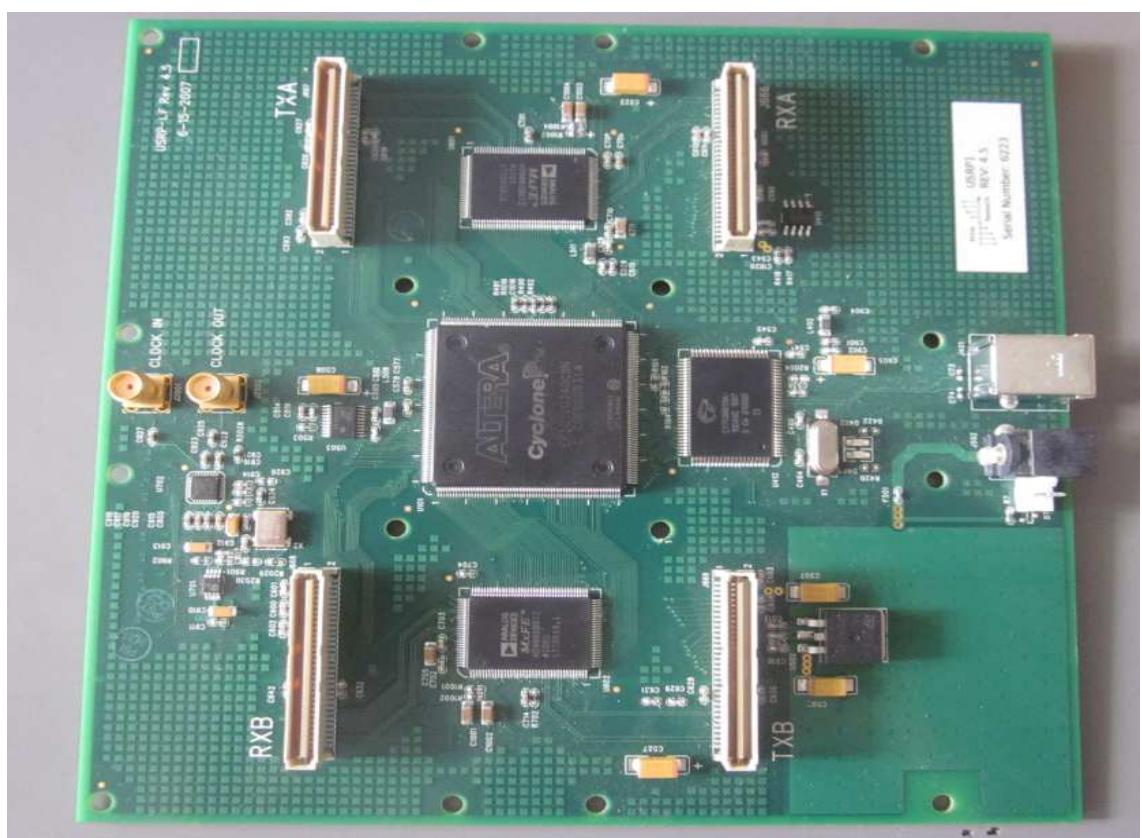


Figure 3.4: USRP1 Motherboard.

Chapter 4

Hardware

The USRP offered by Ettus Research LLC, a subsidiary of National Instruments, is a hardware – working as the digital baseband and IF section of a radio ground station – specifically designed to let simple general purpose personal computers or embedded computing devices to operate as a high bandwidth software radio. It performs the digital up and down conversion, decimation and interpolation, which are done in a high speed FPGA¹ and the frequency shifting, in a specific daughterboard depending on the application needs [11]. The intended purpose is to leave the signal processing, modulation and demodulation to be done on the host computer, that it is connected through a high-speed USB link.

4.1 Motherboard

4.1.1 Block Diagram Description

The USRP used, the version 1, has 4 high-speed ADCs, each of them sampling at 64 Msamples/s and generating 12 bits/sample. There are also 4 DACs, working at 128 Msamples/s and 14 bits/sample. Those are also the 4 inputs and 4 outputs to an Altera Cyclone EPIC12 FPGA [12]. The FPGA is connected to the Cypress FX2 USB² Controller in order to connect through a high-speed USB 2.0 interface with the computer [11]. The Figure 4.1 presents a block diagram of the motherboard of the USRP 1, and it is to say that the blue arrows represent the flux of data between the elements and the red ones the control signalling or auxiliary channels.

For the reception path, the received analog data comes from the daughterboards where it was downconverted in frequency to IF and then it is converted to digital domain in order to get into the FPGA and as the last step to leave the USRP through the USB interface. On the other hand, for the transmission path, the digital signal coming from the computer gets into the FPGA and then the analog signal is constructed and it is shifted up in frequency in the daughterboards in order to be radiated. The performance of the different blocks will be explained in the following sections [11], [13].

¹Field Programmable Gate Array

²Universal Serial Bus

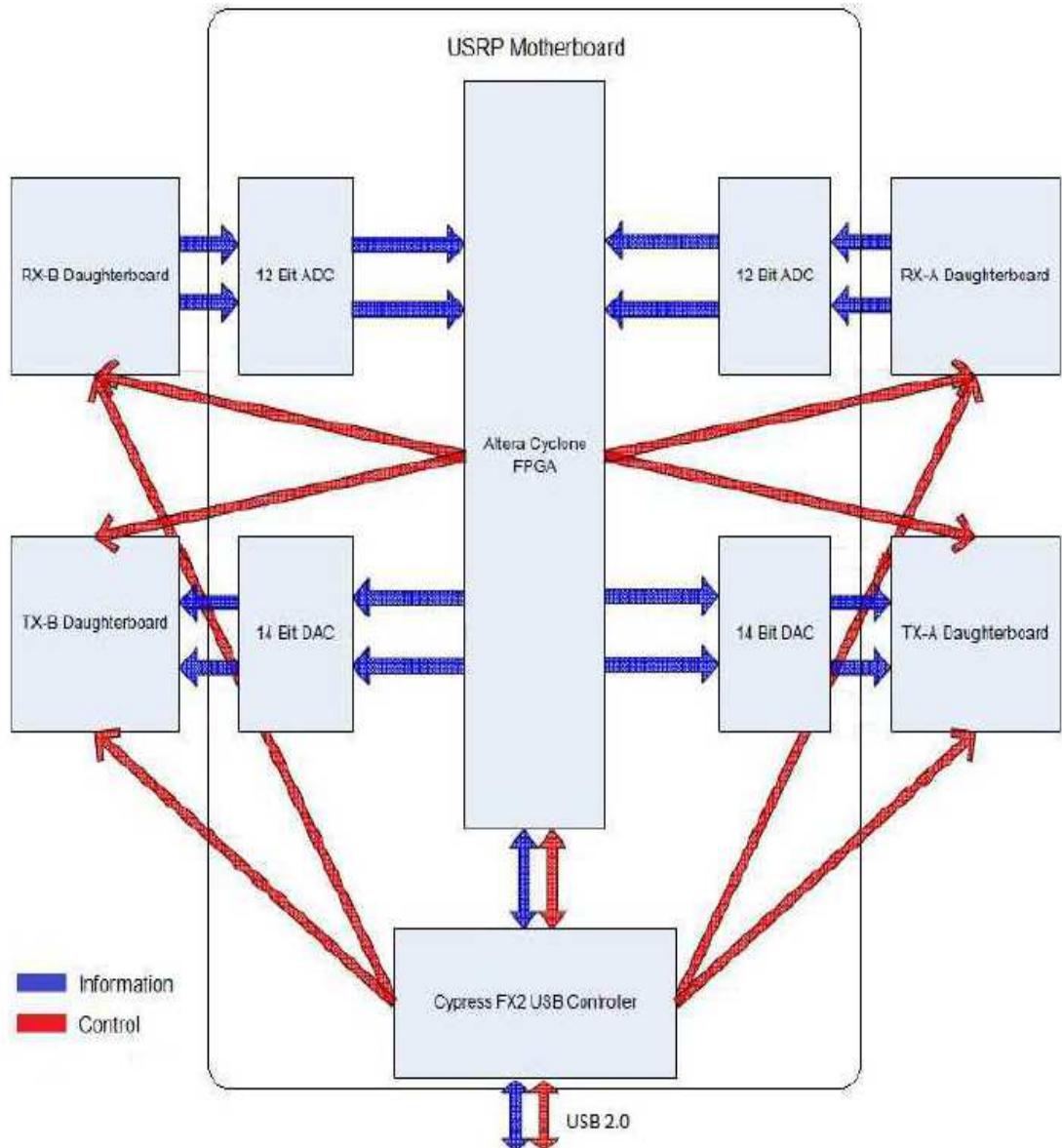


Figure 4.1: USRP block diagram. Blue arrows are information flow and red arrows control signalling flow [11].

4.1.2 Analog-to-Digital and Digital-to-Analog Converters

At the reception path, there are 4 high-speed 12-bit ADCs, with a sampling rate of 64 MHz. Considering Nyquist's theorem, a band as wide as 32 MHz can be digitalized [11], [14]. The ADC uses bandpass-sample signals up to around 200 MHz or even more if some decibels of loss is permitted [15]. Any time we are sampling signals which frequency, i.e. IF, is larger than 32 MHz, there will be aliasing. Even though, we can sample signals at higher frequency as far as

the band of interest is not being degraded and keeping in mind that this band is going to be mapped somewhere between -32 MHz and 32 MHz . The higher the IF is, the more the SNR³ is spoiled by jitter. The recommended value for this IF is around 100 MHz [11].

There are also 4 high-speed 14-bit DACs for the transmission path. Here the clock used is at 128 MHz , so here Nyquist limit is set at 64 MHz [14]. For the reconstruction of the signal it is necessary to filter under this Nyquist limit [15].

4.1.3 Clock Distribution

As we are working with a synchronous digital system, one important section of the system is the clock distribution network or the clock tree. This network distributes the clock signal to the elements in the system that need it, in order to define a time reference for the routing of data within the system.

In this particular system, the master clock signal is generated by a Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO⁴) of 64 MHz [16]. This signal, before being fed into the distribution network, can be modified in frequency, in order to get other clock frequencies [17], the 800 MHz Clock Distribution Divider AD9513 provides us with 3 different output clock signals which frequency is resulting from the division of the master clock frequency by an integer factor and with a certain phase offset and delay compared to the master clock. The current logical configuration of the motherboard clock distribution section provides a non-divided signal clock in a bypass configuration at the three outputs, i.e. a 64 MHz signal [18]. Then, this signal not only governs the time reference in the FPGA but also reaches the daughterboards, in order to have a universal common reference.

This clock signal is necessary for the VCO⁵ at the daughterboard. Nevertheless, there is also the possibility to have an independent crystal oscillator at the daughterboard instead of using the same time reference as in the motherboard [19].

4.1.4 Field Programmable Gate Array

A FPGA is an integrated circuit that can be configured or programmed using a hardware description language by the customer. They can implement any logical function which can be performed by an application-specific integrated circuit [20]. In our USRP, the FPGA holds the task to carry out high bandwidth math and adapt the data rate coming from the ADC to the one that can flow through the USB link, and the other way round. This block is directly connected to the USB interface microcontroller – the Cypress FX2 [17]. The FPGA runs four

³Signal to Noise Ratio

⁴Voltage Controlled Temperature Compensated Crystal Oscillator

⁵Voltage Controlled Oscillator

DDC⁶s. Those converters are implemented with some stage CIC⁷ filters for adds and delays and 31 taps halfband filters placed in cascade with the CIC filters for the spectral shaping and the rejection of signals out of band. For the transmission path, the two DUC⁸s are not included in the FPGA but only their CIC filters [11].

Digital Down Converter

The DDC downconverts the signal from the IF frequency to the baseband, multiplying the input signal by a constant frequency generated from an NCO⁹ [11].

Then, the signal is decimated in order to adapt the data rate to the USB 2.0 bounds of 32 MBytes/s. As the input signal is a complex signal at IF, sampled at a rate of 64 MHz, the output is still a complex signal centered at 0 Hz and decimated with a factor N . The decimation procedure consists of a low-pass filter which selects the frequency band ranging from $-F_s/N$ to F_s/N and a down sampler, to spread the spectrum to the new sampling frequency $F'_s = F_s/N$. The decimation factor ranges from 8 to 256 [11]. The samples leaving the USB interface are in 16-bit integers IQ format, which gives a value of 4 Bytes per complex sample. If we have the full capacity of the USB link at our disposal, the highest new sampling rate across the USB is 8 Msamples/s [11].

$$F'_s = \frac{32 \text{ MBytes/s}}{4 \text{ Bytes/sample}} = 8 \text{ Msamples/s} \quad (4.1)$$

The decimation factor can be easily calculated as

$$F'_s = \frac{F_s}{N} \rightarrow N = \frac{F_s}{F'_s} = \frac{64 \text{ MHz}}{8 \text{ MHz}} = 8. \quad (4.2)$$

In case the full capacity of the USB is not needed, we would just need to increase the decimation factor, to achieve lower sampling rates.

Figure 4.2 represents a simple scheme of the FPGA DDC.

Digital Up Converter

This block converts a baseband IQ sampled signal coming from the USB path to the IF. This is proceeded in two steps, the first is complex multiplication with a signal generated by a fine NCO and a second coarse multiplication with a signal coming from another NCO [11]. At the end the output signal is at the IF.

In between the two complex multiplications an interpolation is done with a programmable interpolation rate L , in order to restore the sampling rate used at

⁶Digital Down Converter

⁷Cascaded Integrator-Comb

⁸Digital Up Converter

⁹Numerical-Controlled Oscillator

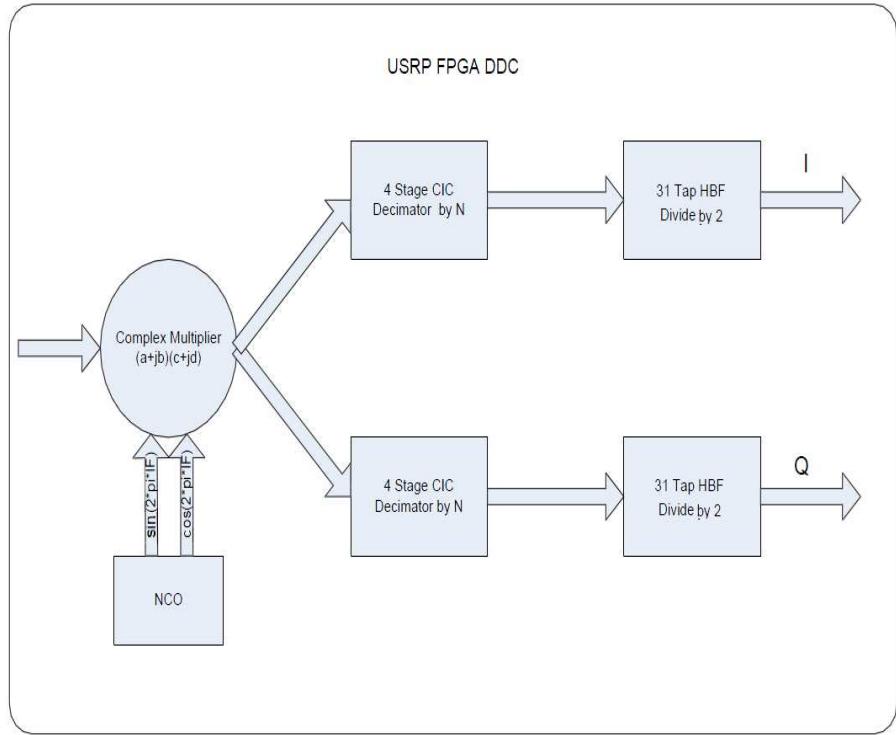


Figure 4.2: FPGA digital down converter [11]. Since the decimation is performed in two steps, the $N_{\text{total}}=2N$.

the DACs (128 MHz). It can be just seen as the reverse process of the DDC. The interpolation filters are two, first a 39-tap LPF¹⁰ followed by a 15-tap one [11].

In contrast to the DDC, the DUC is not performed by the FPGA but by a AD9862 CODEC chip [15], only the CIC interpolators are included in the FPGA.

Figure 4.3 represents the scheme of the USRP DUC.

It is important to mention that the USB link allows full duplex mode, so the maximum capacity of 32 MBytes/s is available for both paths.

4.2 Daughterboard “RFX2400”

For the analog down and up conversion in frequency, from and to IF, a daughterboard is needed, turning a USRP motherboard into a complete RF transceiver system. The selection of the daughterboard depends on the frequency necessary for our application, power specifications, signal to noise requirements or if we need a MIMO¹¹ capable board. There are simple boards for transmission or reception, but also transceiver boards [21].

¹⁰Low-Pass Filter

¹¹Multiple Input Multiple Output

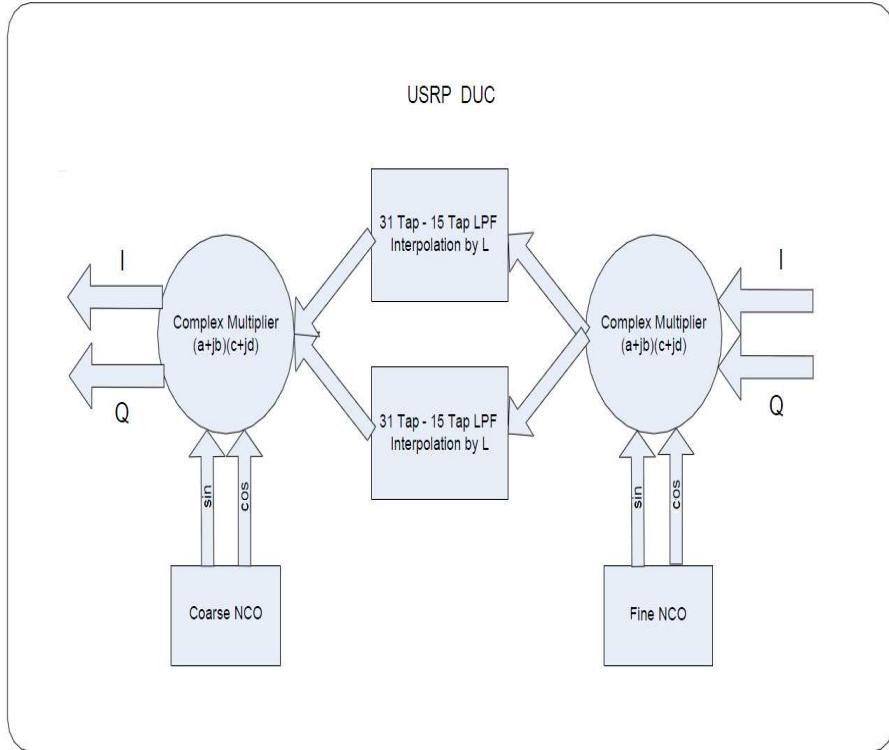


Figure 4.3: USRP digital up converter [11].

The election of the board “RFX2400” lays basically on the need of a transceiver board to work close to the spectral band ranging from 2 GHz to approximately 2.5 GHz established by the three mission frequency requirements. The transmitted power is 50 mW typically and uses synthesizers for independent transmission and reception frequencies, which are in the band from 2.3 GHz to 2.9 GHz. The board “RFX2200” also works around the frequency band needed but in a narrower window so it does not cover all of them, only from 2 GHz to 2.4 GHz [21].

Analyzing either the “RFX2400” frequency response, dynamic range (sensitivity and saturation point) or any other behaviors, is the first step to get to know this board, checking how good it is for our purposes and how it can be adapted to fulfill our expectations (Chapter 7). The next sections are focused on the description of the receiver and transmitter components of the “RFX2400”.

4.2.1 Receiver Components

Since there are two reception ports on the transceiver daughterboard, it is necessary to place a switch to decide which port is feeding the system with the received signal. After this block, the S-Band signal is amplified by a GaAs MMIC¹² low-noise amplifier (MGA82563) working at a center frequency of 2 GHz [19], [22].

¹²Monolithic Microwave Integrated Circuits

Once the signal is amplified, it flows to a quadrature demodulator (AD8347) designed to work with signals from 800 MHz to 2700 MHz [23], which mixes our signal with a local oscillator signal coming from an integrated synthesizer and VCO block (ADF4360-0) in order to convert it to IF. This synthesizer designed for a center frequency of 2.6 GHz generates an output from 2.4 GHz to 2.75 GHz [24]. The time reference is taken from the master clock from the motherboard or it can be taken from an additional and independent crystal oscillator.

The exact frequency value the synthesizer is generating, depends on the frequency we are receiving, set at the GRC tool. This frequency is always 4 MHz less than the RF¹³ signal we are receiving, i.e. the IF is 4 MHz. The problem is that the resolution of the synthesizer is generally around 25 kHz, so when the frequency that the VCO should output is not a multiple of the resolution, then it just downconverts approximately to the IF of 4 MHz. To correct this, at the DDC the NCO, since it is more flexible, downconverts this IF of approximately 4 MHz to exactly baseband.

After the conversion to IF, finally the analog signal gets into the motherboard, and is processed as described in Section 4.1.

4.2.2 Transmitter Components

At the transmission path, the analog signal at IF from the motherboard reaches the mixer AD8349 – prepared to work with signals from 700 MHz to 2700 MHz – which carries out the quadrature modulation to shift up the frequency to S-Band [26].

Again the local oscillator signal for the mixer is generated by a synthesizer and VCO block, ADF4360-0 [24].

As in the receiver path, the frequency value the synthesizer is generating, depends on the frequency we want to transmit. This is always set to be 4 MHz more than the RF signal to be transmitted, i.e. the IF is 4 MHz. Due to the limited resolution of the VCO, it is only approximately 4 MHz. Once again, at the DUC, the NCO corrects this coarse approach the VCO will perform, so at the end, the expected RF value is reached.

Then, the signal is amplified by a GaAs MMIC amplifier (MGA82563) as at the reception path, and then it comes to another broadband high linearity amplifier [22].

The time reference can also be provided by the master clock from the motherboard, or in order to have other timing, a crystal oscillator can be added.

Before leaving the USRP, the signal passes through a microembedded bandpass filter which bandpass goes from 2400 MHz to 2483.5 MHz for ISM¹⁴ applications such as Bluetooth or WLAN¹⁵ [19], [25]. This filter can be avoided with

¹³Radio Frequency

¹⁴Industrial, Scientific, Medical

¹⁵Wireless Local Area Network

a short circuit.

In order to fit this daughterboard to our application frequency, the ADF4360-0 should be replaced by an ADF4360-2 which sweeps from 1850 MHz to 2170 MHz, so that we can take the interesting mission frequencies to the correct IF in which the aliasing consequences are at minimum level [27], and we have to bypass the ISM filter.

4.3 Auxiliary Ports

The USRP has 64 bit high speed digital I/O ports, divided in 32 bit for each path. Those digital I/O pins are connected to the daughterboard interface connectors, and are controlled by certain FPGA registers, being read and written by software. Some pins are used to select the input port for the received signal, to control the power supply for both paths, to detect the synthesizers locking, to carry out the automatic gain control processing, etc, or just to debug the FPGA [11].

Chapter 5

GNU Radio Companion Blocks

GRC is a graphical tool which provides a user interface that lets us create signal flow graphs and activates its source code. This graphical interface, by means of graphical blocks, allows us to set the input parameters which are taken by the source code of each block in order to generate a signal flow, and to visualize the signal at every step of the block chain using graphical sinks.

There are mainly four kind of blocks:

- Source: Their main functionality is to generate an output signal by means of some input parameters. For this reason, these blocks have no input signal. There are many types of sources, depending on the number of output ports, data type, vector lengths, etc.
- Sink: In this case, there is no output signal. Sink blocks receive an input signal with a specific data type and length, and, using certain input parameters, the input signal is stored in a vector, file or sent to a binded TCP¹ or UDP² socket.
- Operation: These blocks use a configurable number of input signals with configurable data types, to produce a certain number of output signals with specific data types, using the input parameters to perform a certain operation on the samples at the input. These operations can be modulations or demodulations, coding operations, filters, synchronizations, type or stream conversions, etc. Among the different parameters needed to perform the operation, the sampling rate stands always out so that a correct treatment of the signal can be done.
- Visualization: These blocks can be classified as a type of sink block which generates a graphical output from the input signals. In this group of blocks, I can mention scopes to provide a time domain representation, FFT³ for a frequency domain screening, constellation plots, etc.

For each of those blocks, the input parameters are introduced by means of a GUI⁴ defined in XML⁵. The different blocks are connected in a proper way so

¹Transmission Control Protocol

²User Datagram Protocol

³Fast Fourier Transform

⁴Graphical User Interface

⁵eXtensible Markup Language

that the signal data can flow along a chain, taking into account data types, vector lengths, etc. The core functionality of each block is defined by Python or C++ code.

For my measurements, I created two scenarios corresponding to both reception and transmission front-ends.

5.1 Reception Path

To evaluate the USRP performance when receiving, I set three main blocks as it can be seen in Figure 5.1.

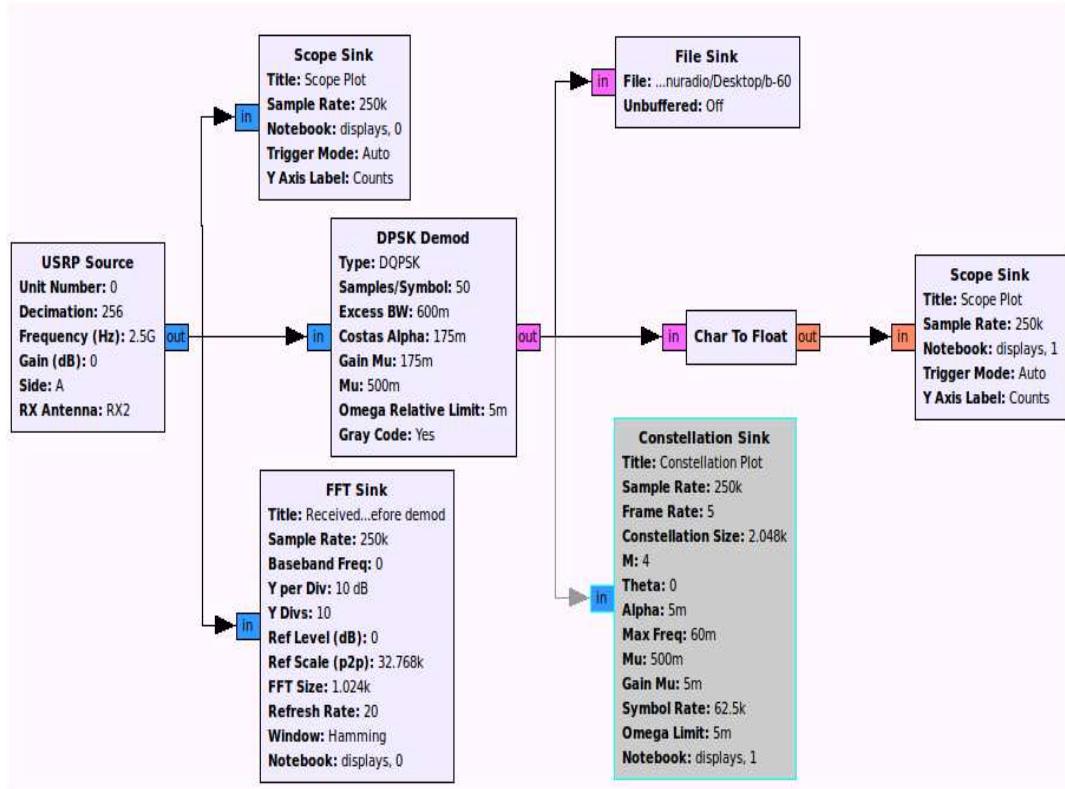


Figure 5.1: GRC front-end receiver scenario.

5.1.1 Measurement Setup

USRP Source : This block, as the beginning of the chain, provides us the received signal coming through the USB link from the USRP motherboard. This signal is a complex digitalized signal with a sample rate of 250 kHz, downconverted to baseband.

The input parameters basically set the S-Band receiving frequency (and its offset if it is required), gain and the decimation factor, which ranges from 8 to 256 and ensures us a proper use of the available 32 MBytes/s band-width at the USB interface. It is also needed to set the format for the complex samples. In this case, samples are in 16 bit integers IQ format, that means 4 Bytes/sample.

DPSK Demodulator : This block takes care of the root raised cosine filtering and performs a differential coherent detection or phase shift demodulation. The input data consists of a complex sampled signal at baseband frequency and the output is a big-endian stream of bits packed 1 bit/Byte.

The parameters that are necessary here are the number of samples per symbol, the excess in bandwidth that refers to the roll-off factor of the root raised cosine filter, the Costa's alpha parameter, the mu factor and its gain, etc. These parameters will be explained on greater detail in this section.

File Sink : Graphically or in a file depending on its data format, sinks are used to visualize the resulting signal at the end of the chain. Input parameters are depending on the kind of input data.

Particularly in our scenario, since I want to screen the resulting byte-type data after the demodulator block, I used a file sink where a binary file is recorded for later processing.

For a proper understanding of the data output at the sink file and future analysis of bit error rates modifying certain parameters of the incoming signal such as power level, frequency ranges and offsets, in this section, the demodulation hierarchical block is going to be explained in further detail.

5.1.2 DPSK Demodulator

As it will be explained in Chapter 6, the incoming signal is a S-Band 2.5 GHz signal with a differential QPSK modulation (which means 2 bits/symbol) using a MSAT⁶ standard which modulation scheme is also explained in Chapter 6. The transmission rate for the measurements is 10 kbps, this is to say, 5 ksymbols/s

$$\frac{10 \frac{\text{kbit}}{\text{s}}}{2 \frac{\text{bit}}{\text{symbol}}} = 5 \frac{\text{ksymbols}}{\text{s}}, \quad (5.1)$$

and its filter is a root raised cosine with a roll-off factor of 0.6 .

For that reason, the input parameters are DQPSK⁷, and an excess bandwidth of 0.6 to match the signal filter. The number of samples/symbol is calculated knowing that the data rate of the signal generated is 10 kbps. This signal is sampled with a higher rate of 250 kHz, so that means, I have for each symbol transmitted 50 samples

⁶Mobile SA Tellite

⁷Differential Quadrature Phase Shift Keying

$$\frac{250 \frac{\text{ksamples}}{\text{s}}}{5 \frac{\text{ksymbols}}{\text{s}}} = 50 \frac{\text{samples}}{\text{symbols}}. \quad (5.2)$$

The complete functionality of the demodulator block is splitted up in different sub-blocks or functions defined in C++ code which are connected by some Python code. The signal is flowing in a chain of sub-blocks, so that the output of a sub-block is the input of the next one (Figure 5.2).

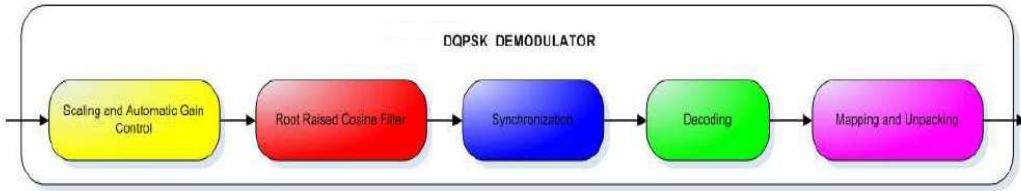


Figure 5.2: Data flow graph in the demodulation block.

In the upcoming sections, these sub-blocks will be explained in detail and its influence on the signal at each step is illustrated, paying special attention to the input and output items number, constellation schemes, etc.

In Figure 5.3 the input parameters for the demodulator block are listed.

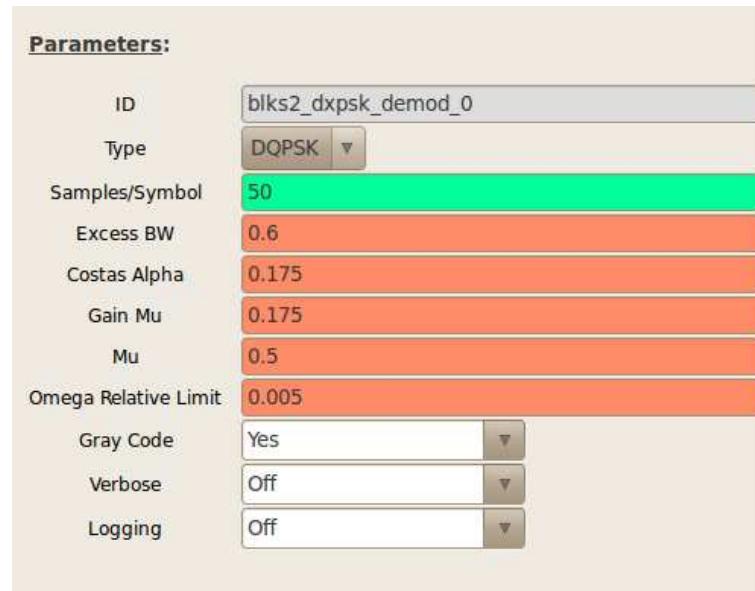


Figure 5.3: Parameter settings for the demodulator block.

Scaling and Automatic Gain Control

In this block the signal is first multiplied by a constant to scale the signal from full-range to ± 1 .

Then an automatic gain control is performed. The procedure consists of a calculation of the maximum power level among the samples taken from a 16 sample window each time. For each window, samples are normalized to the maximum value and then multiply by 2. Until this point, a simple rescaling is performed. The number of output items matches up with the number of input items. All these complex items undergo only a magnitude change, their phase does not suffer any change since the demodulator has not performed any synchronization yet. Due to an unsynchronized sampling, i.e. samples are not being taken at the same instants symbols are transmitted, instead of receiving phase values around the constellation points transmitted, we are sampling mostly at the transitions between points. For this reason, if the constellation is screened we can just see a rotating constellation (Figure 5.4). The transitions observed through the constellation's origin are due to the transition between non-consecutive symbols.

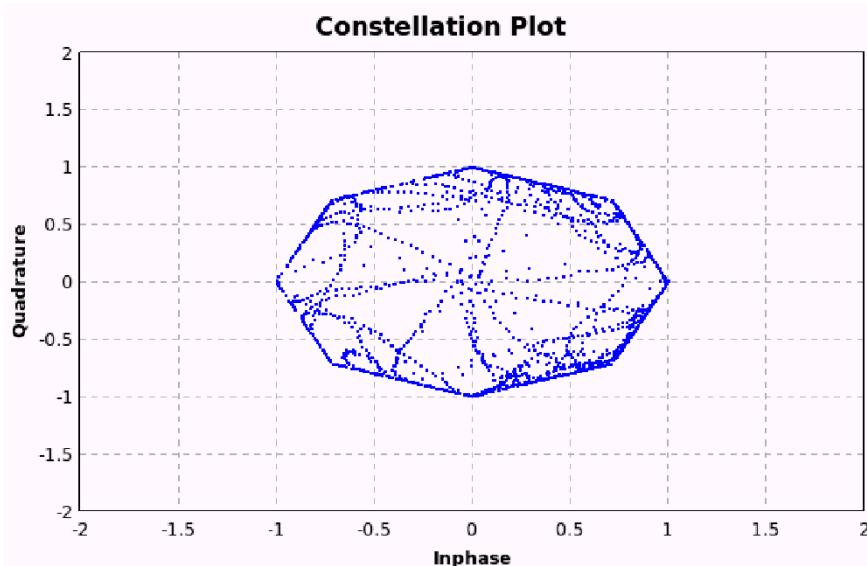


Figure 5.4: Constellation output after the automatic gain control block.

Root Raised Cosine Filtering

After the scaling part, this sub-block performs the raised cosine filtering. In case of having digital modulation, this filtering is required to minimize the ISI⁸, effect that causes the smearing into adjacent time slots due to a symbol-pulse time-spreading [29]. Depending on the rolloff factor and the absolute bandwidth of the filter, it can guarantee a communication without ISI at a certain data rate [29]. Since the modulation standard in our case uses a root raised cosine and a roll-off factor of 0.6 and the filtering at the demodulation must be equal, I also use 0.6 at the demodulator.

⁸Inter-Symbol Interference

This root raised cosine filter is implemented as an adaptive digital FIR⁹ filter, which *filter coefficients* or *tap weights* are calculated in a iterative procedure.

Apart from this functionality, this filter is also used to apply a second step on the interpolation algorithm. The interpolation, as the reverse operation of the decimation, generates, in a first step which is called *expansion* or *sampling rate expanding*, intermediate samples in our received sampled signal in order to increase the sampling rate by a factor of L , which stands for the interpolation factor. In the frequency domain, the spectrum is compressed, producing more copies of the spectrum concentrated in the same digital frequency span. In order to preserve the energy, the filter gain should match up with L , as it can be seen in the Equation 5.3. In our case, the interpolation factor L is 1, that means this functionality is not used. [28]

$$H_1(\omega) = \begin{cases} L & |\omega| \leq \frac{\pi}{L} \\ 0 & |\omega| \geq \frac{\pi}{L} \end{cases} \quad (5.3)$$

Any synchronization has not been performed yet and the output constellation is still rotating (Figure 5.5).

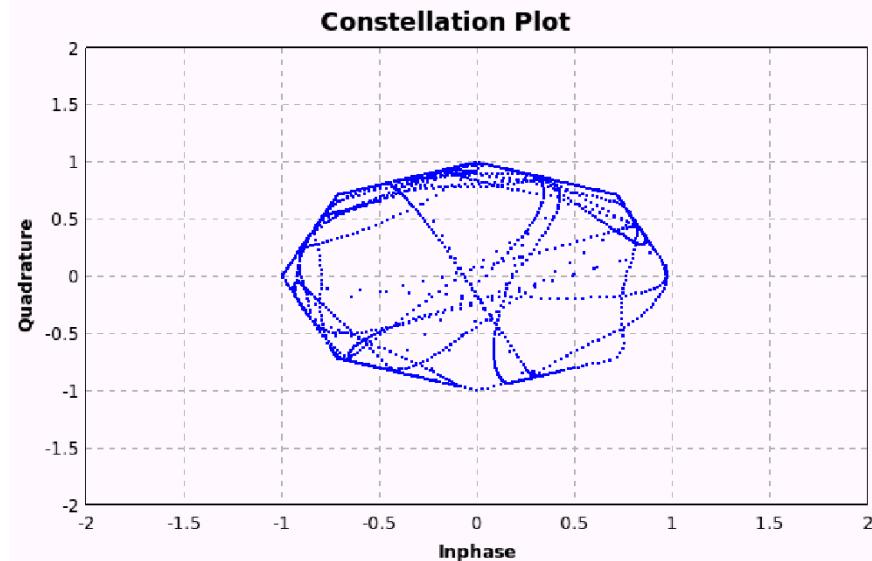


Figure 5.5: Constellation output after the root raised cosine filter.

Synchronization

Since we are taking samples at the transition between symbols instead of at the correct instant the symbols are transmitted, we are getting incorrect information. Synchronization is one of the most important stages for the demodulation performance.

⁹Finite Impulse Response

Basically, synchronization is done in two different steps:

Decimation : Reducing 50 samples/symbol to 1 sample/symbol. If I am taking several samples per symbol one after the other, we are going to keep on sampling at transition points. Once 49 samples for each symbol are deleted, the constellation at the output is a non-rotating constellation and the points at the output can still be de-phased with respect to the expected symbol phase. The reason of this lays on the need of a phase synchronization. As some samples are being discarded, the sampling rate is decreased by the decimation factor $M = 50$, producing an expansion in the spectrum. In order to preserve the spectral energy, it is necessary to rescale the signal spectrum with a gain factor of $\frac{1}{M}$ [28].

$$X_D(\omega) = \frac{1}{M} \sum_{i=0}^M X\left(\frac{\omega}{M} - \frac{2\pi i}{M}\right) \quad (5.4)$$

Phase synchronization : This synchronization requires to use a reference QPSK constellation. This is a constellation in which phase 0 means symbol 0, phase $\frac{\pi}{2}$ means symbol 1, phase π means symbol 2 and phase $-\frac{\pi}{2}$ means symbol 3. The phase error is calculated following the next criteria:

$$\text{Error} = \begin{cases} \text{if } |\text{Re}(x)| > |\text{Im}(x)| \begin{cases} -\text{Im}(x) & \text{if } \text{Re}(x) > 0 \\ \text{Im}(x) & \text{if } \text{Re}(x) < 0 \end{cases} \\ \text{if } |\text{Re}(x)| < |\text{Im}(x)| \begin{cases} \text{Re}(x) & \text{if } \text{Im}(x) > 0 \\ -\text{Re}(x) & \text{if } \text{Im}(x) < 0 \end{cases} \end{cases} \quad (5.5)$$

If the absolute value of the real part is bigger than the absolute value of the imaginary part, if the real part is negative, then the phase error is the imaginary part, and if the real part is negative, the phase error is the negative imaginary part. If the absolute value of the imaginary part is bigger than the one from the real part, then the phase errors are the real part, in case of a positive imaginary part, the phase error change its sign if the imaginary part is negative.

Once this phase error is obtained, the sample per symbol we receive each time is approximated to the closest point in the reference constellation, until the phase error is reduced maximally.

Nevertheless, it can easily be observed that there is an implicit error that the synchronization block cannot fix by itself. The constellation points are close to the values in phase expected but they are not perfectly fitting. This error is due to the frequency offset between signal generator and USRP, and a frequency error in a time-span entails a phase error. In this experimental setup I manually turned the generator to aid the Costa's loop to synchronize.

The output from this block are basically synchronized signal samples as shown in Figure 5.6, but this time the number of output items is lower than the number

of input items, since 49 of each 50 samples are dismissed to get 1 sample/symbol. In this case the magnitude and phase of the input samples are corrected too.

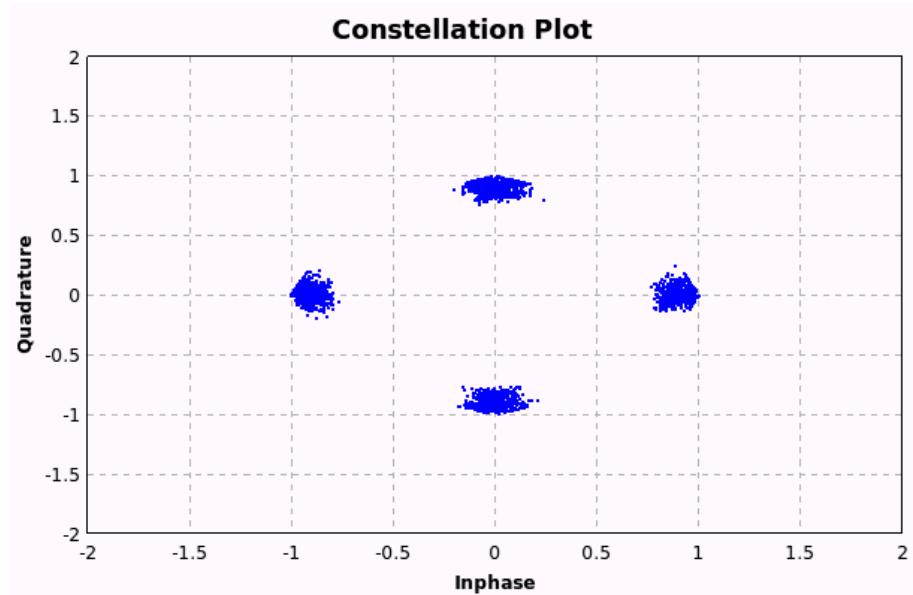


Figure 5.6: Constellation output after synchronization.

Decoding

The demodulation standard employed by the GNU Radio Companion is a differential demodulation. So as a first part of the block, the differential value in phase between consecutive samples is calculated. So at this point the outputs are no longer samples, but undecoded symbols.

Then, a reference constellation is created. In this reference constellation, the phase 0 means symbol 0, phase $\frac{\pi}{2}$ means symbol 1, phase π means symbol 2 and phase $-\frac{\pi}{2}$ means symbol 3. This constellation can be rotated, but it is not in our case. The output of this constellation function is a complex vector in which the components are the different constellation points and each element position in the vector corresponds to their symbol's number, i.e. $\text{symb_ref} = [Ae^{j0}, Ae^{j\frac{\pi}{2}}, Ae^{j\pi}, Ae^{-j\frac{\pi}{2}}]$.

At this point, the different distances between each of the calculated undecoded symbols (input data) and each of the symbols from the reference constellation ($d_{\text{sym_position}}$) are calculated using the Euclidean norm, that means the distances are obtained as the length of the vectors connecting the reference symbols and the received ones.

When the lowest distance is obtained, the undecoded symbol is associated to the vector position of the symbol from the reference constellation which gave us this lowest distance, i.e. which it is apparently closer to the value of the

undecoded symbol. In this way, every difference in phase (input data) is decoded with a number from 0 to 3 (output data).

An example can be seen in Figure 5.7. It shows the different distances between an undecoded received symbol (in red) and each of the symbols from the reference constellation (in blue). Since the lowest distance is d_1 , i.e. the closest reference point is $\text{sym_ref}[1]$, and the decoded output value is 1.

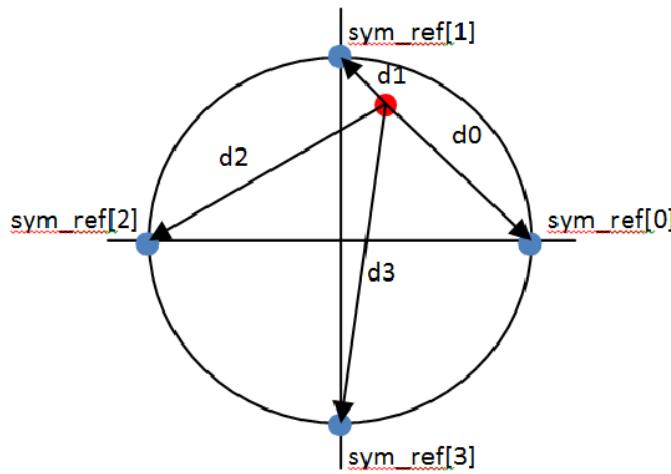


Figure 5.7: Calculated distances from an undecoded received symbol to each of the reference points.

The number of output items matches up with the number of input items, but now the output items are decoded symbols.

This block also takes care of the calculation of the EVM¹⁰ as the sum of all root-mean-square differences between the input data and the closest point from the constellation reference assumed to be the correct one, for each transmitted symbols (*total_error*), divided by the number of transmitted symbols, which is also the number of output items (*noutput_items*) [30]

$$EVM = \frac{\text{total_error}}{\text{noutput_items}}. \quad (5.6)$$

Until this point, the output values are decoded not-mapped symbols. In the Figure 5.8, the constellation at the decoding block output is screened.

Mapping and Unpacking

This block associates two bits per symbol in order to get a binary output signal. Depending if we need a Gray code or a Non-Gray one, symbols 2 and 3 are

¹⁰Error Vector Magnitude

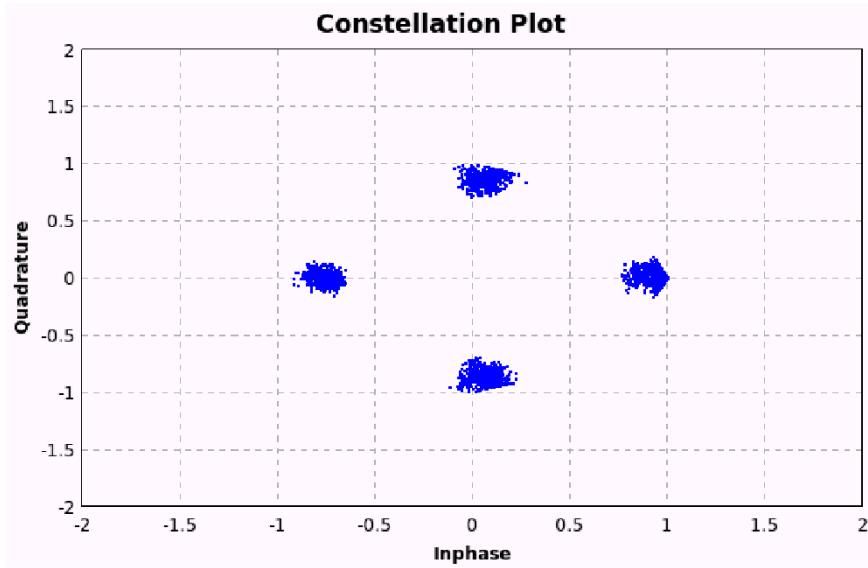


Figure 5.8: Constellation output after decoding.

differently mapped. In case of Gray code, number 2 is mapped with 11 and 3 with 10, and it is the other way round in case of Non-Gray code.

At the output, we have a binary sequence of bits packed as 2 bits/symbol. Now the output is no longer a complex signal, but of byte type. Since the sequence has been treated as packets of two bits each, it is necessary to unpack it, to have a fluent sequence of unpacked bits. After unpacking, we have twice the number of items before unpacking, because now a pair of bits is not longer treated as unity or symbol, but is split into two bytes with either 0x00 or 0x01 each.

The Table 5.1 shows a summary of the mapping and unpacking block for either Gray or Non-Gray coding.

Table 5.1: Mapping and unpacking summary.

Input	Gray-Mapping	Gray Output	Non-Gray Mapping	Non-Gray Output
0	0	0x00 0x00	0	0x00 0x00
1	1	0x00 0x01	1	0x00 0x01
2	3	0x01 0x01	2	0x01 0x00
3	2	0x01 0x00	3	0x01 0x01

5.2 Transmission Path

For the transmission path, the scenario set up is basically constituted of three main different blocks as it is shown in Figure 5.9:

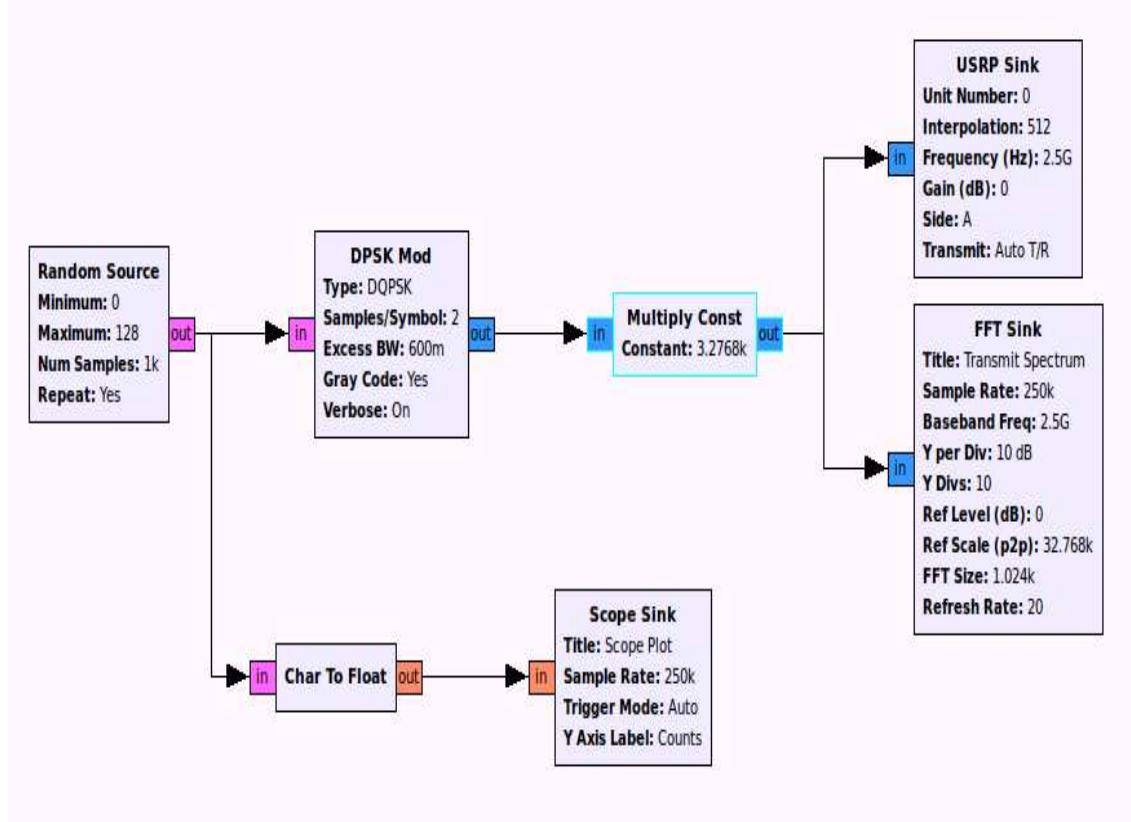


Figure 5.9: GRC front-end transmitter scenario.

5.2.1 Measurement Setup

Random Source : This block, as the beginning of the chain, generates a random digital signal. It provides us a certain number of byte type samples, which values range from 0 to, in our case, 128 – these number is not significant for the meaning of the measurements.

Since it is a data source, it has no data input but one output port. As the output are bytes, it is necessary to perform a unpacking from bytes to a 2-bit vector, i.e. groups of 2-bit chunks, as the number of bits per symbols is 2, to treat the signal bits properly in the demodulation process.

DPSK Modulator : This block takes care of the root raised cosine filtering and performs a phase shift modulation. The input data consists of a byte stream coming from the source and the output is a complex modulated signal at baseband.

The parameters that are necessary here are the number of samples per symbol and the excess in bandwidth that refers to the roll-off factor of the root raised cosine filter. These parameters will be explained on greater detail in this section.

USRP Sink : The sink used here is taking the baseband complex sampled signal at the modulator block output in order to transmit it through the USB link to the USRP motherboard. The sample rate before this block is 250 kHz and taking into account the sampling rate at the DAC converters which is of 128 MHz, it is necessary to set an interpolation factor of 512 .

Basically, the parameters set the S-Band transmitting frequency to which the baseband carrier is going to be upconverted, a frequency offset if it is required, the gain and the interpolation factor to ensure a proper use of the 32 MBytes/s band-width at the USB interface.

To facilitate the understanding of the modulated data output at the USRP sink and to comprehend the transmitted signal, in this section, the modulator hierarchical block is going to be explained in further details.

5.2.2 DPSK Modulator

In order to understand the behavior of the modulation block, the random source is replaced by a vector source so that we can introduce a known binary data. The aim is to transmit a modulated S-Band signal at 2.5 GHz with a differential QPSK modulation (which means 2 bits/symbol) using a certain modulation scheme which will be explained in further detail. The vector source generates a binary sequence from a list of byte type numbers with no predefined timing. The timing is set at the USRP sink and the demodulator block, by means of the sample rate and the factor of samples/symbol. That is to say, for a sample rate of 250 kHz at the USRP sink and a factor of 2 samples/symbol for the interpolation filter at the modulation block, the symbol rate of the source is defined, and its value is 125 ksymbols/s

$$\frac{250 \frac{\text{ksamples}}{\text{s}}}{2 \frac{\text{samples}}{\text{symbol}}} = 125 \frac{\text{ksymbols}}{\text{s}} \quad (5.7)$$

The filter considered for any possible demodulation is a root raised cosine with a roll-off factor of 0.6 .

For that reason, the input parameters are DQPSK and an excess bandwidth of 0.6 to match it the signal filter. The number of samples/symbol is set to 2 to provide a signal with symbol rate of 125 ksymbols/s.

The complete functionality of the modulator block can be easily divided in different sub-blocks or functions defined in C++ code and connected with Python code. The signal is flowing in a chain of sub-blocks, as it can be seen in Figure 5.10.

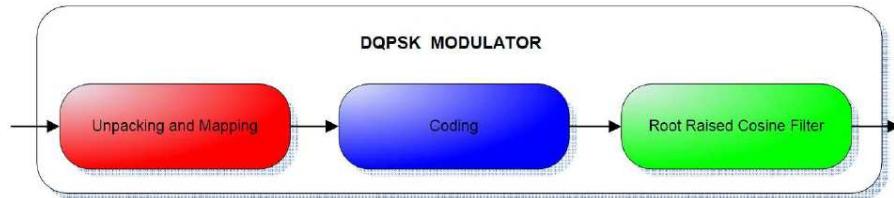


Figure 5.10: Data flow graph in the modulation block.

In the next sections, these sub-blocks will be explained in great detail and its influence on the signal at each step is shown. In Figure 5.11 the input parameters for the modulator block are listed.

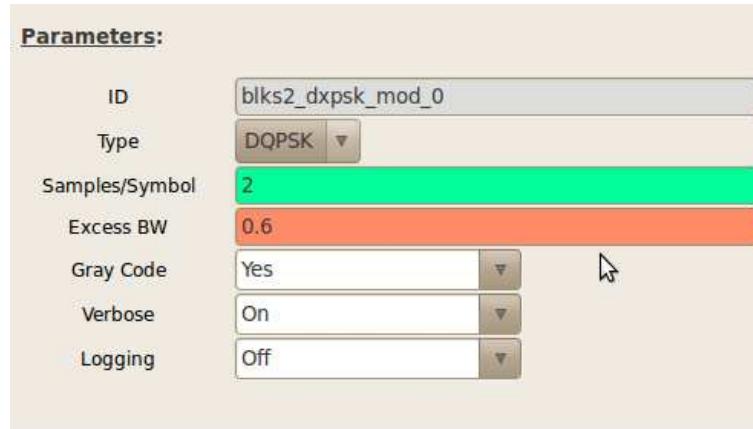


Figure 5.11: Parameter settings for the modulator block.

Unpacking and Mapping

Since the signal at the output of the random source are packed bytes, it is necessary to convert it into a 2-bit-chunk stream in order to perform a proper identification and treatment of the symbols.

After the unpacking, the mapping process on the chunks is executed. In this subblock a binary sequence is mapped to symbols. As the the Gray code is chosen, the mapping to the 2-bit chunks of 11 and 10 corresponds to 0x02 and 0x03, respectively, while 00 and 01 are mapped to 0x00 and 0x01.

The data type is still being byte type at the output.

Coding

The modulation standard used in GNU Radio Companion is a differential modulation. In a differential modulation, the different binary chunks add a certain

change in phase to the current phase in the carrier signal. That means that they take the previous phase into account. During the encoding process, the output results from the addition of the mapped binary 2-bit chunks to the previous output in a iterative process and is divided by the modulus which is 4, getting a cycle where 0x100 corresponds to 0x00 again. The output is still a binary sequence which values are directly related to the phase changes in the carrier signal – the output has the differential information included where the coding information for the carrier phase modification is directly associated to the 2-bit chunks without the need of considering the previous output. To complete the differential coding just an assignment of a complex value to the different 2-bit chunks at the output is needed.

Then, a reference constellation is created. In this reference constellation, the phase 0 means symbol 0 , phase $\frac{\pi}{2}$ means symbol 1 , phase π means symbol 2 and phase $-\frac{\pi}{2}$ means symbol 3 . This constellation is rotated in this case, multiplying the constellation by $0.707 + 0.707j$, which is equivalent to rotate the constellation by 45° . The output of this constellation function is a complex vector in which the components are the different constellation points and each element's position in the vector corresponds to their symbol's number, i.e. $symb_ref = [Ae^{0.707+0.707j}, Ae^{-0.707+0.707j}, Ae^{-0.707-0.707j}, Ae^{0.707-0.707j}]$.

To finalize the coding process, the 2-bit chunks obtained are assigned to a complex value of the reference vector where the index of its position in the vector corresponds to the decimal value of the chunk.

In this concrete case, having a differential output chunk of 0x00 is like transmitting a carrier with a phase of 45° , a chunk of 0x01 is like transmitting with a phase of 135° , if it is 0x11 the phase transmitted is 225° and a differential output of 0x10 is related to a phase of 315° .

The constellation after the coding block can be seen in the Figure 5.12.

The outputs are sampled symbols (1 sample per chunk) and reflect the change in phase of the carrier to be transmitted, i.e. the modulated signal.

Root Raised Cosine Filter

Once the modulated signal is obtained, a raised cosine filtering is carried out. As it was explained in the Section 5.1.2, this filtering is required to minimize the ISI, which causes a smearing into adjacent time slots due to a symbol-pulse time-spreading in a real system. Since the demodulation standard considered in our case uses a root raised cosine pulse shape and a roll-off factor of 0.6 , the filtering at the modulation must be equal.

In a parallel procedure to the demodulator, this filter is implemented as an adaptive digital FIR filter, which *filter coefficients* or *tap weights* are calculated in a iterative algorithm. Then the filtering is performed without any interpolation, i.e. $L = 1$.

At the output we have the complex filtered samples of a baseband carrier ready to be transmitted.

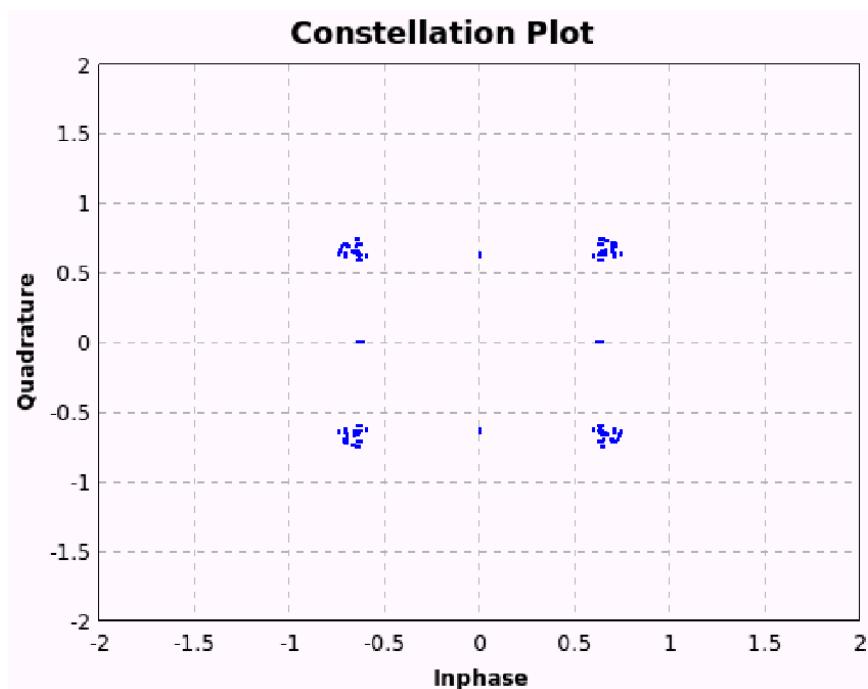


Figure 5.12: Constellation output after coding.

Chapter 6

The QPSK Test Signals

This chapter gives a short description of the signal chosen for the simulation and measurements, according to the requirements of the hardware and the final project expectations, in order to get useful information.

6.1 Reception Path

The generator used to produce a signal for our purposes is the SME-06 from Rohde&Schwarz.

The R&S SME generates the complex signals required for the manufacturing of digital radio receivers. It can supply the signals with specific standards of modulation, data format, TDMA¹ structure and frequency sweep patterns. The version 06 of SME covers the frequency range from 5 kHz to 6 GHz [32].

In order to get interesting results aiming at the final purposes of the project, the characteristics of the signal generated are properly chosen.

6.1.1 Frequency and Power Level

Since the frequency values for our application missions are in the range between 2 GHz and 2.5 GHz, and the USRP is working in a frequency span from 2.3 GHz to 2.9 GHz, the selected frequency for our measurements among all the possibilities is 2.5 GHz.

The power level chosen is an input power within the dynamic range limits and far from the compression point level. Ideally, it is required to work in a linear behavior range. Since the USRP is not perfectly linear, we will consider linear enough the dynamic range input values. For all those reasons, the input power levels selected are from -20 dBm to -15 dBm.

6.1.2 Modulation and Standards

Among all the digital modulation standards the three mission systems are using, our measurements will be oriented to get to know the most common one,

¹Time Division Multiple Access

the QPSK modulation. The Rohde&Schwarz SME-06 QPSK digital modulation supports different modulation standards such as INMARSAT², MSAT, TETRA³, NADC⁴, etc. The differences between them lay basically on the type of QPSK modulation and the constellation scheme employed for coding.

There are different variants of the original QPSK modulation, where the information is placed in the phase value of the carrier signal (only 4 different phase values are supported) and coded into 4 different symbols. One of those is DQPSK. In this case, the information is in the differential value between two consecutive phases of the carrier signal, i.e. in how much the signal phase changes regarding the previous value. One example of such a standard using this modulation scheme is MSAT. Another variant of the original QPSK is $\frac{\pi}{4}$ -DQPSK, employed by the NADC, PDC⁵, TFTS⁶, TETRA and APCO25⁷ standards. $\frac{\pi}{4}$ -DQPSK is pretty similar to the differential one, but here there are two identical symbol constellations rotated $\frac{\pi}{4}$ respectively to each other; even symbols select points at one of the constellations and the odd ones from the other constellation, so that the maximum phase shift is reduced to 135° . And last but not least, there is the OQPSK⁸ where the I and Q data are shifted in time from each other, entailing that both bits are not changing at the same time, avoiding symbol changes from 0x00 to 0x11 or 0x01 to 0x10. This last standard requires more linearity in the amplification of the signal but with less power level, higher SNR is reached, since there are no crossings through the center of the constellation. The commercial standard INMARSAT uses the modulation OQPSK.

Due to the GRC modulation block standard, which is DQPSK, the selected modulation scheme for the signal generated is MSAT. Its default settings employs a bit rate of 6.75 kbits/s and a root raised cosine filter with a roll-off factor of 0.6. In order to ease things at the demodulation block, the bit rate is set to 10 kbits/s, which gives us a symbol rate of 5 ksymbols/s (see Chapter 5).

The constellation scheme used at the modulator in the Rohde&Schwarz SME-06 signal generator can be seen in the Figure 6.1. Transmitting a differential value of 0x00 between consecutive pairs of bits with a cycle module of 4, means transmitting a 0 phase; when transmitting a differential value of 0x01, this changes the phase to $-\frac{\pi}{2}$ and for 0x10 to $\frac{\pi}{2}$. If the differential value 0x11 is transmitted, the carrier phase changes to π .

Comparing to the constellation scheme used by the GNU Radio Companion graphical tool, that can be seen in Figure 6.2, we should take into account that the demodulated decoded binary sequence of 0x10 does not mean a phase change of π and that 0x11 was transmitted, instead, it means a decrease of $\frac{\pi}{2}$ in phase,

²INternational MARitime SATellite

³TERrestrial Trunked RAdio

⁴North American Digital Cellular

⁵Personal Digital Cellular

⁶Time and Frequency Transfer Standard

⁷Association of Public Safety Communication Officials - Project 25

⁸Offset Quadrature Phase Shift Keying

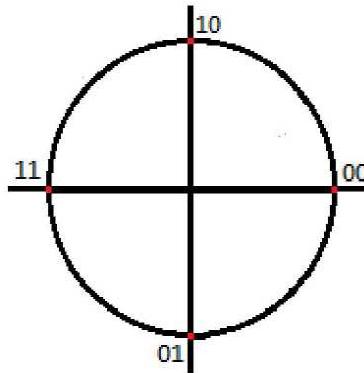


Figure 6.1: MSAT modulation constellation scheme.

and consequently a transmission of 0x11 and viceversa. In order to proceed with the measurements and error testings, every received 0x11 should be replaced for 0x10 and viceversa.

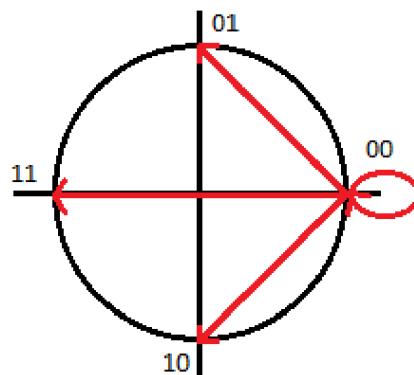


Figure 6.2: GRC demodulation constellation scheme.

Until this point, the transmitted signal is matching the conditions expected at the demodulation block at the GNU Radio Companion, or at worst cases, we already have enough information to completely understand its working procedure.

6.2 Transmission Path

When analyzing a transmission scenario, the signal is generated through the GRC software tool. In this software, as it was shown in the Chapter 5, a random source or a vector source generates a binary sequence from a decimal vector input, with a symbol rate given by the sample rate at the USRP sink and the symbols per sample factor at the modulation block.

The next subsections explain the characteristics of the transmitted signal and the modulations parameters to comprehend the transmission path.

6.2.1 Frequency and Power Level

According to both our application mission frequency ranges and the USRP one, the selected frequency for our measurements among all the possibilities is 2.45 GHz.

The power level cannot be controlled through the software tool, and its value is purely given by the active elements at the hardware. The measured transmitted value is around 0 dBm.

6.2.2 Modulation and Standards

Due to a parallel reasoning to the reception path, the modulation standard chosen for the analysis is DQPSK which is also the only standard GRC currently supports.

The ideal settings at the modulation block in order to establish a consistent analysis with the reception measurements, make us set the roll-off factor to 0.6 and select Gray code. Setting up a sample rate of 500 kHz, which forces to use an interpolation factor of 256 , and a samples per symbol factor of 5 , the symbol rate is 100 kHz.

In order to proceed with the measurements it is necessary to use the VSA⁹ FSQ-70 from Rohde&Schwarz. The R&S FSQ digitalizes the analog received signal in order to measure its magnitude and phase and calculate the EVM, using some predefined modulation standards. These modulation standards, are also classified into QPSK, DQPSK, OQPSK and $\frac{\pi}{4}$ -DQPSK, such as INMARSAT, TETRA, etc [33].

Due to the GRC modulation standard, the selected modulation scheme at the VSA for the demodulation and digitalization of the signal is INMARSAT which in this case is a DQPSK standard. Setting here the symbol rate to 100 kHz, the roll-off factor to 0.6 after choosing a root raised cosine filter and also correcting the central frequency to 2.45 GHz, it is possible to proceed with the demodulation and observe the constellation and the binary sequence.

Nevertheless, the constellation schemes employed at the software and the VSA are not the same, although both are using DQPSK.

The constellation scheme handled at the modulation in the GNU Radio Companion graphical tool can be seen in the Figure 6.3. Transmitting a differential value of 0x00 between consecutive pairs of bits with a cycle module of 4 means transmitting a $\frac{\pi}{4}$ phase; when transmitting a differential value of 0x01, this changes the phase to $\frac{3\pi}{4}$ and for 0x10, to $\frac{\pi}{4}$. If the differential value 0x11 is transmitted, the carrier phase changes to $\frac{5\pi}{4}$.

Comparing this to the constellation scheme used by Rohde&Schwarz FSQ-70 VSA that can be seen in Figure 6.4, we should take into account that receiving no change in phase is receiving a 0x01, when the change is by $\frac{\pi}{2}$, a 0x00 is received.

⁹Vector Signal Analyzer

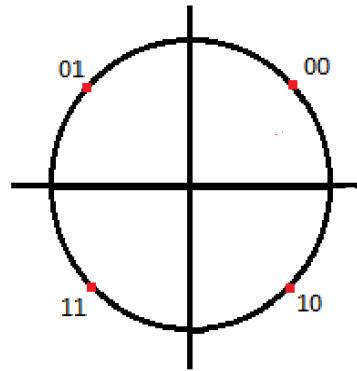


Figure 6.3: GRC modulation constellation scheme.

When the phase changes by π , the received sequence is 0x10 and when the phase is decreased by $\frac{\pi}{2}$, that implies a 0x11 reception.

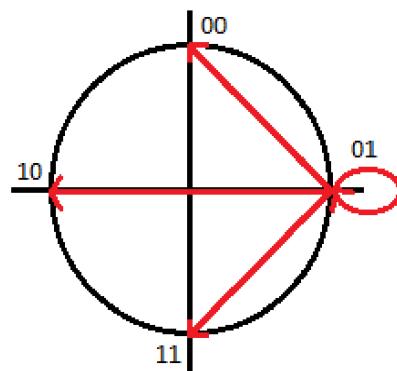


Figure 6.4: INMARSAT demodulation constellation scheme.

With all this information, transmission and reception can be easily understood.

Chapter 7

Measurements

Once the hardware and software is fully explained and the ideal characteristics of the testing signal in order to get the most useful results for prospective steps in this project is also described, the next important step is measuring the digital behavior of the transmitter and the receiver, and analyze the treatment of the given signal along the complete front-end. From this measurements, important conclusions can be taken.

7.1 Receiver

For a complete characterization of the receiver performance in the digital domain, measurements concerning its frequency response, dynamic range, attenuation response and the bit error rate were taken. Concerning the bit error rate, the most important factors which can affect this figure in a receiver comprise the synchronization between signal generator and the USRP and the SNR of the signal. It should be mentioned, that the measurements concerning the output power when receiving where taken using two different tools. The tool employed for the frequency response (Figure 7.1) was a standalone FFT solution of GNU Radio which applies a 45 dB gain, and the tool used for the attenuation response, compression point and IIP₃¹ measurements, was the FFT block included in GNU Radio Companion, which gain is around 15 dB. So that, the gain factors cannot be compared.

7.1.1 Frequency Response

For the reception path, the pass-band (Figure 7.1) is pretty similar than the expected one. It actually extends a bit wider. The test signal is generated using the Rohde&Schwarz signal generator SME-06, where a -20 dBm signal sweep from 2 GHz to 3 GHz is produced. Using an FFT in GRC the frequency response is measured.

¹Third order Input Intercept Point

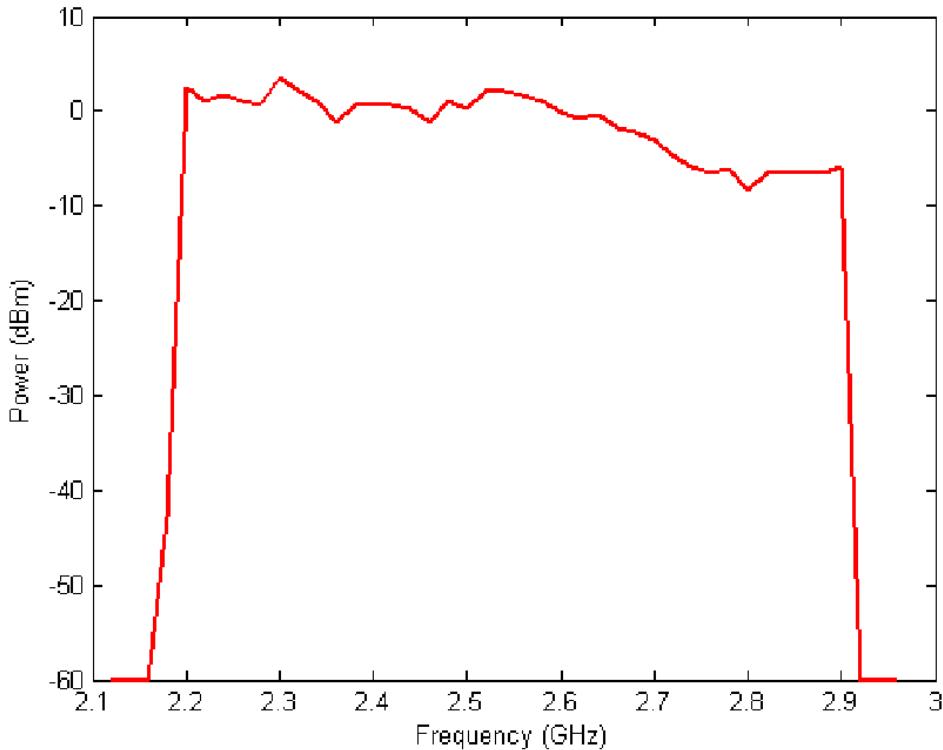


Figure 7.1: Frequency response of the USRP for reception. The power represented is after downconversion, demodulation and FFT. This measurement was taken using a standalone FFT which applied a 45 dB gain factor.

7.1.2 Dynamic Range and Attenuation Response

One of the most important parameters to characterize a system is its dynamic range, the range of power levels it can properly work in. The higher level of this range is usually given by the most sensitive element in the system to high power levels. Looking up in the USRP specifications, the power level restriction for an input impedance of $50\ \Omega$ is 3 V_{pp} for the USRP without daughterboard [11], which is 13.5 dBm for sinusoidal signals. Nevertheless, in order to have a detailed study of the signal power at the different main stages of the daughterboard components chain, Table 7.1 gathers the information with the power restrictions, gain, noise figures and compression and third order intercept points of the three main components the signal has to go through until the differential output on the daughterboard, which are basically a switch (HMC174MS8), an LNA (MGA82563) and the downconverter (AD8347).

As it can be seen from Table 7.1, the most restrictive element is the quadrature modulator responsible of the downconversion. Its maximum power level is 10 dBm. Considering the total gain of the previous components (+11.7 dB), the

Table 7.1: Maximum power, gain, IIP3, CP and noise figure of the main elements is the receiver chain [22], [23], [34].

	HMC174MS8 Switch	MGA82563 Amplifier	AD8347 Mixer	Unit
Max. Power	-	13	10	dBm
Gain	-0.8	12.25	-30	dB
IIP3	56	17.75	10.5	dBm
CP ²	36	4.85	-2	dBm
Noise Figure	0.8	2.1	-	dB

maximum power level at the input cannot be 13.5 dBm but -1.5 dBm not to break the downconverter. However, in order to avoid saturation at the mixer, since the compression point of this downconverter is -2 dBm, and from this value on the mixer is not longer linearly working, the maximum power level to guarantee a proper performance of the system must be approximately -10 dBm, taking into account the gain of the LNA and the losses of the switch and the lines between components.

The minimum power level of this range is given by the sensitivity, which is the lowest input power level for which there is a detectable output change after the USRP in GRC. To determine this value, the attenuation response is studied – the output processed power while the input power is being decreased. The last input power value that would cause any detectable output is around -75 dBm approximately. So the dynamic range goes from -10 dBm to -75 dBm, approx.

As it can be seen in the Figure 7.2, the attenuation response can be approximated by a lineal response for the input power span from -10 dBm to -70 dBm, approximately. For higher input power levels, the function is no longer linear but it bends, producing a curve. This is due to the non-linearity behavior of the USRP for all the input values. After some break point, the USRP is no longer able to output the required power to preserve a linear response. This point is known as compression point [35].

7.1.3 Compression Point

Nonlinear devices, such as amplifiers, do not have a linear response for any input values, and at some point they are not longer outputting any change at the power. This point, where the device does no longer output a consistent output power for a certain input level and the gain response is reduced by a certain amount, is called compression point. Typically, it is recourse to 1 dB-compression point, the criterion followed is to consider the compression point at the input level for which the output is 1 dB less than expected [35].

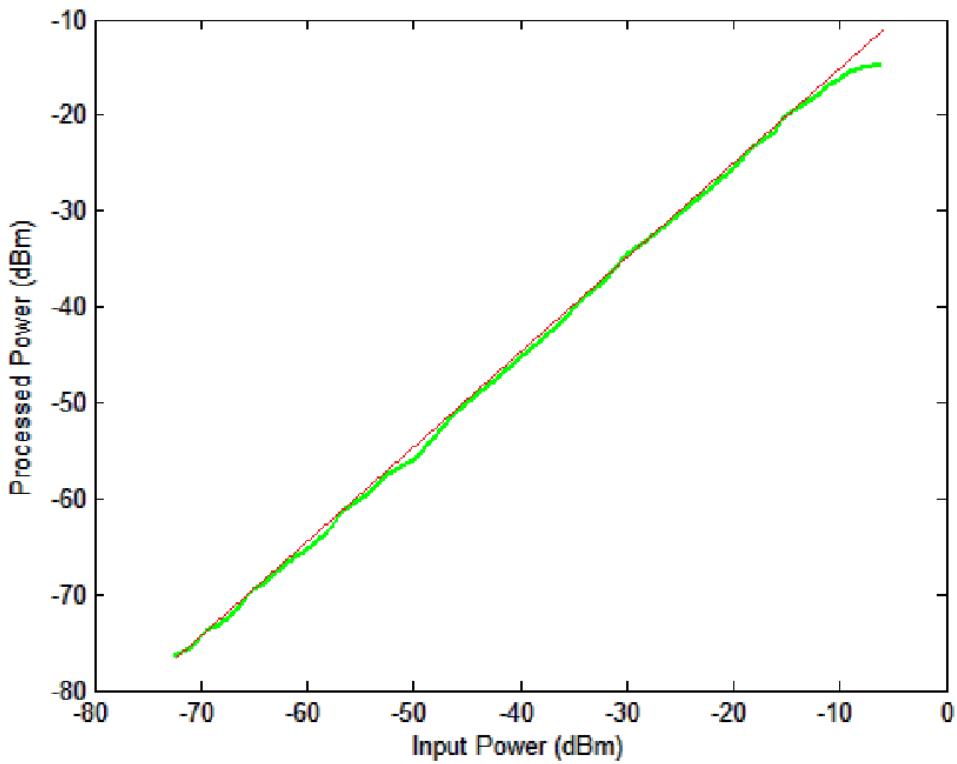


Figure 7.2: Attenuation response for the dynamic range analysis. The power represented is after downconversion, demodulation and FFT when the input frequency is 2.5 GHz. This measurement was taken using the GRC FFT block, which applied a 15 dB gain factor.

As shown in the Figure 7.3 and considering the attenuation response linear in the dynamic range, the compression point is somewhere around -9 dBm where the output response to the input breaks down. This value is an estimation due to a non-perfectly-linear measured gain, so it makes sense if we consider the information posted in Table 7.1, where it is said that the most sensitive element in terms of compression point is the mixer, which starts to compress with an input power of -2 dBm, that means -13.45 dBm at the very input of the front-end if just taking into account the ideal gain of the switch and the LNA.

It is recommended to work at input levels far away from this compression point. That is why most of the measurements are taken with input power levels of -20 dBm or -15 dBm.

7.1.4 Third Order Intercept Point

Another quality measurement for nonlinear systems is the IIP3. This parameter measures the nonlinearity of devices regarding the power level of the intermodulation products generated when there is more than a sinusoidal signal at the

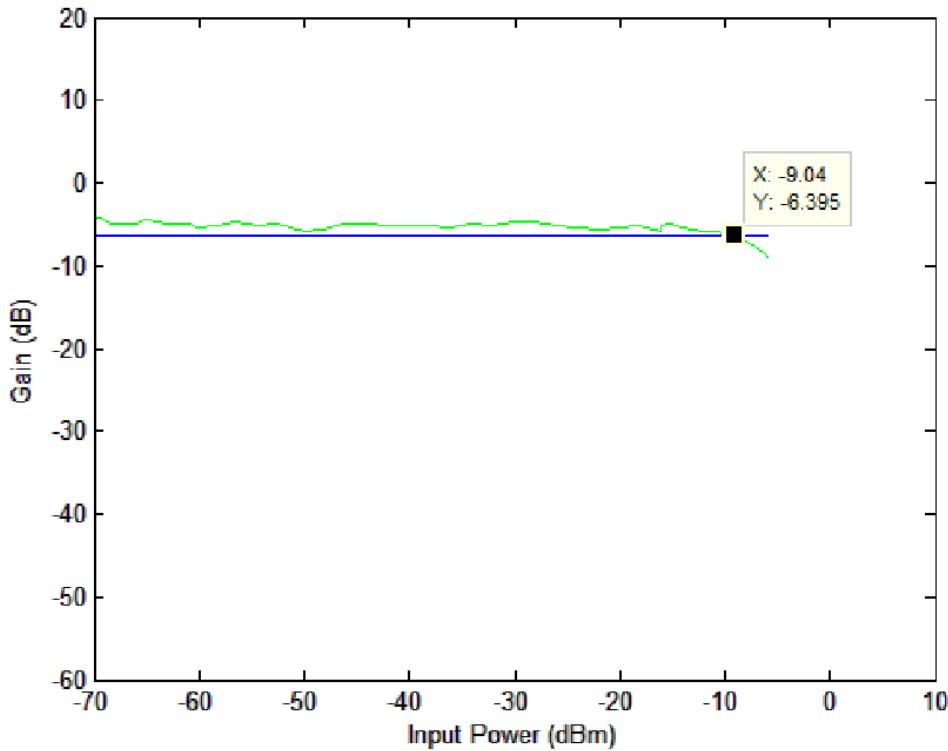


Figure 7.3: Gain response and compression point. The power represented is after downconversion, demodulation and FFT when the input frequency is 2.5 GHz. This measurement was taken using the GRC FFT block, which applied a 15 dB gain factor.

input. This point refers to the input power level to the system which produces an equally output power level in both channels and third order intermodulation products [35].

In order to establish the proper settings for this measurement, the bandwidth of the system must be firstly determined. Manually shifting the frequency separation between both channels, for an input power of -13 dBm per tone, the frequency offset limit in order to notice the third order intermodulation products is 80 kHz due to local oscillator phase noise. For a perfect and defined measurement, the chosen frequency separation is 160 kHz. A recording from GNU Radio can be seen in Figure 7.4.

Then, Figure 7.5 is obtained by measuring, for different input power values, the output for both channels and the intermodulation products. It is important not to exceed the input power of -1.5 dBm in order not to damage the mixer. For that reason the points seen at Figure 7.5 represent the real measured points. Since it is not possible to exceed this limit, the IIP3 is obtained by interpolating the real measured values to that forbidden region.

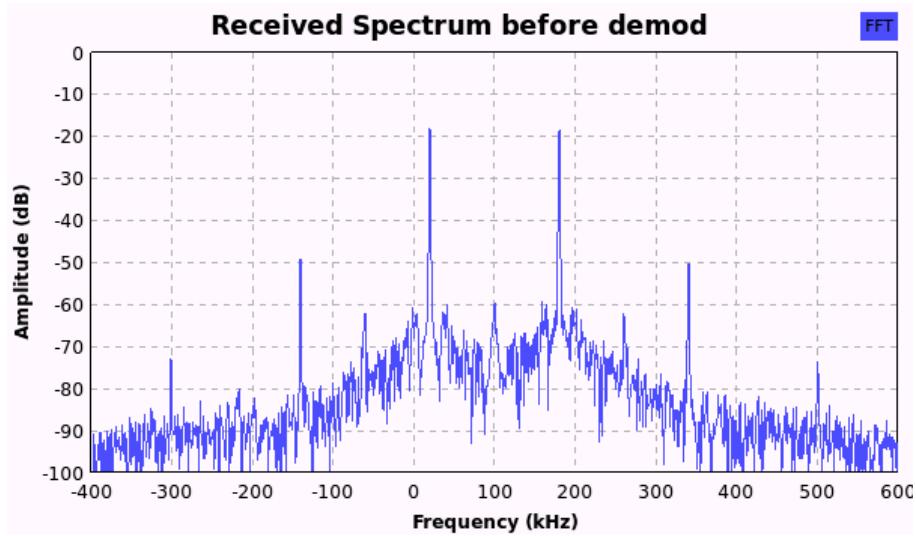


Figure 7.4: Intermodulation products of two-tone measurement. This measurement was taken using the GRC FFT block which applied a 15 dB gain factor.

The result is an IIP3 of approximately +3 dBm, value which is again a rough estimation that might fit into the expected theoretical one of -1 dBm, result of considering again the most restrictive element, the mixer, which IIP3 is 10.5 dBm and the total gain applied at the previous components in the receiver chain of 11.5 dB.

7.1.5 Bit Error Rate vs Input Power Level

Another way to characterize a receiver, is measuring the BER³ for a certain group of input power values (Figure 7.6), like simulating different physical distances of the satellite. For this purpose, a received sequence of 500000 bits, which are 250000 symbols, is recorded. Simply performing a correlation with MatLab, the sequence recorded is compared to the sent one, and the bit error rate is obtained as the quotient from dividing the number of erroneous bits over the total amount of bits received [36]. It is important to clarify that the number of bits recorded is not long enough in order to provide a reliable and consistent BER, but the values obtained can give us an idea of the behavior of the receiver when the power is being reduced.

As it can be seen from Figure 7.6, the lower the input signal power is, the higher the bit error rate is. This is basically due to the fact that the received signal has not enough SNR in order to distinguish the symbols transmitted.

³Bit Error Rate

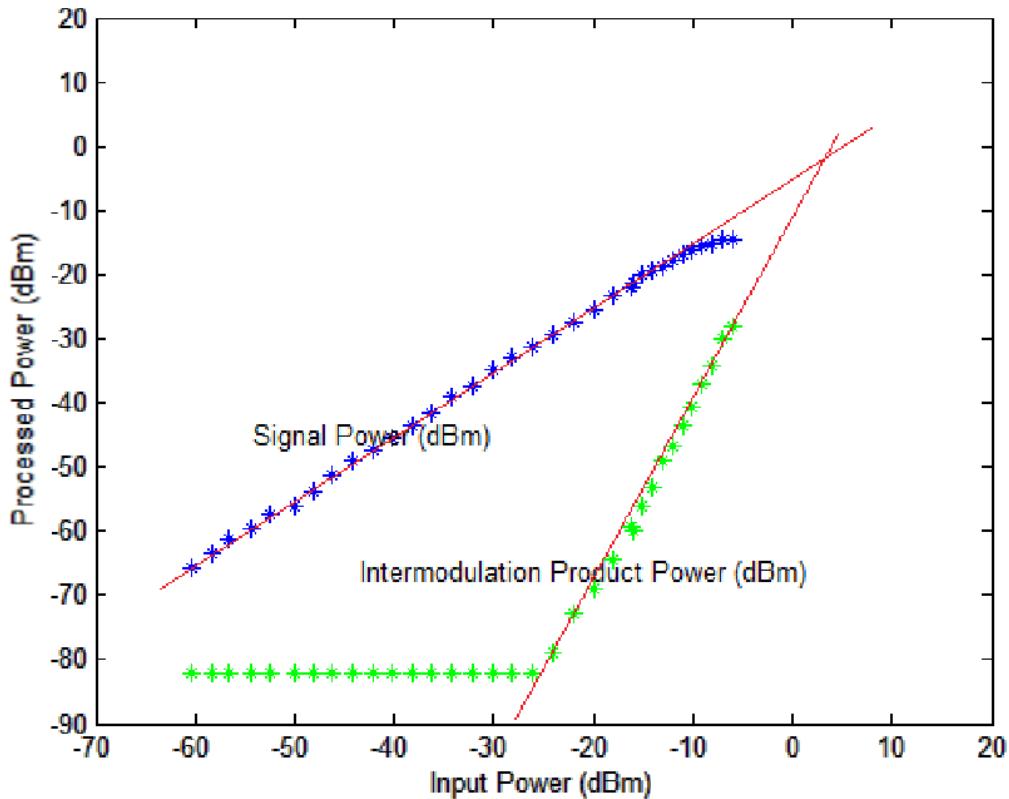


Figure 7.5: Third order intercept point. The input power represents the power per tone. The power represented is after downconversion and FFT. This measurement was taken using the GRC FFT block which applied a 15 dB gain factor.

7.1.6 Error Distribution

Once the rate of errors recorded for each power level is analyzed, the position of these errors in the full-recorded sequence, whether they appear in a burst of flawed bits or discrete bits along the sequence, is also providing very important information about the receiver's block behavior. For certain power levels, the bit error distribution is plotted. For the most powerful values, where the BER is low enough to consider a good behavior, the only errors found are at the end of the sequence. This is due to the cutting processed by MatLab on the sequence recorded in order to make the sequence of exactly 500000 bits. Where the behavior in terms of errors of our system is not so good, it can be seen that the flawed bits are equally distributed along the sequence (Figure 7.8).

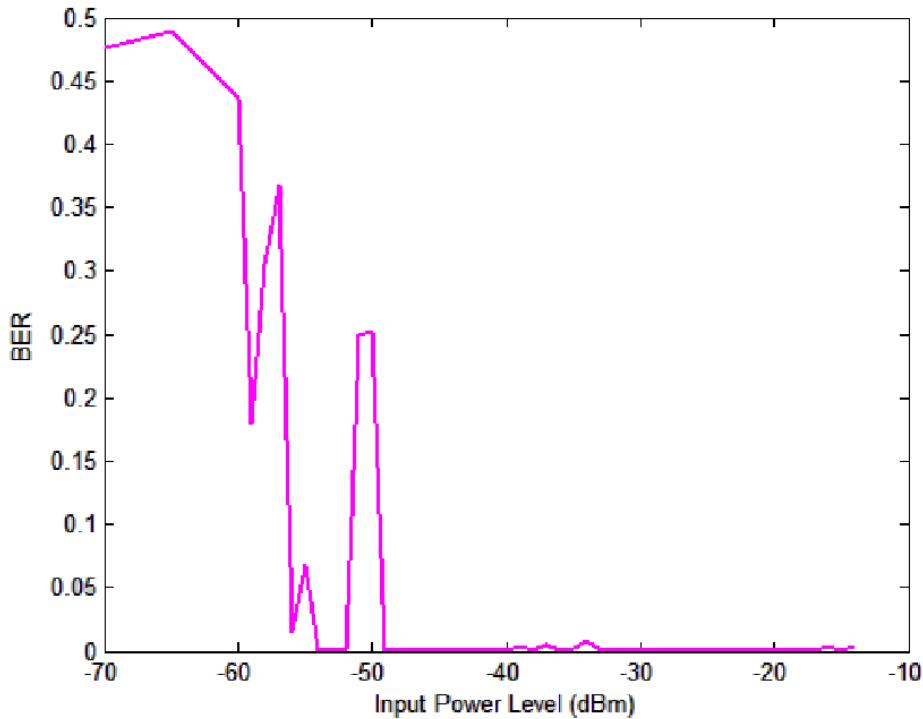


Figure 7.6: Bit error rate depending on the input power.

Bit Error Rate vs Frequency Offset

It is also interesting to know, how the frequency offset affects the number of flawed received bits. If the transmitted signal from the satellite is centered at 2.5 GHz, due to atmospheric effects, Doppler shifts and other causes, the signal reaching the ground station may have experienced some shift in frequency. Depending on the value of this frequency offset, the bit error rate can be seen in Figure 7.9.

As it is shown, the receiver supports a bandwidth of approximately 1610 Hz in which it can receive the signal with a proper enough BER. Outside this band, the Costa's Loop – used for carrier phase recovery at the demodulation block in the software tool gets unlocked and the demodulation block is not longer synchronized with the received signal.

The fact that this bandwidth is not centered at 2.5 GHz, and there is an offset of 29.5 kHz, is due to the missing external synchronization between the signal generator and the USRP. The master clock signal at the USRP is a 64 MHz signal [17] and the internal clock at the signal generator is an independent signal with a TTL⁴ level of 10 MHz [32], so external synchronization was not used.

The phase recovery is done by the synchronization procedure at the demodulation block in the GRC software, which performs sort of a Costa's Loop in order

⁴Transistor-Transistor Logic

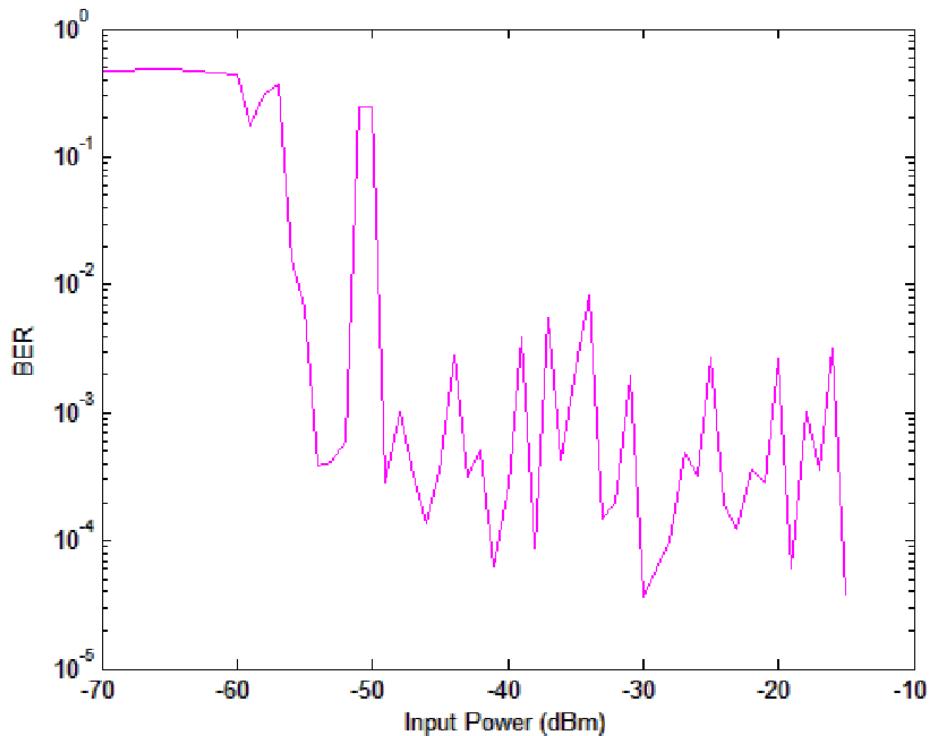


Figure 7.7: Logarithmic graph of the bit error rate.

to lock in phase and perform a proper sampling and demodulation. As a PLL⁵, this can be characterized by two parameters: lock and capture ranges:

- Lock range:** It is the frequency range of the reference signal in which the PLL can stay locked. This value depends on the VCO.
- Capture range:** Considering the PLL unlocked, it is the frequency range the PLL is able to get locked. This value depends on the phase detector and it is usually smaller.

The performed measurements provide us estimated values for those ranges as it can be seen in Figure 7.10.

7.2 Transmitter

In order to characterize the performance at the transmission path in the digital domain, the frequency response and the Error Vector Magnitude were the parameters chosen to be analyzed. The only interesting parameters that can be easily changed by the software tool is the frequency, but there is no possibility to modify the power transmitted. Hence, the EVM is given as a single value.

⁵Phase-Locked Loop

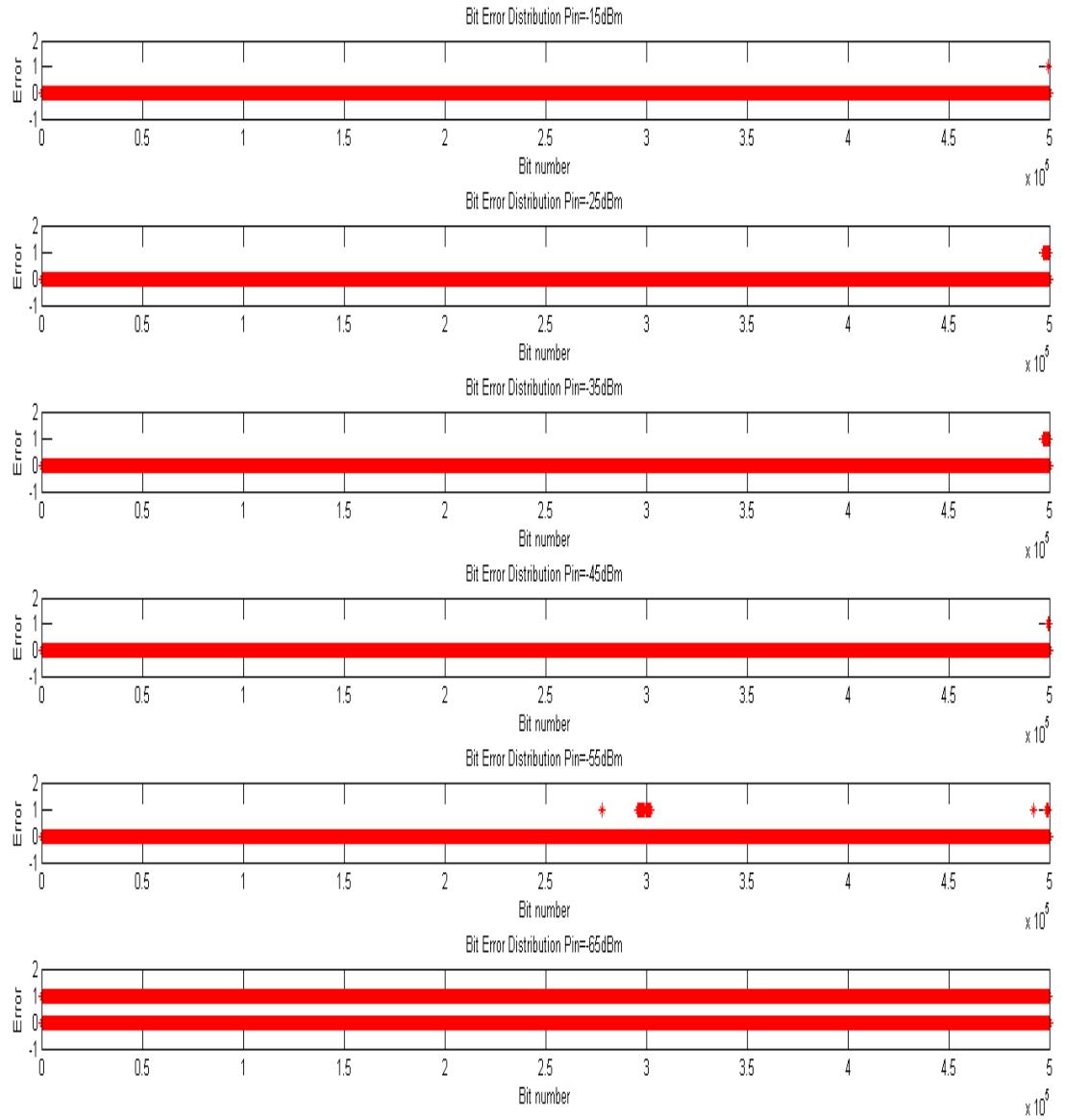


Figure 7.8: Bit error distribution.

7.2.1 Frequency Response

In order to characterize the frequency response of the USRP when transmitting, the frequency of the S-Band carrier is shifted by software from approximately 2 GHz to 3 GHz. It is observable at the Figure 7.11, that the covered band is not exactly the expected one from 2.3 GHz to 2.9 GHz, instead the pass-band ranges from 2400 MHz to 2483.5 MHz. This is due to the band-pass filter explained in Chapter 4, which frequency response can be seen in Figure 7.12. As it was said, this effect can be removed by turning the filter into a shortcircuit.

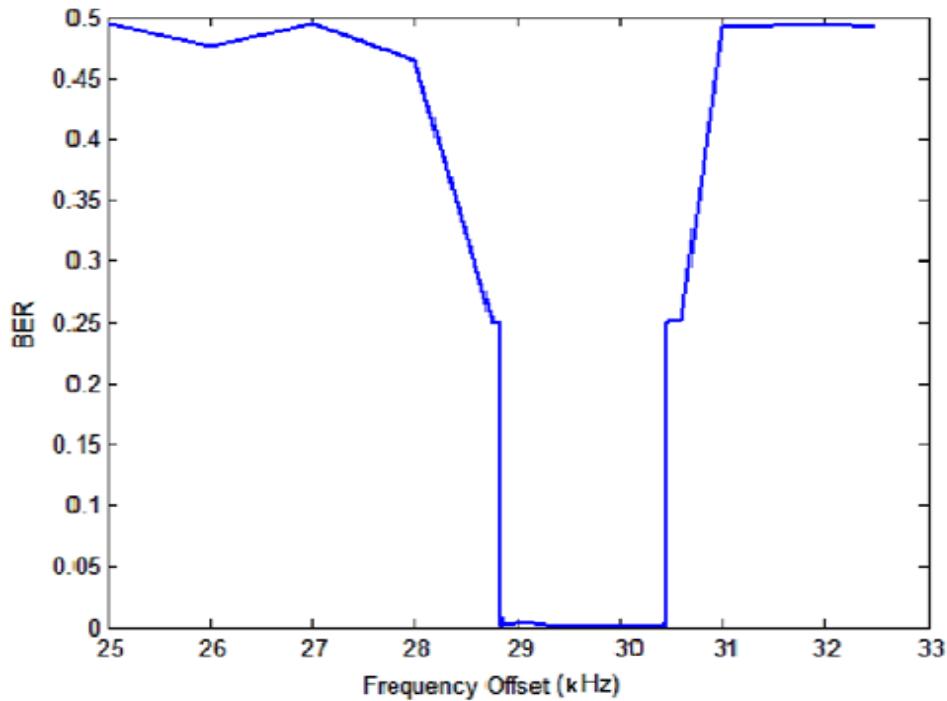


Figure 7.9: Bit error rate depending on the frequency offset.

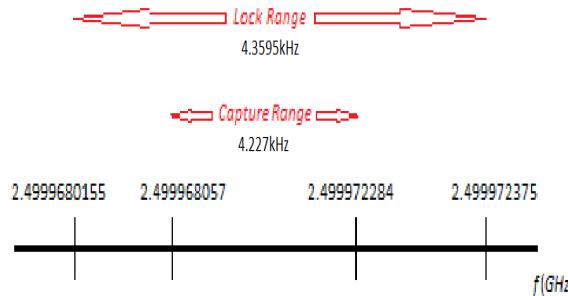


Figure 7.10: Lock and capture frequency ranges.

7.2.2 Error Vector Magnitude

The Error Vector Magnitude is a parameter used to quantify the quality of a digital radio transmission or reception. It measures the deviation from the points received comparing to reference constellation points. This deviation can be the consequence of multiple facts such as phase noise, leakage, etc [30].

In our case, using the Vector Signal Analyzer FSQ-70 from Rohde & Schwarz, the EVM is obtained to quantify the quality of the performance when transmitting. The measurement is shown in Figure 7.13. The measured EVM is 11.9 %.

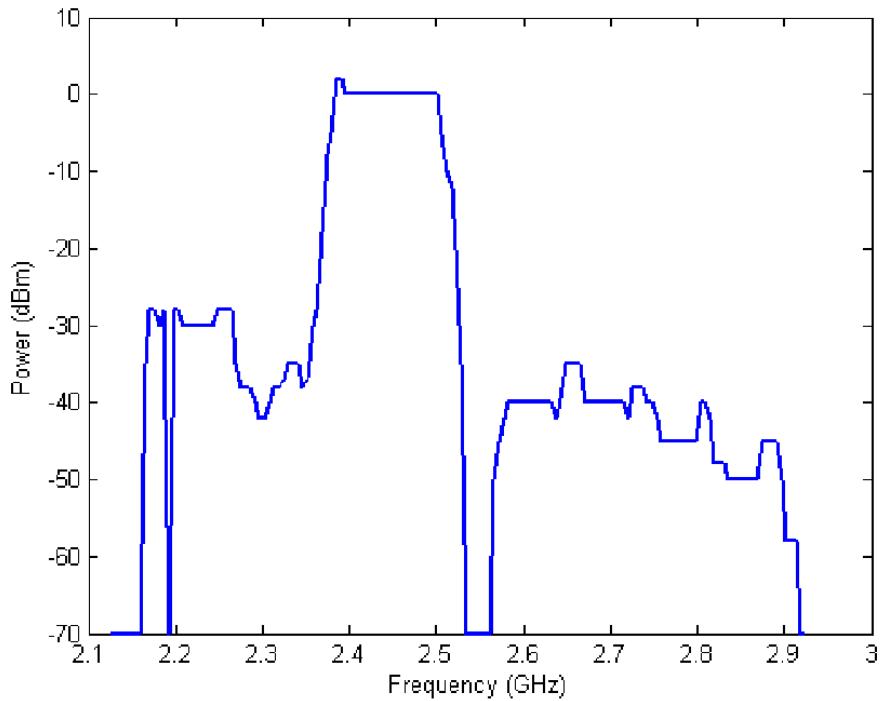


Figure 7.11: Frequency response of the USRP for transmission. The power represented is at the output.

Other results are a phase error of 4.9° , -5.18 kHz of carrier frequency error and the amplitude drop of -0.05 dBm, etc.

7.3 Communication Example

In order to clear up the signal modifications step by step, this section comprises two detailed examples for transmission and reception. The so-called T signals (from 1 to 8) represent the different signal changes since its generation until its visualization after transmission, in 8 steps. The R signals are the different signal status when receiving.

7.3.1 Reception Example

The Rohde&Schwarz SME-06 Signal Generator transmits a repeating pseudo random binary sequence of 511 bits. In our example we will focus only in the first 40 bits. Since the modulation standard employed is *DQPSK*, two bits are used to generate a symbol. The sequence is the following:

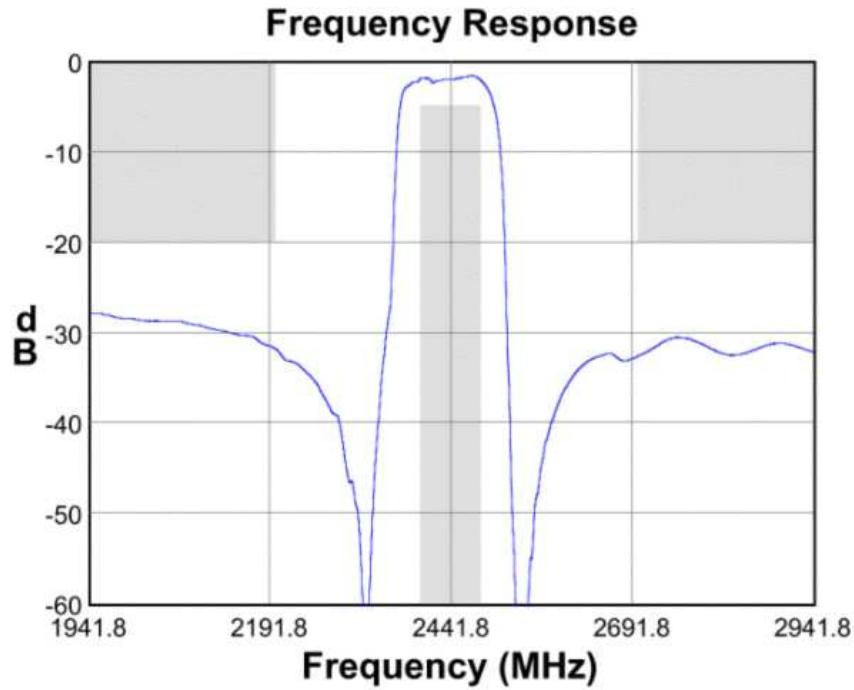


Figure 7.12: Filter frequency response [31].

R1

Generated sequence: 11 11 11 11 10 00 00 11 11 01 11 11 00 01 01 01 11 00
11 00 10

Considering the generator is using Gray code, and that the procedure to produce the differential sequence is adding each pair of bits at the input to a accumulative 4-modulus cyclical sum, the generated sequence comes as shown in steps R2, R3 and R4:

R2

In decimal (Gray coding): 2 2 2 2 3 0 0 2 2 1 2 2 0 1 1 2 0 2 0 3

R3

Accumulative sum: 2 4 6 8 11 11 11 13 15 16 18 20 20 21 22 24 24 26
26 29

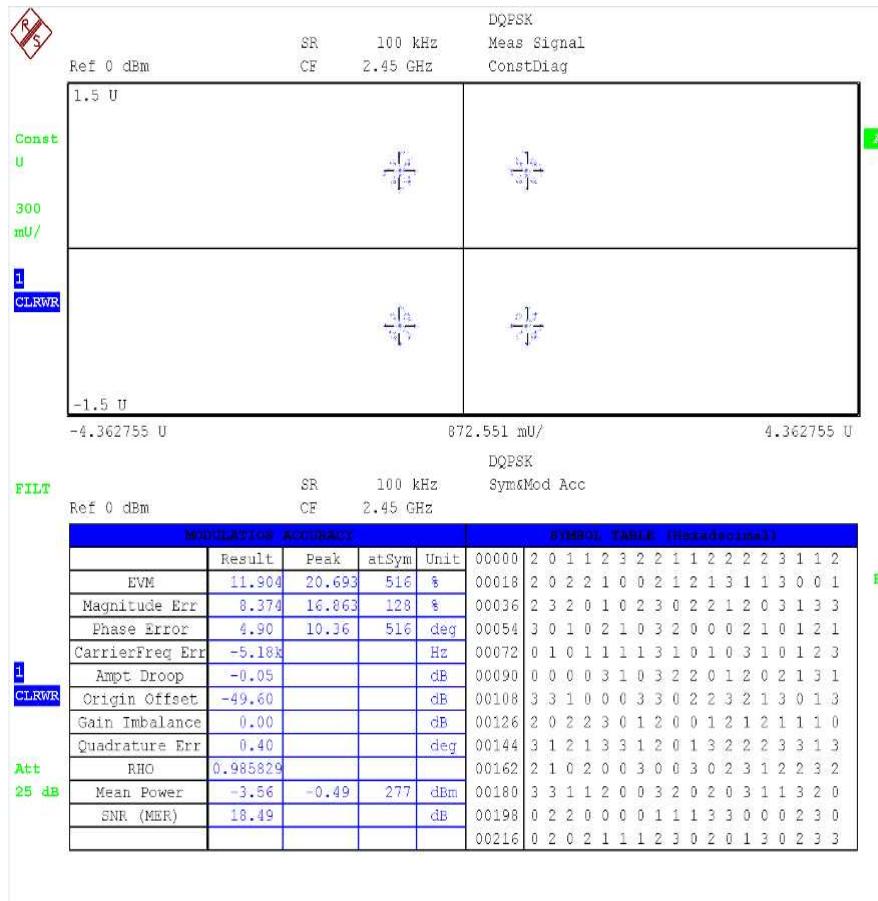


Figure 7.13: Transmitted constellation caption and error measurements.

R4

4-modulus cyclical sum: 2 0 2 0 3 3 3 1 3 0 2 0 0 1 2 0 0 2 2 1

R5

 In binary (Gray decoding): 11 00 11 00 10 10 10 01 10 00 11 00 00 01 11
 00 00 11 11 01

R6

This is the sequence which contains the differential information and now the association to the carrier signal phase is straight, considering the constellation of the modulation standard MSAT used in the Rohde&Schwarz SME-06 Signal Generator (Figure 6.1). Steps R1 to R5 are identical to the steps T1 to T5 in transmission mode.

Phase sequence: $\pi \ 0 \ \pi \ 0 \ \frac{\pi}{2} \ \frac{\pi}{2} \ \frac{\pi}{2} \ -\frac{\pi}{2} \ \frac{\pi}{2} \ 0 \ \pi \ 0 \ 0 \ -\frac{\pi}{2} \ \pi \ 0 \ 0 \ \pi \ \pi \ -\frac{\pi}{2}$

R7

This phase sequence in the carrier signal passes through the USRP and reaches the demodulation block of the GRC. This block first produces an output sequence resulting of calculating the difference between each phase value and the previous one, as follows:

Differential phase sequence: $\pi \ \pi \ \pi \ \pi \ \frac{\pi}{2} \ 0 \ 0 \ \pi \ \pi \ -\frac{\pi}{2} \ \pi \ \pi \ 0 \ -\frac{\pi}{2} \ -\frac{\pi}{2} \ \pi \ 0 \ \pi \ 0 \ \frac{\pi}{2}$

R8

Decoding this sequence with the constellation diagram used in GNU Radio Companion (Figure 6.2) and using Gray coding results in:

Decoded binary sequence: 11 11 11 11 01 00 00 11 11 10 11 11 00 10
10 11 00 11 00 01

Comparing transmitted and received sequence, it is easily proved the only change due to the unmatching constellations is solved by interchanging 0x01 and 0x10, respectively.

All the steps can be seen in the next summary table (Table 7.2).

Table 7.2: Summary table for received signal treatment steps.

R1	11	11	11	11	10	00	00	11	11	01	11	11	00	01	01	...
R2	2	2	2	2	3	0	0	2	2	1	2	2	0	1	1	...
R3	2	4	6	8	11	11	11	13	15	16	18	20	20	21	22	...
R4	2	0	2	0	3	3	3	1	3	0	2	0	0	1	2	...
R5	11	00	11	00	10	10	10	01	10	00	11	00	00	01	11	...
R6	π	0	π	0	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$-\frac{\pi}{2}$	$\frac{\pi}{2}$	0	π	0	0	$-\frac{\pi}{2}$	π	...
R7	π	π	π	π	$\frac{\pi}{2}$	0	0	π	π	$-\frac{\pi}{2}$	π	π	0	$-\frac{\pi}{2}$	$-\frac{\pi}{2}$...
R8	11	11	11	11	01	00	00	11	11	10	11	11	00	10	10	...

7.3.2 Transmission Example

T1

When transmitting a signal with GRC, the inserted decimal sequence in the vector source should be 255, 131, 223, 23 and 50, in order to get the next binary outputted sequence:

Generated sequence: 11 11 11 11 10 00 00 11 11 01 11 11 00 01 01 01 11
00 11 00 10

T2

Considering the modulator at the GRC uses Gray coding, and that the procedure to code the sequence is adding each pair of bits at the input to a accumulative 4-modulus cyclical sum, the produced sequence is obtain in steps T2, T3 and T4:

In decimal (Gray coding): 2 2 2 2 3 0 0 2 2 1 2 2 0 1 1 2 0 2 0 3

T3

Accumulative sum: 2 4 6 8 11 11 11 13 15 16 18 20 20 21 22 24 24 26
26 29

T4

4-modulus cyclical sum: 2 0 2 0 3 3 3 1 3 0 2 0 0 1 2 0 0 2 2 1

T5

In binary (Gray decoding): 11 00 11 00 10 10 10 01 10 00 11 00 00 01 11
00 00 11 11 01

T6

This sequence already contains the differential information, so just assigning directly the phase value for each group of 2 bits, considering the constellation scheme employed by the GNU Radio Companion modulation block (Figure 6.3), the carrier phase sequence is:

Phase sequence: $\frac{5\pi}{4} \frac{\pi}{4} \frac{5\pi}{4} \frac{\pi}{4} \frac{7\pi}{4} \frac{7\pi}{4} \frac{7\pi}{4} \frac{3\pi}{4} \frac{7\pi}{4} \frac{\pi}{4} \frac{5\pi}{4} \frac{\pi}{4} \frac{3\pi}{4} \frac{5\pi}{4} \frac{\pi}{4} \frac{\pi}{4} \frac{5\pi}{4} \frac{5\pi}{4}$

T7

This phase sequence in the carrier signal passes through the USRP and reaches the Rohde&Schwarz FSQ-70 vector signal analyzer, where an output sequence resulting of calculating the difference between each phase value and the previous one is obtained:

Differential phase sequence: $\pi \ \pi \ \pi \ -\frac{\pi}{2} \ 0 \ 0 \ \pi \ \pi \ \frac{\pi}{2} \ \pi \ \pi \ 0 \ \frac{\pi}{2} \ \frac{\pi}{2} \ \pi \ 0 \ \pi \ 0 \ -\frac{\pi}{2}$

T8

Decoding this sequence with the constellation diagram used in the Rohde&Schwarz FSQ-70 vector signal analyzer (Figure 6.4):

Decoded binary sequence: 10 10 10 11 01 01 10 10 00 10 10 01 00 00
10 01 10 01 11

Since the coding used to display the received symbols at the VSA is Non-Gray, the visible sequence is (Figure 7.14):

2 2 2 3 1 1 2 2 0 2 2 1 0 0 2 1 2 1 3

SYMBOL TABLE (Hexadecimal)																			
00000	2	0	2	2	1	0	0	2	1	2	1	3	2	1	2	2	3	1	
00018	1	2	2	0	2	2	1	3	0	2	1	2	1	3	1	2	2	2	2
00036	3	1	1	2	2	0	2	2	1	0	0	2	1	2	1	3	2	2	
00054	2	2	3	1	1	2	2	0	2	2	1	0	0	2	1	2	1	3	
00072	2	2	2	2	3	1	1	2	2	0	2	2	1	0	0	2	1	2	
00090	1	3	2	2	2	2	3	1	1	2	2	0	2	2	1	0	0	2	
00108	1	2	1	3	2	2	2	2	3	1	1	2	2	0	2	2	1	0	
00126	0	2	1	2	1	3	2	2	2	2	3	1	1	2	2	0	2	2	
00144	1	0	0	2	1	2	1	3	2	2	2	2	3	1	1	2	2	0	
00162	2	2	1	0	0	2	1	2	1	3	2	2	2	2	3	1	1	2	
00180	2	0	2	2	1	0	0	2	1	2	1	3	2	2	2	2	3	1	
00198	1	2	2	0	2	2	1	0	0	2	1	2	1	3	2	2	2	2	
00216	3	1	1	2	2	0	2	2	1	0	0	2	1	2	1	3	2	2	

Figure 7.14: Real transmitted sequence.

All the steps can be seen in the next summary table (Table 7.3).

Table 7.3: Summary table for transmitted signal treatment steps.

T1	11	11	11	11	10	00	00	11	11	01	11	11	00	01	01	...
T2	2	2	2	2	3	0	0	2	2	1	2	2	0	1	1	...
T3	2	4	6	8	11	11	11	13	15	16	18	20	20	21	22	...
T4	2	0	2	0	3	3	3	1	3	0	2	0	0	1	2	...
T5	11	00	11	00	10	10	10	01	10	00	11	00	00	01	11	...
T6	$\frac{5\pi}{4}$	$\frac{\pi}{4}$	$\frac{5\pi}{4}$	$\frac{\pi}{4}$	$\frac{-\pi}{4}$	$\frac{-\pi}{4}$	$\frac{-\pi}{4}$	$\frac{3\pi}{4}$	$\frac{-\pi}{4}$	$\frac{\pi}{4}$	$\frac{5\pi}{4}$	$\frac{\pi}{4}$	$\frac{\pi}{4}$	$\frac{3\pi}{4}$	$\frac{5\pi}{4}$...
T7	π	π	π	$\frac{-\pi}{2}$	0	0	π	π	$\frac{\pi}{2}$	π	π	0	$\frac{\pi}{2}$	$\frac{\pi}{2}$...	
T8	10	10	10	11	01	01	10	10	00	10	10	01	00	00	...	

Chapter 8

Conclusions

In this thesis, I investigated the possible use of the software defined radio USRP1 by Ettus as the main hardware component for an RF front-end for the satellite ground station at the Institute of Telecommunications at the Vienna University of Technology. After summarizing the parameters required of the satellite missions considered and the ground station layout envisioned in Chapter 2 and Chapter 3, I analyzed the USRP hardware in Chapter 4 and the corresponding GNU Radio Companion software in Chapter 5. For the transmission and reception measurements on the system, I selected a specific QPSK signal which I have described in Chapter 6. The measurements are presented in Chapter 7.

I fully characterized the system for the transmission path from the digital side to the RF output and for the reception path from RF input to the digital output in Chapter 7. Before the measurements I investigated the expected limits in Chapter 4. The measurements include frequency response, gain, EVM, compression point, IIP3, dynamic range and BER. Since lots of the measurements characterize the system on a specific QPSK signal, I investigated the modulation and demodulation steps and give great details in Chapter 5, Chapter 6 and Chapter 7.3.

For the final purpose of this ongoing project, which is the satellite communication with the MOST, COROT and BRITE missions, an adaptation procedure has to be carried out. In terms of frequency, as a first step, in order to enable the full bandwidth when transmitting, the filter for ISM applications must be removed. Once both transmission and reception bands are fully available from 2.3 to 2.9 GHz, the next task is to shift the frequency band covered to the satellites' working spectrum. Considering a fixed IF in the range from 100 MHz to approximately 500 MHz, the synthesizer used, the ADF4360-0, should be replaced for an ADF4360-2 in order to cover the band of interest from 2.00 GHz to 2.45 GHz. Further, amplifiers are necessary to adapt the signal power range of the USRP to the power levels of the satellites. When necessary, also modifications to the GRC blocks are possible, to provide different modulation schemes. After these modifications a deployment of the USRP in the ground station is possible.

Another prospective future application for the USRP is the use of the "RFX2400" daughterboard in a standalone configuration as the analog RF front-end to existing modems. Here an adapter is necessary. This adapter has to provide both

input and output interfaces for digital and analog signals, replacing the digital and analog connections between daughterboard and motherboard. A microcontroller is then necessary to set up daughterboard and the power has to be provided by a separate power supply. This adapter would further enable an exclusive measurement of the daughterboard's performance without the motherboard and GRC.

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List of Abbreviations

ADC	Analog-to-Digital Converter
APCO25	Association of Public Safety Communication Officials - Project 25
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
BRITE	BRILight Target Explorer
BW	BandWidth
CIC	Cascaded Integrator-Comb
COROT	COndensation ROTation and planetary TRANSits
CP	Compression Point
DAC	Digital-to-Analog Converter
DDC	Digital Down Converter
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DUC	Digital Up Converter
EIRP	Equivalent Isotropically Radiated Power
EVM	Error Vector Magnitude
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
 FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying
GEO	Geostationary Earth Orbit
GFSK	Gaussian Frequency Shift Keying
GRC	GNU Radio Companion
GUI	Graphical User Interface
IF	Intermediate Frequency
IIP3	Third order Input Intercept Point
INMARSAT	INternational MARitime SATellite
ISM	Industrial, Scientific, Medical
ISI	Inter-Symbol Interference
LEO	Low Earth Orbit
LHCP	Left Handed Circular Polarization
LNA	Low Noise Amplifier
LP	Linear Polarization
LPF	Low-Pass Filter
LSB	Least Significant Bit
MEO	Medium Earth Orbit

MIMO	<u>M</u> ultiple <u>I</u> nput <u>M</u> ultiple <u>O</u> utput
MMIC	<u>M</u> onolithic <u>M</u> icrowave <u>I</u> ntegrated <u>C</u> ircuits
MOST	<u>M</u> icrovariability and <u>O</u> scillations of <u>S</u> Tars
MSAT	<u>M</u> obile <u>S</u> ATellite
MSB	<u>M</u> ost <u>S</u> ignificant <u>B</u> it
NADC	<u>N</u> orth <u>A</u> merican <u>D</u> igital <u>C</u> ellular
NCO	<u>N</u> umerical- <u>C</u> ontrolled <u>O</u> scillator
OQPSK	<u>O</u> ffset <u>Q</u> uadrature <u>P</u> hase <u>S</u> hift <u>K</u> eying
PDC	<u>P</u> ersonal <u>D</u> igital <u>C</u> ellular
PLL	<u>P</u> hase- <u>L</u> ocked <u>L</u> oop
PSK	<u>P</u> hase <u>S</u> hift <u>K</u> eying
QPSK	<u>Q</u> uadrature <u>P</u> hase <u>S</u> hift <u>K</u> eying
RF	<u>R</u> adio <u>F</u> requency
RHCP	<u>R</u> ight <u>H</u> anded <u>C</u> ircular <u>P</u> olarization
RRC	<u>R</u> oot <u>R</u> aised <u>C</u> osine
SMA	<u>S</u> ub- <u>M</u> iniature <u>v</u> ersion <u>A</u>
SNR	<u>S</u> ignal to <u>NR</u> atio
TCP	<u>T</u> ransmission <u>C</u> ontrol <u>P</u> rotocol
TDMA	<u>T</u> ime <u>D</u> ivision <u>M</u> ultiple <u>A</u> ccess
TETRA	<u>T</u> Errestrial <u>T</u> runked <u>R</u> adio
TFTS	<u>T</u> ime and <u>F</u> requency <u>T</u> ransfer <u>S</u> tandard
TNC	<u>T</u> erminal <u>N</u> ode <u>C</u> ontroller
TTL	<u>T</u> ransistor- <u>T</u> ransistor <u>L</u> ogic
UDP	<u>U</u> ser <u>D</u> atagram <u>P</u> rotocol
UHF	<u>U</u> ltra <u>H</u> igh <u>F</u> requency
USB	<u>U</u> niversal <u>S</u> erial <u>B</u> us
USRP	<u>U</u> niversal <u>S</u> oftware <u>R</u> adio <u>P</u> eripheral
VCO	<u>V</u> oltage <u>C</u> ontrolled <u>O</u> scillator
VCTCXO	<u>V</u> oltage <u>C</u> ontrolled <u>T</u> emperature <u>C</u> ompensated <u>C</u> rystal <u>O</u> scillator
VGS	<u>V</u> ienna <u>G</u> round <u>S</u> tation
VHF	<u>V</u> ery <u>H</u> igh <u>F</u> requency
VSA	<u>V</u> ector <u>S</u> ignal <u>A</u> alyzer
WLAN	<u>W</u> ireless <u>L</u> ocal <u>A</u> rea <u>N</u> etwork
XML	<u>e</u> Xtensible <u>M</u> arkup <u>L</u> anguage

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