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ENGS 33 LAB 5

Lab 5 Discussion

1. Everything in this lab ended up being fully functional. No errors can be reported.
2. There were numerous problems encountered throughout the lab, most of which were solved by debugging and observing the simulation and waveform response. One notable issue encountered was that initially, our code would not run correctly on the FPGA, despite working perfectly in simulation. This was solved by removing redundant signal assignments and two unnecessary wait states, which resulted in the elimination of two of our latch warnings, and caused the code to function as intended.
3. This was without a doubt, the hardest and most involved lab in this class. As I type this, half of the class is in the digital lab frantically trying to get their code to work on the FPGA. However, this also was one of the most interesting and rewarding labs we have done. The best aspect was that it was cumulative: we built most of the components in previous labs, and then finally linked them all together to create our top level module. Seeing the fruits of our labor display on the putty window was one of the most rewarding things I have experienced with this class, and gave me an appreciation for how much goes into programming the everyday devices that we all take for granted. In the future, I think more emphasis should be placed on *WHY* things can simulate correctly and yet not work in hardware. Some of the aspects of XILINX and the FPGA interface are still somewhat cryptic to many students in the class, and we often just outsource things we don’t understand to the TA’s. More time should be spent learning about .UCF files and the fundamental aspects of going from VHDL code on a computer to the actual pins and voltage levels on the FPGA. Overall, I thought this was the best lab yet, however it was brutal and I don’t’ think that sentiment was 100% shared by other classmates.