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ENGS 31

POSTLAB SYNTHESIS REPORT

Synthesis

1. High level HDL Synthesis (by component) in the VHDL model :
   * Baud Rate Generator <brg>:
     + Found 1-bit register for signal <br\_tick16>.
     + Found 4-bit up counter for signal <brcount>
   * Serial Receiver <SerialRX>:
     + Found 1 4-state FSM
     + Found 5-bit up counter for signal <br\_count>.
     + Found 8-bit register for signal <preg>.
     + Found 1-bit register for signal <SB\_SAMPLE\_COUNT>.
     + Found 1-bit register for signal <SB\_STOPBIT>.
     + Found 4-bit up counter for signal <shift\_count>.
     + Found 10-bit register for signal <shreg>.
     + Found 1-bit register for signal <SyncReg1>.
     + Found 1-bit register for signal <SyncReg2>
   * Serial Transmitter <SerialTx>:
     + Found 1 5-state FSM
     + Found 4-bit up counter for signal <br\_cnt>.
     + Found 4-bit down counter for signal <tx\_ctr>.
     + Found 10-bit register for signal <tx\_reg>.
   * Lab 4 top level summary:

Macro Statistics #

* + - # Counters : 5
      * 4-bit down counter : 1
      * 4-bit up counter : 3
      * 5-bit up counter : 1
    - # Registers : 17
      * 1-bit register : 15
      * 10-bit register : 1
      * 8-bit register : 1

1. Low level HDL synthesis (LUTs, Flip Flops, Slices, IO/Buffers etc.):
   * Device utilization summary:

Selected Device: 3s100ecp132-4

* + - Number of Slices: 62 out of 960 6%
    - Number of Slice Flip Flops: 75 out of 1920 3%
    - Number of 4 input LUTs: 105 out of 1920 5%
      * Number used as logic: 104
      * Number used as Shift registers: 1
    - Number of IOs: 16
    - Number of bonded IOBs: 15 out of 83 18%
    - # IO Buffers 14
      * # IBUF 1
      * # OBUF 13
    - Number of GCLKs: 1 out of 24 4%

1. Pathway Analysis:
   * Critical Timing Path:

Data Path: U3/br\_cnt\_3 to U3/curr\_state\_FSM\_FFd3

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FDE:C->Q 3 0.591 0.706 U3/br\_cnt\_3 (U3/br\_cnt\_3)

LUT4:I0->O 1 0.704 0.455 U3/curr\_state\_FSM\_FFd3-In21\_SW0 (N14)

LUT3:I2->O 1 0.704 0.424 U3/curr\_state\_FSM\_FFd3-In21\_SW1 (N16)

LUT4:I3->O 1 0.704 0.000 U3/curr\_state\_FSM\_FFd3-In281 (U3/curr\_state\_FSM\_FFd3-In28)

FDS:D 0.308 U3/curr\_state\_FSM\_FFd3

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* + Maximum allowable clock frequency: 217.580MHZ
  + Maximum delay: 4.596ns
    - 3.011ns logic, 1.585ns route (65.5% logic, 34.5% route)