Release 14.4 - xst P.49d (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: Lab4.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "Lab4.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "Lab4"

Output Format : NGC

Target Device : xc3s100e-4-cp132

---- Source Options

Top Module Name : Lab4

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 24

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

---- Other Options

Cores Search Directories : {".." }

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\* HDL Compilation \*

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Compiling vhdl file "C:/aaditya/lab\_4/brg.vhd" in Library work.

Architecture behavioral of Entity brg is up to date.

Compiling vhdl file "C:/aaditya/lab\_4/SerialRX.vhd" in Library work.

Architecture behavioral of Entity serialrx is up to date.

Compiling vhdl file "C:/aaditya/lab\_4/SerialTx2.vhd" in Library work.

Architecture behavioral of Entity serialtx is up to date.

Compiling vhdl file "C:/aaditya/lab\_4/Lab4.vhd" in Library work.

Entity <lab4> compiled.

Entity <lab4> (Architecture <behavioral>) compiled.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for entity <Lab4> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <brg> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <SerialRX> in library <work> (architecture <behavioral>).

Analyzing hierarchy for entity <SerialTx> in library <work> (architecture <behavioral>).

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\* HDL Analysis \*

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Analyzing Entity <Lab4> in library <work> (Architecture <behavioral>).

WARNING:Xst:2211 - "C:/aaditya/lab\_4/Lab4.vhd" line 104: Instantiating black box module <mux7seg>.

Entity <Lab4> analyzed. Unit <Lab4> generated.

Analyzing Entity <brg> in library <work> (Architecture <behavioral>).

Entity <brg> analyzed. Unit <brg> generated.

Analyzing Entity <SerialRX> in library <work> (Architecture <behavioral>).

Entity <SerialRX> analyzed. Unit <SerialRX> generated.

Analyzing Entity <SerialTx> in library <work> (Architecture <behavioral>).

Entity <SerialTx> analyzed. Unit <SerialTx> generated.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <brg>.

Related source file is "C:/aaditya/lab\_4/brg.vhd".

Found 1-bit register for signal <br\_tick16>.

Found 4-bit up counter for signal <brcount>.

Summary:

inferred 1 Counter(s).

inferred 1 D-type flip-flop(s).

Unit <brg> synthesized.

Synthesizing Unit <SerialRX>.

Related source file is "C:/aaditya/lab\_4/SerialRX.vhd".

WARNING:Xst:646 - Signal <shreg<0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found finite state machine <FSM\_0> for signal <curr\_state>.

-----------------------------------------------------------------------

| States | 4 |

| Transitions | 7 |

| Inputs | 3 |

| Outputs | 4 |

| Clock | Clk25 (rising\_edge) |

| Power Up State | off |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 5-bit up counter for signal <br\_count>.

Found 8-bit register for signal <preg>.

Found 1-bit register for signal <SB\_SAMPLE\_COUNT>.

Found 1-bit register for signal <SB\_STOPBIT>.

Found 4-bit up counter for signal <shift\_count>.

Found 10-bit register for signal <shreg>.

Found 1-bit register for signal <SyncReg1>.

Found 1-bit register for signal <SyncReg2>.

Summary:

inferred 1 Finite State Machine(s).

inferred 2 Counter(s).

inferred 22 D-type flip-flop(s).

Unit <SerialRX> synthesized.

Synthesizing Unit <SerialTx>.

Related source file is "C:/aaditya/lab\_4/SerialTx2.vhd".

INFO:Xst:1799 - State ssync is never reached in FSM <curr\_state>.

Found finite state machine <FSM\_1> for signal <curr\_state>.

-----------------------------------------------------------------------

| States | 5 |

| Transitions | 8 |

| Inputs | 3 |

| Outputs | 3 |

| Clock | Clk25 (rising\_edge) |

| Power Up State | sidle |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 4-bit up counter for signal <br\_cnt>.

Found 4-bit down counter for signal <tx\_ctr>.

Found 10-bit register for signal <tx\_reg>.

Summary:

inferred 1 Finite State Machine(s).

inferred 2 Counter(s).

inferred 10 D-type flip-flop(s).

Unit <SerialTx> synthesized.

Synthesizing Unit <Lab4>.

Related source file is "C:/aaditya/lab\_4/Lab4.vhd".

WARNING:Xst:647 - Input <tx\_start> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:653 - Signal <tie\_low> is used but never assigned. This sourceless signal will be automatically connected to value 0.

Unit <Lab4> synthesized.

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HDL Synthesis Report

Macro Statistics

# Counters : 5

4-bit down counter : 1

4-bit up counter : 3

5-bit up counter : 1

# Registers : 17

1-bit register : 15

10-bit register : 1

8-bit register : 1

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\* Advanced HDL Synthesis \*

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Analyzing FSM <FSM\_1> for best encoding.

Optimizing FSM <U3/curr\_state/FSM> on signal <curr\_state[1:3]> with gray encoding.

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State | Encoding

--------------------

sidle | 000

ssync | unreached

sload | 001

swait | 011

sshift | 110

sdone | 010

--------------------

Analyzing FSM <FSM\_0> for best encoding.

Optimizing FSM <U2/curr\_state/FSM> on signal <curr\_state[1:2]> with gray encoding.

--------------------

State | Encoding

--------------------

off | 00

count | 01

shift | 11

output | 10

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Reading core <../mux7seg.ngc>.

Loading core <mux7seg> for timing and area information for instance <U\_aaditya>.

WARNING:Xst:2677 - Node <shreg\_0> of sequential type is unconnected in block <U2>.

WARNING:Xst:2677 - Node <shreg\_0> of sequential type is unconnected in block <SerialRX>.

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Advanced HDL Synthesis Report

Macro Statistics

# FSMs : 2

# Counters : 5

4-bit down counter : 1

4-bit up counter : 3

5-bit up counter : 1

# Registers : 32

Flip-Flops : 32

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\* Low Level Synthesis \*

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Optimizing unit <Lab4> ...

Optimizing unit <SerialRX> ...

Optimizing unit <SerialTx> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Lab4, actual ratio is 6.

Final Macro Processing ...

Processing Unit <Lab4> :

Found 2-bit shift register for signal <U2/SyncReg2>.

Unit <Lab4> processed.

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Final Register Report

Macro Statistics

# Registers : 56

Flip-Flops : 56

# Shift Registers : 1

2-bit shift register : 1

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : Lab4.ngr

Top Level Output File Name : Lab4

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 16

Cell Usage :

# BELS : 144

# GND : 2

# INV : 7

# LUT1 : 15

# LUT2 : 11

# LUT3 : 24

# LUT3\_L : 2

# LUT4 : 41

# LUT4\_D : 2

# LUT4\_L : 2

# MUXCY : 15

# MUXF5 : 5

# VCC : 2

# XORCY : 16

# FlipFlops/Latches : 75

# FD : 19

# FDE : 23

# FDR : 5

# FDRE : 20

# FDRSE : 3

# FDS : 3

# FDSE : 2

# Shift Registers : 1

# SRL16 : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 14

# IBUF : 1

# OBUF : 13

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Device utilization summary:

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Selected Device : 3s100ecp132-4

Number of Slices: 62 out of 960 6%

Number of Slice Flip Flops: 75 out of 1920 3%

Number of 4 input LUTs: 105 out of 1920 5%

Number used as logic: 104

Number used as Shift registers: 1

Number of IOs: 16

Number of bonded IOBs: 15 out of 83 18%

Number of GCLKs: 1 out of 24 4%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

Clk25 | BUFGP | 76 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -4

Minimum period: 4.596ns (Maximum Frequency: 217.580MHz)

Minimum input arrival time before clock: 2.059ns

Maximum output required time after clock: 8.070ns

Maximum combinational path delay: No path found

Timing Detail:

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All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'Clk25'

Clock period: 4.596ns (frequency: 217.580MHz)

Total number of paths / destination ports: 584 / 157

-------------------------------------------------------------------------

Delay: 4.596ns (Levels of Logic = 3)

Source: U3/br\_cnt\_3 (FF)

Destination: U3/curr\_state\_FSM\_FFd3 (FF)

Source Clock: Clk25 rising

Destination Clock: Clk25 rising

Data Path: U3/br\_cnt\_3 to U3/curr\_state\_FSM\_FFd3

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDE:C->Q 3 0.591 0.706 U3/br\_cnt\_3 (U3/br\_cnt\_3)

LUT4:I0->O 1 0.704 0.455 U3/curr\_state\_FSM\_FFd3-In21\_SW0 (N14)

LUT3:I2->O 1 0.704 0.424 U3/curr\_state\_FSM\_FFd3-In21\_SW1 (N16)

LUT4:I3->O 1 0.704 0.000 U3/curr\_state\_FSM\_FFd3-In281 (U3/curr\_state\_FSM\_FFd3-In28)

FDS:D 0.308 U3/curr\_state\_FSM\_FFd3

----------------------------------------

Total 4.596ns (3.011ns logic, 1.585ns route)

(65.5% logic, 34.5% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk25'

Total number of paths / destination ports: 1 / 1

-------------------------------------------------------------------------

Offset: 2.059ns (Levels of Logic = 1)

Source: TXD (PAD)

Destination: U2/Mshreg\_SyncReg2 (FF)

Destination Clock: Clk25 rising

Data Path: TXD to U2/Mshreg\_SyncReg2

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 1 1.218 0.420 TXD\_IBUF (TXD\_IBUF)

SRL16:D 0.421 U2/Mshreg\_SyncReg2

----------------------------------------

Total 2.059ns (1.639ns logic, 0.420ns route)

(79.6% logic, 20.4% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk25'

Total number of paths / destination ports: 156 / 13

-------------------------------------------------------------------------

Offset: 8.070ns (Levels of Logic = 5)

Source: U\_aaditya/adcount\_0 (FF)

Destination: seg<0> (PAD)

Source Clock: Clk25 rising

Data Path: U\_aaditya/adcount\_0 to seg<0>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDE:C->Q 14 0.591 1.175 adcount\_0 (adcount<0>)

LUT3:I0->O 1 0.704 0.000 Mmux\_muxy\_3 (Mmux\_muxy\_3)

MUXF5:I1->O 7 0.321 0.883 Mmux\_muxy\_2\_f5 (muxy<0>)

LUT4:I0->O 1 0.704 0.420 seg<0>1 (seg<0>)

end scope: 'U\_aaditya'

OBUF:I->O 3.272 seg\_0\_OBUF (seg<0>)

----------------------------------------

Total 8.070ns (5.592ns logic, 2.478ns route)

(69.3% logic, 30.7% route)

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 5.62 secs

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Total memory usage is 264760 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 6 ( 0 filtered)

Number of infos : 1 ( 0 filtered)