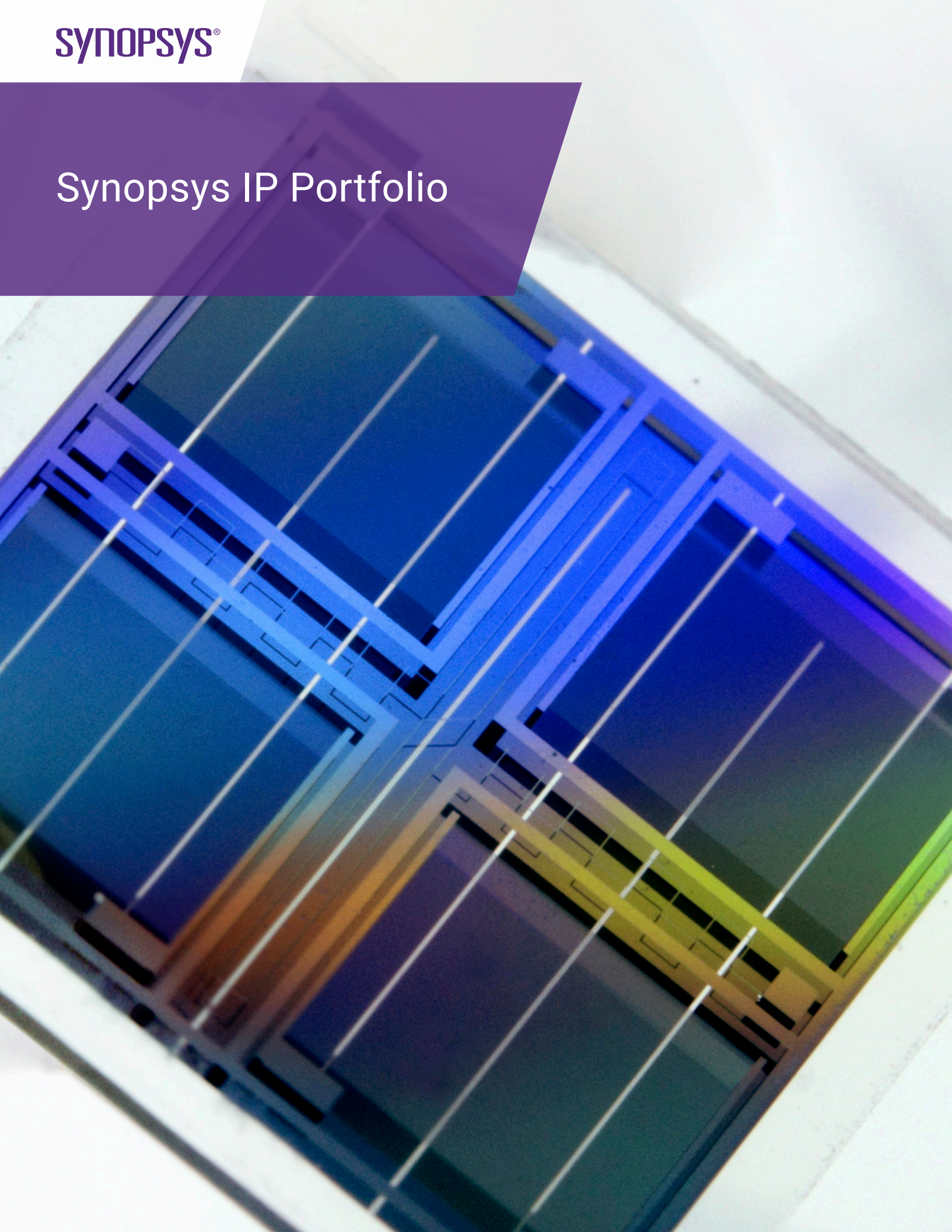
SYNOPSYS®

Synopsys IP Portfolio



Broad IP Portfolio

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, In-chip PVT monitors, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems.

To accelerate your product development cycle, Synopsys' IP Accelerated initiative offers SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support.

Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

Interface IP													
USB	Processes										Controllers/ Features	HS Access & Test	Verification IP
	55/65 nm	40/45 nm	28/22 nm	20 nm	14/ 16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET			
USB4						✓		✓	✓	✓	Device, Router, Host Router	✓	✓
USB-C 3.2 / DisplayPort 1.4TX						✓		✓		✓	Device, Host, DisplayPort Tx, HDCP ESM,DSC	✓	✓
USB 3.2								✓	✓	✓	Device, Host	✓	✓
USB-C 3.1 / DisplayPort 1.4					✓	✓	✓	✓	✓	✓	Dual-Role Device, DisplayPort Tx (HDCP ESM, DSC)	✓	✓
USB-C 3.1					✓	✓		✓	✓	✓	Dual-Role Device, Device, Host	✓	✓
USB 3.1					✓	✓		✓	✓	✓	Dual-Role Device, Device, Host	✓	✓
USB-C 3.0			✓		✓	✓					Dual-Role Device, Device, Host	✓	✓
USB 3.0	✓	✓	✓	✓	✓	✓					Dual-Role Device, Device, Host	✓	✓
USB 2.0/ USB-C 2.0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Dual-Role Device, Device, Host	✓	✓
eUSB2										✓	Dual-Role Device, Device, Host	✓	✓

MIPI	Process Technologies								Controllers	Verification IP	Auto Grade
	40/45 nm	28 nm	22 nm	20 nm	14/16nm FinFET	12nm FinFET	7nm FinFET	5nm FinFET			
C/D-PHY					✓	✓	✓	✓	CSI-2, DSI/DSI-2	✓	
D-PHY	✓	✓	✓	✓	✓	✓	✓		CSI-2, DSI/DSI-2	✓	✓
M-PHY		✓			✓	✓	✓	✓	UFS, UniPro	✓	
CSI-2									Host, Device	✓	✓
DSI									Host, Device	✓	✓
DSC									Encoder, Decoder	✓	
DSI + DSC									DSI/DSI-2 + DSC Encoder	✓	
UniPro									v1.6, v1.8, v2.0	✓	
I3C									Multi-role, Target-Lite	✓	

Interface IP

PCI Express	Process Technologies										Controllers	Con-figu-ration	IDE Security Module	HS Access & Test	Verifi-cation IP	Auto Grade
	40/45/55/65 nm	28 nm	22 nm	20 nm	12/14/16nm Fin FET	10 nm Fin-FET	8 nm Fin-FET	7 nm Fin-FET	6 nm Fin-FET	5 nm Fin-FET						
PCIe 6.0										✓		x2, x4, x8		✓	✓	
PCIe 5.0					✓	✓		✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 4.0		✓			✓			✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16		✓	✓	✓
PCIe 3.1		✓	✓		✓	✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16		✓	✓	✓
PCIe 2.1	✓	✓	✓	✓	✓			✓			Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16		✓	✓	

HDMI	Process Technologies						Controllers	Verification IP
	40/45 nm	28 nm	14/16nm FinFET	12nm FinFET	7nm FinFET	5nm FinFET		
HDMI 2.1			✓	✓	✓	✓	✓	✓
HDMI 2.0	✓	✓	✓	✓			✓	✓
DP 1.4				✓	✓	✓	✓	✓

CXL	Process Technologies					Controllers	Configurations	IDE Security Module	Verification IP
	14/16nm FinFET	10nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET				
CXL 2.0	✓	✓	✓	✓	✓	Device, Host, Dual Mode, Switch Port	x1, x2, x4, x8, x16	✓	✓

CCIX	Process Technologies					Controllers	Verification IP
	14/16nm FinFET	12nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET		
CCIX 1.0	✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch	✓
CCIX 1.1	✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch	✓

HBM	Process Technologies			Controllers	Verification IP
	7nm FinFET	6nm FinFET	5nm FinFET		
HBM3			✓	✓	✓
HBM2				✓	✓
HBM2E	✓	✓	✓	✓	✓

DDR	Process Technologies								Controllers	Platform Architect Support	Verification IP	Auto Grade
	40/45 nm	28 nm	22 nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET	5nm FinFET				
LPDDR5X								✓	Memory controller	✓	✓	
LPDDR5				✓	✓		✓	✓	Memory controller	✓	✓	✓
LPDDR4		✓	✓	✓	✓	✓	✓	✓	Protocol controller, Memory controller	✓	✓	✓
LPDDR4X				✓	✓		✓	✓	Protocol controller, Memory controller	✓	✓	✓
LPDDR3	✓	✓	✓	✓	✓	✓			Protocol controller, Memory controller	✓	✓	
LPDDR2	✓	✓		✓					Protocol controller, Memory controller	✓	✓	
DDR5				✓	✓	✓	✓	✓	Memory controller	✓	✓	
DDR4	✓	✓	✓	✓	✓	✓	✓	✓	Protocol controller, Memory controller	✓	✓	
DDR3	✓	✓	✓	✓	✓	✓			Protocol controller, Memory controller	✓	✓	
DDR2	✓								Protocol controller, Memory controller	✓	✓	

Ethernet	Process Technologies				PCS	Controllers	Verification IP	Auto Grade
	28nm	14/16nm FinFET	7nm FinFET	5nm FinFET				
112G Ethernet (100G/200G/400G/800G)			✓		✓	✓	✓	
56G Ethernet (100G/200G/400G)		✓	✓		✓	✓	✓	
RXAUI/Double XAUI (6.25 G)	✓	✓	✓	✓	✓	✓	✓	
1000BASE-KX, 10GBASE-KR, 10GBASE-KX4	✓	✓	✓	✓	✓	✓	✓	
40GBASE-KR4, 40GBASE-CR4, XLAUI	✓	✓	✓	✓	✓	✓	✓	
100GBASE-CR10, CAUI	✓	✓	✓	✓		✓	✓	
100GBASE-DR4/CR4, CAUI4						✓	✓	
100GBASE-KR2/1		✓	✓	✓		✓	✓	
SGMII	✓	✓	✓	✓	✓	✓	✓	✓
QSGMII	✓	✓	✓	✓	✓	✓	✓	
XFI, SFI (SFF-8431)	✓	✓	✓	✓	✓	✓	✓	
GMII/MII, RGMII, RTBI, TBI, SMII, RMII, RevMII, XGMII, XLGMII					✓	✓	✓	
IEEE TSN/AVB Standards: IEEE 802.1AS, 802.1AS-Rev, 802.1Qav, 802.1Qat, 802.1Qbv, 802.1Qbu & 802.3br						✓	✓	
25G/50G Ethernet Consortium and IEEE specifications		✓	✓		✓	✓	✓	
2.5G/5.0G USXGMII		✓	✓		✓	✓	✓	

Interface IP								
Ethernet (continued)	Process Technologies				PCS	Controllers	Verification IP	Auto Grade
	28nm	14/16nm FinFET	7nm FinFET	5nm FinFET				
Additional Enterprise Protocols								
OIF, CEI-6G/11G	✓	✓	✓	✓				
CPRI, OBSI, JESD204 A/B	✓	✓	✓	✓			✓	
SRIO	✓	✓	✓	✓				

Die-to-Die	Process Technologies				Controllers
	12nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET	
Die-to-Die HBI/AIB		✓		✓	
Die-to-Die 112G USR/XSR	✓	✓	✓	✓	✓

SATA	Process Technologies							Controllers	Verification IP
	65nm	55nm	40/45nm	28nm	22nm	14/16nm FinFET	7nm FinFET		
SATA 6G	✓	✓	✓	✓	✓	✓	✓	Host, Device	✓
SATA 3G	✓	✓	✓	✓		✓	✓	Host, Device	✓

Bluetooth, Thread, Zigbee	Process Technologies		Controller (Link Layer / MAC)
	55nm	40nm	
Bluetooth LE 5.2	✓	✓	✓
IEEE 802.15.4 (Thread, Zigbee)	✓	✓	✓
Combo Bluetooth LE/IEEE 802.15.4	✓	✓	✓

Mobile Storage	Process Technologies							Controllers	Verification IP
	28nm	14/16nm FinFET	12nm FinFET	10nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET		
UFS								✓	✓
UniPro								✓	✓
M-PHY	✓	✓	✓	✓	✓	✓	✓	✓	✓
eMMC	✓	✓	✓		✓	✓		✓	✓
SD	✓	✓	✓		✓	✓		✓	✓
SDIO	✓	✓	✓		✓	✓		✓	✓

AMBA	Synthesizable IP	Verification IP
AMBA APB 3/4, AHB 2/5, AXI 3/4 interconnect fabric, bridges, interconnect matrices and infrastructure IP	✓	✓
AHB and AXI DMA Controllers	✓	✓
SSI Controller (SPI/xSPI)	✓	✓
AMBA Advance peripherals (I^2C, I^2S, UART)	✓	✓
Timers, WDT, RTC, interrupt controllers, GPIOs	✓	✓

Datapath IP	Synthesizable IP	Simulation Models (C++, Verilog)	Verification Models
Floating Point Functions	✓	✓	✓
Fixed Point Functions	✓	✓	✓
Trigonometric Functions	✓	✓	✓

Analog IP									
Data Converters	Process Technologies						Bits	MSPS	Channel Configuration
	90nm	55nm	40nm	28nm	22nm	12/16nm FinFET			
300-1000 MSPS ADCs				✓	✓	✓	12	320 to 750	Single, Dual
150-300 MSPS ADCs				✓	✓	✓	10, 12	160 to 250	Single, Dual
10-150 MSPS ADCs				✓	✓	✓	10, 12	80 to 125	Single, Dual
<10 MSPS ADCs	✓	✓	✓	✓	✓		10, 12, 14	1 to 5	Single
300-1000 MSPS DACs				✓	✓	✓	12	320 to 1000	Single, Dual
<100 MSPS DACs			✓	✓	✓	✓	11, 12	20	Single

Foundation IP												
Embedded Memories	Process Technologies											
	65nm	55nm	40/ 45nm	28nm	22nm	14/16nm FinFET*	12nm FinFET	10nm FinFET	8nm FinFET*	7/6nm FinFET	5nm FinFET	4nm FinFET
Ternary Content-Addressable Memory (TCAM)	✓		✓	✓		✓		✓	✓	✓	✓	✓
Multi-port Memories										✓		
High-Speed Single Port SRAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Ultra High Speed Single Port SRAM									✓			✓
High-Speed Dual Port SRAM	✓	✓	✓	✓		✓	✓	✓	✓			✓
High-Speed 1P Register File (RF) (Cache)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
High-Speed Asynchronous 2-Port Register File			✓	✓		✓						
High Performance Core (HPC) Design Kit			✓	✓	✓	✓	✓		✓	✓	✓	✓
High Speed 2P RF								✓	✓			
Ultra High Speed 2P RF												✓
High Speed Pseudo 4P/QP SRAM				✓		✓				✓		
High-Density Single Port SRAM	✓	✓	✓*	✓	✓	✓	✓		✓	✓	✓	✓
High-Density Dual Port SRAM	✓	✓	✓	✓	✓	✓	✓			✓	✓	
High-Density 1P RF	✓	✓	✓	✓	✓*	✓	✓		✓	✓	✓	✓
High-Density 2P RF	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓
High-Density 3P RF											✓	
High-Density ROM	✓	✓	✓	✓	✓*	✓	✓	✓	✓	✓	✓	✓
High-Density 2P,3P Async Latch Based Compiler				✓		✓				✓		
UHD 1P RF							✓			✓	✓	✓
EHD 1P RF											✓	
UHD Single Port SRAM					✓*	✓	✓			✓	✓	✓
UHD 2P RF	✓	✓	✓*	✓	✓	✓	✓	✓	✓	✓	✓	✓
EHD 2P RF											✓	
UHD 2P SRAM				✓	✓	✓			✓	✓	✓	✓

*Available in Consumer and Automotive

Foundation IP												
Logic Libraries	Process Technologies											
	65nm	55nm	40/ 45nm	28nm	22nm	14/16nm FinFET*	12nm FinFET	8nm FinFET*	7nm FinFET*	6nm FinFET	5nm FinFET	4nm FinFET*
High-Speed Library	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
High-Speed POK	✓	✓	✓	✓	✓	✓		✓	✓		✓	✓
High-Density Library	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
High-Density POK	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
UHD Library	✓	✓	✓	✓	✓	✓	✓	✓				✓
UHD POK	✓	✓	✓	✓	✓	✓	✓	✓				✓
Ultra-low leakage (thick oxide)			✓		✓	✓	✓					
High-Performance Core (HPC) Design Kit			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

*Available in Consumer and Automotive

I/O Products	Process Technologies					
	22nm	14/16nm FinFET	12nm FinFET	6/7nm FinFET	5nm FinFET	4nm FinFET
General-purpose I/Os	✓	✓	✓	✓	✓	✓
Specialty I/Os	✓	✓	✓	✓	✓	
Auto Grade	✓					

Non-Volatile Memory	Process Technologies									Bit Counts	Endurance (Write Cycles)
	150/ 180nm	110/ 130nm	80/90 nm	55/65 nm	40 nm	28 nm	22 nm	14/16nm FinFET	12nm FinFET		
One-Time Programmable (OTP)	✓	✓	✓	✓	✓	✓	✓	✓	✓	16 bit to 1 Mbit	1 per instance
Multi-Time Programmable (MTP) Medium-Density	180nm									16 bit to 512 Kbit	Up to 1,000
MTP EEPROM	180nm	✓		✓	✓					128 bit to 8 Kbit	Up to 1,000,000
MTP ULP	✓									64 bit to 4 Kbit	Up to 100,000
Few-Time Programmable (FTP) Trim	✓	✓								64 bit to 4 Kbit	Up to 1,000
Auto Grade							✓				

In-Chip PVT Monitoring IP	Process Technologies						
	28nm	16nm FinFET	12nm FinFET	7nm FinFET	6nm FinFET	5nm FinFET	3nm FinFET
Hard IP							
Process Detector	✓	✓	✓	✓	✓	✓	✓
Voltage Monitor	✓	✓	✓	✓	✓	✓	✓
Temperature Sensor	✓	✓	✓	✓	✓	✓	✓
Distributed Thermal Sensor					✓	✓	✓
Thermal Diode		✓		✓	✓	✓	✓
Catastrophic Trip Sensor					✓	✓	✓
In-Chip PVT Monitoring Subsystem	✓	✓	✓	✓	✓	✓	✓
Soft IP							
PVT Controller	✓	✓	✓	✓	✓	✓	✓
Software Driver					✓	✓	✓

Path Margin Monitor IP	In-Test
Path Margin Monitor Unit (PMMU)	✓
Path Margin Monitor Controller (PMMC)	✓

Security IP			
Security	Synthesizable IP	Software	Safety Compliant
Cryptography IP	✓	✓	
Security Protocol Accelerators	✓	✓	
Hardware Secure Modules with Root of Trust	✓	✓	✓
HDMI/DisplayPort/USB Type-C Content Protection IP	✓	✓	
PCIe & CXL Integrity and Data Encryption IP	✓	✓	
DDR/LPDDR Inline Memory Encryption IP	✓	✓	

Accelerate Development of Performance-Efficient SoCs

Synopsys ARC® Processors are a family of 32-/64-bit CPUs and DSPs that SoC designers can optimize for a wide range of uses, from deeply embedded to high-performance host applications in a variety of market segments. Designers can differentiate their products by using patented configuration technology to tailor each ARC processor instance to meet specific performance, power and area requirements. The Synopsys ARC processors are also extensible, allowing designers to add their own custom instructions that dramatically increase performance. Synopsys' ARC processors have been used by over 275 customers worldwide who collectively ship more than 2.5 billion ARC-based chips annually.

All Synopsys ARC processors utilize a 16-/32-/64-bit ISA that provides excellent performance and code density for embedded and host SoC applications. The RISC and DSP processors are synthesizable and can be implemented in any foundry or process, and are supported by a complete suite of development tools.

Synopsys ARC processors are supported by a broad ecosystem of commercial and open source tools, operating systems and middleware. This includes offerings from leading industry vendors who are members of the ARC Access Program as well as a comprehensive suite of free and open source software available through embARC.org.

Processor IP									
ARC 32-bit Processors	Max CCM Size (I&D)	Cache Size (I&D)	DSP	MPU	Safety Certified	Enhanced Security Package	MMU	Floating Point	Trace
EM4	2MB			✓		✓		✓	✓
EM6	2MB	64K		✓		✓		✓	✓
EM5D	2MB		✓	✓		✓		✓	✓
EM7D	2MB	64K	✓	✓		✓		✓	✓
EM9D	2MB		✓	✓				✓	✓
EM11D	2MB	64K	✓	✓				✓	✓
EM22FS	2MB	64K	✓	✓	✓			✓	✓
SEM110	2MB			✓				✓	
SEM120D	2MB		✓	✓				✓	
SEM130FS	2MB		✓	✓	✓			✓	
605 LE	512KB			✓					
710D	512KB		✓	✓				✓	✓
725D	512KB	64K	✓	✓				✓	✓
770D	512KB	64K	✓	✓			✓	✓	✓
610D	512KB		✓	✓				✓	✓
625D	512KB	32K	✓	✓				✓	✓
AS211SFX	512KB	32K	✓	✓				✓	✓
AS221BD (dual-core)	512KB ea core	32K ea core	✓	✓				✓	✓

Processor IP									
ARC HS 32-bit Processors	Max CCM Size	L1 Cache (I & D)	DSP	Safety Certified	L1 Coherency	L2 Cache	MMU	Floating Point	Trace
HS34, HS34x2, HS34x4	16MB							✓	✓
HS36, HS36x2, HS36x4	16MB	64K			✓			✓	✓
HS38, HS38x2, HS38x4	16MB	64K			✓	8MB	✓	✓	✓
HS44, HS44x2, HS44x4	16MB							✓	✓
HS46, HS46x2, HS46x4	16MB	64K			✓			✓	✓
HS48, HS48x2, HS48x4	16MB	64K			✓	8MB	✓	✓	✓
HS45D, HS45Dx2, HS45Dx4	16MB		✓					✓	✓
HS47D, HS47Dx2, HS47Dx4	16MB	64K	✓		✓			✓	✓
HS46FS, HS46FSx4	16MB	64K		✓	✓			✓	✓
HS47DFS, HS47DFSx4	16MB	64K	✓	✓	✓			✓	✓
HS48FS, HS48FSx4	16MB	64K		✓	✓	8MB	✓	✓	✓
HS56, HS56MP	16MB	64K			✓	64MB (MP)		SIMD	✓
HS57D, HS57DMP	16MB	64K	✓		✓	64MB (MP)		SIMD	✓
HS58, HS58MP	16MB	64K			✓	64MB	✓	SIMD	✓

ARC HS 64-bit Processors	Max CCM Size	L1 Cache (I & D)	L1 Coherency	Shared L2 Cache/ Cluster Mem.	MMU	Floating Point	Trace
HS66, HS66MP	16MB	64K	✓	64MB (MP)		SIMD	✓
HS68, HS68MP	16MB	64K	✓	64MB	✓	SIMD	✓

ARC VPX DSP Processors	Scalar Execution Unit	Vector Execution Unit	Vector Length	Dual SIMD Multiply Units	Dual Floating Point Vector Engine (optional)	Floating Point Vector Math Engine (optional)	Safety Certified	L1 Coherency	Multicore configurations
VPX2	✓	3	128-bit	✓	✓	✓		✓	2x
VPX2FS	✓	3	128-bit	✓	✓	✓	✓	✓	2x
VPX3	✓	3	256-bit	✓	✓	✓		✓	2x
VPX3FS	✓	3	256-bit	✓	✓	✓	✓	✓	2x
VPX5	✓	3	512-bit	✓	✓	✓		✓	2x, 4x
VPX5FS	✓	3	512-bit	✓	✓	✓	✓	✓	2x, 4x

ARC NPX Neural Processors	MACs	DMA	L2 Shared Memory	L2 Controller	Tensor Accelerator	Tensor Floating Point Unit (FPU) (optional)	Trace	Memory Management Unit (MMU)	ASIL B/D
NPX6-4K	4,096	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6-8K	8,192	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6-16K	16,384	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6-32K	32,768	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6-64K	65,536	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6-96K	98,304	✓	0-64 MB	✓	✓	✓	✓	✓	
NPX6FS-4K	4,096	✓	0-64 MB	✓	✓	✓	✓	✓	✓
NPX6FS-8K	8,192	✓	0-64 MB	✓	✓	✓	✓	✓	✓
NPX6FS-16K	16,384	✓	0-64 MB	✓	✓	✓	✓	✓	✓
NPX6FS-32K	32,768	✓	0-64 MB	✓	✓	✓	✓	✓	✓
NPX6FS-64K	65,536	✓	0-64 MB	✓	✓	✓	✓	✓	✓
NPX6FS-96K	98,304	✓	0-64 MB	✓	✓	✓	✓	✓	✓

Processor IP										
Embedded Vision Processors	DNN/CNN Accelerator (MACs)	Vision CPU MACs	DMA	32-bit Scalar	# of Vector DSPs	Vector DSP Bit Width	L1 Cache Coherency	Floating Point Unit (FPU)	Vector Floating Point Unit	Safety Certified
EV71	880, 1,760, or 3,520	64	✓	1	1	512		✓	✓	
EV72	880, 1,760, or 3,520	128	✓	2	2	512	✓	✓	✓	
EV74	880, 1,760, or 3,520	256	✓	4	4	512	✓	✓	✓	
EV71FS	880, 1,760, or 3,520	64	✓	1	1	512		✓	✓	✓
EV72FS	880, 1,760, or 3,520	128	✓	2	2	512	✓	✓	✓	✓
EV74FS	880, 1,760, or 3,520	256	✓	4	4	512	✓	✓	✓	✓

ARC Processor IP Subsystems	Supported ARC Processors	Hardware Accelerators	Integrated Peripherals	Included Software
IoT Communications IP Subsystem	EM11D	✓	SPI, UART(s), GPIO, Digital Front End (DFE), PMU and RTC	DSP library, base communications library, device drivers
Data Fusion IP Subsystem	EM5D, EM7D, EM9D, EM11D	✓	SPI, I²C, I²S, UART, PDM, ADC I/F, APB I/F, GPIO	DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs
Sensor and Control IP Subsystem	EM4, EM6	✓	SPI, I²C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO	DSP library, motor control library, peripheral I/O drivers (bare metal), reference designs

IP Accelerated Initiative

With IP Accelerated, Synopsys has augmented its broad portfolio of silicon-proven Synopsys IP portfolio with SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, IP prototyping kits, and comprehensive silicon bring-up support to accelerate your product development cycle.

IP Subsystems support many protocols and deliverables for IP integration including configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts and implementation scripts. The subsystems also include AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic.

Hardening and SIPI provide a GDSII for integration in an SoC and include On-chip decoupling capacitance, power and ground pins, PHY & SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/address, and command/control timing budgets.

With your vision and our expertise, we can tune IP to your SoC, enabling your team to focus on product differentiation.

IP Subsystems				
Interface IP Subsystems	Supported IP	Multi-Protocol Support	Integrated Logic	Included Scripts
IP Protocol-Specific Subsystems	USB, PCIe, DDR, Ethernet, HDMI, MIPI, AMBA, Security, MACsec, PCIe switch, CXL 2.0 switch	✓	AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic	Configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts, implementation scripts

IP Subsystems							
Interface IP Subsystems	**Combo Subsystems**	**Auto Grade**	**UVM**	**Spyglass**	**SRAM/ MBIST**	**UPF**	**DFT**
PCIe/CXL	PCIe-Ethernet, PCIe-USB, PCIe-SATA PCIe-CCIX, CXL	ASIL B	✓	✓	✓	✓	✓
DDR3/4/5	DDR-LPDDR4/4X/5						
HBM	✓						
Ethernet	Ethernet-PCIe, Ethernet-USB						
USB	USB-DP, USB-DP-HDMI, USB-PCIe, USB-Ethernet						
HDMI	HDMI-DP, HDMI-USB-DP						
MIPI	✓						

Configurable IP Subsystems	**Combo Subsystems**	**Auto Grade**	**UVM**	**Spyglass**	**SRAM/ MBIST**	**UPF**	**DFT**
CXL 2.0 switch	✓	ASIL B	✓	✓	✓	✓	✓
PCIe switch							
MACsec							

Signal/Power Integrity Analysis & IP Hardening		
Supported IP	**Multi-Protocol Support**	**Consultation Expertise**
DDR, LPDDR, HBM, PCIe, USB, MIPI, Ethernet, HDMI	✓	On-chip decoupling capacitance, power and ground pins, PHY & SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/ address, command/control timing budgets

IP Hardening											
Supported IP	**Multi-protocol Support**	**Synthesis to GDSII**	**Floor Planning**	**Scan Insertion**	**Power Grid**	**Skew Balancing**	**RDL Routing**	**Bump Assign-ment**	**IR/EM-Analysis**	**DRC/ LVS**	**GLS**
DDR/LPDDR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HBM2E / HBM3											
PCIe											

Signal/Power Integrity Analysis										
Supported IP	**Multi-protocol Support**	**Floorplan Review**	**Pre/Post Layout Analysis**	**Decap Cell Size/ Placement**	**Power Impedance Simulations**	**Eye Quality Analysis**	**End to End Analysis**	**Timing Budget Analysis**	**Signal Quality PVT Corner Analysis**	**Full Report**
DDR/LPDDR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HBM2E / HBM3										
HBI										
PCIe										
MIPI										
Ethernet										

IP Prototyping Kits and Software Development Kits				
Protocol/Standard	IP Prototyping Kit with ARC HS DP	IP Prototyping Kit with PCIe Connection to PC	IP Prototyping Kit with ARC HSDK	IP Prototyping Kit with PCIe Connection to PC
	Soft Deliverable	Soft Deliverable	Soft Deliverable	Soft Deliverable
	HAPS-100	HAPS-100	HAPS-80	HAPS-80
USB 3.1 Host				✓
USB 3.1 Device				✓
CXL 2.0 EndPoint		✓		✓
CXL 2.0 Root Complex	✓		✓	
PCIe 5.0 Endpoint		✓		✓
PCIe 5.0 Root Complex	✓		✓	
PCIe 4.0 Endpoint		✓		✓
PCIe 4.0 Root Complex	✓		✓	
PCIe 3.0 Endpoint		✓		✓
PCIe 3.0 Root Complex	✓		✓	
DDR 4/3		✓		✓
LPDDR 4		✓		✓
DDR 5 / Memory Model PHY		✓		
LPDDR 5 / FPGA PHY		✓		

For more information on Synopsys IP, visit synopsys.com/ip.

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