FlexRAN 5G New Radio Reference Solution L1-L2

API Specification

March 2021

Revision 10.0

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Contents

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Revision History

Revision	Description:	Date
10.0	Updated for FlexRAN Software Release v21.03: • Updated Section 1.4 • Updated Section 3.2.2 • Updated Section 3.2.4	March 2021
9.0	Updated for FlexRAN Software Release v20.11: • Updated Table 12, DLPDUDataStruct Structure Type • Updated Table 13, CRCIndicationStruct Structure Type • Updated Table 14, ULSCHPDUDataStruct Structure Type • Updated Table 15, ULSCHUCIPDUDataStruct Structure Type • Updated Table 16, ULUCIPDUDataStruct Structure Type • Updated Table 19, CONFIG.request Message Body • Updated Table 31, DLSCH PDU • Updated Table 36, ULCCH_UCI PDU • Updated Table 41, CRC.indication Message Body	November 2020
8.0	Updated for FlexRAN Software Release v20.08: • Updated Table 13, `nSNR` • Updated Table 16, `nSNR` • Updated Table 21, `nMode` • Updated Table 30, 31, and 32, `nTxRUIdx[MAX_TXRU_NUM]` • Updated Table 35, `nRxRUIdx[MAX_RXRU_NUM]`	August 2020
7.0	Updated for FlexRAN Software Release v20.04 • Updated Tables 1, 7, 13, 16, 34,35	April 2020
6.0	Updates for Release 20.02: • Section 3.2.2 has a new section for MAC2PHY_QUEUE_EL, tMac2PhyApiQueueElem and updated descriptions to some of the API fields • Section 3.2.3 has notes added for consumers detailing which API fields are currently available in this release and updated details for API fields. • Added nUrllcCapable and reserved to Table 19. • Updated details to Table 30, DL DCI PDU. • Added nID to Table 30. • Added nGroupID to Table 36. • Added details to Table 31, 35, 36, 37, and 38.	February 2020
5.0	Updates for Release 19.10: • Updated Table 1, Terminology • Updated Table 2, Reference Documents and Resources added URL for nFAPI and FAPI specifications • Updated Section 1.0 introduction • Updated nSlot description in Table 6	October 2019
4.0	Updates for Release 19.06	July 2019
3.0	Updates for Release 19.03	April 2019

2.0	Updates for Release 18.12	December 2018
1.0	Initial release for Release 18.09	October 2018

1.0 Introduction

The Functional Application Programming Interface (FAPI) controls the interaction between the 5G-RAN L1 PHY and L2/L3 software.

1.1 Scope

This document gives a description of the FAPI between the 5G-RAN L1 PHY and L2/L3 software. The Application Programming Interfaces (APIs) between L1 and L2/L3 are defined in this document.

1.2 Intended Audience

The intended audience for this document includes designers and engineers designing applications using the FlexRAN Reference Solution

1.3 Terminology

Table 1. Terminology

Term	Description
5G-NB	5G Node B
ACK	Acknowledgment
API	Application Programming Interface
CRI	CRS-RS Resource Indicator
CRS	Cell-Specific Reference Signal
CQI	Channel Quality Indicator
CSI	Channel Status Information
DCI	Downlink Control Information
DL	Downlink
FAPI	Functional Application Programming Interface
HARQ	Hybrid Automatic Repeat Request
LI	Layer Indicator
MAC	Medium Access Control
MU-MIMO	Multiple Users Multiple Input Multiple Output
NACK	Negative Acknowledgement
nFAPI	Network Functional Application Programming Interface

Term	Description
NR	New Radio
ORAN	Open Radio Access Network
PBCH	Physical Broadcast Channel
PDSCH	Physical Downlink Shared Channel
PDCCH	Physical Downlink Control Channel
PDU	Protocol Data Unit
PHY	Physical Layer (L1)
PMI	Precoder Matrix Indicator
PDCP	Packet Data Convergence Protocol
PRACH	Physical Random Access Channel
PUCCH	Physical Uplink Control Channel
PUSCH	Physical Uplink Shared Channel
RI	Rank Indicator
RLC	Radio Link Control
RNTI	Radio Network Temporary Identifier
RRC	Radio Resource Control
RS	Reference Signal
RSRP	Reference Signal Receiving Power
SFN	System Frame Number
SRS	Sounding Reference Signal
SUL	Supplementary Uplink
SU-MIMO	Single User Multiple Input Multiple Output
UCI	Uplink Control Information
UE	User Equipment
UL	Uplink
URLLC	Ultra-Reliable Low Latency Communication

1.4 Reference Documents and Resources

Table 2. Reference Documents and Resources

Reference Number	Document	Location
222.10.02	*SCF222 5G FAPI: PHY API Specification*	https://scf.io/en/documents/222_5G_FAPI_PHY_API_Specification.php
TS 38.211	*NR; Physical Channels and Modulation*	https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3213
TS 38.213	*NR; Physical Layer procedures for Control*	https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3215
TS 38.214	*Physical Layer Procedures for Data*	https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3216
TS 38.331	*NR; Radio Resource Control (RRC); Protocol Specification*	https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3197

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2.0 5G Introduction

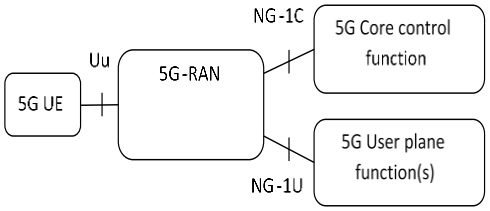
This document describes the FAPI's relationship between the 5G-RAN L1 PHY and L2/L3 software. The APIs between L1 and L2/L3 are also defined in this document.

2.1 5G-RAN Introduction

The 5G-RAN consists of 5G Node Bs (NBs), providing the 5G-RA user plane (PDCP/RLC/MAC/PHY) and control plane (RRC) protocol terminations towards the UE. The 5G NBs are connected using the NG interface to the core network.

The 5G-RAN architecture is illustrated in Figure 1 below:

Figure 1. Overview of the 5G-RAN architecture

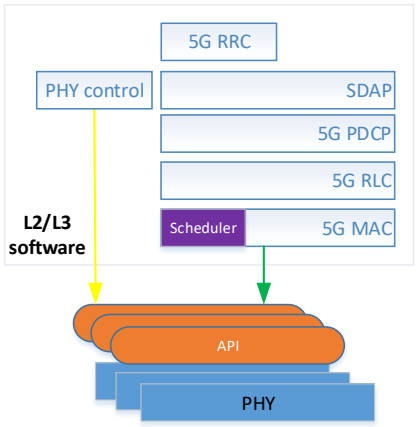


2.2 5G FAPI Introduction

The 5G FAPI, defined in this document, resides within the B 5G-NB (5G Node) component. If the carrier aggregation is supported, then one instance of the 5G FAPI exists for each carrier.

The API interaction is illustrated in Figure 2 below:

Figure 2. API Interactions



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3.0 5G FAPI

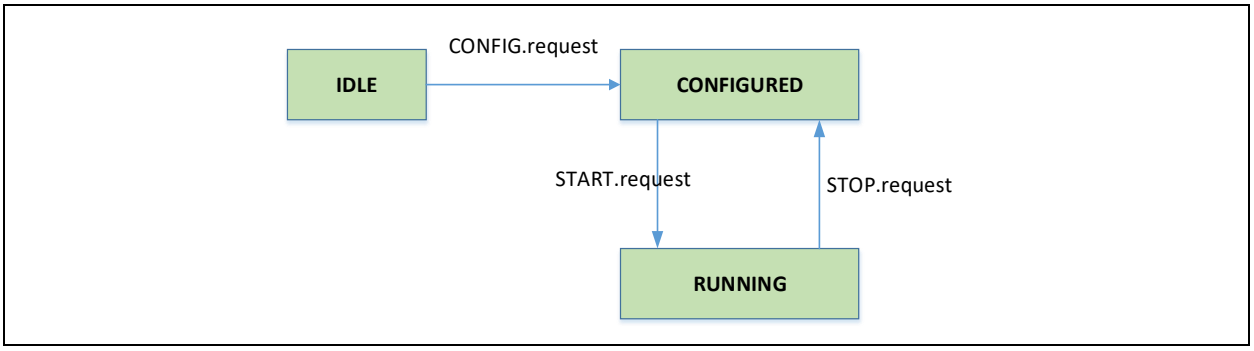
3.1 5G FAPI Procedures

This section depicts two types of procedures using the 5G FAPI. PHY configuration procedures handle the management of the PHY layer. Slot procedures determine the structure of each slot and operate with a slot duration periodicity. Slot duration depends on the 5G NR numerologies, and it could be 1 ms, 0.5 ms, 0.25 ms, 0.125 ms, 0.0625 ms.

3.1.1 PHY Configuration Procedures

This section depicts how PHY interacts with L2/L3 through API messages to change the PHY state. PHY state consists of the IDLE, CONFIGURED, and RUNNING states, as shown in Figure 3.

Figure 3. PHY Layer States



3.1.2 Slot Procedures

The slot procedures have two purposes. First, slot procedures are used to indicate the DL and UL Slot structures. Second, they are used to transfer the data between the L2/L3 and L1.

The slot procedures supported by the FAPI are:

- Transmission of a slot message
- Synchronization of SFN/Slot between the L2/L3 software and PHY
- Transmission of the BCH transport channel
- Transmission of the DL-SCH transport channel and reception of Acknowledgment (ACK)/NACK response
- Reception of the RACH transport channel
- Reception of the ULSCH transport channel and transmission of ACK/NACK response
- Reception of the sounding reference signal
- Reception of Channel Quality Indicator (CQI), RI, PMI, Cell-Specific Reference Signal (CRS)-RS Resource Indicator (CRI), L1-RSRP reporting
- Reception of scheduling request information

3.1.2.1 SFN/Slot Synchronization

The SFN/Slot synchronization procedure is used to maintain a consistent SFN/Slot value between the L2/L3 and L1. Maintaining this synchronization is essential since different slots may have different structures.

PHY must be configured only as a master to initialize the SFN/ Slot and ensure the L2/L3 software remains synchronous.

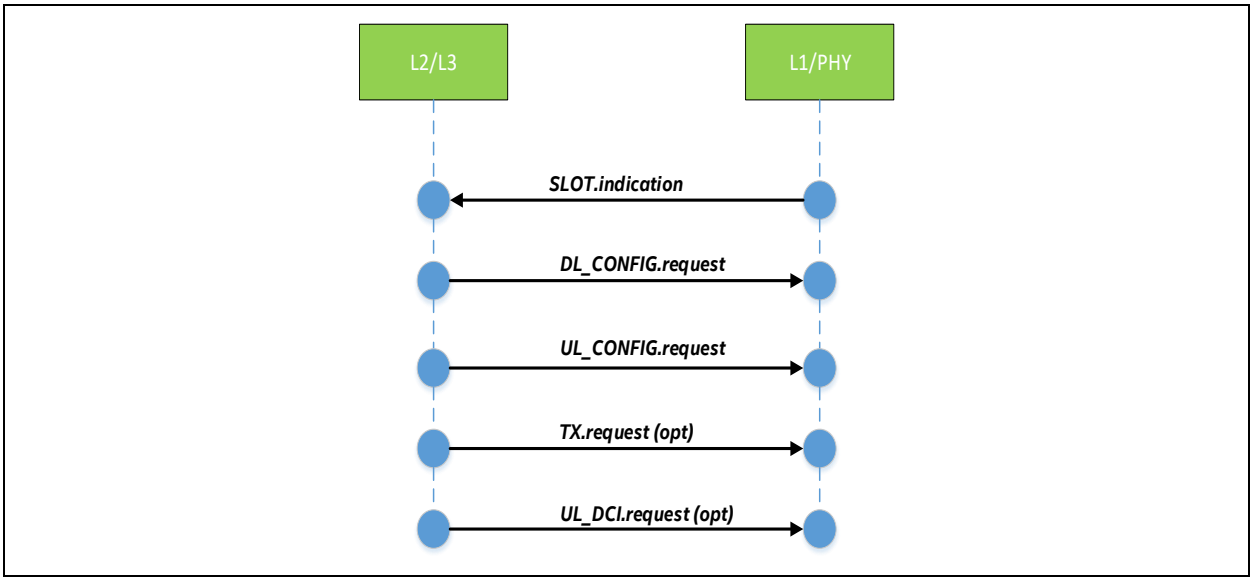
3.1.2.2 API Message Order

The FAPI has constraints of when specific slot messages can be sent or received, by the L2/L3 software. Figure 4 shows the Downlink API Messages.

The downlink API message constraints are as below:

- The SFN/SF included in the `SLOT.indication` message is expected in the corresponding `DL_CONFIG.request`.
- The `DL_CONFIG.request` must be sent for every slot and must be the next message.
- The `UL_CONFIG.request` must be sent for the slot conveying the uplink channel and must be the next message.
- The `TX.request` and `UL_DCI.request` messages are optional. They are not required to be sent in every slot.
- There must be only one `DL_CONFIG.request`, one `UL_CONFIG.request`, one `UL_DCI.request`, and one `TX.request` for a slot.

Figure 4. Downlink API Messages

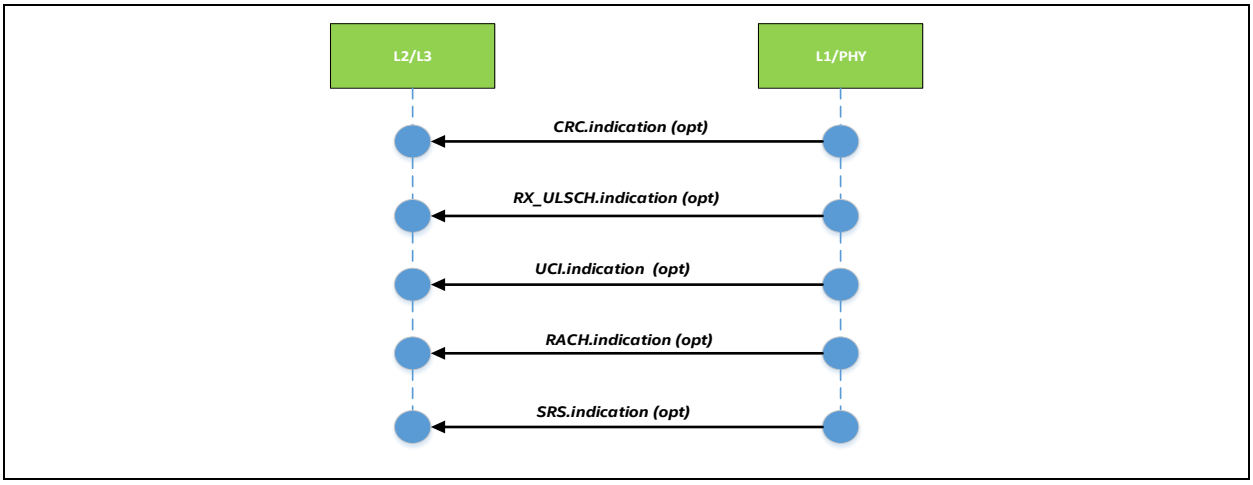


The uplink API message constraints are shown in Figure 5.

- The UL API messages are optional. They are not required to be sent in every slot.
- If present, the messages can be in any order.
- The `CRC.indication` message is included if the uplink data PDUs were expected in the slot.
- The `RX_ULSCH.indication` message is included if the uplink data PDUs were expected in the slot.

- The `UCI.indication` message is included if `CQI/RI/PMI/CRI/L1-RSRP/SR/ACK` were expected in the slot.
- There is only one `CRC.indication`, one `RX_ULSCH.indication`, one `UCI.indication`, one `RACH.indication`, and one `SRS.indication` message per slot.

Figure 5. Uplink API Messages

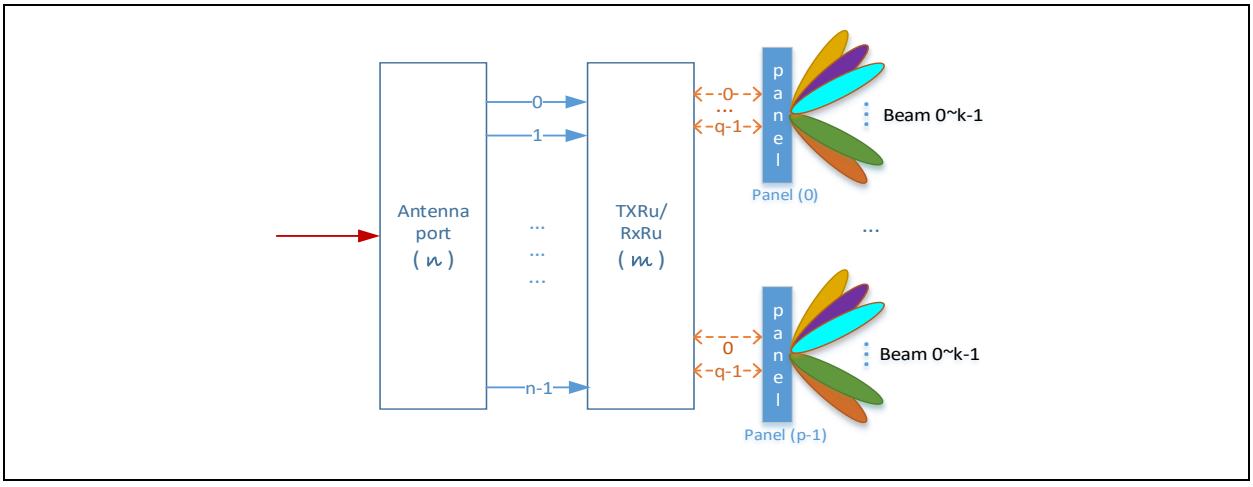


3.1.3 Beam Forming

L2 should schedule the resources of antenna port, TxRU/RxRU, and beam management of physical channels. Figure 6 shows the logical mapping relationship of antenna port, TxRU/RxRU, and beam.

Antenna port `n <= TxRU(RxRU)` number m, and `m=p*q` (p is panel number, q is TxRU/RXRU number per panel), k is the maximum beam number in one antenna panel.

Figure 6. Beam Forming



NOTE: For current RF, n=m=4, q=1, p=4, k=21.

3.2 5G FAPI Messages

This section describes the L1-L2/L3 API message formats. It defines the API message header and the full message bodies associated with the L1-L2/L3 API.

NOTE: Shared memory is used to communicate between L1 and L2. The byte order for 16-bit and 32-bit fields is little-endian.

3.2.1 General Message Format

This section describes the general message format of the L1-L2/L3 API.

Each L1 API message consists of a header followed by a message body. The generic header consists of a message type ID and a message body length (for example, refer to Table 6).

Table 3 provides the current list of message types.

The L1 API messages follow a standard naming convention where:

- All .request messages are sent from the L2/L3 to the L1.
- All .indication and .response messages are sent from the L1 to the L2/L3.

Table 3. L1-L2 API Message Types

Message Type	Message Type ID	Message body definition
CONFIG.request	0x01	Refer to Table 19.
CONFIG.response	0x02	Refer to Table 20.
START.request	0x03	Refer to Table 21.
START.response	0x04	Refer to Table 22.
STOP.request	0x05	Refer to Table 23.
STOP.response	0x06	Refer to Table 24.
ERROR.indication	0x07	Refer to Table 27.
Shutdown.request	0x8	Refer to Table 25.
Shutdown.response	0x9	Refer to Table 26.
RESERVED	0x0a-0x0f	
SLOT.indication	0x10	Refer to Table 28.
DL_CONFIG.request	0x11	Refer to Table 29.
UL_CONFIG.request	0x12	Refer to Table 34.
UL_DCI.request	0x13	Refer to Table 46.
TX.request	0x14	Refer to Table 40.
CRC.indication	0x15	Refer to Table 41.
RX_ULSCH.indication	0x16	Refer to Table 42.
UCI.indication	0x17	Refer to Table 43.
RACH.indication	0x18	Refer to Table 44.
SRS.indication	0x19	Refer to Table 45.

Message Type	Message Type ID	Message body definition
RESERVED	0x1a-0xffff	

Table 4. PDU Type Definitions

PDU Type	PDU Type ID
DL_PDU_TYPE_DCI	0x0
DL_PDU_TYPE_PDSCH	0x1
DL_PDU_TYPE_PBCH	0x2
DL_PDU_TYPE_CSIRS	0x3
UL_PDU_TYPE_ULSCH	0x4
UL_PDU_TYPE_ULCCH_UCI	0x5
UL_PDU_TYPE_ULSCH_UCI	0x6
UL_PDU_TYPE_SRS	0x7
UL_PDU_TYPE_PRACH	0x8

3.2.2 Structure Definitions

MAC2PHY_QUEUE_EL, tMac2PhyApiQueueElem

Table 5. MAC2PHY_QUEUE_EL, tMac2PhyApiQueueElem Structure Type

Field	Type	Description
pNext	Structure	Pointer to next MAC2PHY_QUEUE_EL element in the link list
nMessageType	uint8_t	Message Type as described in Table 3.
nMessageLen	uint32_t	Length of message in bytes.
nNumMessageInBlock	uint8_t	Number of messages in current block. Value: 0 to 255
nAlignOffset	uin32_t	Length in bytes of each API message in this block
nTimeStamp	uint64_t	Time Stamp for this API message
reserved[6]	uint8_t	Reserved

L1L2MessageHdr

Table 6. L1L2MessageHdr Structure Type

Field	Type	Description
nMessageType	uint16_t	Message Type as described in Table 3.
nMessageLen	uint16_t	Length of message in bytes.

SFN_SlotStruct

Table 7. SFN_SlotStruct Structure Type

Field	Bitfield	Description
nSFN	bits 0:9	System frame number 0 to 1023
nSlot	bits 10:18	Slot number 0 to 159
nCarrierIdx	bits 19:23	Carrier Index, 0 to 23
nSym	bits 24:27	Symbol number, 0 to 13. For URLLC, start the symbol of the mini-slot.
nRsv	bits 28:31	Reserved

SLOTCONFIGStruct

Table 8. SLOTCONFIGStruct Structure Type

Field	Type	Description
nSymbolType [MAX_NUM_OF_SYMBOL_PER_SLOT]	uint8_t	Array defines the Symbol type for all 14 symbols in a slot. 0: DL, 1: UL, 2: Guard
reserved[2]	uint8_t	reserved

PDUStruct

Table 9. PDUStruct Structure Type

Field	Type	Description
nPDUType	uint16_t	Set from Table 4
nPDUSize	uint16_t	Size of the PDU control information (in bytes). This length value includes the four bytes required for the PDU type and PDU size of parameters.

PDSCHGroupInfoStruct

Table 10. PDSCHGroupInfoStruct Structure Type

Field	Type	Description
nUE	uint8_t	Number of UEs in this group. For SU-MIMO, one group includes one UE only. For MU-MIMO, one group includes up to six UEs.
rsv1[3]	uint8_t	reserved
nPduIdx[MAX_DL_PAIRED_UE_NUM]	uint8_t	This value is an index of the number of PDU identified by nPDU to be part of this group.

PUSCHGroupInfoStruct

Table 11. PUSCHGroupInfoStruct Structure Type

Field	Type	Description
nUE	uint8_t	Number of UEs in this group. For SU-MIMO, one group includes one UE only. For MU-MIMO, one group includes up to six UEs.
rsv1[3]	uint8_t	reserved

Field	Type	Description
nPduIdx[MAX_UL_PAIRED_UE_NUM]	uint8_t	This value is an index of the number of PDU identified by nPDU to be part of this group.

DLPDUDataStruct

Table 12. DLPDUDataStruct Structure Type

Field	Type	Description
nPduIdx	uint8_t	This value is an index for the number of PDU identified by nPDU in DL_CONFIG.request message. It should comply with sPDSCHGroupInfoStruct in DL_CONFIG.request message.
nPduLen1	uint32_t	Length in bytes for first transport block (codeword 0).
nPduLen2	uint32_t	Length in bytes for second transport block (codeword 1).
pPayload1	uint8_t	Pointer to the content of first transport block, the first PRERESERVED_DATA_HEADER_LEN bytes are reserved for SW-FPGA header
pPayload2	uint8_t	Pointer to the content of second transport block, the first PRERESERVED_DATA_HEADER_LEN bytes are reserved for SW-FPGA header

CRCIndicationStruct

Table 13. CRCIndicationStruct Structure Type

Field	Type	Description
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nRNTI	uint16_t	The RNTI associated with the UE Value: 1 to 65535
nSNR	int16_t	Reported SNR in 1/256 dB steps, estimated by this PUSCH. Divide by 256 to obtain actual estimated SNR
nTA	int16_t	Timing advance value in samples estimated by this PUSCH The sample unit time is 64*Tc*(2^-nSubcSpacing)*(2048/nULFftSize)
nCrcFlag	uint8_t	CRC flag to indicate if error detected: 0: CRC error 1: CRC correct
nChanDetected	uint8_t	Channel detected flag: 0: Channel not detected for this slot, L1 begins the count to determine if UE has left the cell. 1: Channel detected for this slot
nDtxDetected	uint8_t	DTX detected flag: 0: UE is still present 1: DTX detected for this UE , if nChanDetected is detected to be 0 for 10 consecutive slots.

ULSCHPDUDataStruct

Table 14. ULSCHPDUDataStruct Structure Type

Field	Type	Description
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nRNTI	uint16_t	The RNTI associated with the UE Value: 1 to 65535
nPduLen	uint32_t	The total length (in bytes) of PDU payload, without the padding bytes.
pPayload	uint8_t	Pointer to the contents of the ULSCH PDU should be only a buffer address in the current implementation.

ULSCHUCIPDUDataStruct

Table 15. ULSCHUCIPDUDataStruct Structure Type

Field	Type	Description
nId	uint16_t	UE index in the sector Value: from 0 to 1199

Field	Type	Description
nRNTI	uint16_t	The RNTI associated with the UE Value: 1 to 65535
nPduUciAckLen	uint16_t	The total length (in bits) of UlSch UCI Ack/Nack PDU payload, without the padding bytes. Value: from 1 to 640
nUciDetected	uint8_t	Indicates L1 was able to decode UCI Ack/Nack or not. (0 = detected / 1 = dtx). For sizes < 11 bits
nUciCrc	uint8_t	CRC flag for UCI Ack/Nack. (0 = crc error, 1 crc good). For sizes > 11 bits, Polar coded.
nPduUciCsiP1Len	uint16_t	The total length (in bits) of UlSch UCI CSI Part 1 PDU payload, without the padding bytes. Value: from 1 to 640
nUciCsiP1Detected	uint8_t	Indicates L1 was able to decode UCI Csi Part 1 or not. (0 = detected / 1 = dtx). For sizes < 11 bits
nUciCsiP1Crc	uint8_t	CRC flag for UCI Csi Part 1. (0 = crc error, 1 crc good). For sizes > 11 bits, Polar coded.
nPduUciCsiP2Len	uint32_t	The total length (in bits) of UlSch UCI Csi Part 2 PDU payload, without the padding bytes. Value: from 1 to 640
nUciCsiP2Detected	uint8_t	Indicates L1 was able to decode UCI Csi Part 2 or not. (0 = detected / 1 = dtx). For sizes < 11 bits
nUciCsiP2Crc	uint8_t	CRC flag for UCI Csi Part 2. (0 = crc error, 1 crc good). For sizes > 11 bits, Polar coded.
nUciAckBits[MAX_UCI_BIT_BYTE_LEN]	uint8_t	Buffer containing decoded UCI Ack/Nack payload for this UE
nUciCsiP1Bits[MAX_UCI_BIT_BYTE_LEN]	uint8_t	Buffer containing decoded UCI Csi Part 1 payload for this UE
nUciCsiP2Bits[MAX_UCI_BIT_BYTE_LEN]	uint8_t	Buffer containing decoded UCI Csi Part 2 payload for this UE

NOTE: This field is not supported in the current release. For further information, contact your Intel representative.

ULUCIPDUDataStruct

Table 16. ULUCIPDUDataStruct Structure Type

Field	Type	Description
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nRNTI	uint16_t	The RNTI associated with the UE Value: 1 to 65535
nSRPresent	uint8_t	Whether SR present, valid for Format0. Value 0 or 1
pucchDetected	uint8_t	Indicates if L1 was able to decode PUCCH or not (0 – CRC fail / 1 – CRC pass / 2 – DTX / 3 – UE has left the cell)

Field	Type	Description
nPduBitLen	uint16_t	The total length (in bits) of PDU Payload Value: from 0 to 640
nSNR	int16_t	Reported SNR in 1/256 dB steps, estimated by this PUCCH. Divide by 256 to obtain actual estimated SNR
nTA	int16_t	Timing advance value in samples, estimated by this PUCCH The sample unit time is 64*Tc*(2^-nSubcSpacing)*(2048/nULFftSize)
nUciBits[MAX_UCI_BIT_BYTE_LEN]	uint8_t	Contents of the ULUCI PDU

PreambleStruct

Table 17. PreambleStruct Structure Type

Field	Type	Description
nTA	uint16_t	Timing Advance measured by this detected PRACH. Value depends on search window size
nPreambIdx	uint8_t	Detected preamble index. Value: from 0 to 63
nStartSymbIdx	uint8_t	The Index of the first OFDM symbol of the specified PRACH. Value: from 0 to 13
nStartSlotdx	uint16_t	The Index of the first slot of the specified PRACH in a system frame. Value: from 0 to 79
nFreqIdx	uint16_t	The Index of the specified PRACH in the frequency domain. Value: from 0 to 7
nPreambPwr	uint32_t	Receiving power Value: 0 to 170000, 0.001 dB step, -140 to 30 dBm
nUlCarrier	uint8_t	The UL carrier used for Msg1 transmission 0: normal carrier 1: Supplementary Uplink (SUL) carrier

ULSRSEstStruct

Table 18. ULSRSEstStruct Structure Type

Field	Type	Description
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nRNTI	uint16_t	The RNTI associated with the UE Value: 1 to 65535
nNrOfSymbols	uint8_t	Number of symbols for this SRS

Field	Type	Description
nNrOfBlocks	uint8_t	Number of the frequency sub-block One sub-block covers four RBs
nNrOfPort	uint8_t	Number of SRS ports for this user.
nNrOfAnts	uint8_t	Number of Rx Antennas for this user.
nNrOfRbs	uint16_t	Number of resource blocks programmed.
nIsChanEstPres	uint8_t	If set to 1, then pSrsChanEst field is filled with valid pointers. Will be set to 0 for non-Massive MIMO scenarios.
nWideBandSNR[4]	int8_t	SNR in dB measured within configured SRS bandwidth on each symbol, up to four symbols can be configured
nBlockSNR[4][68]	int8_t	SNR in dB measured within four RBs on each symbol, up to 68 blocks in case of SRS bandwidth 272 RBs
pSrsChanEst[MAX_SRS_PORT_PER_UE][MAX_NUM_ANT]	int16_t	Pointer to SRS channel estimation for all ports and receive antennas for Massive MIMO scenarios.

3.2.3 PHY Configuration Messages

CONFIG.request

Table 19. CONFIG.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
nCarrierIdx	uint8_t	Cell index Value: from 0 to 15
nDMRSTypeAPos	uint8_t	dmrs-TypeA-Position 2: pos2, 3: pos3
nPhyCellId	uint16_t	Physical cell id Value: from 0 to 1007
nDLAbsFrePointA	uint32_t	Absolute frequency of DL pointA in KHz Value: from 450000 to 52600000
nULAbsFrePointA	uint32_t	Absolute frequency of UL pointA in KHz Value: from 450000 to 52600000

Field	Type	Description
nDLBandwidth	uint16_t	Carrier bandwidth for DL in MHz Value: from 5 to 400
nULBandwidth	uint16_t	Carrier bandwidth for UL in MHz Value: from 5 to 400
nDLFftSize	uint16_t	ifft/fft size for DL Value: 512, 1024, 2048, 4096
nULFftSize	uint16_t	ifft/fft size for UL Value: 512, 1024, 2048, 4096
nSSBPwr	uint32_t	SSB block power Value: 0 means using default value. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to SSB default value
nSSBAbsFre	uint32_t	absoluteFrequencySSB in KHz Value: from 450000 to 52600000
nSSBPeriod	uint8_t	SSB periodicity in msec Value: from 0 to 5 0: ms5 1: ms10 2: ms20 3: ms40 4: ms80 5: ms160
nSSBSubcSpacing	uint8_t	SS/PBCH block Subcarrier spacing (see Table 2, 3GPP* 38.213, section 4.1). Value: from 0 to 4 0: Case A 15 kHz 1: Case B 30 kHz 2: Case C 30 kHz 3: Case D 120 kHz 4: Case E 240 kHz
nSSBSubcOffset	uint8_t	ssb-subcarrierOffset Value: from 0 to 23
nSSBPrbOffset	uint8_t	ssb-resrouceBlockOffset Value: from 0 to 253
nMIB[3]	uint8_t	MSB->LSB of the first byte corresponds to bit0 to bit7 The same bit order applies to the other two bytes.
nDLK0	uint8_t	L1 parameter k0 for DL (see 3GPP 38.211, section 5.3.1) Value: 0: -6, 1: 0, 2: 6. **See Note.**

Field	Type	Description
nULK0	uint8_t	L1 parameter k0 for UL (see 3GPP 38.211, section 5.3.1) Value: 0: -6, 1: 0, 2: 6. **See Note.**
nSSBMask[2]	uint32_t	Bitmap for actually transmitted SSB. 0: not transmitted 1: transmitted. MSB->LSB of the first 32-bit number corresponds to SSB 0 to SSB 31 MSB->LSB of the second 32-bit number corresponds to SSB 32 to SSB 63
nNrOfTxAnt	uint8_t	The number of physical transmission antennas (1 to 64).
nNrOfRxAnt	uint8_t	The number of physical receiving antennas (1 to 64).
nNrOfDlPorts	uint8_t	The maximum number of transmitting ports (1 to 16). Must be less than or equal to nNrOfTxAnt.
nNrOfULPorts	uint8_t	The maximum number of receiving virtual ports (1 to 8). Must be less than or equal to nNrOfRxAnt.
nCarrierAggregationLevel	uint8_t	Number of total carriers present
nFrameDuplexType	uint8_t	Frame Duplex type: 0 -> FDD, 1 -> TDD
nSubcCommon	uint8_t	subCarrierSpacingCommon if a carrier frequency <6 GHz, 0: 15 kHz, 1: 30 kHz if a carrier frequency > 6 GHz, 2: 60 kHz, 3: 120 kHz Value: from 0 to 3
nTddPeriod	uint8_t	TDD Period If nFrameDuplexType = TDD(1), then this config defines the TDD periodicity. The number of slots that TDD config in sSlotConfig will start to repeat.
sSlotConfig[MAX_TDD_PERIODICITY]	SLOTCONFIGStruct	TDD Slot configuration - If nFrameDuplexType = TDD(1), then this config defines the slot config type for each slot. The number of slots needs to be equal to the nTddPeriod. Refer to Table 7
nBeamId[64]	uint8_t	According to SSB Mask, the beam index filled. For example, if SSB mask bit 26 is set to 1, then nBeamId[26] will be used to indicate beam ID of SSB 26. **See Note.** Value: from 0 to 63

Field	Type	Description
nNrofTxRUPerBeam[64]	uint8_t	According to nBeamId[64], if nBeamId[26] is used, nNrofTxRUPerBeam[26] indicates the number of TxRU. **See Note.** Value: from 1 to 4
nTxRUIdx[64][MAX_TxRU_NUM]	uint8_t	TxRU index for SSB beam, refer to spec 36.897, section 5.2.2-1 and this document, Section 3.1.3 **See Note.** Value: from 0 to 3
nPrachConfIdx	uint8_t	PRACH Configuration Index Value: from 0 to 255
nPrachSubcSpacing	uint8_t	PRACH Subcarrier spacing Value: from 0 to 3
nPrachZeroCorrConf	uint8_t	PRACH zeroCorrelationZoneConfig Value: from 0 to 15
nPrachRestrictSet	uint8_t	PRACH restrictedSetConfig Value: from 0 to 2 0: unrestricted 1: restrictedToTypeA 2: restrictedToTypeB
nPrachRootSeqIdx	uint16_t	PRACH Root Sequence Index Value: from 0 to 837
nPrachFreqStart	uint16_t	The offset of lowest PRACH transmission occasion in the frequency domain Value: from 0 to 272
nPrachFdm	uint8_t	PRACH-FDM Value: 1, 2, 4,8
nPrachSsbRach	uint8_t	SSB-per-RACH-occasion Value: from 0 to 7 0: 1/8, 1:1/4, 2:1/2, 3:1,4:2, 5:4, 6:8, 7:16
nPrachNrOfRxRu	uint8_t	The number of receiving antennas for PRACH (1 to 4).
nCyclicPrefix	uint8_t	0 for normal, 1 for extended cyclic prefix
nGroupHopFlag	uint8_t	Group Hopping Flag for PUCCH Value: 0 or 1
nSequenceHopFlag	uint8_t	Sequence Hopping Flag for PUCCH, Value: 0 or 1
nHoppingId	uint16_t	Cell-Specific scrambling ID for group and sequence hopping for PUCCH
nUrllcCapable	uint16_t	Flag. Set equal to 1 to specify that the cell is URLLC capable. Set to 0 if it is not.
nUrllcMiniSlotMask	uint16_t	BitMask (14 Bits) which indicate which symbol numbers to send URLLC SLOT_IND to L2

NOTE: This field is not supported in the current release. Contact your Intel representative.

CONFIG.response

Table 20. CONFIG.response Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6
nCarrierIdx	uint8_t	Cell index Value: from 0 to 15
nStatus	uint8_t	Response 0: The configuration is completed 2: The configuration is not completed

START.request

Table 21. START.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7
nMode	uint32_t	0 = Radio mode, non-oran compliant. 1 = Timer mode (Test MAC). 2 = N/A for 5GNR 3 = Radio mode with ferrybridge front haul 4 = Radio mode, oran/xran compliant
nCount	uint32_t	For test mode only
nPeriod	uint32_t	For test mode only

START.response

Table 22. START.response Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nStatus	uint8_t	Response 0: starting succeeded 1: starting failed

STOP.request

Table 23. STOP.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.

Field	Type	Description
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.

STOP.response

Table 24. STOP.response Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nStatus	uint8_t	Response 0: stopping succeeded 1: stopping failed

Shutdown.request

Table 25. Shutdown.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nTestType	uint32_t	Used for internal unit testing

Shutdown.response

Table 26. Shutdown.response Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nStatus	uint32_t	Response 0: stopping succeeded 1: stopping failed

ERROR.indication

Table 27. ERROR.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.

Field	Type	Description
nStatus	uint8_t	Possible responses: /******ERROR indication*******/ #define MSG_OK (0x00) #define MSG_INVALID_STATE (0x01) #define MSG_INVALID_CONFIG (0x02)

3.2.4 Slot Messages

SLOT.indication

The SLOT.indication message format shows in Table 28. It is sent from every slot in the PHY.

Table 28. SLOT.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.

NOTE: Only send one slot.indication for all the carriers.

DL_CONFIG.request

The format of the DL_CONFIG.request message is shown in Table 29.

A DL_CONFIG.request message indicates the control information in a downlink slot. This message is sent from the L2 to L1.

The following combinations of PDUs are required:

- A Downlink DCI PDU
- A DLSCH PDU
- A BCH PDU
- A CSI-RS PDU

The PDUs included in this structure have no ordering requirements.

Table 29. DL_CONFIG.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nDCI	uint8_t	The number of DL DCIs included in this message.

Field	Type	Description
nPDU	uint8_t	Number of PDUs included in this message. All PDUs in the message are numbered in order. Range from 0 to 255
nGroup	uint8_t	The number of UE Groups included in this message.
nLte_CRS_Present	uint8_t	LTE 4G being transmitted concurrently on this slot. 0 = no 4 g, 1 = 4 g present, only valid for numerology = 0 (15 KHz)
nLte_CRS_carrierFreqDL	uint16_t	LTE 4G Downlink Center frequency (0 … 16383). Field from lte-CRS-ToMatchAround in ServingCellConfigCommon.
nLte_CRS_carrierBandwidthDL	uint8_t	LTE 4G bandwidth, number of resource blocks {n6, n15, n25, n50, n75, n100, spare2, spare1}. Field from lte-CRS-ToMatchAround in ServingCellConfigCommon
nLte_CRS_nrofCRS_Ports	uint8_t	LTE 4G, number of Tx Antennas {n1, n2, n4}. Field from lte-CRS-ToMatchAround in ServingCellConfigCommon.
nLte_CRS_v_shift	uint8_t	LTE 4G vShift = nPhyCellId % 6. {n0, n1, n2, n3, n4, n5}. Field from lte-CRS-ToMatchAround in ServingCellConfigCommon.
nPdcchPrecoderEn	uint8_t	Enable Precoder for DL and UL DCI PDUs. 0 = All PDCCH will be transmitted on 1 Tx Port as specified in 3GPP. 1 = All PDCCH will go through pre-defined precoder and transmitted on all Tx Ports.
nSSBPrecoderEn	uint8_t	Enable Precoder on SSB. 0 = SSB will be transmitted on 1 Tx Port as specified in 3GPP. 1 = SSB will go through pre-defined precoder and transmitted on all Tx Ports.
nRsv[1]	uint8_t	reserved
sPDSCHGroupInfoStruct	PDSCHGroupInfoStruct	PDSCH Group Information Structure. Refer to Table 10.
For Number of PDUs		
sDLPDU[]	PDUStruct	Pointer to each PDU Structure 0: DL DCI PDU, refer to Table 30. 1: DLSCH PDU, refer to Table 31. 2: CSI-RS PDU, refer to Table 32. 3: BCH PDU, refer to Table 33.

Downlink (DL) Control Information (DCI) Protocol Data Unit (PDU)

Table 30. DL DCI PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nRNTI	uint16_t	The RNTI associated with the UE Value: from 1 to 65535
nBWPSize	uint16_t	Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275
nBWPStart	uint16_t	Bandwidth part start RB. **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type. **See Note.** 0: Normal; 1: Extended
nFreqDomain[2]	uint32_t	CORESET-freq-dom.frequencyDomainResources. The bits of the bitmap has a one-to-one mapping with non-overlapping groups of 6 RBs. The most significant bit of the first word corresponds to the most significant bit defined in 3GPP 38.331. See Table 2 for the 3GPP Spec location.
nStartSymbolIndex	uint8_t	Starting OFDM symbol for the CORESET Value: from 0 to 13
nNrOfSymbols	uint8_t	The contiguous time duration of the CORESET in number of symbols
nCCEToREGType	uint8_t	CORESET-CCE-to-REG-mapping-type 0: non-interleaved CCE-to-REG mapping 1: interleaved CCE-to-REG mapping
nREGBundleSize	uint8_t	CORESET-REG-bundle-size, Variable R in section 7.3.2.3 in spec 38.211. See Table 2 for 3GPP Spec location. Value: 2,3,6
nShift	uint16_t	Refer to section 7.3.2.2 in spec 38.211. See Table 2 for the 3GPP Spec location. If it is for a PDCCH transmitted in a CORESET configured by the PBCH or SIB1, L2 needs to set it to a physical cell ID. Otherwise, L2 needs to set it to CORESET-shift-index.

Field	Type	Description
nScid	uint16_t	Refer to section 7.3.2.3 in spec 38.211. See Table 2 for the 3GPP Spec location. For a UE-specific search space, it equals the higher-layer parameter PDCCH-DMRS-Scrambling-ID if configured. Otherwise, L2 needs to set it to a physical cell ID.
nCCEStartIndex	uint8_t	CCE start Index used to send the DCI: Value: from 0 to 135
nAggrLvl	uint8_t	Aggregation level used: Value: 1,2,4,8,16
nInterleaveSize	uint8_t	CORESET-interleaver-size Value: 2,3,6
nCoreSetType	uint8_t	Value: 0 or 1 0: CORESET is configured by the PBCH or SIB1 1: otherwise
nRNTIScramb	uint16_t	Refer to section 7.3.2.3 in spec 38.211. See Table 2 for the 3GPP Spec location. It is given by the C-RNTI for a PDCCH in a UE-specific search space if the higher-layer parameter PDCCH-DMRS-Scrambling-ID is configured, otherwise L2 needs to set it to zero.
nTotalBits	uint16_t	The total DCI length including padding bits
nEpreRatioOfPDCCHToSSB	uint16_t	PDCCH DATA EPRE Value: 0 means using default value. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to current SSB value
nEpreRatioOfDmrsToSSB	uint16_t	PDCCH DMRS EPRE Value: 0 means using default value. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to current SSB value
nDciBits [DCI_PAYLOAD_BYTE_LEN]	uint8_t	DCI payload, bit order is as following bit0-bit7 are mapped to the first byte of MSB - LSB
nBeamId	uint8_t	Beam index that UE DL DCI used. **See Note.** Value: from 0 to 63
nNrofTxRU	uint8_t	TxRU number. **See Note.** Value: from 0 to 4
nID	uint16_t	Refer to section 7.3.2.3 in spec 38.211. See Table 2 for the 3GPP Spec location. It equals the higher-layer parameter Data-scrambling-Identity if configured, and the RNTI equals the C-RNTI. Otherwise, L2 needs to set it to physical cell id.

Field	Type	Description
nTxRUIdx[MAX_TXRU_NUM]	uint8_t	Mapping to the Tx stream index to the RRU. Will map to the DL Port index used by this PDCCH. The range will be determined by nNrOfDlPorts, as defined in the CONFIG_REQ message. Value: from 0 to (nNrOfDlPorts – 1)

NOTE: This field is not supported in the current release. Contact your Intel representative.

DLSCH PDU

Table 31. DLSCH PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nRNTI	uint16_t	The RNTI used for identifying the UE when receiving the PDU. Value: from 1 to 65535.
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nBWPSize	uint16_t	Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275
nBWPStart	uint16_t	Bandwidth part starts the RB index. **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing. **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type. **See Note.** 0: Normal; 1: Extended
nMcsTable	uint8_t	MCS-Table-PDSCH 0: set to '64QAM' 1: set to '256QAM' 2: set to '64QAMLowSE'
nNrOfCodeWords	uint8_t	Up to 2 code words Value: 1, 2
nMCS[2]	uint8_t	MCS index Value: from 0 to 31 Support 2 code words
nRV[2]	uint8_t	Redundancy version Value: from 0 to 3 Support 2 code words

Field	Type	Description
nNDI[2]	uint8_t	New data indication 0: retransmission 1: new data Support 2 code words
nNrOfLayers	uint8_t	Layer number Value: from 1 to 8 single user, up to 8 layers multi-user, up to 4 layers
nNrOfAntennaPorts	uint8_t	Number of antenna ports Value: from 1 to 8
nTBSize[2]	uint32_t	Transmit block size (in bytes) Support 2 code word
nPortIndex[8]	uint8_t	Antenna port index 0: port 1000 1: port 1001 2: port 1002 .... 11: port 1011 Value: from 0 to 11
nHARQID	uint8_t	HARQ Process number, 0 to 15
nSCID	uint8_t	For DMRS generation Value: 0, 1
nNIDnSCID	uint16_t	Refer to section 7.4.1.1.2 in spec 38.211. See Table 2 for the 3GPP Spec location. It is given by the higher-layer parameter DL-DMRS-Scrambling-ID if provided, and the PDSCH is scheduled by the PDCCH with the CRC scrambled by the C-RNTI or CS-RNTI. Otherwise, the L2 needs to set it to physical cell id.
nVRBtoPRB	uint8_t	VRB-to-PRB-mapping. **See Note.** 0: non-interleaved VRB-to-PRB mapping 1: interleaved VRB-to-PRB mapping
nRBBundleSize	uint8_t	Resource block bundle size L, refer to section 7.3.1.6 in spec 38.211. See Table 2 for the 3GPP Spec location. **See Note.**
nStartSymbolIndex	uint8_t	Start symbol index of PDSCH mapping, include both DMRS and data Value: from 0 to 13
nNrOfSymbols	uint8_t	PDSCH duration in symbols include both DMRS and data Value: from 1 to 14

Field	Type	Description
nRBStart	uint16_t	For resource allocation type 1. The starting resource block for this DLSCH allocation.
nRBSize	uint16_t	For resource allocation type 1. The number of resource blocks allocated to this DLSCH grant should match the value sent in the DL DCI PDU, which allocated this grant.
nResourceAllocType	uint8_t	Resource allocation type (currently only support type 1). 0: type 0 1: type 1
nNrOfRBGs	uint8_t	For resource allocation type 1. Number of Resource Blocks per group. **See Note.**. Valid Values: 1 to 5
nRBGSize	uint8_t	For resource allocation type 0. **See Note.** RBG size Value: 2,4,8,16
rsv	uint8_t	Reserved
nRBGIndex[5]	uint32_t	For resource allocation type 0. **See Note.** RBG index allocated for this DLSCH in the bitmap. The most significant bit represents the RBG of the lower Index. The maximum number is 138, with 275 RBs and RBG size 2.
nMappingType	uint8_t	PDSCH mapping Type 0: mapping type A 1: mapping type B
nDMRSConfigType	uint8_t	DL DMRS config type 0: type 1 1: type2
nNrOfCDMs	uint8_t	Several DM-RS CDM groups without data, it determines the ratio of PDSCH EPRE to DM-RS EPRE. Refer to Table 4.1-1 in spec 38.214. See Table 2 for the 3GPP Spec location. Value: 1, 2, 3
nNrOfDMRSSymbols	uint8_t	DL DMRS symbol number 1: single symbol 2: double symbol
nDMRSAddPos	uint8_t	DL additional DMRS position DL-DMRS-add-pos Value: from 0 to 3

Field	Type	Description
nPTRSPresent	uint8_t	DL-PTRS-present 0: PT-RS is not present 1: PT-RS is present
nNrOfPTRSPorts	uint8_t	DL-PTRS-ports (currently only support 1). Up to 2 ports Value: 1, 2
nPTRSTimeDensity	uint8_t	PT-RS time density Value: 0,1, 2 or 4 0 means PT-RS is not present
nPTRSPortIndex[2]	uint8_t	Value: from 0 to 11 0: port 1000 1: port 1001 2: port 1002 .... 11: port 1011
nNrOfDMRSAssPTRS[2]	uint8_t	The number of DM-RS ports associated with PT-RS.it should be relative to DMRS-group. Value: from 1 to 6
nPTRSFreqDensity	uint8_t	PT-RS frequency density Value: 0, 2 or 4 0 means PT-RS is not present
nPTRSReOffset	uint8_t	DL-PTRS-RE-offset, refer to Table 7.4.1.2.2-1 in spec 38.211. See Table 2 for 3GPP Spec location. Value: from 0 to 3
nEpreRatioOfPDSCHToPTRS	uint8_t	PDSCH-to-PT-RS EPRE ratio ratio of PDSCH EPRE to PTRS EPRE, refer to Table 4.1-2 in spec 38.213. See Table 2 for the 3GPP Spec location. Value: from 0 to 3
rsv1	uint8_t	Reserved
nTransmissionScheme	uint8_t	0: non-codebook-based transmission 1: codebook-based transmission
nCodebookType	uint8_t	codebookType in spec 38.214, see Table 2 for 3GPP Spec location. 0: Type1 Single-Panel 1: Type I Multi-Panel 2: Type II 3: Type II Port Selection
nCodebookMode	uint8_t	0: codebook mode 1 1: codebook mode 2

Field	Type	Description
nPMI	uint8_t	Codebook index Refer to Table 5.2.2.2.1-1 in 38.214. See Table 2 for the 3GPP Spec location.
n1n2	uint16_t	n1_n2 = n1 << 8 + n2, n1 n2 values are corresponding to table 5.2.2.2.2.1-2 in 38.214. See Table 2 for 3GPP Spec location.
nEpreRatioOfDmrsToSSB	uint16_t	PDSCH DMRS EPRE Value: 0 means using default value. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to current SSB value
nNid	uint16_t	Refer to section 7.3.1.1 in spec 38.211. See Table 2 for the 3GPP Spec location. It equals the higher-layer parameter Data-scrambling-Identity if configured, and the RNTI equals the C-RNTI. Otherwise, L2 needs to set it to physical cell id.
nBeamId	uint8_t	Beam index. **See Note.** Value: from 0 to 63
nNrofTxRU	uint8_t	Number of TxRU. **See Note.** Value: from 1 to 4
nEpreRatioOfPDSCHToSSB	uint16_t	PDSCH DATA EPRE Value: 0 means using default vale. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to current SSB value
rv2	uint16_t	Reserved
nTxRUIdx[MAX_TXRU_NUM]	uint8_t	Mapping to the Tx stream index to the RRU. Will map to the DL Port index used by this PDSCH. The range will be determined by nNrOfDlPorts, as defined in the CONFIG_REQ message. Value: from 0 to (nNrOfDlPorts – 1)

NOTE: This field is not supported in the current release. Contact your Intel representative.

CSI-RS PDU

Table 32. CSI-RS PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nBWPSize	uint16_t	Bandwidth part size Value: from 0 to 275 Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275

Field	Type	Description
nBWPStart	uint16_t	Bandwidth part start RB index. **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing. **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type **See Note.** 0: Normal; 1: Extended
nStartRB	uint16_t	PRB where this Channel Status Information (CSI) resource starts. Only multiples of four are allowed.
nNrOfRBs	uint16_t	Number of PRBs across which this CSI resource spans. Value: from 0 to nBWPSize
nCSIType	uint8_t	CSI Type 0:TRS 1:CSI-RS 2:CSI-IM NZP 3:CSI-IM ZP
nRow	uint8_t	The row in table 7.4.1.5.3-1 of 38.211. See Table 2 for the 3GPP Spec location. Value: from 1 to 18
nFreqDomain	uint16_t	Bitmap for frequencyDomainAllocation
nNrOfPorts	uint8_t	nrofPorts Value: 1,2,4,8,12,16,24,32
nCDMType	uint8_t	cdm-Type Value: 0: noCDM, 1: fd-CDM2, 2: cdm4-FD2-TD2, 3: cdm8-FD2-TD4
nSymbL0	uint8_t	firstOFDMSymbolInTimeDomain Value: from 0 to 13
nSymbL1	uint8_t	firstOFDMSymbolInTimeDomain2 Value: from 0 to 13
nFreqDensity	uint8_t	CSI-RS-Density 0: dot5, 1: one, 2: three
nCombOffset	uint8_t	RB level comb offset only if CSI-RS-Density is dot5 0: even RB, 1: odd RB
nScrambId	uint16_t	ScramblingID Value: from 0 to 1023
nEpreRatioToSSB	Uint16_t	CSI-RS EPRE Value: 0 means using default value. from 1 to 20000 means 0.001 dB step, -6dB to 14 dB difference to current SSB value
nBeamId	uint8_t	Beam index. **See Note.** Value: from 0 to 63

Field	Type	Description
nNrofTxRU	uint8_t	TxRU number. **See Note.** Value:1, 2
nTxRUIdx[MAX_TXRU_NUM]	uint8_t	Mapping to the Tx stream index to the RRU. Will map to the DL Port index used by this CSI-RS. The range will be determined by nNrOfDlPorts, as defined in the CONFIG_REQ message. Value: from 0 to (nNrOfDlPorts – 1)

NOTE: This field is not supported in the current release. Contact your Intel representative.

BCH PDU

Table 33. BCH PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nSSBSubcOffset	uint8_t	ssb-subcarrierOffset Value: from 0 to 23
nSSBPrbOffset	uint8_t	ssb-PrbOffset value: 0 to 253
nMIB[3]	uint8_t	MSB->LSB of the first byte corresponds to bit0 to bit7 The same bit order applies to the other two bytes

UL_CONFIG.request

The following combinations of the PDUs are required in UL_CONFIG.request:

- The ULSCH PDU is present when a UE has been instructed to send uplink data
- The ULCCH_UCI PDU is present when a UE has been instructed to send uplink UCI
- The ULRACH PDU is present when PRACH is transmitted in the slot
- The SRS PDU is present when a UE has been instructed to send Sounding Reference Signal (SRS).

Table 34. UL_CONFIG.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nPDU	uint16_t	Number of PDUs that are included in this message.
nGroup	uint8_t	Several UE Groups included in this message. Value: 1-8

Field	Type	Description
nUlsch	uint8_t	Several of ULSCH PDUs that are included in this message.
nUlcch	uint16_t	Several of ULCCH PDUs that are included in this message.
nRachPresent	uint8_t	0: do not receive RACH in this slot; 1: receive RACH in this slot
nUlsrs	uint8_t	Several of SRS PDUs that are included in this message.
sPUSCHGroupInfoStruct [MAX_MIMO_GROUP_NUM]	PUSCHGroupInfoStruct	Describes how many UEs and which UEs are part of each PUSCH Group. Maximum number of PUSCH groups supported is MAX_MIMO_GROUP_NUM, which is defined to be 16
For the number of PDUs:		
sULPDU[]	PDUStruct	Pointer to each PDU Structure 4: ULSCH_PDU, refer to Table 35. 5: ULCCH_PDU, refer to Table 36. 7: SRS_PDU, refer to Table 38. 8: ULRACH_PDU, refer to Table 39.

ULSCH PDU

Table 35. ULSCH PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nRNTI	uint16_t	The RNTI used for identifying the UE when receiving the PDU Value: from 1 to 65535.
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nBWPSize	uint16_t	Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275
nBWPStart	uint16_t	Bandwidth part start RB index. **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing. **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type. **See Note.** 0: Normal; 1: Extended
nULType	uint8_t	Uplink frequency. **See Note.** 0: NR UL ; 1: supplementary UL

Field	Type	Description
nMcsTable	uint8_t	MCS-Table-PDSCH 0: set to '64QAM' 1: set to '256QAM' 2: set to '64QAMLowSE'
nMCS	uint8_t	MCS index Value: from 0 to 31
nTransPrecode	uint8_t	0: transform precoding disabled 1: transform precoding enabled
nTransmissionScheme	uint8_t	0: non-codebook-based transmission 1: codebook-based transmission
nNrOfLayers	uint8_t	Number of layers Value: from 1 to 4
nPortIndex[4]	uint8_t	Antenna port index 0: port 0 1: port 1 2: port 2 .... 11: port 11 Value: from 0 to11
rsv1	uint8_t	Reserved
nSCID	uint8_t	For DMRS generation Value: 0, 1
nNIDnSCID	uint16_t	Refer to section 7.4.1.1.2 in spec 38.211. See Table 2 for the 3GPP Spec location. It is given by the higher-layer parameter UL-DMRS-Scrambling-ID if provided, and the PUSCH is not an msg3 PUSCH. Otherwise, L2 needs to set it to physical cell id.
nNrOfAntennaPorts	uint8_t	Number of antenna ports Value: 1, 2, 4
nVRBtoPRB	uint8_t	VRB-to-PRB-mapping. See **Note** 0: non-interleaved VRB-to-PRB mapping 1: interleaved VRB-to-PRB mapping
nRBBundleSize	uint8_t	Resource block bundle size L. See **Note** Refer to Section 6.3.1.6 in spec 38.211. See Table 2 for the 3GPP Spec location.
nPMI	uint8_t	Precoding matrix indicator Value: from 0 to 27
nStartSymbolIndex	uint8_t	Start symbol index of PUSCH mapping, include both DMRS and data

Field	Type	Description
		Value: from 0 to 13
nNrOfSymbols	uint8_t	PUSCH duration in symbols include both DMRS and data Value: from 1 to 14
nResourceAllocType	uint8_t	Resource allocation type (currently only supports type 1). 0: type 0 1: type 1
nRBGSize	uint8_t	For resource allocation type 0. See **Note**, RBG size Value: 2,4,8,16
nRBStart	uint16_t	For resource allocation type 1. The starting resource block for this ULSCH allocation.
nRBSize	uint16_t	For resource allocation type 1. The number of resource blocks allocated to this ULSCH grant should match the value sent in the DCI Format 0 PDU, which allocated this grant.
nRBGIndex[5]	uint32_t	For resource allocation type 0. **See Note.** RBG index allocated for this DLSCH in the bitmap. The most significant bit represents the RBG of the lower Index. The maximum number is 138, with 275 RBs and RBG size 2.
nTBSize	uint32_t	Transmit block size (in bytes)
nNrOfRBGs	uint8_t	For resource allocation type 0. **See Note.** Number of RBGs
nRV	uint8_t	Redundancy version Value: from 0 to 3
nHARQID	uint8_t	HARQ Process number. Value: from 0 to 15
nNDI	uint8_t	Specify whether this received xPUSCH is a new transmission from UE. This should match the value sent in the DCI Format 0 PDU, which allocated this grant. 0: retransmission 1: new data
nMappingType	uint8_t	PUSCH mapping type 0: mapping type A

Field	Type	Description
		1: mapping type B
nDMRSConfigType	uint8_t	UL DMRS config type 0: type 1 1: type2
nNrOfCDMs	uint8_t	Several DM-RS CDM groups without data. It determines the ratio of PUSCH EPRE to DM-RS EPRE. Refer to Table 6.2.2-1 in spec 38.214. See Table 2 for the 3GPP Spec location. Value: from 1 to 3
nNrOfDMRSSymbols	uint8_t	Number of UL DMRS symbols 1: single symbol 2: double symbol
nDMRSAddPos	uint8_t	UL additional DMRS position. Refer to Table 6.4.1.1.3-3 and Table 6.4.1.1.3-4 in spec 38.211. See Table 2 for the 3GPP Spec location. UL-DMRS-add-pos Value: from 0 to 3
nPTRSPresent	uint8_t	UL-PTRS-present 0: PT-RS is not present 1: PT-RS is present
nNrOfPTRSPorts	uint8_t	UL-PTRS - (currently only supports 1). Up to 2 ports Value: from 1 to 2
nPTRSTimeDensity	uint8_t	PT-RS time density Value: 0,1, 2 or 4 0 means PT-RS is not present
nPTRSPortIndex[2]	uint8_t	0: port 0 1: port 1 2: port 2 .... 11: port 11 Value: from 0 to 11
nPTRSFreqDensity	uint8_t	PT-RS frequency density Value: 0, 2 or 4 0 means PT-RS is not present
nPTRSReOffset	uint8_t	UL-PTRS-RE-offset, refer to Table 6.4.1.2.2.1-1 in spec 38.211. See Table 2 for the 3GPP Spec location. Value: from 0 to 3
nTpPi2BPSK	uint8_t	TP with Pi2BPSK. 0: TpPi2BPSK Disabled 1: TpPi2BPSK Enabled

Field	Type	Description
nNid	uint16_t	Refer to section 6.3.1.2 in spec 38.211. See Table 2 for the 3GPP Spec location. It equals the higher-layer parameter Data-scrambling-Identity if configured, and the RNTI equals the C-RNTI. Otherwise, L2 needs to set it to physical cell id.
nAlphaScaling	uint8_t	Refer to Section 6.3.2 in spec 38.331, PUSCH-Config. See Table 2 for 3GPP Spec location. Scaling configured by higher layer parameter. ENUMERATED for UCI-onPUSCH RRC {f0p5, f0p65, f0p8, f1 }, Value 0 to 3
nBetaOffsetACKIndex	uint8_t	ACK Beta offset Index Value from 0 to 15
nAck	uint16_t	Number of UCI HARQ ACK/NACK bits multiplexed with PUSCH. 0 means ACK bits are not multiplexed with PUSCH. Value 0 to 640.
nBetaOffsetCSIP1Index	uint8_t	CSI Part 1 Beta offset Index Value from 0 to 18
nBetaOffsetCSIP2Index	uint8_t	CSI Part 2 Beta offset Index Value from 0 to 18
nCSIPart1	uint16_t	Number of UCI CSI Part 1 bits multiplexed with PUSCH. 0 means CSI Part 1 bits are not multiplexed with PUSCH. Value 0 to 640.
nCSIPart2	uint16_t	Number of UCI CSI Part 2 bits multiplexed with PUSCH. 0 means CSI Part 2 bits are not multiplexed with PUSCH. Value 0 to 640.
nBeamId	uint8_t	Beam index. **See Note.** Value: from 0 to 63
nNrofRxRU	uint8_t	Number of RxRU. **See Note.** Value: from 1 to 4
nTPPuschID	uint16_t	nPUSCH-Identity
nRxRUIdx[MAX_RXRU_NUM]	uint8_t	Mapping to the Rx stream index to the RRU. Will map to the UL Port index used by this PUSCH. The range will be determined by nNrOfUlPorts, as defined in the CONFIG_REQ message. Value: from 0 to (nNrOfUlPorts – 1)

NOTE: This field is not supported in the current release. Contact your Intel representative.

ULCCH_UCI PDU

Table 36. ULCCH_UCI PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nRNTI	uint16_t	The RNTI used for identifying the UE when receiving the PDU Value: from 1 to 65535
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199
nBWPSize	uint16_t	Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275
nBWPStart	uint16_t	Bandwidth part start RB index **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing. **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type. **See Note.** 0: Normal; 1: Extended
nULType	uint8_t	Uplink frequency. **See Note.** 0: NR UL; 1: supplementary UL
nFormat	uint8_t	PUCCH format Value: from 0 to 4
nID	uint16_t	Data scrambling identity if high layer configured otherwise is nCellID valid for Format 2, 3, and 4. Value: from 0 to 1023
nScramID	uint16_t	Using for reference signal scrambling valid for Format 2. Value: from 0 to 65535
nSRPriodAriv	uint8_t	Whether SR period arrived valid for Format 0. Value: 0, 1
nStartSymbolx	uint8_t	Index of first symbol Value: from 0 to 13
nStartPRB	uint16_t	Index of the first PRB before frequency hopping or no-hopping Value: from 0 to 275
n2ndHopPRB	uint16_t	Index of the first PRB after frequency hopping Value: from 0 to 272
nPRBs	uint16_t	Several PRBs (valid for Formats 2 and 3)

Field	Type	Description
		Value: from 1 to 272
nSymbols	uint8_t	Number of symbols Value: 1,2, from 4 to 14
nFreqHopFlag	uint8_t	Frequency hopping for a PUCCH resource enabled or disabled (valid for Formats 1, 3, and 4) Value: 0, 1
nM0	uint16_t	Format 0: Value: 0 to 8 for SR only. (9,10,11 used by PUCCH algorithm for noise estimation) 0 to 4, 6 to 10 for 1 bit ACK/NACK (5 and 11 used by PUCCH algorithm for noise estimation) Value: 0 to 11 for all other scenarios Format 1: Value: 0 to 8. (9,10,11 used by PUCCH algorithm for noise estimation)
nAddDmrsFlag	uint8_t	Flag for additional DMRS (valid for Format 3 and 4) Value: 0, 1
rsv	uint8_t	Reserved
nFmt1OrthCCodeIdx	uint8_t	An index of an orthogonal cover code in case of PUCCH Format 1 Value: from 0 to 6
nFmt4OrthCCodeIdx	uint8_t	An index of an orthogonal cover code in case of PUCCH Format 4 Value: 0,1,2,3
nFmt4OrthCCodeLength	uint8_t	A length of an orthogonal cover code in case of PUCCH Format 4 Value: 2,4
modType	uint8_t	Modulation type for PUCCH Format 3 and 4, Value: 1-pi/2 BPSK or 2-QPSK
nBitLenUci	uint16_t	The bit length of UCI payload for formats 1, 2, 3, and 4 orbit length of UCI payload excludes SR for Format 0.
nBeamId	uint8_t	Beam index. **See Note.** Value: from 0 to 63
nNrofRxRU	uint8_t	Number of RxRU. **See Note.** Value: from 1 to 4
nGroupId	uint16_t	Group ID for Format 1

Field	Type	Description
		Value: 0 to 200
nRxRUIdx[MAX_RXRU_NUM]	uint8_t	RxRU index, refer to 3.1.3 and spec 36.897, section 5.2.2-1. **See Note.** Value: from 0 to 3

NOTE: This field is not supported in the current release. Contact your Intel representative.

ULRACH PDU

Table 37. ULRACH PDU

Field	Type	Description
sPDUHdr	PDUStruct	Header showing the PDU type and length. Refer to Table 9.
nNrofPrachOcas	uint8_t	Number of PRACH occasion per slot value: from 1 to7, according to spec, max to 7 PRACH occasions per slot
nNrofBeamPerOcas	uint8_t	Number of beams per PRACH Occasion Value: from 1 to 4
nBeamIdPerSlot [MAX_PANEL_NUM]	uint8_t	Beam index per slot, MAX_PANEL_NUM is set to 4. **See Note.** Value: from 0 to 63
nNrofRxRuPerBeam [MAX_PANEL_NUM]	uint8_t	RxRU number per beam. **See Note.** Value: from 1 to 4
nRxRUIdx[MAX_PANEL_NUM] [MAX_RxRU_NUM]	uint8_t	RxRU index, refer to Section 3.1.3 and spec 36.897, section 5.2.2-1. See Table 2 for the 3GPP Spec location. **See Note.** Value: from 0 to 3

NOTE: This field is not supported in the current release. Contact your Intel representative.

SRS PDU

Table 38. SRS PDU

Field	Type	Description
sPDUHdr	PDUStruct	The header shows the PDU type and length. Refer to Table 9.
nRNTI	uint16_t	The RNTI used for identifying the UE when receiving the PDU Value: from 1 to 65535
nUEId	uint16_t	UE index in the sector Value: from 0 to 1199

Field	Type	Description
nBWPSize	uint16_t	Bandwidth part size. The minimum size is equal to SSB size (20 RBs). **See Note.** Value: from 20 to 275
nBWPStart	uint16_t	Bandwidth part starts the RB index. **See Note.** Value: from 0 to 254
nSubcSpacing	uint8_t	subcarrierSpacing. **See Note.** Value: from 0 to 4
nCpType	uint8_t	Cyclic prefix type. **See Note.** 0: Normal; 1: Extended
nStartPos	uint8_t	startPosition, the starting position in the time domain (see 3GPP 38.211 Sec 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 5
nNrOfSymbols	uint8_t	Number of SRS symbols Value: 1, 2, 4.
nComb	uint8_t	Transmission comb (see 3GPP 38.211 section 6.4.1.4.2). See Table 2 for 3GPP Spec location. Value: 2, 4
nCombOffset	uint8_t	combOffset (see 3GPP 38.211 section 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 3
nNrOfSrsPorts	uint8_t	Number of SRS ports Value: 1, 2, 4.
nCyclicShift	uint8_t	cyclicShift (see 3GPP 38.211 section 6.4.1.4.2). See Table 2 for 3GPP Spec location. Value: from 0 to 11
nBSrs	uint8_t	b-SRS , SRS bandwidth index Bsrs (3GPP 38.211 Section 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 3
nCSrs	uint8_t	c-SRS, SRS bandwidth config index Csrs (3GPP 38.211 section 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 63
nBHop	uint8_t	b-hop (see 3GPP 38.211 section 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 3

Field	Type	Description
nHopping	uint8_t	groupOrSequenceHopping Value: from 0 to 2 0: neither, 1: groupHopping, 2: sequenceHopping
nFreqPos	uint8_t	freqDomainPosition, nRRC (see 3GPP 38.211 section 6.4.1.4.3). See Table 2 for 3GPP Spec location. Value: from 0 to 67
nResourceType	uint8_t	Value: from 0 to 2 0: aperiodic, 1: semi-persistent, 2: periodic
nFreqShift	uint16_t	freqDomainShift, nShift Value: from 0 to 268
nSrsId	uint16_t	The SRS sequence identity, sequenceId (see 3GPP 38.211 section 6.4.1.4.2). See Table 2 for 3GPP Spec location. Value: from 0 to 1023
nRepetition	uint8_t	repetitionFactor Value: 1, 2, 4.
nTsrs	uint16_t	SRS-Periodicity in slots Value: 1,2,3,4,5,8,10,16,20,32,40,64,80,160,320,640,1280,2560
nToffset	uint16_t	SRS-Periodicity offset in slots Value: from 0 to 2559
nBeamId	uint8_t	Beam index. **See Note.** Value: from 0 to 63
nNrofRxRU	uint8_t	Number of RxRU, refer to Section 3.1.3. **See Note.** Value: from 1 to 4
nRxRUIdx[MAX_RXRU_NUM]	uint8_t	RxRU index, refer to and Section 3.1.3 and spec 36.897, section 5.2.2-1. **See Note.** Value: from 0 to 3

NOTE: This field is not supported in the current release. Contact your Intel representative.

UL_DCI.request

UL_DCI.request message includes DCI content used for the scheduling of PUSCH.

Table 39. UL DCI PDU

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. See Table 7.
nDCI	uint8_t	The number of UL DCI PDUs included in this message.
For several UL DCIs:		
sULDCIPDU	DL_DCI_PDU	See Table 22. PDUType is set to DL_PDU_TYPE_DCI.

3.2.4.1 Downlink Data

TX.request

The format of the TX.The request message is described in Table 40. This message contains the MAC PDU data for transmission over the air interface. The PDUs described in this message must follow the same order as DL_CONFIG.request. This message is sent from the L2 to PHY.

Table 40. TX.request Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7. SFN_SlotStruct Structure Type.
nPDU	uint8_t	Number of PDUs that are included in this message. Range from 0 to 255
For number of PDUs:		
sDLPDUDataStruct[]	uint8_t	Pointer to DLPDUDataStruct. Refer to Table 12.

3.2.4.2 Uplink Data

CRC.indication

Table 41. CRC.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7. SFN_SlotStruct Structure Type.
nCrc	uint8_t	Number of CRCs included in this message: Value from 0 to 255
For each CRC:		

Field	Type	Description
sULCRCStruct[]	ULCRCStruct	Pointer to CRC structure. Refer to Table 13. CRCIndicationStruct Structure Type.

RX_ULSCH.indication

Table 42. RX_ULSCH.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nUlsch	uint8_t	The number of ULSCH PDUs included in this message. Value: from 0 to 255
For each ULSCH PDU:		
sULSCHPDUDataStruct[]	ULSCHPDUDataStruct	Pointer to each ULSCH PDU Data Structure. Refer to Table 14.

UCI.indication

UCI.indication message includes UCI payload in PUCCH or PUSCH.

Table 43. UCI.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nUci	uint8_t	The number of ULUCI PDUs included in this message. Value: from 0 to 255
For each ULUCI PDU:		
sULUCIPDUDataStruct[]	ULUCIPDUDataStruct	Pointer to each ULUCI Data Structure. Refer to Table 16.

RACH.indication

RACH.indication message includes received PRACH information.

Table 44. RACH.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nNrOfPreamb	uint8_t	The number of preambles detected.
For each preamble:		

Field	Type	Description
sPreambleStruct[]	PreambleStruct	Pointer to each PRACH Preamble detected. Refer to Table 17.

SRS.indication

SRS.indication message includes received SRS information.

Table 45. SRS.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nNrOfSrs	uint8_t	The number of SRS PDUs included in this message.
For each SRS PDU:		
sULSRSEstStruct[]	ULSRSEstStruct	Pointer to each SRS Estimation structure. Refer to Table 18. ULSRSEstStruct Structure Type.

RX_ULSCH_UCI.indication

RX_ULSCH_UCI.indication message includes received PUSCH multiplex with UCI information.

Table 46. RX_ULSCH_UCI.indication Message Body

Field	Type	Description
sMsgHdr	L1L2MessageHdr	Message Header. Refer to Table 6.
sSFN_Slot	SFN_SlotStruct	System Frame Number Structure. Refer to Table 7.
nUlschUci	uint8_t	The number of ULSCH UCI PDU's included in this message. Value: from 0 to 255
For each ULSCH UCI PDU:		
sULSCHUCIPDUDataStruct[]	ULSCHUCIPDUDataStruct	Pointer to each ULSCH UCI Data structure. Refer to Table 15.

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