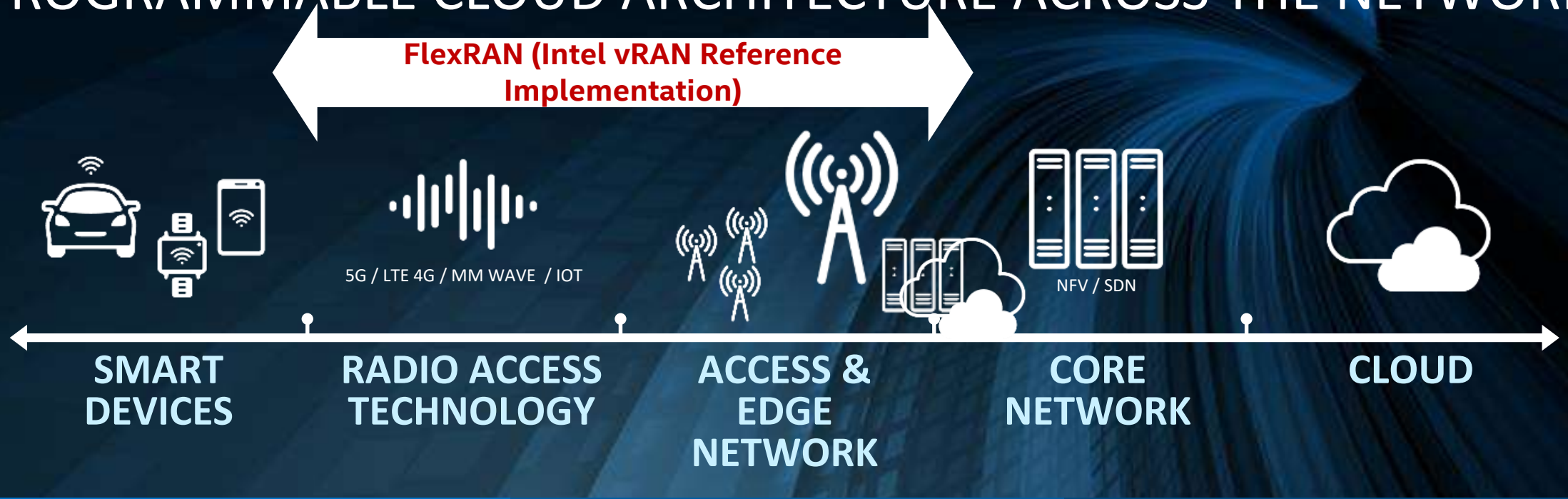
INTEL FLEXRAN

5G Infrastructure Division
Network Platforms Group
Intel Corporation

June 2018

NETWORK TRANSFORMATION END-TO-END

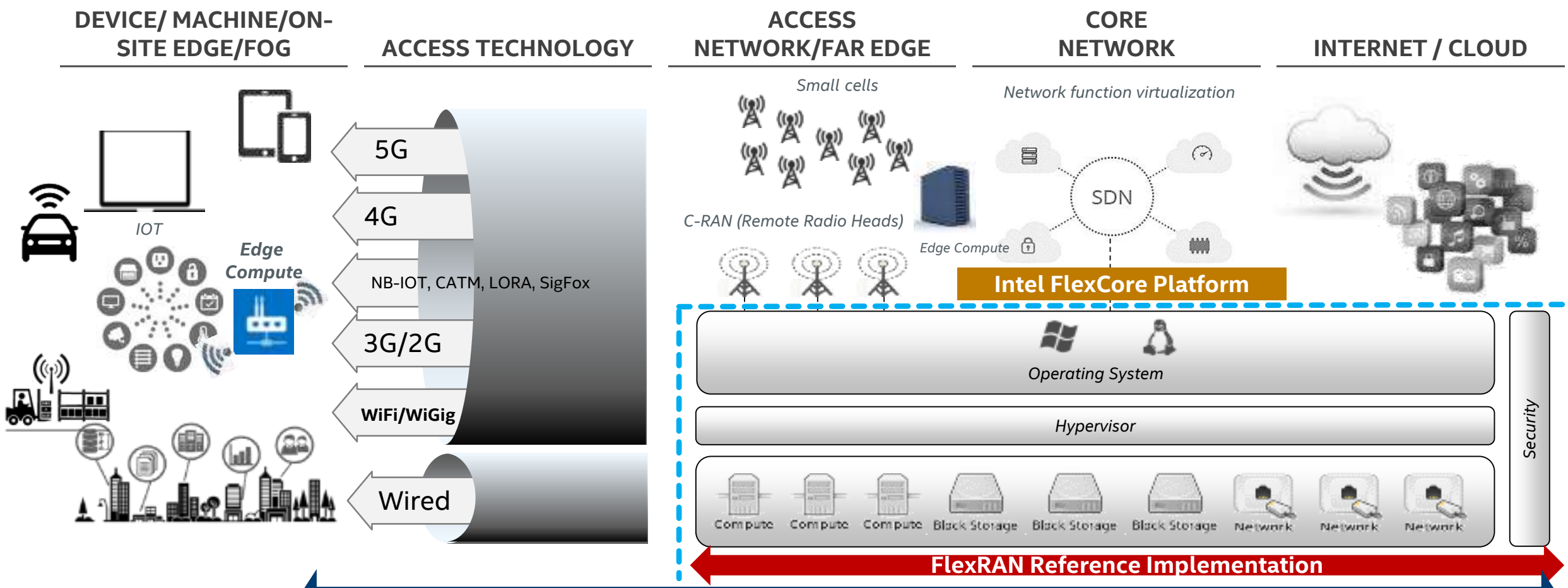
PROGRAMMABLE CLOUD ARCHITECTURE ACROSS THE NETWORK



VIRTUALIZED | SOFTWARE-DEFINED | CLOUD-READY

INTEL ENABLING VIRTUALIZATION OF THE RADIO ACCESS NETWORK

5G + IOT E2E COMMUNICATION TRANSFORMATION



Benefits of Network Virtualization

Benefits of vRAN for Comms Service Providers and Enterprises

- Coordination, centralization and virtualization in mobile networks.
- Enabler of new services at the network edge.
- Supports resource pooling (more cost-efficient processor sharing) and load balancing.
- Scalability (more flexible hardware capacity expansion) from high capacity cells to low capacity cells.
- Layer interworking (tighter coupling between the application layer and the RAN).
- Support different front-haul splits as they evolve.
- Technology gains such as Spectral efficiency.

Virtualized Platform enables a variety of applications and use cases

FlexRAN (Intel vRAN Reference Implementation) Overview

FlexRAN is a 4G/5G reference implementation from Intel that is available today for active customer engagements under a free Intel software license agreement.

What is FlexRAN

- Software Reference Implementation of BBU software (L1 – L3).
- Targeting 4G and 5G (NR) networks.
- Runs on Centralized or Distributed Intel Silicon Platforms.
- Intel Provides L1. Eco system partners provide L2 & L3.

FlexRAN Objective

- Demonstrate Baseband functionality on Intel Silicon.
- Help eco system optimize L1 on Intel Silicon.
- Support the eco-system in accelerating the development of commercial solutions.

Engagement Model

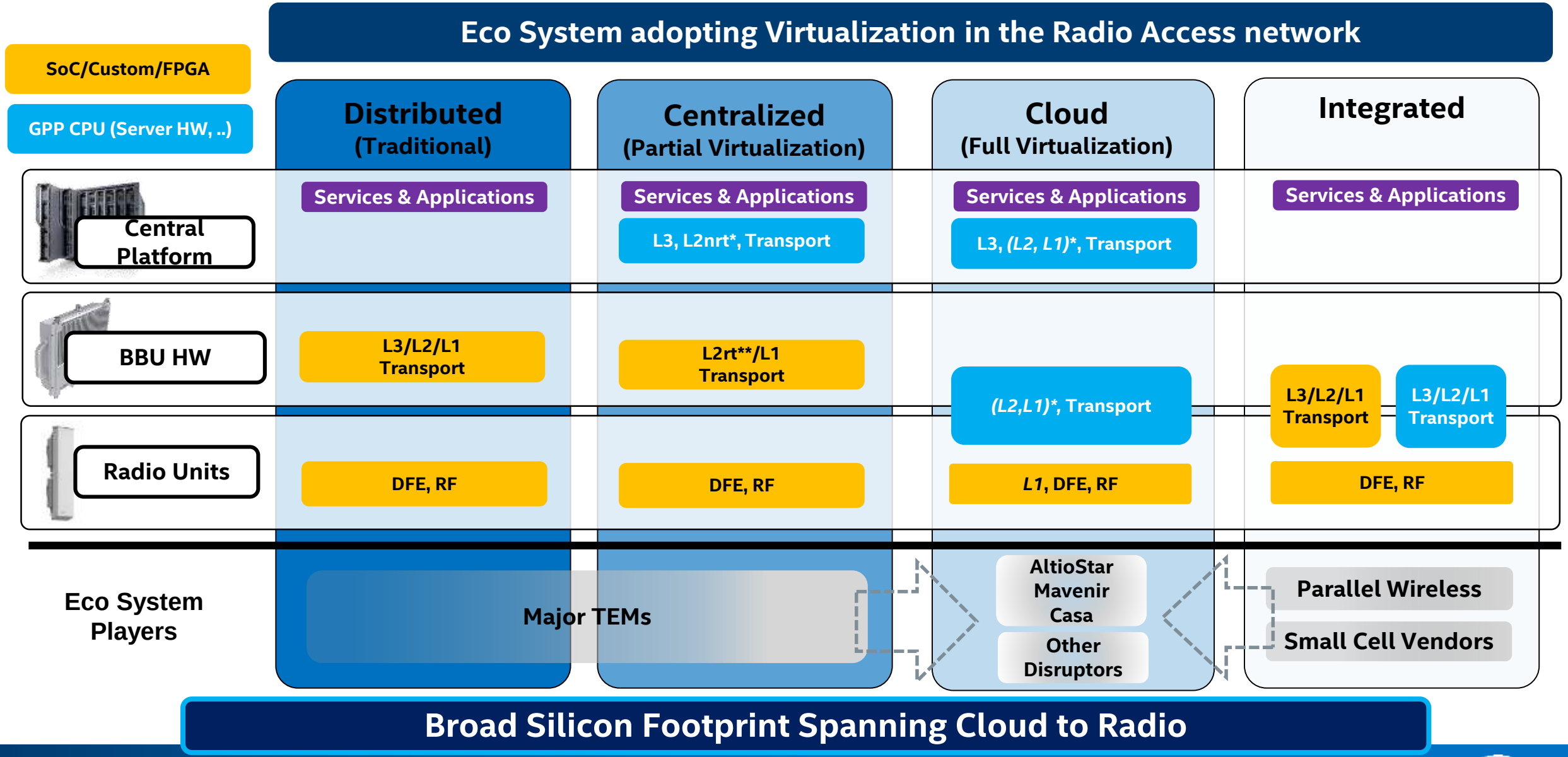
- Intel licenses the FlexRAN L1.
- Only allowed to run it on Intel silicon.
- Customer use it as an SDK or integrate modules into their code.

FlexRAN Segments

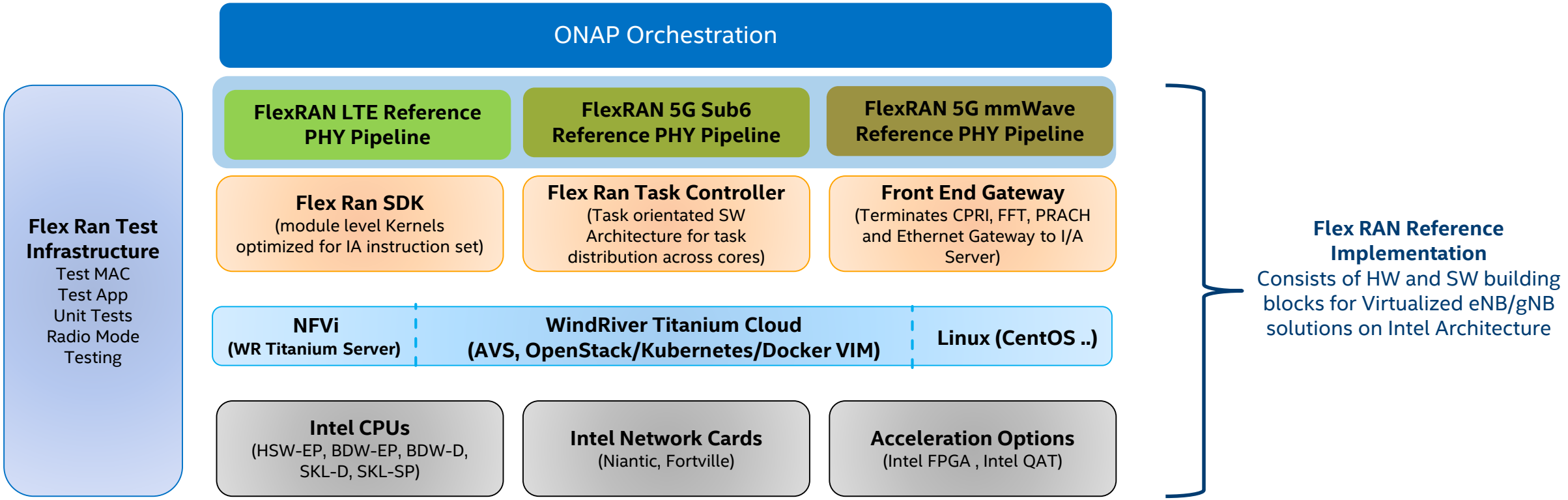
- Outdoor and Indoor (Rural, Urban, Enterprises, Venues, Stadiums, Malls, Public Spaces etc.)
- Scales from single carrier to multiple carriers
- Centralized, Distributed and Integrated network architectures

Simple & Cost Effective Approach To Deploy RAN On General Purpose Processing

Diverse 5G RAN Deployment Options



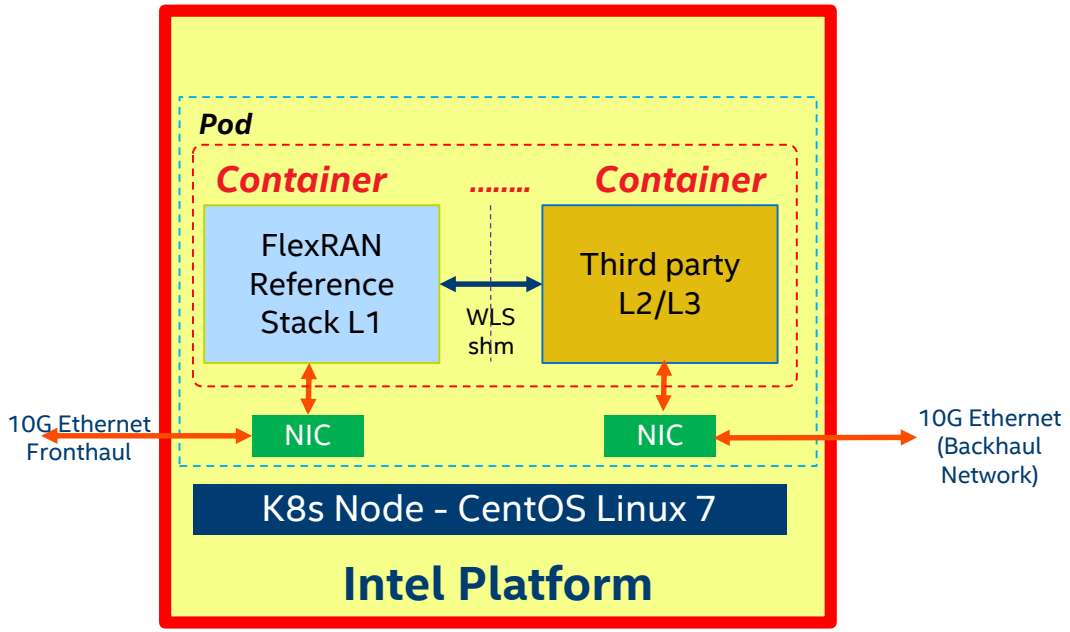
FlexRAN Reference Implementation Overview



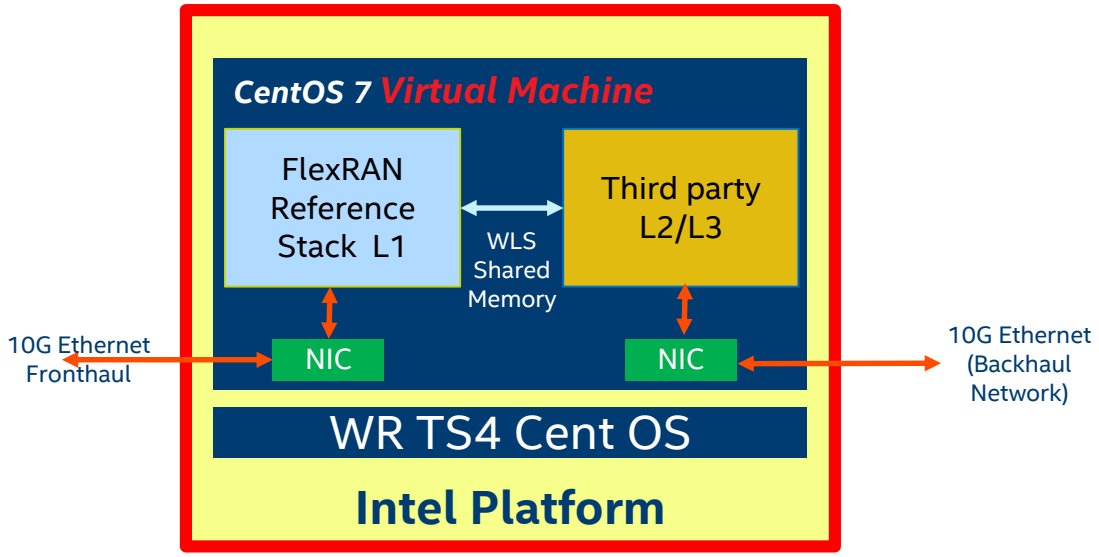
Release Cadence : Per Quarter to eco-system partners

FlexRAN now supports VM Cloud and Container Cloud

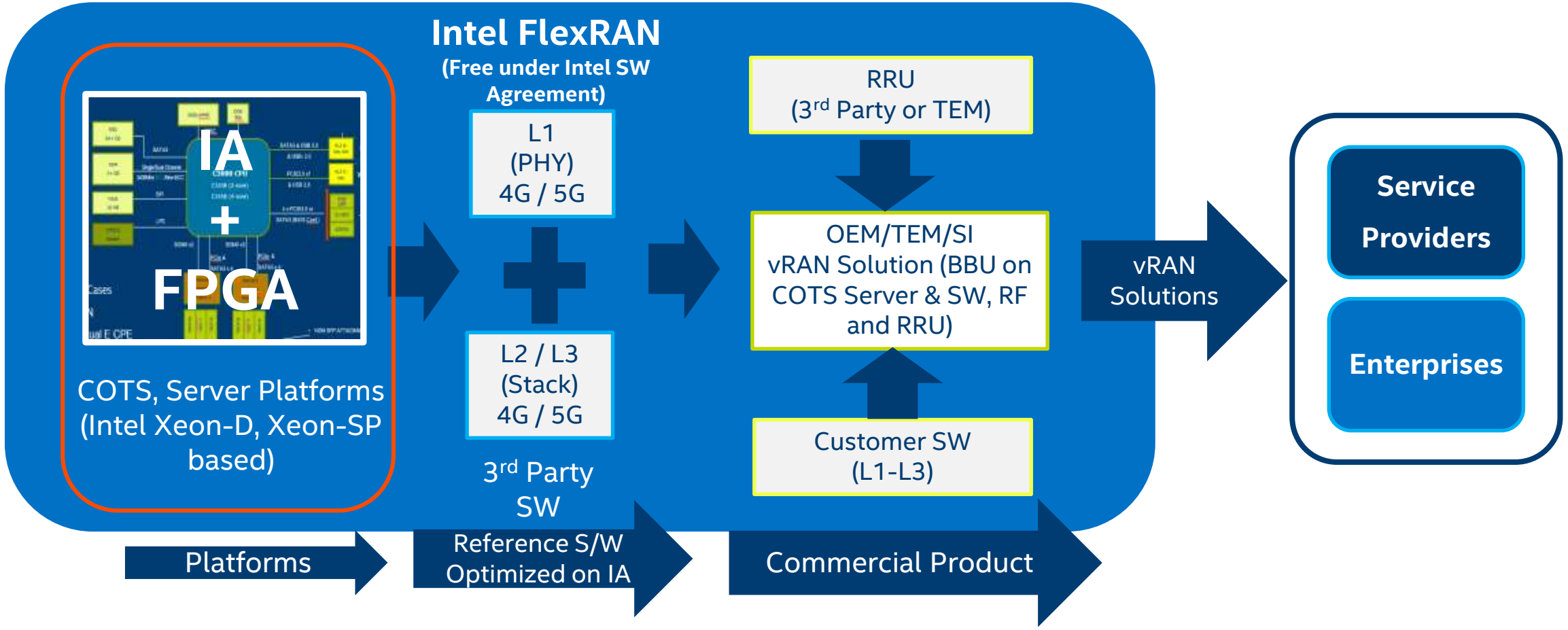
Kubernetes/Docker Container Deployment



Openstack/VM Deployment



Ecosystem Enabling Model based on FlexRAN



Intel working closely with eco-system to accelerate the development of VRAN solutions

FlexRAN Solution Ingredients

L2-L3 Commercial Software (Vendors)

L1 Reference Software
(4G initially, with roadmap to 5G)

CentOS **Virtualization** WIND

Platform (IA + FPGA)
Xeon-D: Broadwell-DE to Skylake-D & next gen;
Atom: Denverton-NS & next gen
Intel FPGA: Arria10 to Stratix10 & next gen

Ecosystem

4G LTE + 4G Scale out and 5G:
Intel working with Eco system partners (e.g. TIP, xRAN) to enable vendors and solutions providers with FlexRAN Software.

Some ecosystem vendors include:
Altiostar, Mavenir, ASTRI and Parallel Wireless.

RRU vendors such as CommScope etc.

3GPP A GLOBAL INITIATIVE

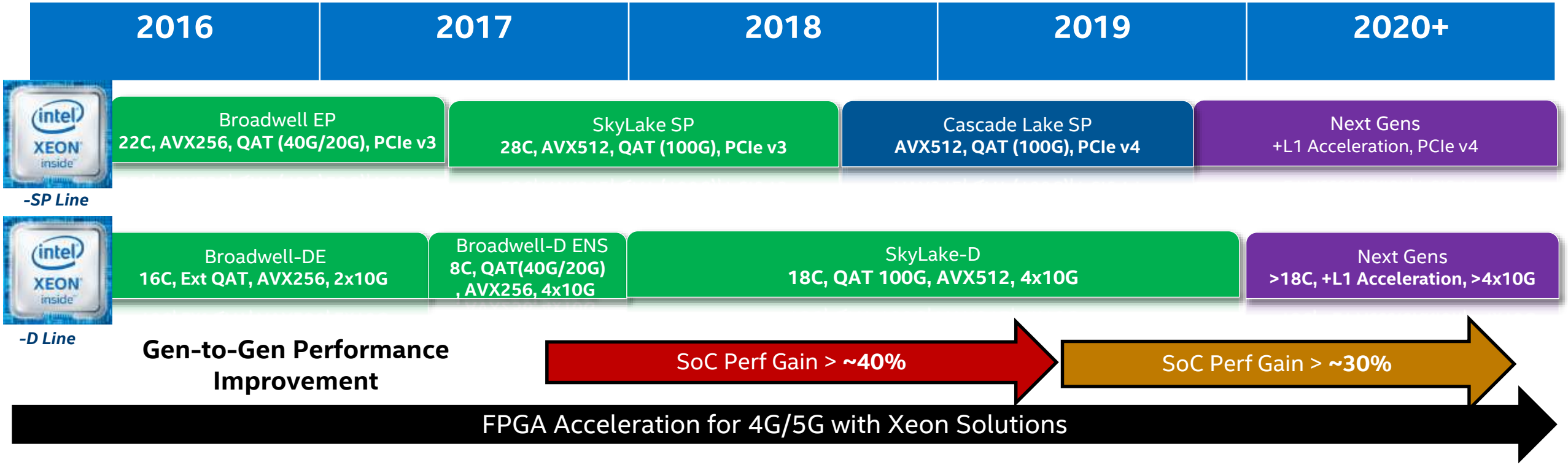
xRAN.org

TELECOM INFRA PROJECT

openRAN
https://telecominfraproject.com/project/access-projects/openran/

FLEXRAN CPU AND SOFTWARE ROADMAP

Intel Network Infrastructure CPU Roadmap



2016-2017

- Develop *LTE vRAN* L1-L3 on x86.
- Take Advantage of Accelerators and Instruction Sets
- FPGA for L1 Acceleration and RRU

2018-2019

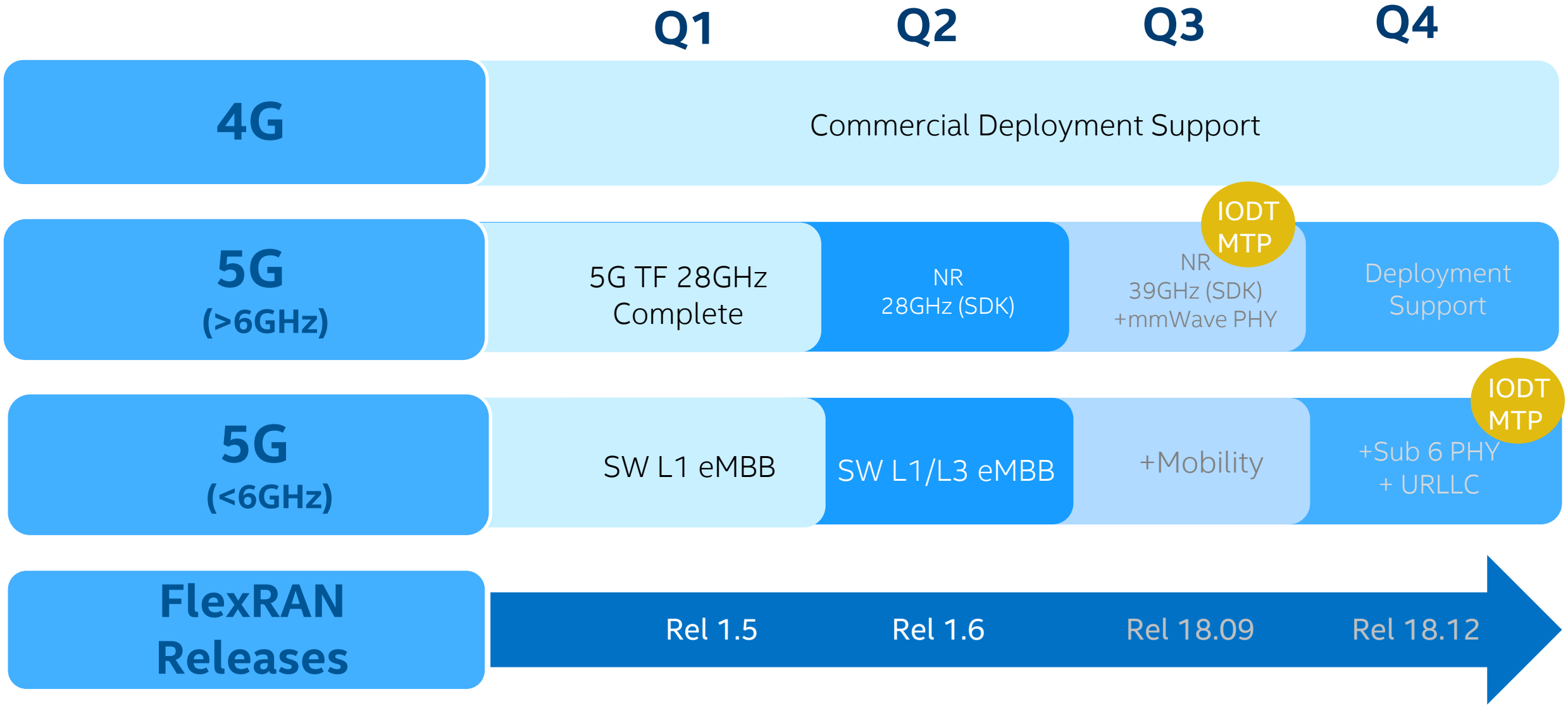
- Develop *5G vRAN* L1-L3 on x86.
- Take Advantage of Accelerators and Instruction Sets Enhancements
- FPGA for L1 Acceleration and RRU

2020+

- Optimize Code with new Accelerators

*All features are subject to change without notice

2018 FlexRAN Roadmap*

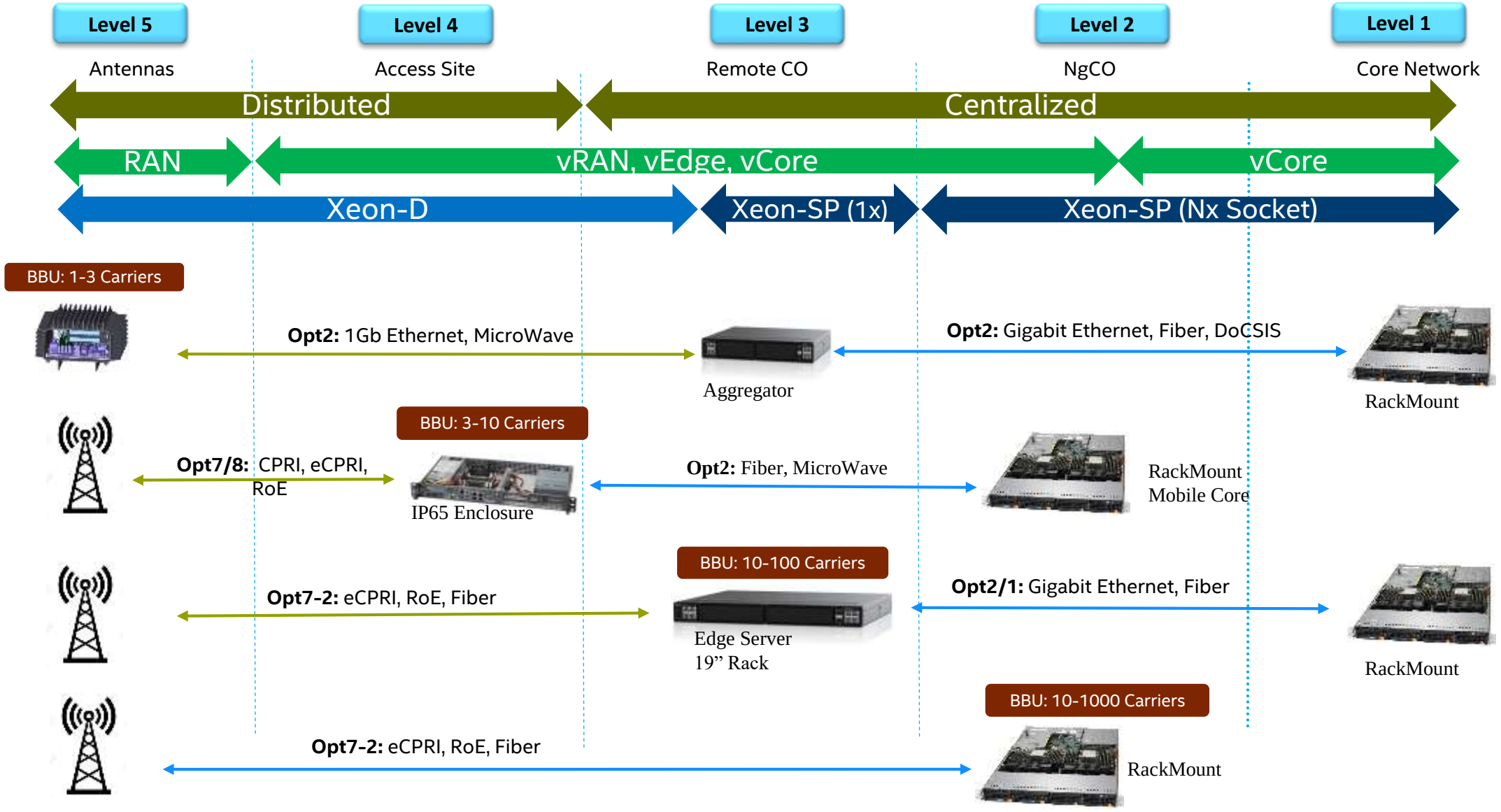


*Schedules are subject to change.

Updated: 6/18

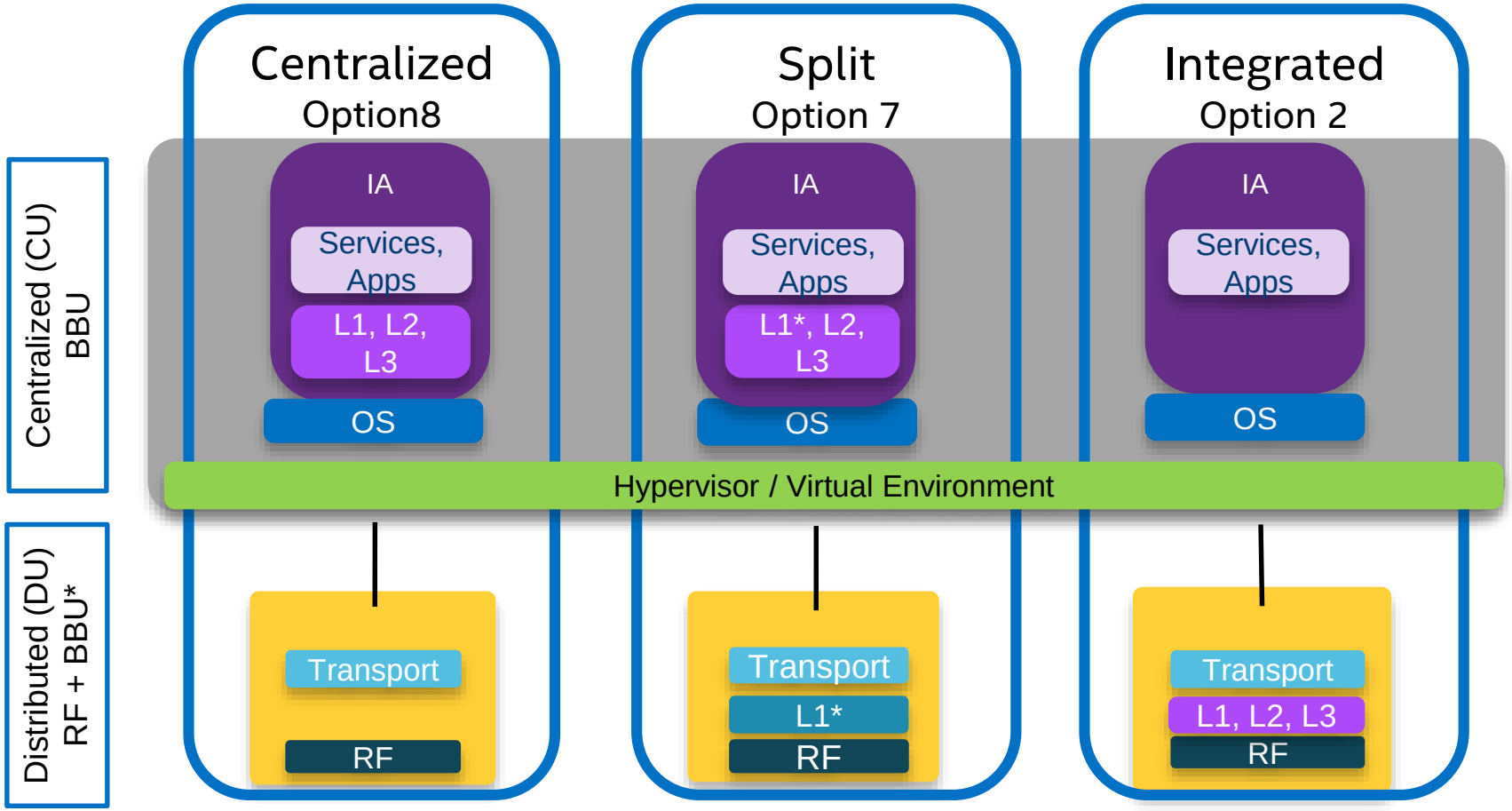
INTEL SYSTEM IMPLEMENTATIONS

RAN DEPLOYMENT MODELS → DIVERSE NETWORK ARCHITECTURES



RAN Deployment Options 4G/5G Architectures (Enabled with FlexRAN)

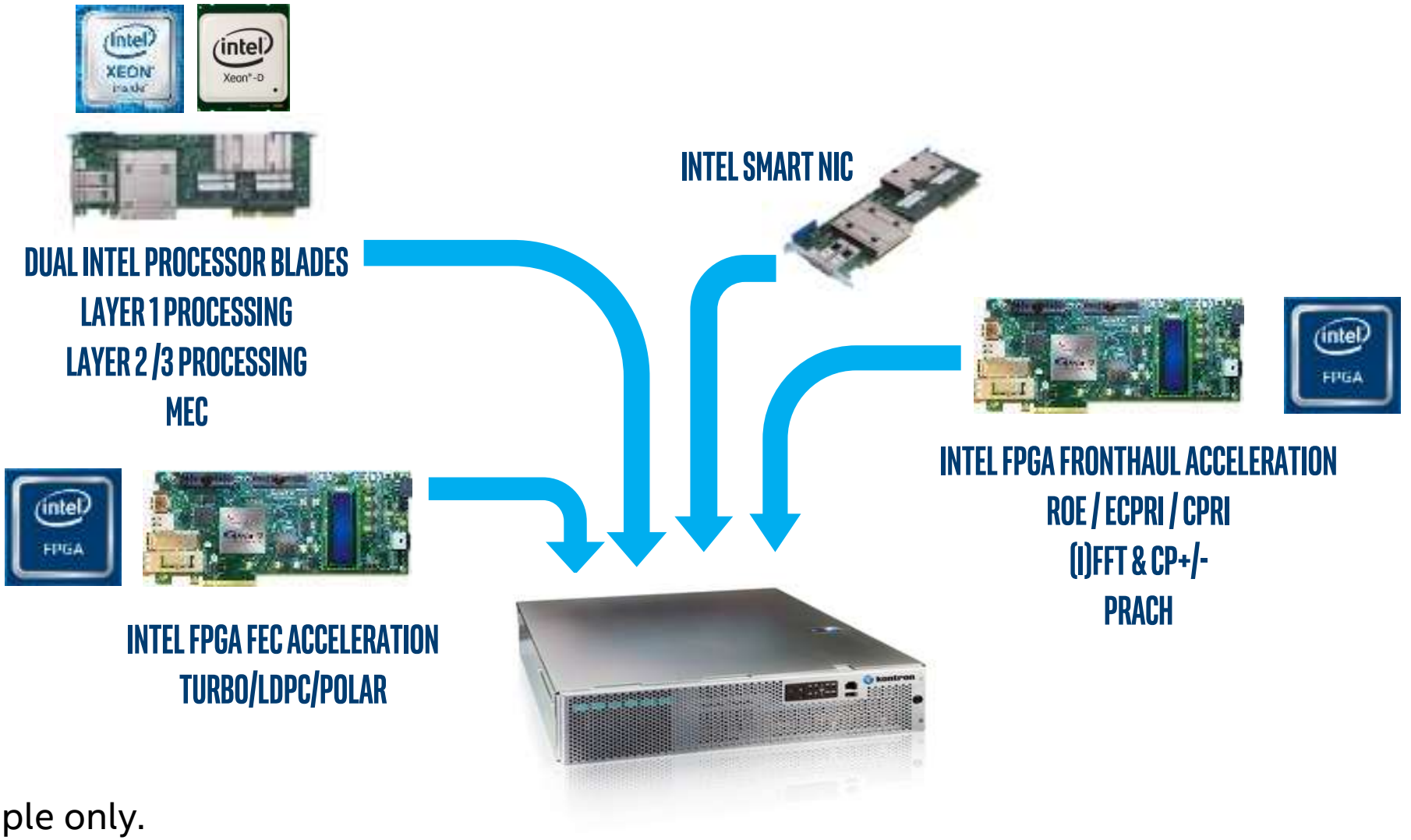
Uniform Software Architecture supporting different deployment models from Macro to Small Cells



Intel Building blocks for RAN

* Relevant BBU Processing for the split

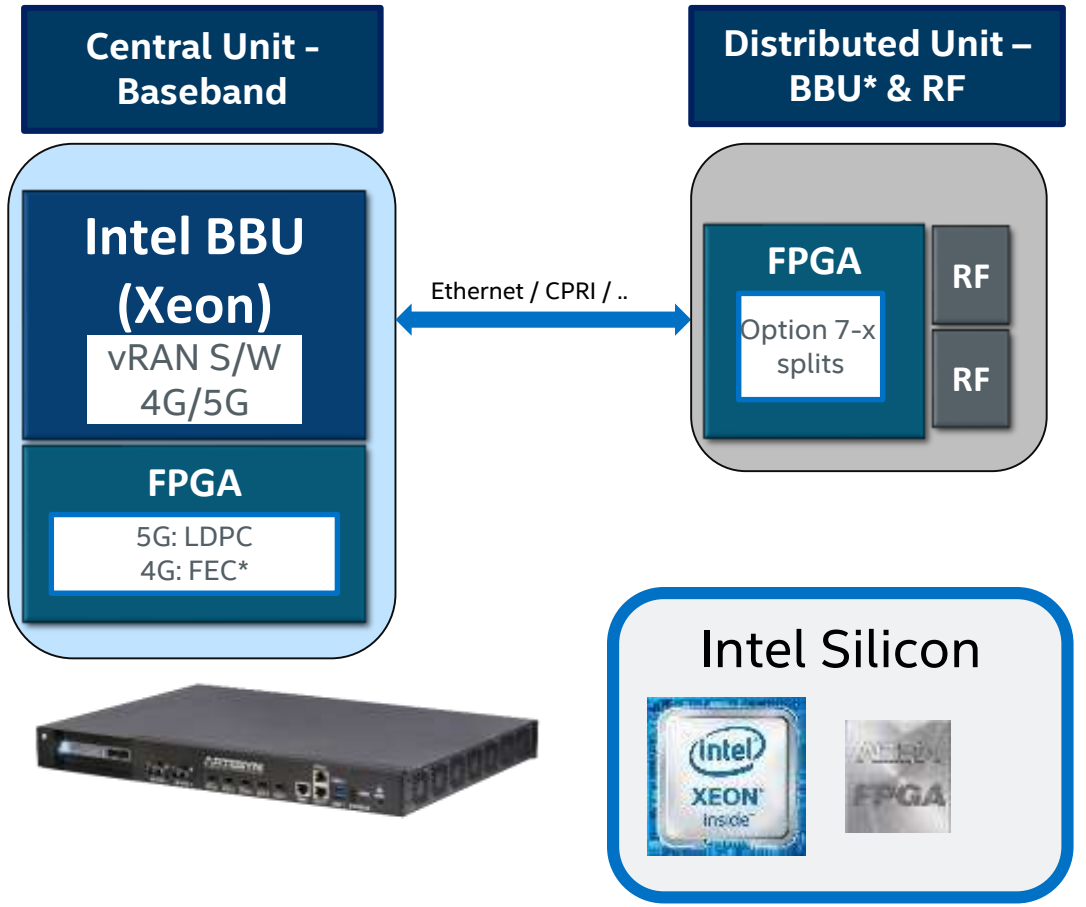
FlexRAN Hardware
(COTS Implementation – Example)



*HW shown are example only.

FlexRAN – Split Layer Processing

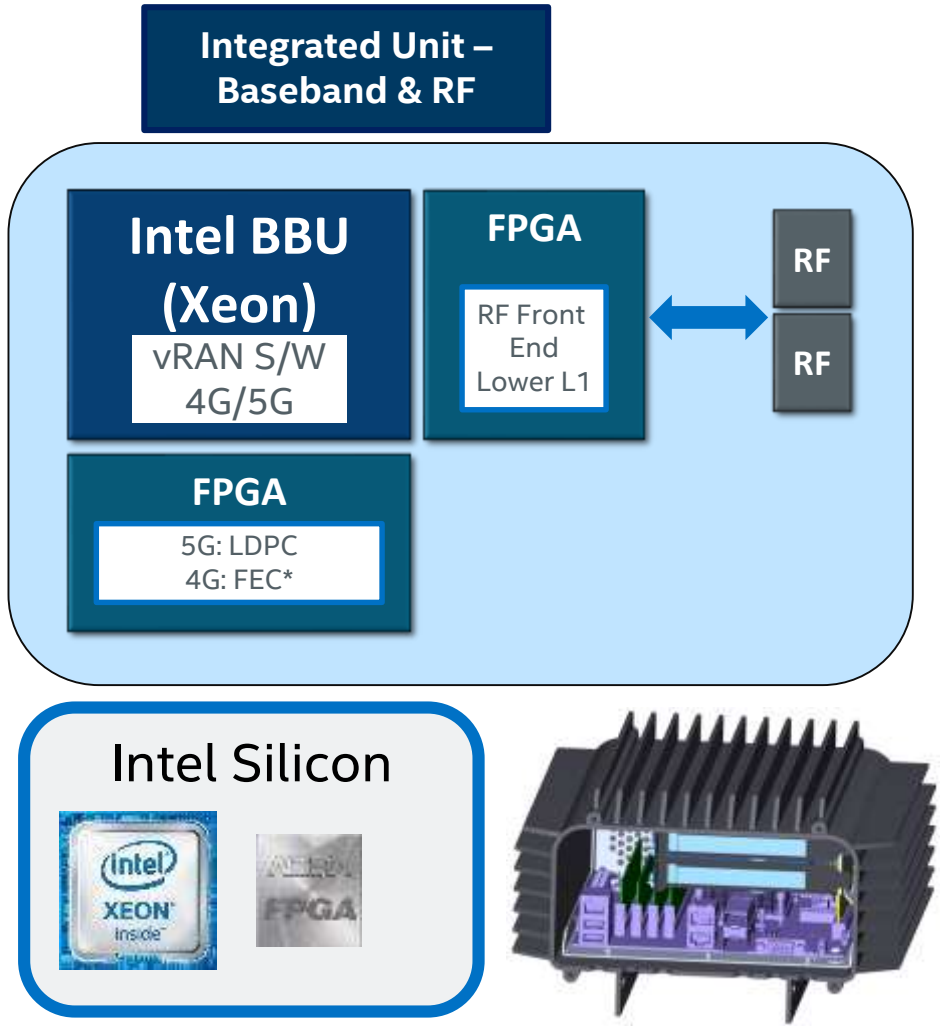
- **Target segments: Enterprise, Venues, and Outdoor**
- Solution:
  - Central BBU located in the cloud or IT closet or venue infrastructure.
  - Radio units distributed within the Enterprise, Venue or Outdoor location
- Scalable Small cell solution – add more capacity with more CPU Processors and RRUs



* Relevant BBU Processing for the split

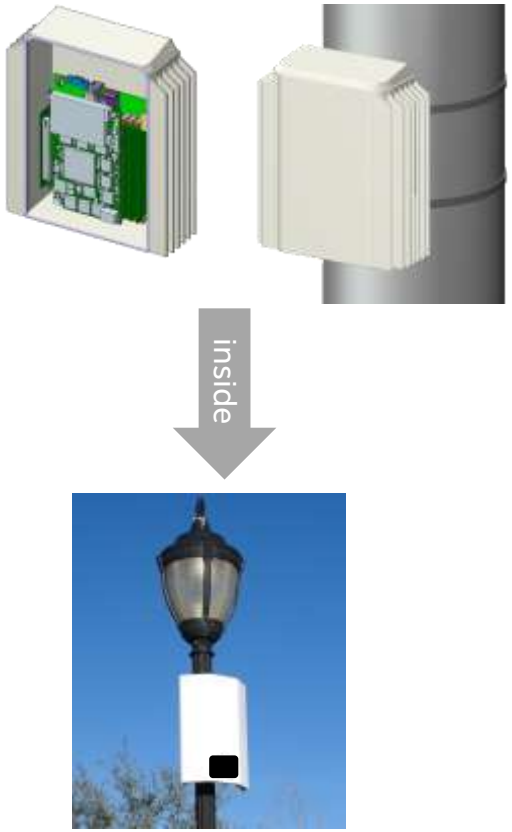
FlexRAN – Integrated Solution

- **Target segments: Rural, Venues, and Outdoor**
- Solution:
  - BBU and Radio in one box
- High capacity standalone small cell Solution

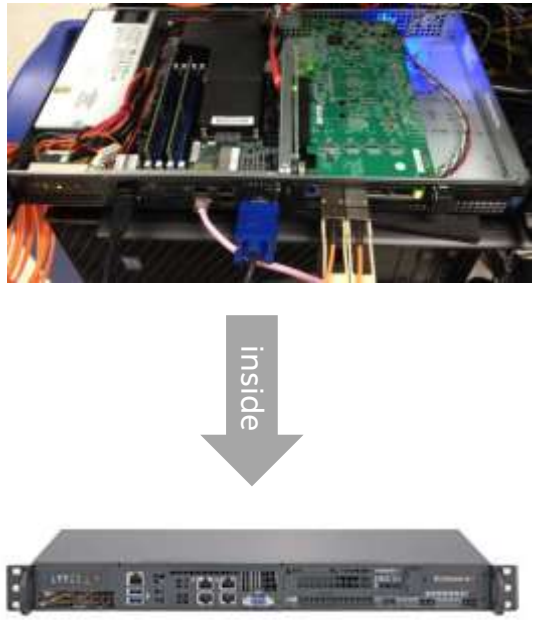


FLEXRAN SITE IMPLEMENTATION EXAMPLES

5G FlexRAN Site Implementation Examples



Compact Form Factor (Pole mountable)



1U Single CPU Socket Based

Bladed Form Factor

1U/2U Dual socket CPU Based

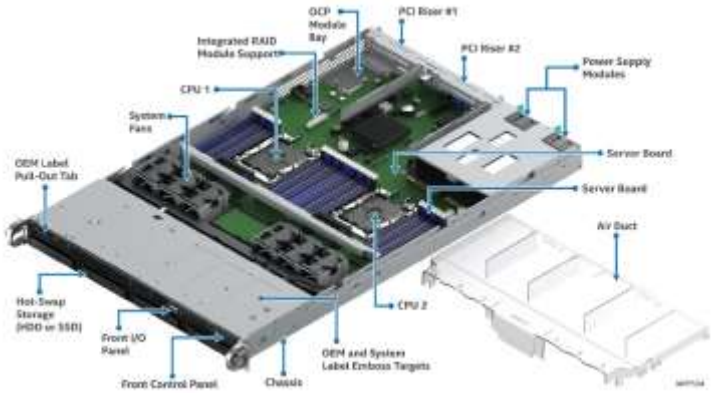
5G FlexRAN supports Scalable Platform Design based on the deployment configuration required

Next Gen Central Office Example

- Physical Characteristics
  - Data-Center environment
  - 19-inch full height, half height racks
  - Accessible from Front & Rear
  - Air Conditioned (Alarmed)
  - High Availability Environment
  - AC Power to Rack (30KW /Rack)
  - Manned 24/7
- Workloads
  - Core (EPC, BNG, CDN, MEC)
  - RAN - L2/L3 (3GPP Split-2)
  - RAN L1u –assuming fiber to Access site

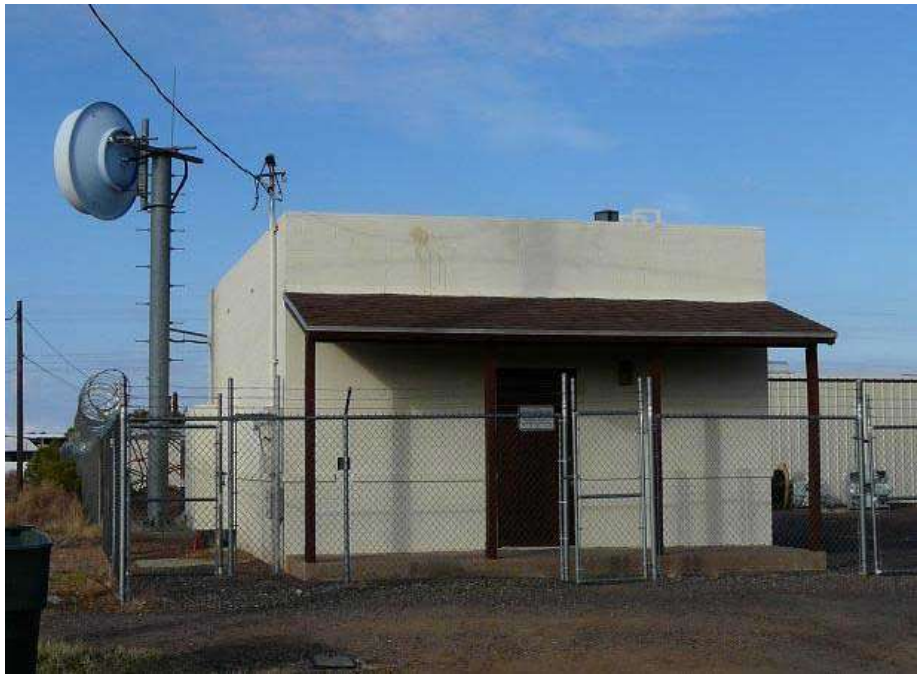
Equipment Characteristics

- 1U/2U COTS Rackmount Servers
- 10 – 40deg C - air inlet
- Redundant AC power



Aggregated Access Example

- Physical Characteristics
  - Telco-CO environment
  - 19-inch racks, <600mm depth
  - Accessible from Front only.
  - Air Conditioned (Alarmed)
  - High Availability Environment
  - DC Power (-48Vdc or 12Vdc) (5 – 8KW per Rack)
  - Un-Manned
- Front-Haul – Fiber
- Backhaul - Fiber
- Workloads
  - vRAN - L1u, L2/L3 (3GPP Split-2)
  - MEC
  - vBNG, DSL etc.



Equipment Characteristics

- 19" Telco Rack
- 0 – 70deg C - air inlet
- DC Power

Access Site Example

- Physical Characteristics
  - Varied environments
  - IP65 rated enclosures, ~350mm depth
  - AC Power (-48Vdc or 12Vdc) (5 – 8KW per Rack)
  - Un-Manned
- Fronthaul:- Fiber, Copper
- Backhaul:- Fiber, Copper Microwave
- Workloads
  - RAN - L1/L2/L3
  - RAN - L1/L2 (3GPP Split-2)
  - MEC

Equipment Characteristics

- IP65 rated.
- Extended Temp rated
- Non redundant
- 3 – 10 sector carriers

Pole-Mount Example

- Physical Characteristics
  - Varied environments
  - Custom Enclosures
  - Passive Cooling
  - DC Power (-48Vdc or 12Vdc)
- Fronthaul: Not Applicable
- Backhaul:- Fiber, Copper, Microwave
- Workloads
  - RAN - L1/L2/L3
  - RAN - L1/L2 (3GPP Split-2)
  - MEC

Equipment Characteristics

- IP65 rated.
- Extended Temp rated
- Custom Form Factor
- 1 – 3 sector carriers

FLEXRAN ECOSYSTEM ACTIVITES

Industry Momentum to enable vRAN

Intel is supporting extensive activities enabling ecosystem to innovate on vRAN

xRAN.org

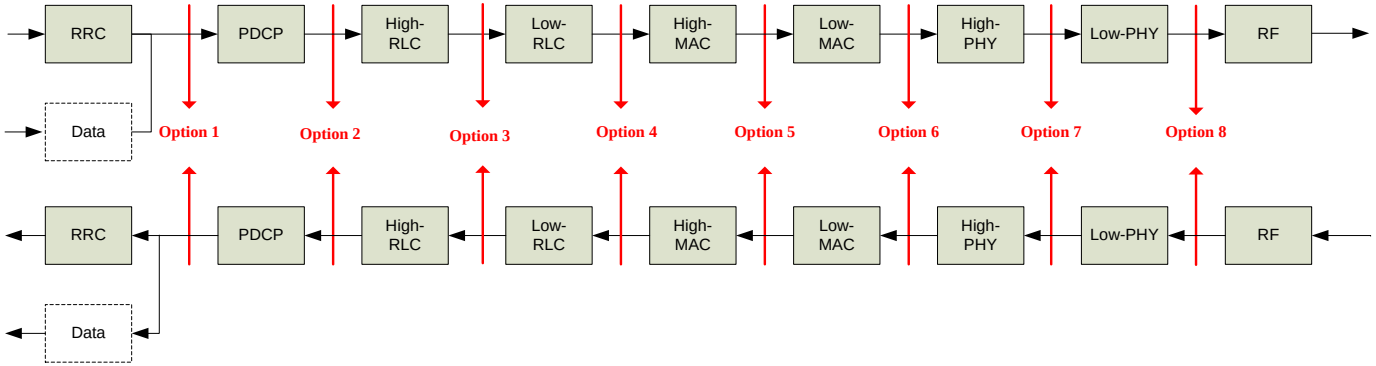
xRAN fundamentally advances the RAN architecture in three areas – decouples the RAN control plane from the user plane, builds a modular eNB software stack that operates on common-off-the-shelf (COTS) hardware and publishes open north and southbound interfaces to the industry.

TELECOM INFRA PROJECT

vRAN Fronthaul

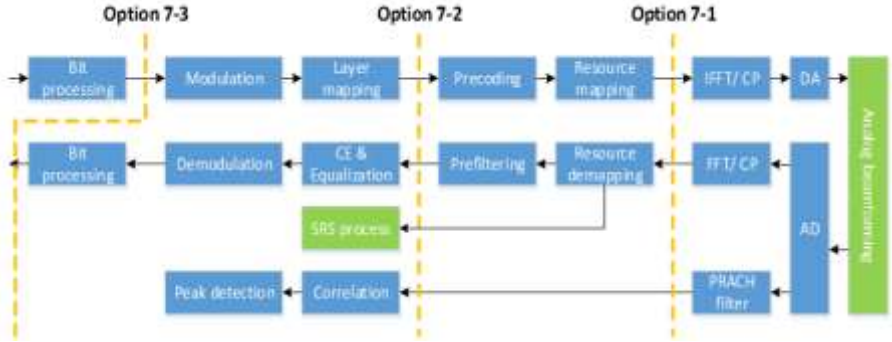
The group will focus on virtualization of the RAN for non-ideal backhaul, in particular maximizing the performance through optimization of physical layer, compression, and other methods.

3GPP A GLOBAL INITIATIVE



8 Split Options are under studied by 3GPP – option 2.

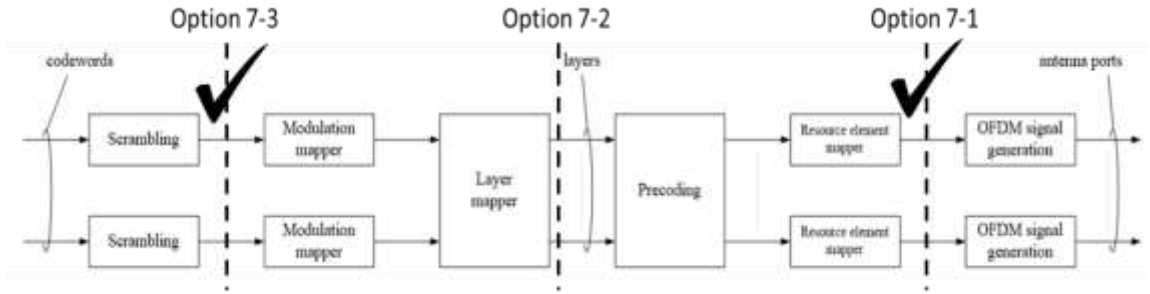
Industry looking at splits around option 7.x



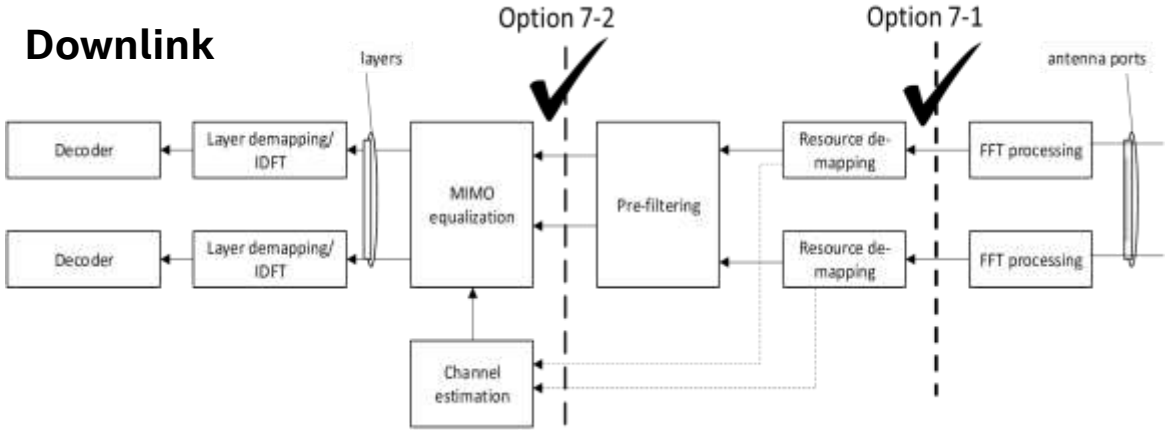
3GPP Physical Layer Split Options

Potential Split Architecture Options
(driven by xRAN - Under Consideration)

Uplink



Downlink



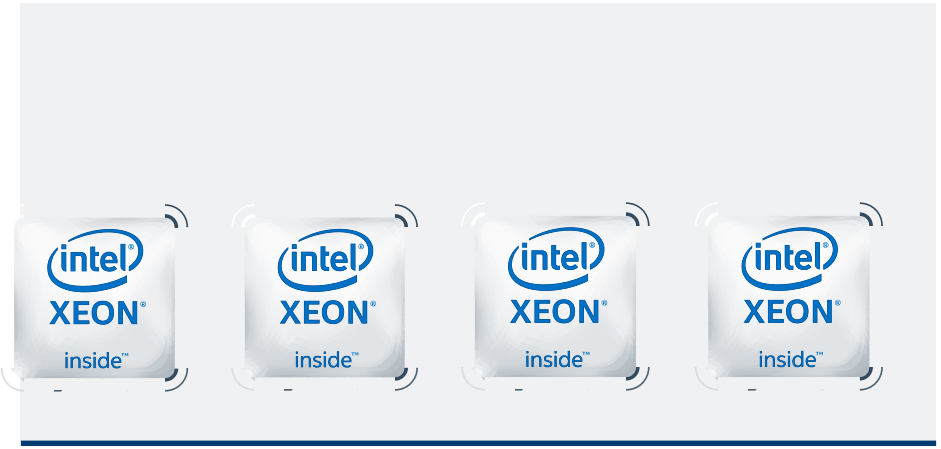
- **Option 8**, **Option 7-1** and **Option 7-2** are being considered as part of our initial development plan
- Intel plans to follow **xRAN** specification

INTEL CPU FEATURES

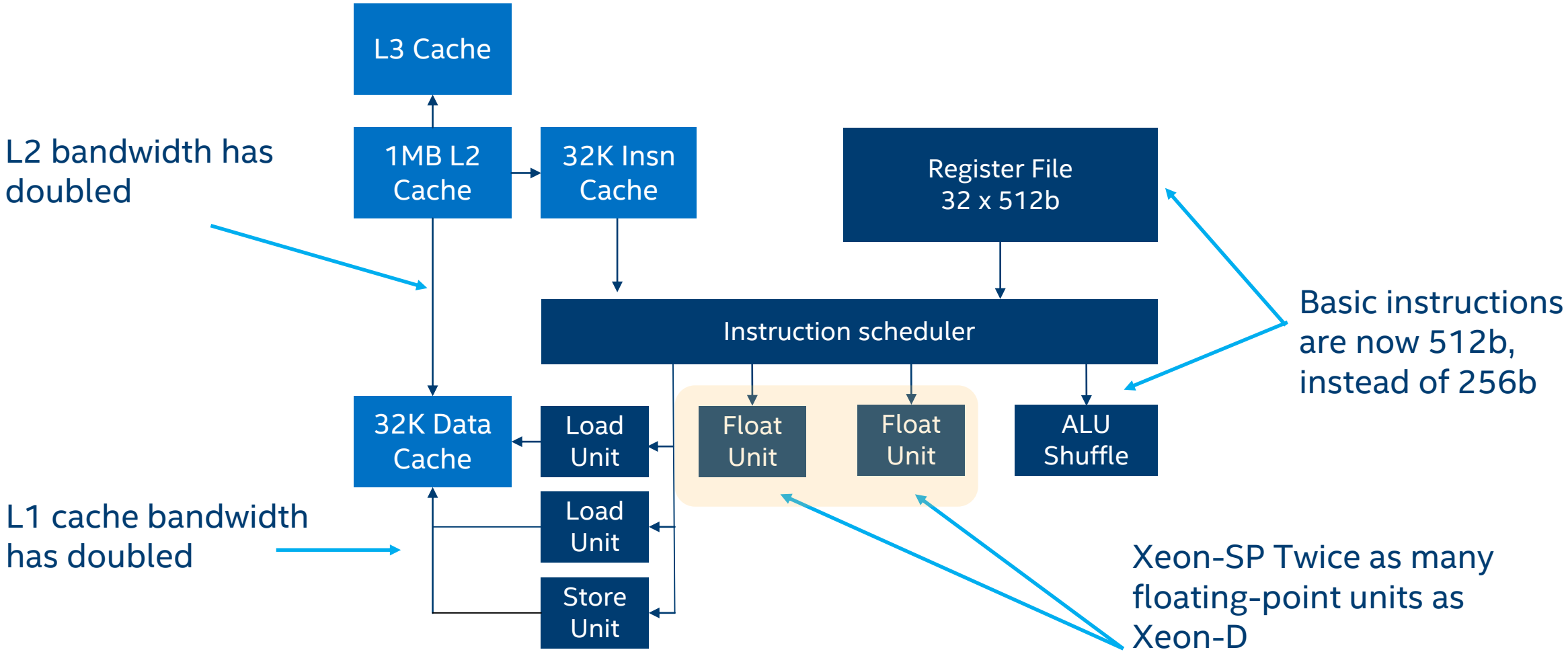
Intel® Xeon® Processors

The Xeon Scalable Processor has many improved features over the previous generation Xeon processors:

- Intel® AVX-512: A comprehensive extension to the existing vector instruction set.
- Improvements to the cache hierarchy.
- Improved microarchitecture to deliver more instructions per cycle.



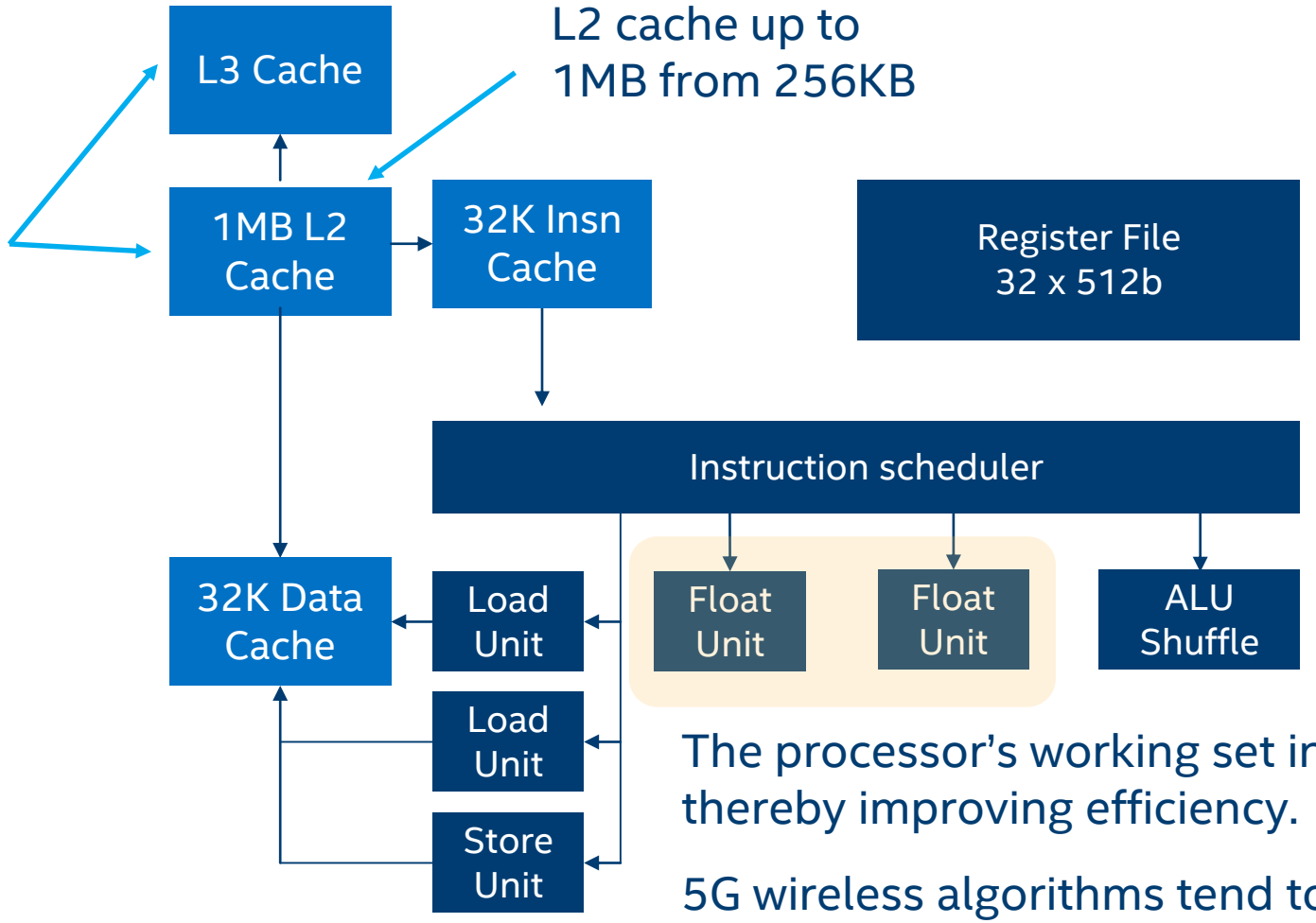
Compute: 2x Data Throughput compared to previous generation



https://www.intel.com/content/www/us/en/architecture-and-technology/avx-512-overview.html

Data: 4x as Much Storage as previous generation

Non-inclusive caching improves the overall efficiency of the memory hierarchy (i.e., data is not replicated in different cache levels), and gives each core more storage.



The processor's working set increases in size, thereby improving efficiency.

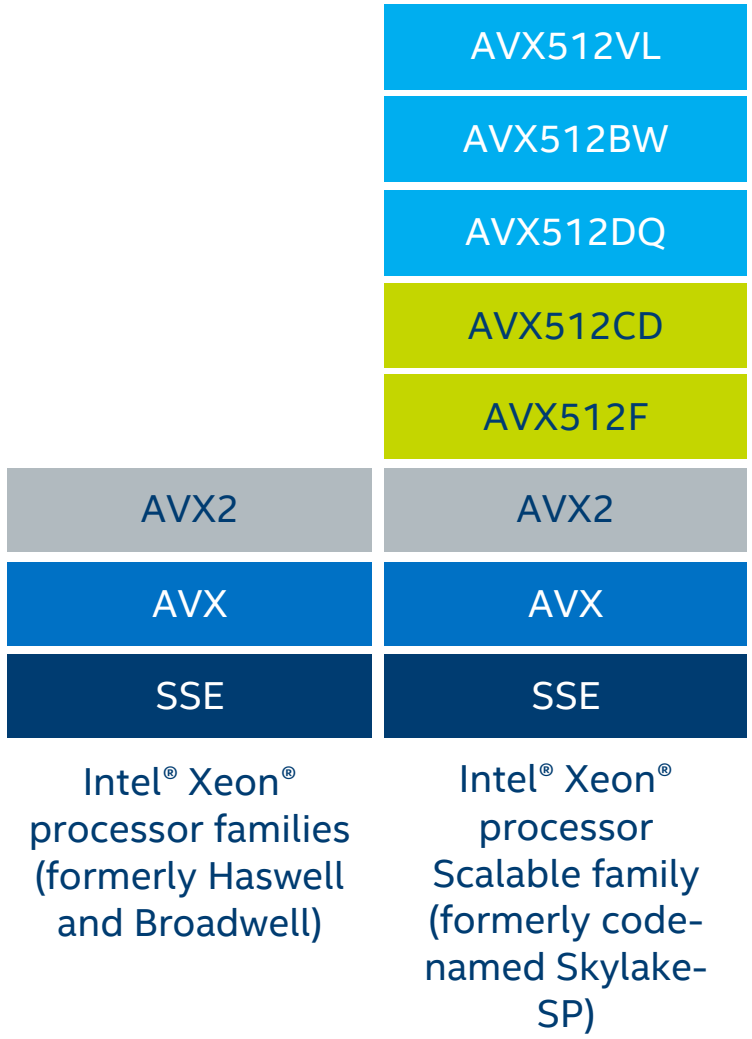
5G wireless algorithms tend to fit neatly into the new register sizes, making them more efficient.

New Instructions: Intel® AVX-512

Many new instructions, ranging from bit manipulation to sophisticated floating-point operations.

Instructions aren't just wider but do more too. What took several instructions in previous processors can now be done in one instruction.

In combination the compute efficiency has improved. There is 2x as much compute resource, and more than 2x as much processing can be done.



https://www.intel.com/content/www/us/en/architecture-and-technology/avx-512-overview.html

Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

Intel® AVX2 (Broadwell-DE)	Intel® AVX-512 (Skylake-D)
• 32 SP/16 DP Flops/Cycle • Float16 • 2 256-bit FP FMAs (Fused Multiply-Add) • 256-bit integer • PERMD • Gather	• One 512-bit FMAs • 512-bit FP and Integer • 32 registers • 8 mask registers • 32 SP/16 DP Flops/Cycle (SKUs with 1 512-bit FMA) • Embedded rounding • Embedded broadcast • Scalar/SSE/AVX “promotions” • Native media additions • HPC additions • Transcendental support • Gather/Scatter

INTRODUCING THE NEW INTEL® XEON® D-2100 PROCESSOR

INTEL'S FASTEST LOW-POWER EDGE PROCESSOR

GROUNDBREAKING INTEL® MESH ARCHITECTURE

Innovative processor architecture enables performance and efficiency improvements

UP TO **2.9X** PERFORMANCE IMPROVEMENT VS. D-1500 NS[1] **NETWORK**

UP TO **2.8X** PERFORMANCE IMPROVEMENT VS. D-1500[2] **STORAGE**

UP TO **1.6X** PERFORMANCE IMPROVEMENT VS. D-1500[3] **COMPUTE**

INTEGRATED INTEL® **AVX-512 ACCELERATION**

UP TO **3.0** GHZ WITH INTEL® **TURBO** BOOST TECHNOLOGY 2.0

UP TO **512 GB** DDR4 ECC **2666** MHZ

INTEGRATED **INTEL® QUICKASSIST TECHNOLOGY**

UP TO **100 GBPS** CRYPTOGRAPHY, DECRYPTION, AND ENCRYPTION ACCELERATION

&

INTEGRATED **INTEL® ETHERNET**

UP TO **4 X 10 GBE**

OPTIMIZED SYSTEM-ON-A-CHIP (SOC) FOR FLEXIBLE, SCALABLE, HIGH-DENSITY NETWORK, STORAGE AND CLOUD EDGE SOLUTIONS

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Benchmark results were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

INTEL® XEON® D2100 PROCESSOR FOR CUSTOMER PREMISE EQUIPMENT (CPE)

INTEL® XEON® D-2100 PROCESSOR: NEXT-GEN CPE

4X More Memory Capacity	More Application Scale
Enhanced Intel® QuickAssist Technology	2.5X Faster Crypto Processing[6]
Enhanced I/O, PCIe*, MISO, Intel® Ethernet	Implementation Flexibility
1.125X More Processing Cores	More Virtualized Network Functions[5]

ENHANCED CAPABILTIES AND CAPACITY WITH LOWER TCO FOR SPACE-CONSTRAINED CPE SOLUTIONS

UP TO 2.9X
NETWORK PERFORMANCE IMPROVEMENT
COMPARED WITH INTEL® XEON® D-1500 PROCESSOR NETWORK SERIES[1]

New Intel® Xeon® D-2100 Processor
Intel's Fastest Low-Power Edge Processor

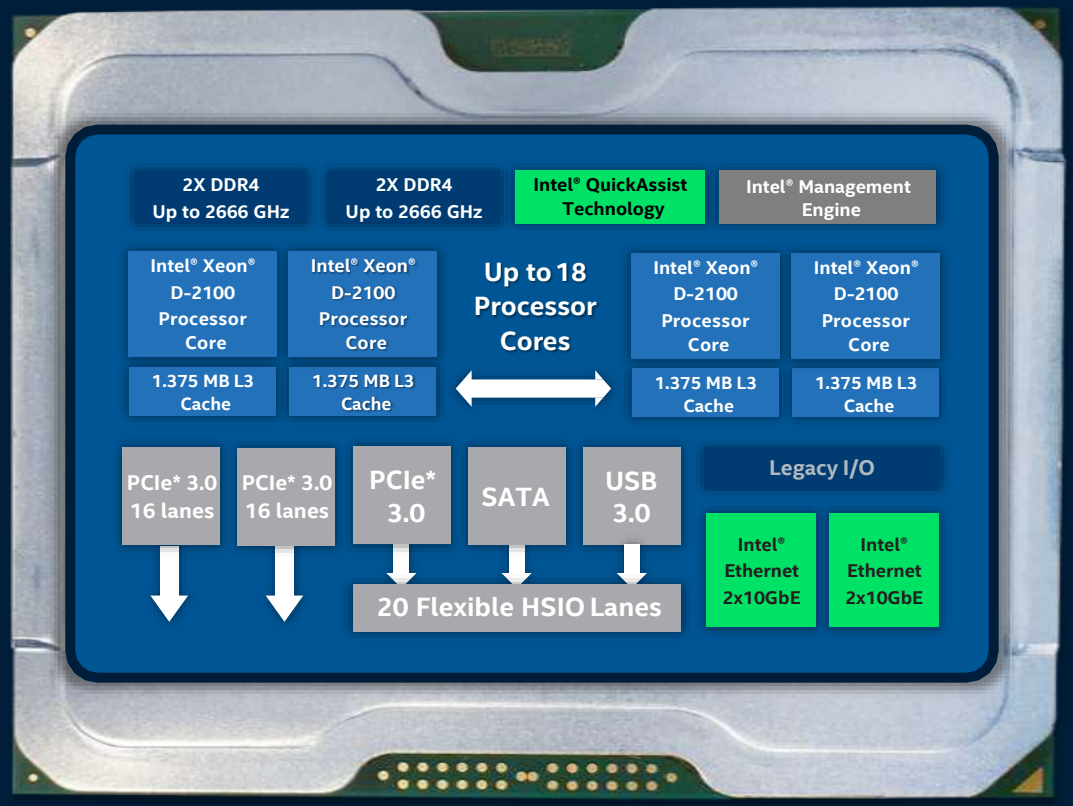
For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Benchmark results were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

NEW INTEL® XEON® D-2100 PROCESSOR

ADVANCED INTELLIGENCE FOR HIGH-DENSITY EDGE SOLUTIONS

Intel® Xeon® D-2100 Processor
(System On A Chip - SoC)

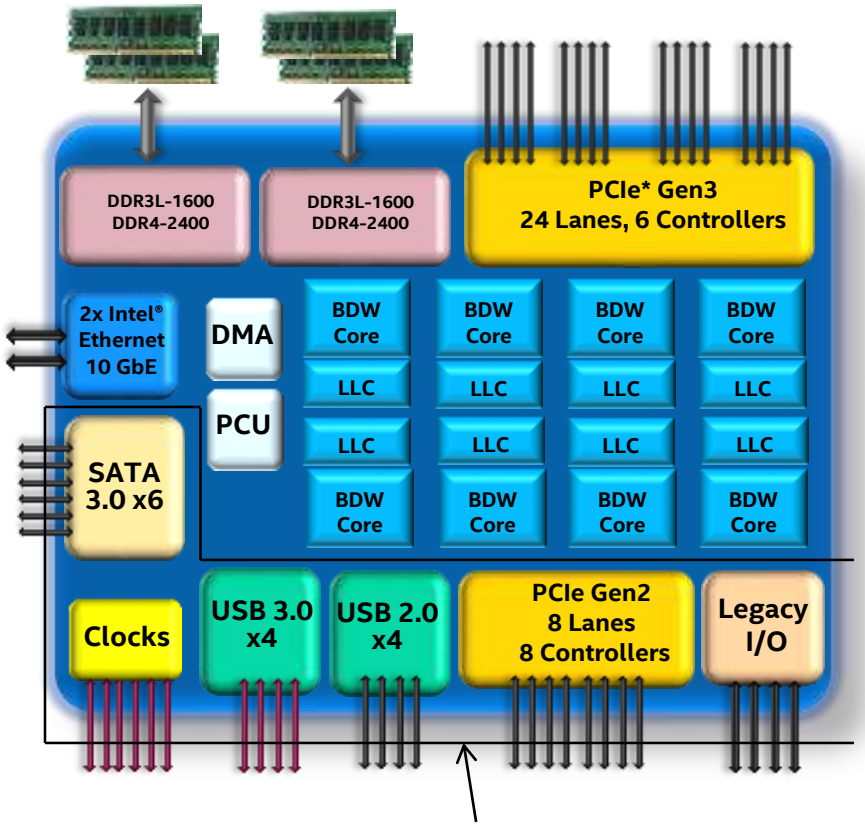


Picture and diagrams are provided for illustration purposes only.
Diagrams (above) and table (right) are not a comprehensive list of product features or capabilities.
Please visit www.intel.com/xeond for the latest product information.

Processor Manufacturing Process	Intel's optimized 14nm process technology featuring Intel® Mesh Architecture
Maximum Core Count Supported	Up to 18
Maximum Base Frequency Supported	Up to 2.3 GHz
Maximum Intel® Turbo Boost Technology 2.0 Frequency Supported (Single Core)	Up to 3.0 GHz
Processor Cache Memory Support	L3 is 1.375 MB/Core, up-to 24.75 MB featuring rebalanced Intel® Cache hierarchy
Processor Performance Support	Intel® Turbo Boost 2.0 Technology, Intel® Hyper-Threading Technology (Intel® HT), Intel® Speed Shift Technology
Intel® Advanced Vector Extension 512 (Intel® AVX-512) Support	Intel® AVX-512 with up to 1 FMA support
Intel® QuickAssist Technology Support	Available integrated with up to 100 Gbps of crypto, decrypt and encrypt accelerated throughput
Thermal Design Point (TDP) Range	Approximately 60 to 110 Watts
Socket Type and Size	Socket FCBGA 45 mm x 52.5 mm
System Memory Support	Up to 64 GB per DIMM. Up to 4 channels of DDR4 2666 MHz, 2 DPC. RDIMM and LRDIMM with ECC support.
Maximum System Memory Supported	Up to 512GB
PCI Express* Gen 3 Support	Up to 32 lanes
Flexible High-Speed I/O (HSIO)	PCI Express* 3.0 – Up to 20 lanes SATA* 3.0 – Up to 14 lanes USB* 3.0 – Up to 4 ports
Legacy I/O Support	Enhanced Serial Peripheral Interface (eSPI), Low Pin Count Interface (LPC) and System Management Bus (SMBus*)
Intel® Management Engine (Intel® ME)	Intel® ME 11.11
Intel® Ethernet Support	Available integrated with up to four, 10 GbE adapters with Accelerated Remote Direct Memory Access (RDMA) and native Software Fault Isolation (SFI). Supported via direct and dedicated PCIe* Gen 3 connection to the CPU.

Intel® Xeon® Processor D SoC Architecture Overview

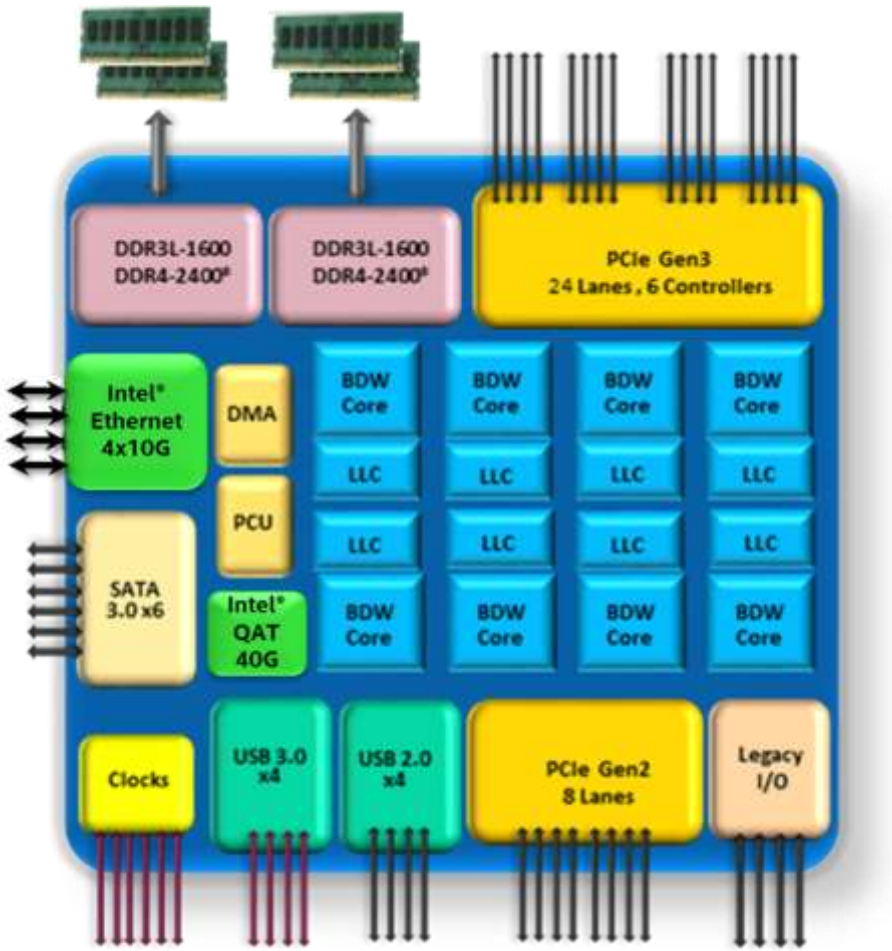
CPU	2-16 Core Intel® Xeon® Processors (14nm)
L1 Cache	32K data, 32k instruction per core
L2 Cache	256K per core
LLC Cache	1.5 Mb (12-way associative) per Cbo (core slice)
Frequency	TBD – will vary with SKU
Addressing	46 bits physical / 48 bits virtual
Memory	DDR4 up to 2133 MT/s DDR3L up to 1600 MT/s Two channels (2 DIMMs/channel)
DIMM Types	SODIMM, UDIMM, RDIMM with ECC and non-ECC
Memory RAS	Enhanced ECC single bit error correction – dual bit error detection (SEC-DED) covers address and data paths, DDR scrambler to reduce error rate.
PCIe*	x24 PCIe Gen3 with up to 6 controllers x8 PCIe Gen2 with up to 8 controllers
Integrated I/O	2x Intel® Ethernet 10 GbE, x4 USB 3.0, x4 USB 2.0, and x6 SATA 3
Technologies	Intel® VT-x2, Intel® VT-d, Core RAPL, PECI over SMBus
Package	FCBGA, Ball Pitch: 0.7 mm minimum (balls anywhere) Dimension: 37.5 mm x 37.5 mm
Legacy I/O	SPI for boot flash, SMBus, UART LPC, GPIO, 8259, I/O APIC, 8254 timer, RTC
Target Launch	Mid Q4 2015 (8C and Below); End Q4 2015 (Above 8C); Q1 2016 (eTemp)



All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Broadwell DE NS SoC Architecture Overview

CPU	2-8 Core Intel® Xeon™ (14nm) CPUs
L1 cache	32K data, 32k instruction per core
L2 cache	256K per core
LLC cache	1.5MB per core
Addressing	46 bits physical / 48 bits virtual
Memory	DDR4 up to 2400* MT/s DDR3L up to 1600 MT/s Two Channels (2 DIMMs/Channel)
Memory Capacity	RDIMM: 128 GB (32 GB/DIMM) UDIMM/SODIMM: 64 GB (16 GB/DIMM)
DIMM Types	SODIMM, UDIMM, RDIMM with ECC and non-ECC
Memory RAS	Enhanced ECC Single bit Error Correction – Dual bit Error Detection (SEC-DED) covers address and data paths, DDR scrambler to reduce error rate.
PCI-E*	x24 PCIe Gen3 with up to 6 controllers x8 PCIe Gen 2 with up to 8 controllers
Integrated IO	x4 Intel® Ethernet10GbE {10G-KR only}, x4 USB 3.0, x4 USB 2.0, and x6 SATA 3
Technologies	Intel® VT, Core RAPL, PECI over SMBUS, PSE
Crypto	Up to 40G bulk crypto @ 1K packet size + 40Kops PKE 2K
Compression	Up to 40G total compression or decompression
Power Management	FIVR, PCPS, EET, UFS Hardware PM
Legacy I/O	SPI for boot flash, SMBus, UART LPC, GPIO, 8259, I/O APIC, 8254 Timer, RTC



* DDR4-2400 is only available on select skus

REFERENCE MATERIAL

4G LTE vs 5G NR Spec

	LTE (4G)	5G NR
Max BW (per CC)	20 MHz	50 MHz (@15 KHz), 100 MHz (@30 KHz), 200 MHz (@ 60 KHz), 400 MHz (@120 KHz)
Max CC	5	16
Subcarrier Spacing	15 KHz	2n*15 KHz (TDD and FDD muxing)
Waveform	CP-OFDM (DL); SC-FDMA (UL)	CP-OFDM (DL); CP-OFDM and DFT-s-OFDM (UL)
No of Subcarriers	1200	3300
Frame Length (Air interface)	10 ms	1 ms
Symbol Length	7 symbols per 500 us	14 symbols (duration depends on sc spacing), 2,4,7 symbols per mini slot
Coding Scheme	Turbo (data); TBCC (ctrl)	LDPC (data); Polar (ctrl)
Initial Access	No analog beamforming; Digital beamforming (upto 8 layers)	Analog beamforming and Digital beamforming (upto 12 layers)

5G NR – Draft Spec – Layer 1

Parameter	Specification		Notes
	mmWave NR	Sub-6 GHz NR	
Bandwidth	N x 100 MHz N = up to 8 CC's	100 MHz	Nominal 100 MHz BW support
Duplex scheme	TDD	TDD	Focus on TDD in the initial phase followed by FDD
Subcarrier Spacing	120 KHz – initial priority	30 KHz – initial priority	Additional sub-carrier spacing will be addressed in later phase
FFT size	1K, 2K	1K, 2K, 4K	4K is priority for sub-6 GHz NR
Basic waveform design	DL: CP-OFDM UL: CP-OFDM	DL : CP-OFDM UL : CP-OFDM	Normal CP, DFT-s-OFDM in UL will be addressed in later phase
Slot Duration	0.125 msec	0.5 msec	Initial priority
Modulation (DL, UL)	Up to 64 QAM	Up to 256 QAM	MCS based on link adaptation
Channel Coding	Data Channel : LDPC Control Channel : Polar code		LDPC – being considered to be off-loaded to accelerator Polar – currently planned to be implemented in SW
MIMO	Hybrid BF Upto 4 virtual Antenna streams	32T32R or 64T64R Upto 8 virtual Antenna streams	Some parameters TBD and dependent on the radio
Spatial Multiplexing	4 layers (DL), 2 or 4 layers (UL)	4 or 8 layers (DL) 2 or 4 layers (UL)	Software to be scalable to address maximum but validation may be at a lower number of layers

- Initial phase of development focused on eMBB
- uRLLC to be addressed in later development phases around ~2H'18 once we have clarity on the 3GPP spec.
- FlexRAN NR platform will support LTE

Worldwide 5G Spectrum in Different Regions

	Frequency Spectrum	Europe	China	Japan	Korea	US
Sub-6GHz	**700MHz**	700 MHz	700Mhz (future)			600MHz
	3.5 GHz	3.4-3.8 GHz	3.3-3.6 GHz	3.6-4.2 GHz		CBRS 3.5GHz
	4.5GHz		4.4-4.5 GHz 4.8-5.0 Ghz	4.4-4.9 GHz		
mmWave	**26/28 GHz**	24-27.5 GHz		27.5-29.5 GHz	26.5-29.5 GHz	27.5-28.5GHz
	39 GHz		39 GHz			37.6-38.6 GHz 38.6-40GHz