FlexRAN 4G Reference Solution L1

User Guide Software Release v20.08

August 2020

Revision 4.0

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Document Number: 570228-4.0

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Revision Number	Description	Revision Date
4.0	Document Changes for FlexRAN software v20.08 release: Section 2.4 Step 4, DPDK patch number updated Section 3.2, Step 4 Note revised	August 2020
3.0	Document Changes for FlexRAN software v20.02 release: Updated DPDK version from v18.08 to v19.11 Section 2.4, Step 6 Updated compile option	April 2020
2.1	Document Changes for software v20.02 release: Added additional clarifying information to Section 3.2	January 2020
2.0	Document Changes for software v19.06 Release: Updated the DPDK Configuration instructions in Section 2.4	July 2019
1.9	Document Changes for FlexRAN 4G v1.69.12 Release: Updated build instructions in Section 3.2.1.1 (Layer One) Application	December 2018
1.8	Document Changes for FlexRAN 4G v1.68.09 Release: Updated build instructions in Section 3.2.1.1 (Layer One) Application Updated instructions in Section 3.4, Test and Debug Applications	October 2018
1.7	Document Changes for FlexRAN v1.6.0 Release: Removed Software Configuration section (was v2.2) Removed recommended kernel command line argument for Host Removed recommended kernel command line argument for Guest	June 2018
1.6	Document changes for v1.5.0 release: Updated Section 3.4, Intel DPDK Configuration Updated Section 3.7, nFAPI Application and configuration Updated Section 3.2, L1 Application	April 2018
1.5	Document was updated with changes for 1.4.1 release.	February 2018
1.4	Document was updated with changes for 1.4.0 release.	January 2018
1.3	Document was updated with changes for 1.3.0 release.	September 2017
1.2	Document was updated with changes for 1.2.0 release.	June 2017
1.1	Supports Release 1.1.2.	June 2017
1.0	Initial release of the document reflecting FlexRAN v1.1.0. TDD and TDD CA support was added.	April 2017
0.4	Document was updated per version-0.5.1 OOC release changes	February 2017

Revision Number	Description	Revision Date
0.3	Document was updated with phase 2 scenarios and changes	December 2016
0.2	TM500* script and VM configuration were added	November 2016
0.1	Initial draft	October 2016

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1.0 Introduction

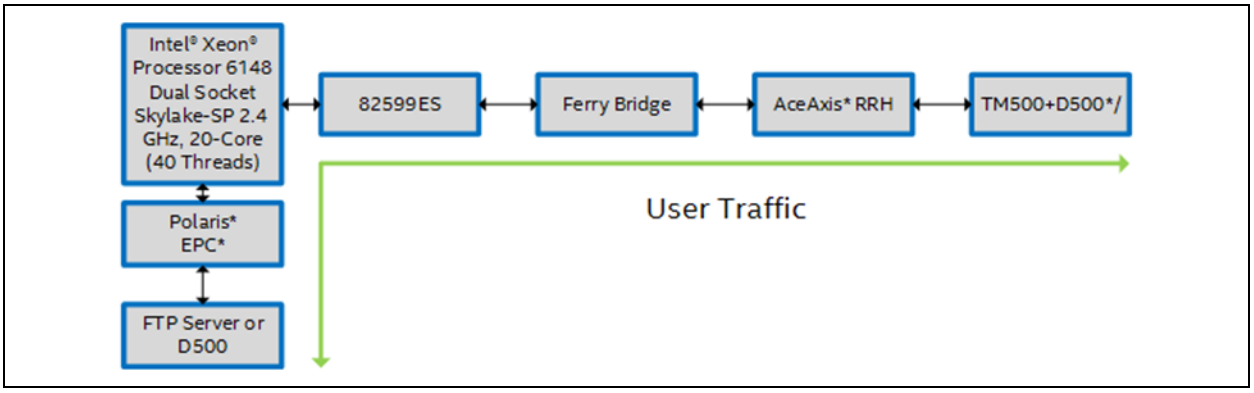
This User Guide describes the overall setup and components required to demonstrate the capabilities and performance of the FlexRAN implementation based on the Intel® Xeon® processor using Wind River* Titanium* Cloud (TiC5).

The goal of this document is to enable users to quickly configure, build, and run FlexRAN applications on an Intel® Xeon® processor-based platform.

1.1 Overview

The FlexRAN platform consists of an Intel® Sever Board S2600WF Family (Formerly Wolf Pass) Server with a dual-socket Intel® Xeon® 6148 processors running at 2.4 GHz. This Platform is used for LTE FDD/TD-LTE 3GPP Release10 cell at 20 MHz bandwidth, with two-component carriers. The Wolf Pass Server is configured to use a PCIe* slot with an Intel® 82599ES 10 Gigabit Ethernet Controller, connected through a 10 GB optical Ethernet to the Intel® Ferry Bridge Field Programmable Gate Array (FPGA) that provides Ethernet-to-CPRI conversion. The Ferry Bridge FPGA's CPRI port connects to an AceAxis* Advanced Radio Tester (ART) remote radio head (RRH). RF ports on the RRH are connected to either the CUEs* or a Viavi* TM500* multi-UE emulator. The Wolf Pass server runs the eNodeB function of an LTE network. The setup includes EPC* and Linux* FTP Server/Viavi* D500*, used to perform end-to-end testing data traffic over the LTE network.

Figure 1. FlexRAN Block Diagram



1.2 Hardware

The hardware configuration used for testing:

- Intel® Server Board S2600WF Family (Formerly Wolf Pass) with two 20-core Intel® Xeon® Gold 6148 Processor at 2.4 GHz
- Intel® 82599ES 10 Gigabit Ethernet Controller
- Intel® Ferry Bridge FPGA module
- RRH:
  - AceAxis* Remote Radio Head with 2x2 antenna configuration (for non-CA)
  - AceAxis* Remote Radio Head with 4x4 antenna configuration (CA, and 4x4 MIMO)

- FTP server
- Viavi* D500 traffic generation
- LTE EPC server
- UE side:
  - Samsung S10 Model SM-G977U, 5GNR/LTE Band2/13 FDD/TDD
  - Viavi* TM500 Multi UE emulator (non-CA, CA, and 4x4 MIMO)
- 1 Gigabit switch

The TM500 emulator's hardware configuration requires a UMBRA2 (20 MHz) reconfigurable radio card running the LMY7.6.1 Software Package.

1.3 Terminology

Table 1. Terminology

Term	Description
ART	Advanced Radio Tester
AVX2	Intel® Advanced Vector Extensions
BBU	Base Band Unit
CA	Carrier Aggregation
CC	Component Carrier
CPRI	Common Public Radio Interface
CUE	Commercial UE
DDP	Dynamic Device Personalization
EPC	Evolved Packet Core
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
FTP	File Transfer Protocol
HO	Hardware Offload
ISA	Instruction Set Architecture
L1	Layer One or Physical Layer
L2	Layer Two or Media Access Control Layer
MIMO	Multiple Input Multiple Output
nFAPI	Network Functional Application Platform Interface
NIC	Network Interface Card
NVM	Node Version Manager
LTE	Long Term Evolution
OTA	Over-the-Air
PCIe*	Peripheral Component Interconnect-Express
PF	Physical Function

Term	Description
RAN	Radio Access Network
RRH	Remote Radio Head (for example, Ace Axis ART)
TiC5	Titanium Cloud 5
UDP	User Datagram Protocol
UE	User Equipment
VM	Virtual Machine
VF	Virtual Function
WLS	Wireless Subsystem Interface
WR	Wind River*

1.4 Reference Documents and Resources

Table 2. Reference Documents and Resources

Title	Intel Document Number Location
FlexRAN Reference Solution Software Release Notes	575822
FlexRAN Reference Solution L1 XML Configuration User Guide	571741
FlexRAN Reference Solution LTE eNB L2-L1 Application Programming Interface [API] Specification	571742
FlexRAN Reference Solution L2-L1 nFAPI Specification	576423
FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide	575891
Intel® Sever Board S2600WF Family (Formerly Wolf Pass) Server Documentation	https://ark.intel.com/products/codename/80739/Wolf-Pass
Advanced Radio Tester Product Fact Sheet	https://aceaxis.co.uk/test-radio/
TM500 LTE TEST Mobile Application User Guide*	https://www.viavisolutions.com/en-us/products/tm500-network-tester
ART Radio User Guide	See Note 1
Intel® C++ Compiler in Intel® Parallel Studio XE	https://software.intel.com/content/www/us/en/develop/tools/compilers/c-compilers/choose-download.html
DPDK documentation	*http://dpdk.org/doc/guides/*
Wind River Titanium Server Installation for Systems with Controller Storage, 16.10*	*https://knowledge.windriver.com*
Polaris EPC User Guide*	See Note 2
Total eNodeB User Guide	https://www.radisys.com/support-portal

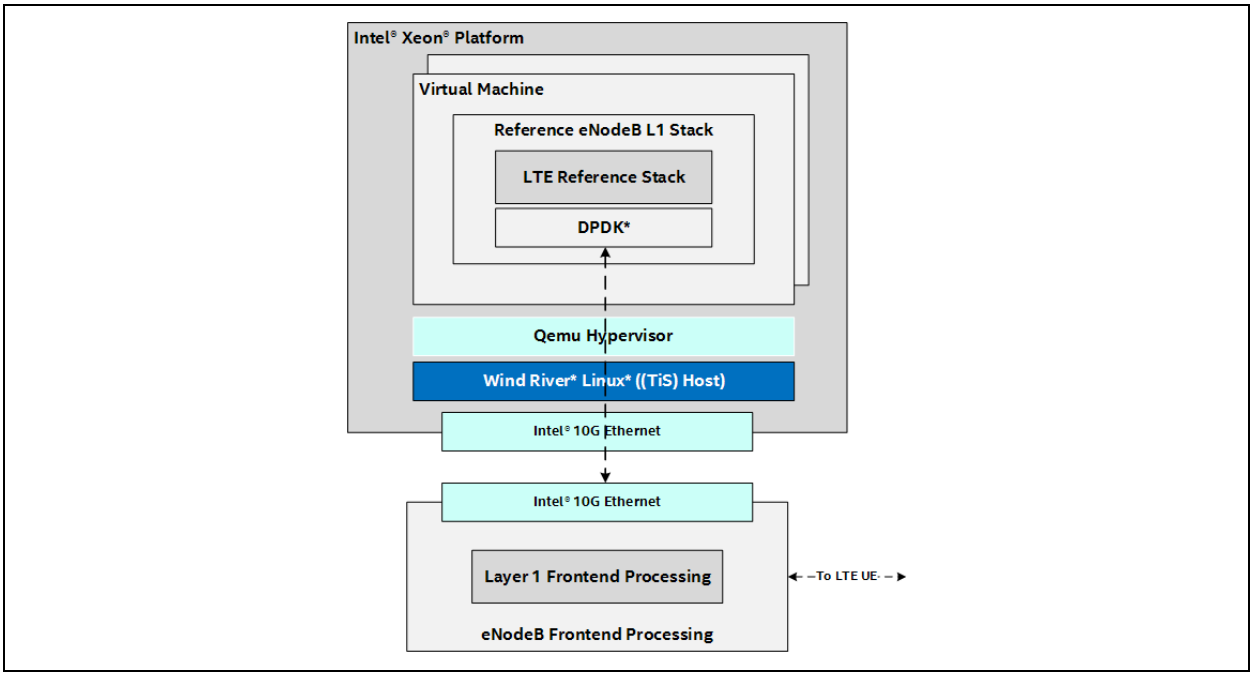
NOTES:

1. The ART Radio User Guide is provided by AceAxis* when customers purchase their Remote Radio Head.
2. Polaris* software provides the User Guide with the purchase of the software.

1.5 FlexRAN Application Environment

The software stack for FlexRAN applications is based on Wind River* Titanium Cloud for Host and CentOS* for Guest. The user is expected to install the Wind River Titanium Cloud environment before going further in this document. Refer to the FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide in Reference Documents and Resources, Table 2.

Figure 2. FlexRAN Software Stack



The host and guest versions of the Titanium Cloud* (TiC) and guest OS have been tested with the current release of Long Term Evolution (LTE) eNodeB. For the current version, refer to the FlexRAN Reference Solution Software Release Notes in Reference Documents and Resources, Table 2.

In general, other versions of Wind River* TiC can be used as well, because there is no direct dependency between the LTE eNodeB applications and TiC components. However, Intel recommends using a proven combination of versions to avoid unexpected issues with the build and configuration of the FlexRAN Application.

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2.0 Target Platform Configuration

Configure the target platforms with:

- Wind River Titanium* Cloud 5* (TiC5*)
- Virtio* Interface for Guest Systems
- Intel® C++ Compiler version v18.01

2.1 Wind River* Titanium Cloud Installation

For the Wolf Pass Server installation, refer to Reference Documents and Resources, Table 2. Wind River* Titanium Server Installation for Systems with Controller Storage, Section 16.10, and FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide documents. Wind River provides additional information on how to install the Wind River* Titanium Cloud using the installer image. Refer to https://knowledge.windriver.com/ for more information.

The FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide document (refer to Table 2) is intended to address cloud deployment because of specific hardware requirements for deployment.

NOTE: If cloud deployment is not currently intended, then continue to use the existing FlexRAN environment.

For any further questions, contact your Intel representative.

2.2 Guest Configuration

By default, TiC networking is configured to use the Virtio* Interface for Guest Systems. No other networking interfaces are configured. For a FlexRAN eNodeB application running in a Virtual Machine (VM), a 10 G dedicated networking port in pass-through is required. Refer to section “NIC Pass-through” in the FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide listed in Table 2. This interface is expected to be connected directly to the Ferry Bridge Ethernet port.

2.3 Intel® C++ Compiler

The Intel® C++ Compiler is required to compile DPDK and L1 (Layer 1) software.

Recommended Intel® C++ Compiler version: v19.0.3206 (refer to Table 2)

NOTE: Instructions on how to install the Intel® C++ Compiler package are outside of the scope of this document.

The DPDK and L1 packages must be compiled with the Intel® C++ Compiler.

2.4 DPDK Configuration

The FlexRAN Application requires DPDK v19.11.

1. Download: http://dpdk.org/browse/dpdk/snapshot/dpdk-19.11.tar.gz
2. Unzip to `/opt/dpdk-19.11`
3. Install the numactl library:
   ```
   yum install numa*
   ```
4. Patch DPDK to support the Intel Niantic NIC, DPDK Wireless Subsystem Interface (WLS) memory, and BBDEV:
   a. A DPDK patch file will is included in the release package. It should be named something like:

```
dpdk-19.11_20_08.patch
```

b. Copy the patch file to the directory where DPDK has been un-tarred (/opt/dpdk-19.11, for example). Confirm that this is a clean version of DPDK v19.11.
c. Patching an already patched version may introduce issues.
d. Use the following command to patch the DPDK:

```
git apply dpdk-19.11_20_08.patch
```

5. Configure the DPDK with the commands:

```
/opt/dpdk-19.11# cd ./usertools/
/opt/dpdk-19.11/usertools# ./dpdk-setup.sh
```

a. Select:

```
[39] x86_64-native-linuxapp-icc
```

b. Select:

```
[18] Insert IGB UIO module
```

c. Exit from `dpdk-setup.sh`

6. Configure DPDK to run with BBDEV enabled:

```
/opt/dpdk-19.11# vi config/common_base
```

Change the parameter to be:

```
CONFIG_RTE_BBDEV_SDK_AVX2=y
```

Compile with option 39, as listed above.

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3.0 FlexRAN eNodeB Applications

3.1 Prerequisites for Compilation

- Wind River* Titanium* Cloud compute node with installed and configured VM.
- An Intel compiler that must be installed in the VM.
- The kernel source files must be available for the compilation of the wls.ko module in the VM.
- The FlexRAN software package includes:
  - Ferry Bridge Library source code
  - wls_mod source code
  - LTE PHY source code
- Radisys* Layer 2/3 eNodeB binaries must be obtained from Radisys*. They are needed for the following scenarios:
  - FDD non-CA (Carrier Aggregation)
  - FDD CA
  - FDD 4x2 MIMO (Multiple Input Multiple Output)
  - TDD non-CA
  - TDD CA
- Enter the following commands in CMake:

```
wget https://cmake.org/files/v3.9/cmake-3.9.2.tar.gz --no-check-certificate
tar xvzf CMake-3.9.2.tar.gz
cd cmake-3.9.2
./configure
make
sudo make install
```

3.2 L1 (Layer One) Application

Extract all components of the FlexRAN release using extract.sh.

For example:

```
/home/turner/work/flexran
├── bin
├── build
├── framework

├── libs
        ├── ferrybridge
        ├── mlog
        └── roe
├── misc
├── nfapi
├── sdk
├── source
├── tests
```

```
        └── lte
└── wls_mod
```

To build the L1 application, follow these steps:

1. To display available options use:
```
source ./set_env_var.sh -h
./flexran_build.sh -h
```
2. For an AVX2 system (for example, Broadwell):

   To set path to DPDK, ICC, and SDK:
```
source ./set_env_var.sh -d -i avx2
```
   To compile only the SDK and wls modules:
```
./flexran_build.sh -e -r lte -i avx2 -m wls -m sdk
```
   To compile all modules:
```
./flexran_build.sh -e -r lte -i avx2
```
3. For an AVX512 system (for example, Skylake):

   To set path to DPDK, ICC, and SDK:
```
source ./set_env_var.sh -d -i avx512
```
   To compile only the BBU framework and mlog:
```
./flexran_build.sh -e -r lte -i avx512 -m bbu -m mlog
```
   To compile all of the modules:
```
./flexran_build.sh -e -r lte -i avx512
```
4. To compile with the BBDEV option enabled:
```
./flexran_build.sh -e -r lte -b -i avx2
```

NOTE: Notice the "-b option" to turn on the BBDEV compile-time flags. The -b option will work for both Intel® Advanced Vector Extensions (Intel® AVX2) and AVX512 ISA options.

- The field <dpdkBasebandFecMode> located in phycfg.xml will configure using either software Forward Error Correction (FEC) or hardware FEC (N3000 or ACC100 for Turbo Encoder/Decoder) through the BBDEV interface. 0 => SW, 1 = HW.
- Set PCIe* address to appropriate address by setting <dpdkBasebandDevice> located in phycfg.xml.
- Use Linux command to obtain PCIe address: lspci | grep acc
- The PCIe device address of the N3000 for LTE FEC is the one listed under the Device (0d8f)
- The PCIe device address of the ACC100 for LTE FEC is the one listed under the Device (0d5c)
- Refer to the readme file to setup FEC Queues for N3000 and ACC100, located in:
```
./misc/bbdev_config_service/README.md
```

5. The resulting PHY binary can be found in this directory:
```
./bin/lte/l1
|-- dpdk.sh
|-- l1.sh
|-- l1app
|-- phycfg.xml
```
6. If logging back into the system after logging out, execute to setup export paths:
```
source ./set_env_var.sh -d -i avx512
```

3.3 L2 (Layer Two) Application

The L2 Application is provided in binary form by the Layer Two partner Radisys*.

Five binaries and configuration files support the following scenarios:

- Cell: FDD Non-CA (with 10 MHz config)
- 1 Cell: FDD 4x2 MIMO
- 1 Cell: FDD CA with two CC
- 1 Cell: TDD Non-CA
- 1 Cell: TDD CA with two CC

```
/home/turner/work/l2
|-- fdd
|   |-- 10mhz
|   |   `-- wr_cfg.txt
|   |-- checksum.md5
|   |-- enodeb
|   |-- l2.sh
|   `-- wr_cfg.txt
|-- fdd_4x2_mimo
|   |-- checksum.md5
|   |-- enodeb
|   |-- l2.sh
|   `-- wr_cfg.txt
|-- fdd_ca
|   |-- checksum.md5
|   |-- enodeb
|   |-- l2.sh
|   `-- wr_cfg.txt
|-- tdd
|   |-- checksum.md5
|   |-- enodeb
|   |-- l2.sh
|   `-- wr_cfg.txt
`-- tdd_ca
    |-- checksum.md5
    |-- enodeb
    |-- l2.sh
    `-- wr_cfg.txt
```

3.4 Test and Debug Applications

The FlexRAN package includes multiple supporting applications used for execution test scenarios and parsing debug information:

- `testapp`
- `testmac`

1. Build Wireless SDK component.

   The SDK package can be located anywhere in the file system. If it is located in `/home/turner/work/flexran/SDK` issue the commands:

   a. For AVX2 system (for example, Broadwell):

   ```
   ./flexran_build.sh -e -r lte -m sdk -i avx2
   ```

   b. For AVX512 system (for example, Skylake):

```
./flexran_build.sh -e -r lte -m sdk -i avx512
```

2. Build testapp (bit-exact tests):

```
./flexran_build.sh -e -r lte -m lte_testapp
```

The resulting `lte_testapp` elf file can be found in:

```
/home/turner/work/flexran/tests/lte.
```

3. Build testmac (simulation of L2):

```
./flexran_build.sh -e -r lte -m lte_testmac
```

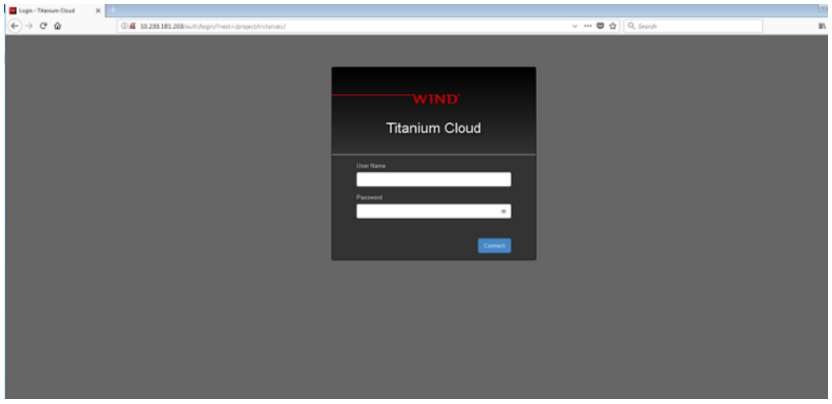
The resulting testmac elf file can be found in:

```
/home/turner/work/flexran/bin/lte/testmac
```

3.5 How to Start End-to-end Scenario

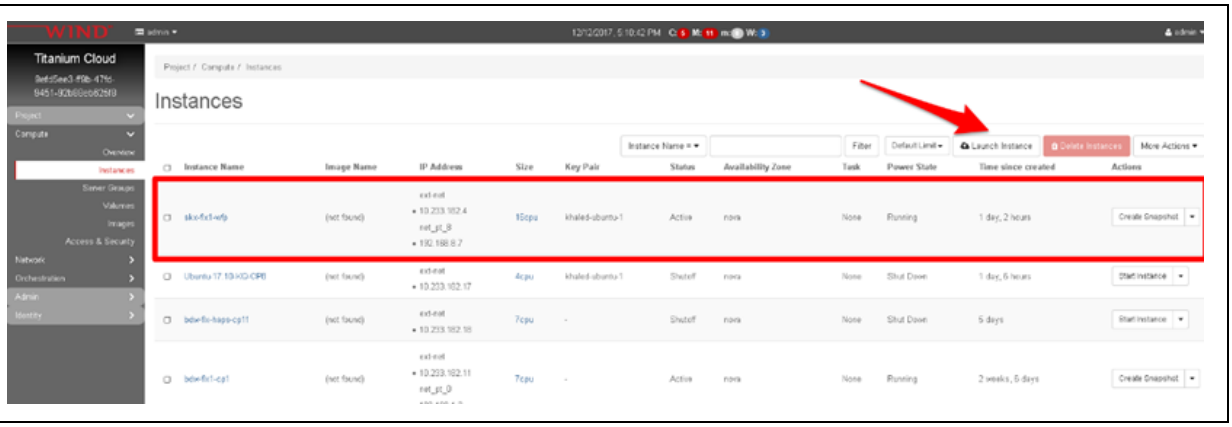
Configuration of the Compute node and the VM instance must be performed in the Titanium Cloud Administrative Console:

Figure 3. Titanium Cloud Administrative Console



From the dropdown menu, select **Project -> Instances** and select **Launch Instance** (refer to Figure 4).

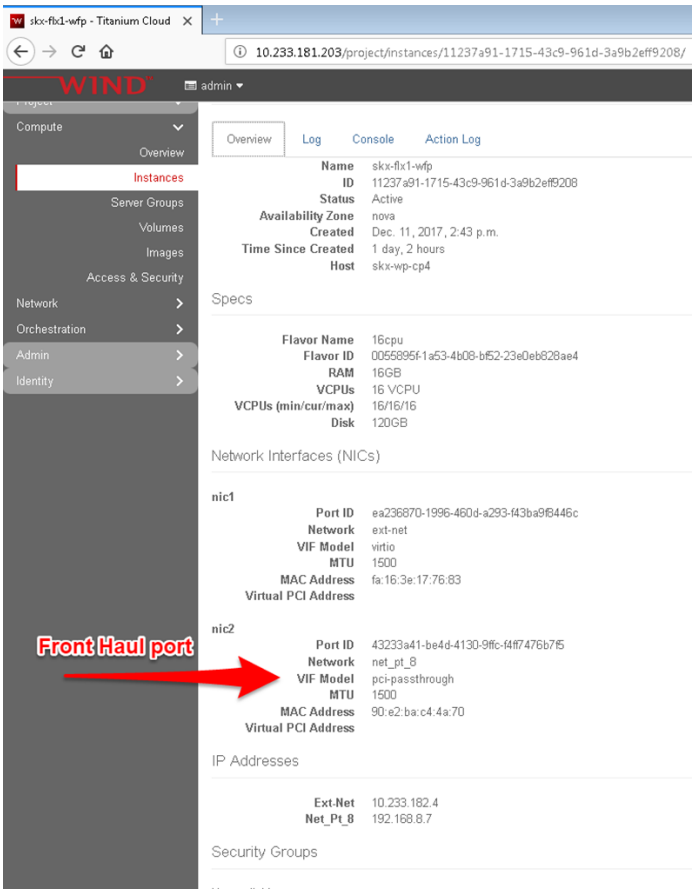
Figure 4. Launch Instance



Refer to the Reference Documents and Resources, Table 2, *FlexRAN, and Mobile Edge Compute (MEC) Platform Setup Guide* for instructions and/or full configuration of the VM instance.

A dedicated pass-through 10 G networking card must be added to the configuration of the FlexRAN VM for the Ferry Bridge Front-haul connection (refer to Figure 5).

Figure 5. Configuration of Dedicated Pass-through 10 G Networking Card



Refer to Reference Documents and Resources, Table 2, *FlexRAN, and Mobile Edge Compute (MEC) Platform Setup Guide* document for more detailed information on network configuration, as well as overall Titanium Cloud 5 (TiC5) node configuration.

3.5.1 Start L1

To start the L1 software, copy the L1 binaries and start-up scripts to VM.

For the given example, the location of the L1 application is /home/turner/work/ and the location of the L2 application is `/home/turner/work/rsys/bundle/`.

The script `dpdk.sh` has to be updated with correct Peripheral Component Interface–express* (PCIe*) bus information for a given PCIe Network Interface Card (NIC).

```
#
vm0-skx-wp-cp4:~# lspci |grep Eth
00:03.0 Ethernet controller: Red Hat, Inc Virtio network device
00:05.0 Ethernet controller: Intel Corporation 82599ES 10-Gigabit SFI/SFP+ Network
Connection
#cat ./dpdk.sh
```

```
…
$RTE_SDK/usertools/dpdk_nic_bind.py --bind=igb_uio 0000:00:05.0
…

Modify the phycfg.xml to use the same Ethernet port with a correct number of cells.

<Radio>
        <!-- Enable/disable radio                [0 - disable (external app control
radio), 1 - use Lib-Radio, 2 - use phy app (obsolete)] -->
        <radioEnable>1</radioEnable>
        <!--  DPDK memory size allocated from hugepages [MB]  [default: 2048] -->
        <dpdkMemorySize>6144</dpdkMemorySize>
        <!--  DPDK Interrupt mode enable         [0 - disabled, PMD is used, 1 -
enabled, uio irq is used] -->
        <dpdkIrqMode>0</dpdkIrqMode>
        <!--  Ferry Bridge (FB) mode             [0 - LTE MODE, 1 - CPRI BYPASS MODE] -
->
        <ferryBridgeMode>0</ferryBridgeMode>
        <!--  Number of Ethernet ports on FB     [0 - DPDK port 0, 1 - DPDK port 1, 2 -
both DPDK port 0 and port 1 (CA mode with two ETH)] -->
        <ferryBridgeEthPort>1</ferryBridgeEthPort>
        <!--  FB Synchronized CPRI ports         [0 - no reSync REC & RE FPGA, 1 -
reSync REC & REC FPGA] -->
        <ferryBridgeSyncPorts>0</ferryBridgeSyncPorts>
        <!--  FB Loopback Mode                   [0 - no optical loopback connected
REC<->RE, 1 - optical loopback connected REC<->RE] -->
        <ferryBridgeOptCableLoopback>0</ferryBridgeOptCableLoopback>

        <!--  Radio Config 0 -->
        <RadioConfig0>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg0PCIeEthDev>0000:00:05.0</radioCfg0PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg0DpdkRx>1</radioCfg0DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg0DpdkTx>2</radioCfg0DpdkTx>
            <!--  Number of Tx Antenna          [1, 2, 4] -->
            <radioCfg0TxAnt>4</radioCfg0TxAnt>
            <!--  Number of Rx Antenna          [1, 2, 4] -->
            <radioCfg0RxAnt>4</radioCfg0RxAnt>
            <!--  Rx AGC configuration          [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg0RxAgc>0</radioCfg0RxAgc>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg0NumCell>1</radioCfg0NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg0Cell0PhyId>0</radioCfg0Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg0Cell1PhyId>1</radioCfg0Cell1PhyId>
        </RadioConfig0>
```

From Guest OS, set up the environment with the command:

```
export DIR_WIRELESS_SDK_ROOT=/home/turner/work/flexran/sdk
```

For AVX2 system (for example, Broadwell):

```
export SDK_BUILD=build-avx2-icc
```

```
export WIRELESS_SDK_TARGET_ISA=avx2
export DIR_WIRELESS_SDK=${DIR_WIRELESS_SDK_ROOT}/${SDK_BUILD}
```

For the AVX512 system (for example, Skylake):

```
export SDK_BUILD=build-avx512-icc
export WIRELESS_SDK_TARGET_ISA=avx512
export DIR_WIRELESS_SDK=${DIR_WIRELESS_SDK_ROOT}/${SDK_BUILD}
```

For all three environments, run these commands:

```
cd /home/turner/work/flexran/bin/lte/l1app
./l1.sh
```

After starting L1 application, wait for a minimum of 10 seconds before starting the L2 application.

Configuration of threads can be specified using phycfg.xml:

```
       <bbuPoolCores>28</bbuPoolCores>
<!-- Wireless Subsystem Thread: Core, priority, Policy [0: SCHED_FIFO 1: SCHED_RR] -->
        <wlsRxThread>6, 96, 0</wlsRxThread>

        <!-- Wireless Subsystem Worker Thread: Core, priority, Policy [0: SCHED_FIFO
1: SCHED_RR] -->
        <wlsWorkerThread>6, 96, 0</wlsWorkerThread>

        <!-- System Threads: Core, priority, Policy [0: SCHED_FIFO 1: SCHED_RR] -->
        <systemThread>0, 0, 0</systemThread>

        <!-- Timer Thread: Core, priority, Policy [0: SCHED_FIFO 1: SCHED_RR] -->
        <timerThread>0, 96, 0</timerThread>

        <!-- DPDK Radio Master Thread: Core, priority, Policy [0: SCHED_FIFO 1:
SCHED_RR] -->
        <radioDpdkMaster>0, 99, 0</radioDpdkMaster>

        <!-- Enable L1 processing on Single Core per Cell -->
        <singleCore>0</singleCore>
    </Threads>
```

3.5.2 Start L2

After the L2 application is started successfully, check the L1 console for messages as mentioned below. Try to connect UEs only after you see those messages on the L1 console.

Log in the Guest OS, using a different console using the following:

```
#cd /home/turner/work/rsys/bundle
#./l2.sh
```

3.5.3 PHY Application Output Example (non-CA)

Start of l1app with 4x4 RRH (Remote Radio Head) with 1Cell non-CA configuration:

```
vm0-skx-wp-cp4:/lte_phy# ./l1.sh
HugePages_Total:       8
HugePages_Free:        7
HugePages_Rsvd:        0
HugePages_Surp:        0
Hugepagesize:    1048576 kB
12864
```

```
kernel.sched_rt_runtime_us = -1
./l1.sh: line 46: /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu1/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu10/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu11/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu12/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu13/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu14/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu15/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu2/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu3/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu4/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu5/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu6/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu7/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu8/cpufreq/scaling_governor: No such file
or directory
./l1.sh: line 46: /sys/devices/system/cpu/cpu9/cpufreq/scaling_governor: No such file
or directory
kernel.shmmax = 2147483648
kernel.shmall = 2147483648
Note: Forwarding request to 'systemctl disable irqbalance.service'.
0001
0001
0001
0001
0001
0001
0001
0001
0001
0001
0001
0001
RADIO Mode
Unloading any existing DPDK UIO module
Loading DPDK UIO module
VM

Network devices using DPDK-compatible driver
============================================
<none>

Network devices using kernel driver
===================================
0000:00:03.0 'Virtio network device' if=eth0 drv=virtio-pci unused=igb_uio
```

```
Other network devices
=====================
0000:00:05.0 '82599ES 10-Gigabit SFI/SFP+ Network Connection' unused=igb_uio
Crypto devices using DPDK-compatible driver
===========================================
<none>

Crypto devices using kernel driver
==================================
<none>

Other crypto devices
====================
<none>

Network devices using DPDK-compatible driver
============================================
0000:00:05.0 '82599ES 10-Gigabit SFI/SFP+ Network Connection' drv=igb_uio unused=

Network devices using kernel driver
===================================
0000:00:03.0 'Virtio network device' if=eth0 drv=virtio-pci unused=igb_uio

Other network devices
=====================
<none>

Crypto devices using DPDK-compatible driver
===========================================
<none>

Crypto devices using kernel driver
==================================
<none>

Other crypto devices
====================
<none>
Command String =
using configuration file phycfg.xml
>> Running... ././l1app --cfgfile=phycfg.xml
FlexRAN SDK bblib_lte_scramble version #DIRTY#
FlexRAN SDK bblib_lte_turbo version #DIRTY#
FlexRAN SDK bblib_lte_crc version #DIRTY#
FlexRAN SDK bblib_lte_rate_matching version #DIRTY#
FlexRAN SDK bblib_lte_dft_idft version #DIRTY#
FlexRAN SDK bblib_lte_tbcc version #DIRTY#
FlexRAN SDK bblib_lte_modulation version #DIRTY#
FlexRAN SDK bblib_lte_demodulation version #DIRTY#
FlexRAN SDK bblib_lte_precoding version #DIRTY#
FlexRAN SDK bblib_lte_deinterleave version #DIRTY#
=========================
LTE PHY Application
=========================
cline_get_string:Searching for string: cfgfile. Length of string: 7
cline_get_string:Found cfgfile: Val = phycfg.xml

PhyCfg XML file parsed
Version found returned 0 6.6
```

```
---------------------------
PhyCfg.xml Version: 6.6
---------------------------

Apply config..
cline_print_info:Incomming settings:
 --version=6.6
 --mac2PhyBatchApi=1
 --phy2MacBatchApi=1
 --successiveNoApi=15
 --wls_dev_name=/dev/wls
 --dlIqLog=0
 --ulIqLog=0
 --iqLogDumpToFile=0
 --phyMlog=1
 --phyStats=1
 --powerSaveEnable=0
 --radioEnable=1
 --dpdkMemorySize=6144
 --dpdkIrqMode=0
 --ferryBridgeMode=0
 --ferryBridgeEthPort=1
 --ferryBridgeSyncPorts=0
 --ferryBridgeOptCableLoopback=0
 --radioCfg0PCIeEthDev=0000:00:05.0
 --radioCfg0DpdkRx=1
 --radioCfg0DpdkTx=2
 --radioCfg0TxAnt=4
 --radioCfg0RxAnt=4
 --radioCfg0RxAgc=0
 --radioCfg0NumCell=1
 --radioCfg0Cell0PhyId=0
 --radioCfg0Cell1PhyId=1
 --radioCfg1PCIeEthDev=0000:03:00.1
 --radioCfg1DpdkRx=1
 --radioCfg1DpdkTx=1
 --radioCfg1TxAnt=4
 --radioCfg1RxAnt=4
 --radioCfg1RxAgc=0
 --radioCfg1NumCell=2
 --radioCfg1Cell0PhyId=2
 --radioCfg1Cell1PhyId=3
 --radioCfg2PCIeEthDev=0000:05:00.0
 --radioCfg2DpdkRx=10
 --radioCfg2DpdkTx=11
 --radioCfg2TxAnt=4
 --radioCfg2RxAnt=4
 --radioCfg2RxAgc=0
 --radioCfg2NumCell=2
 --radioCfg2Cell0PhyId=4
 --radioCfg2Cell1PhyId=5
 --radioCfg3PCIeEthDev=0000:05:00.1
 --radioCfg3DpdkRx=12
 --radioCfg3DpdkTx=13
 --radioCfg3TxAnt=4
 --radioCfg3RxAnt=4
 --radioCfg3RxAgc=0
 --radioCfg3NumCell=2
```

```
--radioCfg3Cell0PhyId=6
--radioCfg3Cell1PhyId=7
--radioCfg4PCIeEthDev=0000:00:08.0
--radioCfg4DpdkRx=14
--radioCfg4DpdkTx=15
--radioCfg4TxAnt=4
--radioCfg4RxAnt=4
--radioCfg4RxAgc=0
--radioCfg4NumCell=2
--radioCfg4Cell0PhyId=8
--radioCfg4Cell1PhyId=9
--radioCfg5PCIeEthDev=0000:08:00.0
--radioCfg5DpdkRx=16
--radioCfg5DpdkTx=16
--radioCfg5TxAnt=4
--radioCfg5RxAnt=4
--radioCfg5RxAgc=0
--radioCfg5NumCell=2
--radioCfg5Cell0PhyId=10
--radioCfg5Cell1PhyId=11
--radioCfg6PCIeEthDev=0000:00:05.0
--radioCfg6DpdkRx=16
--radioCfg6DpdkTx=16
--radioCfg6TxAnt=4
--radioCfg6RxAnt=4
--radioCfg1RxAgc=0
--radioCfg6NumCell=2
--radioCfg6Cell0PhyId=12
--radioCfg6Cell1PhyId=13
--radioCfg7PCIeEthDev=0000:00:06.0
--radioCfg7DpdkRx=16
--radioCfg7DpdkTx=16
--radioCfg7TxAnt=4
--radioCfg7RxAnt=4
--radioCfg7RxAgc=0
--radioCfg7NumCell=2
--radioCfg7Cell0PhyId=14
--radioCfg7Cell1PhyId=15
--radioPort0=0
--radioPort1=1
--radioPort2=2
--radioPort3=3
--radioPort4=4
--radioPort5=5
--radioPort6=6
--radioPort7=7
--taFiltEnable=1
--ircEnable=0
--mmseDisable=0
--fecDecEarlyTermDisable=0
--fecDecNumHalfIter=0
--pucchFormat2DetectThreshold=0
--prachDetectThreshold=100
--TimerModeFreqDomain=0
--MlogSubframes=128
--MlogCores=10
--MlogSize=3084
--apiThread=2, 96, 0
--prachThread=4, 95, 0
--fftMainThread=3, 98, 0
```

```
--fftProc0Thread=3, 98, 0
--fftProc1Thread=4, 98, 0
--fftProc2Thread=5, 98, 0
--fftProc3Thread=6, 98, 0
--ifftMainThread=2, 97, 0
--ifftProc0Thread=2, 97, 0
--ifftProc1Thread=4, 97, 0
--ifftProc2Thread=5, 97, 0
--ifftProc3Thread=6, 97, 0
--dlMainThread=2, 96, 0
--dlProc0Thread=6, 96, 0
--dlProc1Thread=6, 96, 0
--dlProc2Thread=2, 96, 0
--dlProc3Thread=6, 96, 0
--ulMainThread=3, 96, 0
--ulProc0Thread=4, 96, 0
--ulProc1Thread=4, 96, 0
--ulProc2Thread=3, 96, 0
--ulProc3Thread=4, 96, 0
--wlsRxThread=6, 96, 0
--wlsWorkerThread=6, 96, 0
--systemThread=0, 0, 0
--timerThread=0, 96, 0
--radioDpdkMaster=0, 99, 0
--singleCore=0
--BbuPoolConfigEnable=0
--BbuPoolSleepEnable=1
--BbuPoolThreadDefault=28, 94, 0
--BbuCoresCell1Ant1=12
--BbuCoresCell2Ant1=28
--BbuCoresCell3Ant1=60
--BbuCoresCell4Ant1=124
--BbuCoresCell5Ant1=508
--BbuCoresCell6Ant1=1020
--BbuCoresCell7Ant1=4092
--BbuCoresCell8Ant1=8188
--BbuCoresCell1Ant2=12
--BbuCoresCell2Ant2=28
--BbuCoresCell3Ant2=60
--BbuCoresCell4Ant2=124
--BbuCoresCell5Ant2=508
--BbuCoresCell6Ant2=1020
--BbuCoresCell7Ant2=4092
--BbuCoresCell8Ant2=8188
--BbuCoresCell1Ant4=28
--BbuCoresCell2Ant4=60
--BbuCoresCell3Ant4=252
--BbuCoresCell4Ant4=508
--BbuCoresCell5Ant4=2044
--BbuCoresCell6Ant4=4092
--BbuCoresCell7Ant4=8188
--BbuCoresCell8Ant4=16380
--BbuCoresCell1Ant8=28
--BbuCoresCell2Ant8=60
--BbuCoresCell3Ant8=252
--BbuCoresCell4Ant8=508
--BbuCoresCell5Ant8=2044
--BbuCoresCell6Ant8=4092
--BbuCoresCell7Ant8=8188
--BbuCoresCell8Ant8=16380
```

```
 --wckTeIrqNum=135
 --wckTeIrqCoreBind=2
 --TestUeModeEnable=0
 --dpdkIoThread=0, 90, 0
 --dpdkPort=0
 --dpdkDev=0000:00:00.0

phycfg_apply: Initialize Radio Interface with Ferry Bridge library
cline_set_thread_info: dpdkIoThread 0 90 1
cline_set_thread_info: wlsRxThread 6 96 1
cline_set_thread_info: wlsWorkerThread 6 96 1
cline_set_thread_info: systemThread 0 0 1
cline_set_thread_info: timerThread 0 96 1
cline_set_thread_info: radioDpdkMaster 0 99 1
cline_set_thread_info: BbuPoolThreadDefault 28 94 1
PhyCfg File completely read: 0
phycfg_apply:
PHY Logs Enabled:
phycfg_apply:-----------------
phycfg_apply:MLOG:                    YES
phycfg_apply:DL IQ:                   NO
phycfg_apply:UL IQ:                   NO
phycfg_apply:PHY STATS:               YES
phycfg_apply:RADIO IQ DUMP TO FILE:   NO
phycfg_apply:FFT/IFFT on RADIO :      YES
phycfg_apply:-----------------
sys_load_app_in_ram:
sys_load_app_in_ram:AppInRam: Start: pid=12957
sys_load_app_in_ram:[err] AppInRam: Warning. Looked for 2 args in 'proc//maps' string,
found: 2
sys_load_app_in_ram:[err] AppInRam: Warning. Looked for 2 args in 'proc//maps' string,
found: 2
sys_load_app_in_ram:[err] AppInRam: Warning. Looked for 2 args in 'proc//maps' string,
found: 2
sys_load_app_in_ram:AppInRam: End. 0 areas checked to be loaded in RAM

sys_init:Initialization
cmgr_init:initialization of console
System clock (rdtsc) resolution 2394266095 [Hz]
Ticks per us 2394
MLogOpen: filename(l1mlog.bin) mlogSubframes (128), mlogCores(10), mlogSize(3084)
mlog_mask (-1)
MLogTimerInit
        System clock (rdtsc) resolution 2394267909 [Hz]
        Ticks per us 2394
    mlogSubframes (128), mlogCores(10), mlogSize(3084)
 MLOG not opened!!!
MLog Storage: 0x7fea266a3010 -> 0x7fea26a6783c
MLogInitializeMlogBuffer
MLogFreqReg: 2394. Storing: 2394
MLogGetResId: Assigning arr 0 to core 0
Mlog Open successful
----------------------------------------
MLog Info: virt=0x00007fea266a3010 size=3950636
----------------------------------------
wls_layer_init: WLS_Open /dev/wls
wls_lib: Open /dev/wls 0xc0085701
wls_lib: User Space Lib Context: us va 0x00007fea32d84000 kernel va 0xffff8800b97b0000
pa 0x00000000b97b0000 size 65536
wls_lib:
```

```
Mode 0
wls_lib:
WLS device /dev/wls [8]
wls_lib: hugePageSize on the system is 1073741824
wls_lib: shm open /tmp/phyappshm__dev_wls
wls_lib: Attach to shared memory
wls_lib: pvirtAddr  0x00002aaac0000000
wls_lib: WLS_Alloc: 0x00002aaac0000000 [1046478848]
wls_rx_handler:           [PID:  12958] binding on [CPU  6] [PRIO: 96] [POLICY:  1]
di_radio_initdi_radio_cfg_setup nCC 1 radioItf 1
bbuPool cores mask  0xfffff
DPDK cores mask  0xfffff
DPDK memory size 6144
EAL: Detected 16 lcore(s)
EAL: Probing VFIO support...
EAL: WARNING: cpu flags constant_tsc=yes nonstop_tsc=no -> using unreliable clock
cycles !
EAL: PCI device 0000:00:05.0 on NUMA socket -1
EAL:   probe driver: 8086:10fb net_ixgbe
num_ports 1
 ports[0] 0 ports[1] 0
DPDK cores 16
rte_eth_dev_count 1
valid_num_ports 1
 num_ports 1  ports[0] 0 ports[1] 0
RX_MBUF_POOL_PORT 0 size 640155648
TX_MBUF_POOL_PORT 0 size 640155648
[0] rxRings 128 txRings 128 rx total 16384
Port 0 MAC: 90 e2 ba c4 4a 70
DPDK port 0
2048-point IFFT initialization. Optimization by Intel Lab China. 2011/11/30.
phy_bbupool_set_config: Using cores: 0x000000000000001c for BBU Pool
bbuPoolSleepEnable: 1
BBU Pooling: coreId = 2 is available!
BBU Pooling: coreId = 3 is available!
BBU Pooling: coreId = 4 is available!
BBU Pooling: taskId =  0 taskName =      MAC2PHY_API is registered
BBU Pooling: taskId =  1 taskName =       DL_PHY_FEC is registered
BBU Pooling: taskId =  2 taskName = DL_PHY_TURBO_SCR is registered
BBU Pooling: taskId =  3 taskName =       DL_PHY_MOD is registered
BBU Pooling: taskId =  4 taskName =          DL_IFFT is registered
BBU Pooling: taskId =  5 taskName =     DL_POST_IFFT is registered
BBU Pooling: taskId =  6 taskName =   DL_COMPRESSION is registered
BBU Pooling: taskId =  7 taskName =        DL_IQ_LOG is registered
BBU Pooling: taskId =  8 taskName =  UL_PARA_PREPARE is registered
BBU Pooling: taskId =  9 taskName =     UL_PHY_DEMOD is registered
BBU Pooling: taskId = 10 taskName =       UL_PHY_FEC is registered
BBU Pooling: taskId = 11 taskName =       UL_PHY_CRC is registered
BBU Pooling: taskId = 12 taskName =     UL_PHY_PUCCH is registered
BBU Pooling: taskId = 13 taskName =       UL_PHY_SRS is registered
BBU Pooling: taskId = 14 taskName =         UL_PRACH is registered
BBU Pooling: taskId = 15 taskName =        UL_IQ_LOG is registered
BBU Pooling: taskId = 16 taskName =           UL_FFT is registered
BBU Pooling: taskId = 17 taskName = UL_PHY_PROFILE_END is registered
BBU Pooling: next taskList of      MAC2PHY_API:        DL_PHY_FEC
BBU Pooling: next taskList of       DL_PHY_FEC:  DL_PHY_TURBO_SCR
BBU Pooling: next taskList of DL_PHY_TURBO_SCR:        DL_PHY_MOD
BBU Pooling: next taskList of       DL_PHY_MOD:           DL_IFFT
BBU Pooling: next taskList of          DL_IFFT:      DL_POST_IFFT
BBU Pooling: next taskList of     DL_POST_IFFT:    DL_COMPRESSION
```

```
BBU Pooling: next taskList of   DL_COMPRESSION:         DL_IQ_LOG
BBU Pooling: next taskList of        DL_IQ_LOG:               N/A

BBU Pooling: next taskList of  UL_PARA_PREPARE:         UL_IQ_LOG
BBU Pooling: next taskList of     UL_PHY_DEMOD:        UL_PHY_FEC
BBU Pooling: next taskList of       UL_PHY_FEC:        UL_PHY_CRC
BBU Pooling: next taskList of       UL_PHY_CRC:  UL_PHY_PROFILE_END
BBU Pooling: next taskList of     UL_PHY_PUCCH:        UL_PHY_CRC
BBU Pooling: next taskList of       UL_PHY_SRS:        UL_PHY_CRC
BBU Pooling: next taskList of         UL_PRACH:               N/A

BBU Pooling: next taskList of        UL_IQ_LOG:            UL_FFT
BBU Pooling: next taskList of          UL_FFT:      UL_PHY_DEMOD            UL_PRACH
UL_PHY_PUCCH          UL_PHY_SRS
BBU Pooling: next taskList of UL_PHY_PROFILE_END:               N/A

enter RtThread Launch
launching Thread 2 Queue 0 Core 2 Priority 94 Policy 1 nRtCoreSleep 1 nFriendCnt 1
FriendQueueIdx 1
3 thread associated with queue 0:0 2 3
Leave RtThread Launch
launching Thread 3 Queue 0 Core 3 Priority 94 Policy 1 nRtCoreSleep 1 nFriendCnt 1
FriendQueueIdx 1

============================
 PHY VERSION
============================
$Version: #DIRTY# $ (x86)
IMG-date: Dec 12 2017
IMG-time: 18:25:54
============================
 DEPENDENCIES VERSIONS
============================
FlexRAN BBU pooling version #DIRTY#
FlexRAN SDK bblib_lte_crc version #DIRTY#
FlexRAN SDK bblib_lte_deinterleave version #DIRTY#
FlexRAN SDK bblib_lte_demodulation version #DIRTY#
FlexRAN SDK bblib_lte_dft_idft version #DIRTY#
FlexRAN SDK bblib_lte_modulation version #DIRTY#
FlexRAN SDK bblib_lte_rate_matching version #DIRTY#
FlexRAN SDK bblib_lte_scramble version #DIRTY#
FlexRAN SDK bblib_lte_tbcc version #DIRTY#
FlexRAN SDK bblib_lte_turbo version #DIRTY#
FlexRAN SDK bblib_lte_precoding version #DIRTY#
============================

launching Thread 4 Queue 0 Core 4 Priority 94 Policy 1 nRtCoreSleep 1 nFriendCnt 1
FriendQueueIdx 1
lte_bs_mac2phy_api_recv:  [PID:  12979] binding on [CPU  6] [PRIO: 96] [POLICY:  1]
PHY>welcome to application console

2nd time -bbupool_core_main pthread_setaffinity_np succeed: coreId = 0, result = 0
PHY_INIT_REQ: 0
MLogGetResId: Assigning arr 1 to core 6
[lte_bs_mac2phy_api_proc_phy_init] phyInstance: 0
---------------------------------------------------------------------
 mem_mgr_leak_detector_display_size:
        Num Memory Alloc:           8
        Total Memory Size:        864
---------------------------------------------------------------------
```

```
Interfaces Enabled:
--------------------

phyCfg                                  0x00000307:
PHYINIT_PHY_MAINTAINS_PBCH:             YES
PHYINIT_USE_TXSDU_POINTER:              NO
PHYINIT_LOW_LATENCY_PATH:               YES
PHYINIT_MUTE_RXSDU_FOR_SR_RACH:         NO
PHYINIT_USE_SCATTERED_TXSDU_POINTERS:   YES
PHYINIT_USE_SCATTERED_RXSDU_POINTERS:   NO
PHYINIT_GLOBAL_IRC_ENABLE:              NO

phydi_init Carrier 0: DL[SizePerSfn: 122880, NumSfn: 128], UL[SizePerSfn: 122880,
NumSfn: 128]
phydi_init: pPhyDiCtx->frb_nPorts  1
phydi_init: pPhyDiCtx->frb_offload 1
phydi_init: pPhyDiCtx->prachConfigurationIndex 8
phydi_init: pPhyDiCtx->prachFrequencyOffset 43
phydi_init: pPhyDiCtx->frtypeDuplexmode 0
phydi_init: pPhyDiCtx->ulDlConfig 0
phydi_init: pPhyDiCtx->specialSubfraeConfig 0
lte_bs_mac2phy_api_proc_phy_init inst 0 ctx 0
lte_bs_tx_global_initialize: contextNum: 0 phyInstance: 0 fftSize: 2048 numSubCarrier:
1200
lte_bs_tx_global_initialize: contextNum: 1 phyInstance: 0 fftSize: 2048 numSubCarrier:
1200
lte_bs_rx_global_initialize: contextNum: 0 phyInstance: 0 numRxAnt = 2
lte_bs_rx_global_initialize: contextNum: 1 phyInstance: 0 numRxAnt = 2
lte_bs_fec_dec_global_initialize: contextNum: 0 phyInstance: 0
lte_bs_fec_dec_global_initialize: contextNum: 1 phyInstance: 0
lte_bs_ue_rnti_map_initialize: contextNum: 0 phyInstance: 0
lte_bs_ue_rnti_map_initialize: contextNum: 1 phyInstance: 0
lte_bs_ue_beamforming_initialize: contextNum: 0 phyInstance: 0
lte_bs_ue_beamforming_initialize: contextNum: 1 phyInstance: 0
lte_bs_mac2phy_api_proc_phy_init inst 0 ctx 1

Phy Stats Parser Version 102
----------------------------
PhyStats [Ctx 0]    at: 0x7fea0d2bc040 (size: 24501960 bytes)
Global Variables:
-----------------------------------------------------
gPhyInternalBch:                    1
gUseScatteredTxSduPointers:         1
gUseScatteredRxSduPointers:         0
gMuteRxSduForSrRach:                0
gUseTxSduPointer:                   0
gLowLatencyFlag:                    1
gTAFilt:                            1
gIrcFlagEnabled:                    0
gMmseFlagEnabled:                   0
gUseBatchMessageDeliveryDl:         1
gUseBatchMessageDeliveryUl:         1
gPrachDetectThreshold:              100
gPucchFormat2DetectThreshold:       0
gCarrierAggLevel:                   0
gCarrierAggLevelInit:               1
gSupportedAVX2                      1
-----------------------------------------------------
```

```
PHY_START_REQ: 0
lte_bs_mac2phy_api_proc_phy_start 0
MLogRestart
MLogOpen: filename(l1mlog.bin) mlogSubframes (128), mlogCores(10), mlogSize(3084)
mlog_mask (-1)
MLogTimerInit

PHY>
PHY>        System clock (rdtsc) resolution 2394267510 [Hz]
        Ticks per us 2394
    mlogSubframes (128), mlogCores(10), mlogSize(3084)
 MLOG not opened!!!
MLog Storage: 0x7fea0bad2b20 -> 0x7fea0be9734c
MLogInitializeMlogBuffer
MLogFreqReg: 2394. Storing: 2394
MLogGetResId: Assigning arr 0 to core 6
Mlog Open successful
portId 0 rxQueueId 10 txQueueId 0 pRxPool 0x7fe9bfe44700 pTxPool 0x7fe999522340
FB_VERSION 0x3600

--------- RPE ETHERNET SETUP START ---------

--------- RPE ETHERNET SETUP COMPLETE ---------
loop 0 K0 -84
nco_calc: K0 -84
nco_calc: freq_val 718750
nco_calc: phase_val 100488533 (0x05fd5555)
nco_calc: phase_mod 3774873600 (0xe1000000)
nco_phi_inc from model nco_calc -100488533
[0] UL AGC OFF
[0] Configuring CPRI to REC
[0] Configuring CPRI for 4 antenna
[0] cpriConfig.loopback 0
[0] cpriRfpReSync 0
[0] FDD UL offset on CPRI [basic 63 start 64]
Launched Rx and Tx CPRI threads
mode = 0, count = 0, num_txant/period = 0
Ferry Bridge LTE mode
PHYDI-START[0]: Mode: 0, Count: 4294967295, Period: 0
frb_start: 0

-------------------------------------------------------------------------------
[0] start frb_lte_tx_func
[0] TX ant num: 4
[0] RX ant num: 4
[0] Waiting on CPRI link and first TTI packet from FRB
 - HeapInfo

-----------------------------------------------------------------
String Name                 Start               End           Size
-----------------------------------------------------------------
- pStoredInitParm     (0x00000101fa7540 .. 0x00000101fa75ab}    108
- pStoredInitParm     (0x00000101fb3f40 .. 0x00000101fb3fab}    108
- pStoredInitParm    (0x00000101fb8b40 .. 0x00000101fb8bab}     108
- pStoredInitParm     (0x00000101fc3840 .. 0x00000101fc38ab}    108
- pStoredInitParm     (0x00000101fc9940 .. 0x00000101fc99ab}    108
- pStoredInitParm     (0x00000101fd0640 .. 0x00000101fd06ab}    108
- pStoredInitParm     (0x00000101fef240 .. 0x00000101fef2ab}    108
- pStoredInitParm     (0x00000102016340 .. 0x000001020163ab}    108
- gpBsTxCommonParams  (0x007fea08000900 .. 0x007fea08000e67}   1384
```

```
- gpBsTxDataParams     (0x007fea08000ec0 .. 0x007fea08008177}  29368
- gpBsTxDataParamsMpd (0x007fea080081c0 .. 0x007fea0801686f}  59056
- gpBsTxInitPtrs       (0x007fea080168c0 .. 0x007fea08016917}     88
- gpBsTxControlPtrs    (0x007fea08016980 .. 0x007fea080169ef}    112
- gpBsTxCommonPtrs     (0x007fea08016a40 .. 0x007fea08017a3f}   4096
- gpBsDlCntrl_ParsMal (0x007fea08017a80 .. 0x007fea08019e77}   9208
- pdschRsrMapLocTabPt (0x007fea32d63040 .. 0x007fea32d83d3f} 134400
......
- pAG                  (0x007fea0b92ff40 .. 0x007fea0b93ef3f}  61440
- p_winCodeBlockBits   (0x007fea0b93efc0 .. 0x007fea0b941fbf}  12288
- pRmOut               (0x007fea0fccc040 .. 0x007fea0fd140ff} 295104
- pCodeBlock           (0x007fea0b942000 .. 0x007fea0b95cfff} 110592
- pAG                  (0x007fea0b95d040 .. 0x007fea0b96c03f}  61440
- p_winCodeBlockBits   (0x007fea0b96c080 .. 0x007fea0b96f07f}  12288
- pRmOut               (0x007fea0fc83040 .. 0x007fea0fccb0ff} 295104
- pCodeBlock           (0x007fea0b96f100 .. 0x007fea0b98a0ff} 110592
- pAG                  (0x007fea0b98a140 .. 0x007fea0b99913f}  61440
- p_winCodeBlockBits   (0x007fea0b999180 .. 0x007fea0b99c17f}  12288
- gpActiveRntiMap      (0x007fea04fa3040 .. 0x007fea07fff043} 708484
- gpActiveUeBeamformi (0x007fea0fc2c040 .. 0x007fea0fc82043}
- ApiErrorCheck1       (0x007fea0bac6d80 .. 0x007fea0bac6f3f}    448
- ApiErrorCheck3       (0x007fea0bac6f80 .. 0x007fea0bac70ab}    300
- gpLteBsPhyStats      (0x007fea0d2bc040 .. 0x007fea0ea19f07}  24501960
- pLteBsPhyStatsRntiM (0x007fea0fbe9040 .. 0x007fea0fc2b043} 270340
----------------------------------------------------------------------
                          Total Alloc: 192739482
----------------------------------------------------------------------

----------------------------------------------------------------------

----------------------------------------------------------------------
 mem_mgr_leak_detector_display_size:
        Num Memory Alloc:       11636
        Total Memory Size:  192739482
----------------------------------------------------------------------


MLogGetResId: Assigning arr 1 to core 1
[0][0x1 stat: sfn sync 0 frb status 1 dl_u 0 dl_o 0 ul_o 0](2000 0) [97126918 ms] (min
0 max 0) alloc cnt 1 inv pusch 0
BBU Pooling: enter multicell Activate!
lte rt thread start on 4 core at 232521858359306 at sf=1 with queue 0 successfully
BBU Pooling: active result: Q_id = 0,currenSf = 1, curCellNum = 0, activesfn = 5,
CellNumInActSfn = 1
BBU Pooling: multiCell Activate sucessfully!
lte rt thread start on 2 core at 232521858359064 at sf=1 with queue 0 successfully
lte rt thread start on 3 core at 232521858348242 at sf=1 with queue 0 successfully
MLogGetResId: Assigning arr 2 to core 3
[5]        phy_bbupool_set_final: ERROR: gBbuPoolTtiStart[1][0][2] is not set
MLogGetResId: Assigning arr 3 to core 2
[5]        phy_bbupool_set_final: ERROR: gBbuPoolTtiStart[1][0][1] is not set
[6]        phy_bbupool_set_final: ERROR: gBbuPoolTtiStart[0][0][2] is not set
MLogGetResId: Assigning arr 4 to core 4
[6]        phy_bbupool_set_final: ERROR: gBbuPoolTtiStart[0][0][1] is not set
[0][0x1 stat: sfn sync 0 frb status 1001 dl_u 0 dl_o 0 ul_o 0](2100 0) [1000 ms] (min
973 max 1017) alloc cnt 65 inv pusch 0
```

3.5.4 Radisys eNodeB Application Output Example (Non-CA)

Start of eNodeB with 4x4 RRH with 1Cell non-CA configuration:

```
vm0-skx-wp-cp4:/home/vzakharc/rsys/bundle/q1# ./l2.sh
Setting memory parameters for kernel socket buffers
net.core.rmem_max = 16777216
net.core.rmem_default = 16777216
net.core.wmem_max = 16777216
net.core.wmem_default = 16777216
HugePages_Total:       8
HugePages_Free:        1
HugePages_Rsvd:        0
HugePages_Surp:        0
Hugepagesize:    1048576 kB
kernel.sched_rt_runtime_us = -1
./l2.sh: line 43: /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu1/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu10/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu11/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu12/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu13/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu14/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu15/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu2/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu3/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu4/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu5/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu6/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu7/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu8/cpufreq/scaling_governor: No such file
or directory
./l2.sh: line 43: /sys/devices/system/cpu/cpu9/cpufreq/scaling_governor: No such file
or directory
kernel.shmmax = 2147483648
kernel.shmall = 2147483648
Note: Forwarding request to 'systemctl disable irqbalance.service'.
0001
0001
0001
0001
0001
0001
0001
0001
0001
```

```
0001
0001
0001
start eNodeB
 gWrWlsDeviceName Read as /dev/wls
Read the WLS params from wr_cfg.txt file successfully wls_lib: Open /dev/wls
0xc0085701
wls_lib: User Space Lib Context: us va 0x00007fe09987c000 kernel va 0xffff880064a90000
pa 0x0000000064a90000 size 65536
wls_lib:
Mode 1
wls_lib:
WLS device /dev/wls [8]
wls_lib: hugePageSize on the system is 1073741824
wls_lib: shm open /tmp/phyappshm__dev_wls
wls_lib: Attach to shared memory
wls_lib: pvirtAddr  0x00002aaac0000000
wls_lib: WLS_Alloc: 0x00002aaac0000000 [1031378048]
wls_lib: Connecting to remote peer ...
wls_lib: Remote: pWls_us 0x0x7fe099872000
wls_lib: size wls_us_ctx_t 37544
wls_lib:     ul free  : off 0x0000000000002028
wls_lib:     get_queue: off 0x0000000000006048
wls_lib:     put_queue: off 0x0000000000007860

 *************
 WLS memory: 2aaac0000000, 1027183744
 ******

 *************
 Static memory: 7fe05f000010, 947630080
 ******
Creating thread here ../..//mt/mt_ss.c 4045
mlog start with tick 1995
Rsys memlog initialized

 Num of Tx antenna is  ::2
CNM:nghCellCfg plmnId:102

 CNM Status ::0
DSCP is disabled gWrRtRlcDlMacSchClCore Affinity Read 6
 gWrNrtPdcpDatAppGtpCore Affinity Read 6
 gWrRrcAppS1apCore Affinity Read 6
Read the wr_cfg.txt file successfully Set priority 58
Creating thread here ../..//mt/mt_ss.c 3918

 @@@@ Setting RRC_S1AP Thread affinity [6] @@@@
Set priority 58
Creating thread here ../..//mt/mt_ss.c 3918

 @@@@ Setting EGTP_DAT_APP Thread affinity [6] @@@@
Set priority 90
Creating thread here ../..//mt/mt_ss.c 3918
Creating RT thread ########################

 @@@@ Setting RLC_MACSCH_CL Thread affinity [6] @@@@
Log File:               [dbglog]
Log level:              [(null)]
Module Mask:            [0]
File Size Limit:        [5242880]
```

```
Maximum Log Files:      [3]
Time Zone:              [GMT]
Binary Logging:         [Disabled]
Remote Logging:         [Disabled]
Console Logging:        [Disabled]
Ring Buffer Created with id =2 rSize:5120 eSize:40 15cb220
Ring Buffer Created with id =10 rSize:1024 eSize:8 15cb240

**********MT Task Handler********
PRACH FREQ Offset value is 43

**********MT Task Handler********
m_enCqiPrdcty 6 usUeIndex 0 usCqiCfgIdx  159
 m_enCqiPrdcty 6 usUeIndex 1 usCqiCfgIdx  161
 m_enCqiPrdcty 6 usUeIndex 418 usCqiCfgIdx  195
 m_enCqiPrdcty 6 usUeIndex 419 usCqiCfgIdx  197

[APP] SapProcId 100 inst 1
cellId = 1
 ysCb.numOfCells: 0
cellId = 1
 ysCb.numOfCells: 1

 Server Socket FD =[10]
wrEmmSendSchedEnbCfg:: numTxAntPorts=2   ulSchdType=2    ulPfs.tptCoeffi=0
ulPfs.fairCoeffi=0
MIMO_DBG:: SCH:: numAntPorts=2

dlSchdType 2 ulSchdType 2 dlTptCoeffi 0 dlFairCoeffi 0  ulTptCoeffi 0 ulFairCoeffi 0
CA_DBG:: PUCCH configuration: N2_RB 1 N1_PUCCH 64 deltaShift 1 cyclicShift 0
CRAN DEBUG: ulSpsCell->spsSbStart = 0 ulSpsCell->numSpsSb =31 j= 0

 CRAN : Inside else initMask[0]=0 value=31 maskshift: 32

 CRAN : Inside else initMask[0]=0

 CRAN: initMask[j]=0

 CRAN: initMask[j]=-1

 CRAN: initMask[j]=-1

 CRAN: initMask[j]=-1

msg: qlen: 0001 mlen: 0026   00-->00 region: 00

dat: 60 40 04 03 00 01 00 00 00 1d 50 6a 09 48 10 40 `@........Pj.H.@
     c2 1c 21 9a 84 b0 22 40 00 00                  ..!..."@..
     Before Vendor Params
cellId = 1
 ysCb.numOfCells: 257
CL:MIMO_DBG:: !!!! num Antenna ports =2!!!!

 in ysMsCfgAddCellCfg still able to get cellId =1
Received Phy Init Indication
MIMO_DBG:: cellCb->cellCfg.antennaCfg.antPortsCnt 2Start Log Restriction
starting mem Leak tool

 No vectors prsent in the list...
 No vectors prsent in the list...
```

```
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...Returning from mtTmrHdlr()

 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
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 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
 No vectors prsent in the list...
Time : 30 sec
PDCP Stats: SDUs Dropped = (0),SDUs Queued for SPAcc Cipher = (0), Decipher = (0)
EGTP: SendDropsReason19 = (0)

 ****** CRC(0), PUSCH(0) DL Nacks/Acks:cw0(0/0) cw1(0/0) gPucchDrp0
 ****** Total LateAPI(0), UL Cqi<5(0)


Bucket Memory: region 0
====================================================
Bucket             Number of Blks configured  Size  Allocated
====================================================
 0                500000            256         29        129
 1                 11000            512          0          0
 2                400000           2048          1          5
 3                   256           4096          0          0
 4                  4096          16384        287        294

---------------
Heap Memory: region 0
Heap Size: 6194304
Heap Allocated: 0


Bucket Memory: region 1
```

```
=====================================================
Bucket            Number of Blks configured  Size  Allocated
=====================================================
 0                 500000            128      2703      2704
 1                 500000            256        33        35
 2                 200000           2048       115       121
 3                  40960           4096         6         6
 4                  10240          16384        28        30

---------------
Heap Memory: region 1
Heap Size: 10485760
Heap Allocated: 7368336

Time : 60 sec
PDCP Stats: SDUs Dropped = (0),SDUs Queued for SPAcc Cipher = (0), Decipher = (0)
EGTP: SendDropsReason19 = (0)

 ****** CRC(1), PUSCH(70) DL Nacks/Acks:cw0(0/118) cw1(0/0) gPucchDrp10
 ****** Total LateAPI(0), UL Cqi<5(0)


Bucket Memory: region 0
=====================================================
Bucket  Number of Blks configured  Size  Allocated
=====================================================
 0                 500000            256       354       421
 1                  11000            512         0         0
```

The output may vary depending on the build options, and the scenario started.

3.6 nFAPI Application

The use of nFAPI as the interface between FlexRAN L1 and MAC allows test cases to be run via VNF and PNF network connections.

3.6.1 How to Build

This section provides instructions for building the L1 Application, FAPI, PNF, and VNF functions required to use the nFAPI interface application.

3.6.1.1 Preparation Before Building

1. Set the environment parameters to build the FAPI:
   ```
   export FAPI=true
   ```
2. Run the PHY in timer mode, and set the `TIMER_MODE` environment parameters using:
   ```
   export TIMER_MODE=true
   ```

3.6.1.2 Build the L1 Application

Refer to Section `3.2, L1 (Layer One) Application` to build the L1 Application.

3.6.1.3 Build FAPI

```
cd /home/turner/flexran/fapi
make clean
```

```
make
```

3.6.1.4 Build Dependent Libraries

Install other dependent software libraries to build and run the PNF/VNF. These software libraries include `libxml2`, `lksctp`, and `zlib`.

1. Install `libxml2`:
   a. Download the `libxml2` source code from:
      ```
      ftp://xmlsoft.org/libxml2/libxml2-2.9.7.tar.gz
      ```
   b. Unzip the tar file:
      ```
      tar xf libxml2-2.9.7.tar.gz
      ```
   c. Enter `libxml2` folder:
      ```
      cd libxml2-2.9.7
      ```
   d. Run the following commands to build and install:
      ```
      ./configure, make, make install
      ```
   e. The `libxml2` is installed in the following location by default:
      ```
      /usr/local/ folder
      ```
2. Install the `lksctp`:
   a. Download the `lksctp` library source code from https://nchc.dl.sourceforge.net/project/lksctp/lksctp-tools/lksctp-tools-1.0.17.tar.gz
   b. Unzip the tar file:
      ```
      tar xf lksctp-tools-1.0.17.tar.gz
      ```
   c. Enter `lksctp-tools` folder:
      ```
      cd lksctp-tools-1.0.17
      ```
   d. Run the following commands to build and install `lksctp`:
      ```
      ./configure, make, make install
      ```
   e. The `libsctp` is installed in the following location by default:
      ```
      /usr/local/ folder
      ```
   f. To check if the `sctp` is installed, run the following test:
      ```
      cd src/func_tests, make v4test
      ```
3. Install zlib:
   a. Download the `zlib` library source code from http://www.zlib.net/zlib-1.2.11.tar.gz
   b. Unzip tar file: `tar xf zip-1.2.11.tar.gz`
   c. Enter `zlib` folder: cd zip-1.2.11
   d. Run the following commands to build and install `zlib`:
      ```
      ./configure, make, make install
      ```
   e. by default, `libz` is installed in `/usr/local/ folder`.

3.6.1.5 Apply the patch to PNF Code

1. Download open-nFAPI code from https://github.com/cisco/open-nFAPI.git, check out to commit-id:

```
eda0c42f3d082a6681f05921c07edd4184dbb3cb
```

2. Unzip the open-nFAPI-master.zip file:

```
cd /home/turner/flexran/nfapi/
unzip -q open-nFAPI-master.zip
```

3. Change the folder name from open-nFAPI-master to PNF:

```
cd  /home/turner/flexran/nfapi/
mv open-nFAPI-master pnf
```

4. Copy the patch diff file into the PNF folder:

```
cp /home/turner/flexran/nfapi/patch.diff /home/turner/flexran/nfapi/pnf/
```

5. Run the following command in the PNF folder to generate PNF code:

```
cd /home/turner/flexran/nfapi/pnf
patch -p1 < patch.diff
```

3.6.1.6 Build PNF

The P7 port in the nFAPI uses User Datagram Protocol (UDP) packets to transfer the nFAPI messages between the PNF and VNF. Both the VNF and PNF can be used with the Linux* kernel or DPDK to send/receive UDP packets.

To build the PNF with the Linux kernel to transmit and receive the UDP packets use the following:

```
cd /home/turner/flexran/nfapi/pnf
make clean
make
```

To build the PNF with DPDK to transmit and receive the UDP packets:

```
cd /home/turner/flexran/nfapi/pnf
make clean
make DPDK=1
```

3.6.1.7 Apply the patch to VNF Code

1. Download the open-nFAPI code from https://github.com/cisco/open-nFAPI.git, check out to commit-id:

```
eda0c42f3d082a6681f05921c07edd4184dbb3cb
```

2. Unzip the open-nFAPI-master.zip by using the following:

```
cd /home/turner/flexran/nfapi/
unzip -q open-nFAPI-master.zip
```

3. Change the folder name from open-nFAPI-master to VNF:

```
cd /home/turner/flexran/nfapi/
mv open-nFAPI-master vnf
```

4. Copy the patch diff file into the VNF folder:

```
cp /home/turner/flexran/nfapi/vnf.diff
/home/turner/flexran/nfapi/vnf/
```

5. Run this command in the VNF folder to generate VNF code:

```
cd /home/turner/flexran/nfapi/vnf
patch -p1 < vnf.diff
```

3.6.1.8 Build VNF

To build VNF with Linux kernel to transceive UDP packets:

```
cd /home/turner/flexran/nfapi/vnf
make clean
```

```
make
```

To build VNF with DPDK to transceive UDP packets:

```
cd /home/turner/flexran/nfapi/vnf
make clean
make DPDK=1
```

3.6.2 Test VNF and PNF in PHY Timer Mode

This section describes how to test the VNF and PNF functions with the L1 PHY running in Timer Mode.

3.6.2.1 Prepare for First Run

Add the path of libraries that are needed by VNF/PNF to the Linux OS environment variable `LIBRARY_PATH` so that the Linux OS can automatically find these libraries.

For example, if the SCTP library is located under `/usr/local/lib, add /usr/local/lib` to `LIBRARY_PATH`:

export `LIBRARY_PATH=$LIBRARY_PATH:/usr/local/lib`

3.6.2.2 Run VNF

If the Linux Kernel was used to transmit and receive UDP packets, no options are needed when running the VNF.

Before running the VNF, configure the P7 IP address in the VNF configuration file.

```
cd /home/turner/flexran/nfapi/vnf
./build/vnf_test
```

If the DPDK is used to transmit and receive UDP packets, options for the DPDK are needed when running the VNF.

Before running the VNF, bind one Ethernet port to the DPDK, and configure the P7 IP address, VNF/PNF Ethernet port MAC address in the VNF configuration file vnf.xml:

```
cd /home/turner/flexran/nfapi/vnf
./build/vnf_test <options for DPDK>
```

For example, the command to run the VNF can be:

```
./build/vnf_test -c 0x300 --socket-mem=1024 --file-prefix=pg1
```

3.6.2.3 Run L1APP

Refer to Section 3.5.1, Start L1, to run the L1 application.

3.6.2.4 Run PNF

If the Linux Kernel is used to transmit and receive UDP packets, no options are needed when running the PNF. Before running the PNF, users only need to configure the P7 IP address in the PNF configuration file.

```
cd /home/turner/flexran/nfapi/pnf
./build/pnf_phy
```

If using the DPDK to transmit and receive UDP packets, options for the DPDK are needed when running the PNF. Users should bind one Ethernet port to the DPDK, and configure the P7 IP address, VNF/PNF Ethernet port MAC address in the PNF configuration file `pnf.xml`.

```
cd /home/turner/flexran/nfapi/pnf
./build/pnf_phy <options for DPDK>
```

For example, the command to run the PNF can be:

```
/build/pnf_phy -c 0x300 --socket-mem=1024 --file-prefix=pg1
```

3.6.3 VNF and PNF Setup Configuration

The location of the VNF configuration file is in the vnf.xml folder, and the PNF configuration is in the pnf.xml folder.

These two configuration files will be read by the VNF and PNF, respectively. Users should make sure they are appropriately configured.

§

4.0 FlexRAN Setup Configuration

This section gives examples of FlexRAN configurations for supported end-to-end scenarios.

Details are provided for hardware (Ferry Bridge) setup, L1 configuration (phycfg.xml), and eNodeB L2 configuration (wr_cfg.txt) for the supported scenarios.

4.1 FlexRAN Supported Scenarios

The six primary system configurations that have been verified and are supported are provided below:

- 1 cell FDD non-CA: TM500 with 400 connected UEs and 256 UEs with full-duplex traffic
- 1 cell TDD non-CA: TM500 with 64 connected UEs and 64 UEs with full-duplex traffic
- 1 cell FDD CA: TM500 with 400 connected UEs and 256 UEs with full-duplex traffic
- 1 cell TDD CA: TM500 with 64 connected UEs and 64 UEs with full-duplex traffic
- 1 cell FDD 4x2 MIMO: TM500 with 400 connected UEs and 256 UEs with full-duplex traffic
- 1 cell FDD non-CA: 2 Commercial UEs connected and running arbitrary DL and UL traffic.

Other scenarios are outside of the scope of this User Guide and are not supported. More information on features and limitations can be found in the *FlexRAN Reference Solution Software Release Notes, refer to Reference Documents* and Resources, Table 2.

Different scenarios require changes in the connection of the different RRHs and the corresponding RF cables, as well as the use of the correct Ferry Bridge FPGA (Field Programmable Gate Array) image.

The Non-CA Cell scenario requires 2x2 RRH. The corresponding image for the Ferry Bridge FPGA must be programmed.

The CA and 4x4 MIMO Cell scenarios require a 4x4 RRH. The corresponding image for the Ferry Bridge FPGA must be programmed.

The 4x4 RRH can also be used for a Non-CA Cell scenario. In this case, Radio 0 of the 4x4 RRH acts as a 2x2 radio. The 4x4 RRH always requires the corresponding 4x4 Ferry Bridge FPGA image.

4.2 Ferry Bridge

To set up the Ferry Bridge, use the following steps:

1. Connect the Ethernet cable to the 10 Gbps physical NIC on the Wolf Pass dedicated to the eNodeB application.
2. Connect the Common Public Radio Interface (CPRI) port to the RRH.
   a. 4x4 RRH CPRI port is on the back panel.
   b. 2x2 RRH CPRI port is on the front panel marked as SFP1.
3. Program the FPGA image according to the instructions provided in Appendix A.2, Updating FPGA Image.
   a. For 2x2 RRH, use image fbr_fpga_wrap_2x2_rec_rec.jic
   b. For 4x4 RRH, use image fbr_fpga_wrap_4x4_rec_rec.jic

Figure 6. Ferry Bridge Port Connections

4.3 eNodeB

Configure the eNodeB configuration using the wr_cfg.txt file provided as part of the Radisys* package for the L2 Application.

Below is an example of a working configuration for the TM500 setup. Based on this configuration, the user can change the IP address of the Evolved Packet Core* (EPC*) (MME) and the eNodeB according to the network environment as well as the LTE RF Band being used.

4.3.1 PHY Configurations (phycfg.xml)

Two PHY configurations are supported, depending on the antenna used.

4.3.1.1 2x2 RRH and 2x2 Ferry Bridge Image

```
...
<Radio>
        <!-- Enable/disable radio                [0 - disable (external app control
radio), 1 - use Lib-Radio, 2 - use phy app (obsolete)] -->
        <radioEnable>1</radioEnable>
        <!--  DPDK memory size allocated from hugepages [MB]  [default: 2048] -->
        <dpdkMemorySize>6144</dpdkMemorySize>
        <!--  DPDK Interrupt mode enable         [0 - disabled, PMD is used, 1 -
enabled, uio irq is used] -->
        <dpdkIrqMode>0</dpdkIrqMode>
        <!--  Ferry Bridge (FB) mode             [0 - LTE MODE, 1 - CPRI BYPASS MODE] -
->
        <ferryBridgeMode>0</ferryBridgeMode>
        <!--  Number of Ethernet ports on FB     [0 - DPDK port 0, 1 - DPDK port 1, 2 -
both DPDK port 0 and port 1 (CA mode with two ETH)] -->
        <ferryBridgeEthPort>1</ferryBridgeEthPort>
```

```
        <!--  FB Synchronized CPRI ports        [0 - no reSync REC & RE FPGA, 1 -
reSync REC & REC FPGA] -->
        <ferryBridgeSyncPorts>0</ferryBridgeSyncPorts>
        <!--  FB Loopback Mode                  [0 - no optical loopback connected
REC<->RE, 1 - optical loopback connected REC<->RE] -->
        <ferryBridgeOptCableLoopback>0</ferryBridgeOptCableLoopback>

        <!--  Radio Config 0 -->
        <RadioConfig0>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg0PCIeEthDev>0000:00:04.0</radioCfg0PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg0DpdkRx>1</radioCfg0DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg0DpdkTx>2</radioCfg0DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg0TxAnt>2</radioCfg0TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg0RxAnt>2</radioCfg0RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg0RxAgc>0</radioCfg0RxAgc>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg0NumCell>1</radioCfg0NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg0Cell0PhyId>0</radioCfg0Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg0Cell1PhyId>1</radioCfg0Cell1PhyId>
        </RadioConfig0>
...
```

4.3.1.2 4x4 RRH and 4x4 Ferry Bridge Image

```
...
<Radio>
        <!-- Enable/disable radio              [0 - disable (external app control
radio), 1 - use Lib-Radio, 2 - use phy app (obsolete)] -->
        <radioEnable>1</radioEnable>
        <!--  DPDK memory size allocated from hugepages [MB]  [default: 2048] -->
        <dpdkMemorySize>6144</dpdkMemorySize>
        <!--  DPDK Interrupt mode enable        [0 - disabled, PMD is used, 1 -
enabled, uio irq is used] -->
        <dpdkIrqMode>0</dpdkIrqMode>
        <!--  Ferry Bridge (FB) mode            [0 - LTE MODE, 1 - CPRI BYPASS MODE] -
->
        <ferryBridgeMode>0</ferryBridgeMode>
        <!--  Number of Ethernet ports on FB    [0 - DPDK port 0, 1 - DPDK port 1, 2 -
both DPDK port 0 and port 1 (CA mode with two ETH)] -->
        <ferryBridgeEthPort>1</ferryBridgeEthPort>
        <!--  FB Synchronized CPRI ports        [0 - no reSync REC & RE FPGA, 1 -
reSync REC & REC FPGA] -->
        <ferryBridgeSyncPorts>0</ferryBridgeSyncPorts>
        <!--  FB Loopback Mode                  [0 - no optical loopback connected
REC<->RE, 1 - optical loopback connected REC<->RE] -->
        <ferryBridgeOptCableLoopback>0</ferryBridgeOptCableLoopback>

        <!--  Radio Config 0 -->
```

```
        <RadioConfig0>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg0PCIeEthDev>0000:00:04.0</radioCfg0PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg0DpdkRx>1</radioCfg0DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg0DpdkTx>2</radioCfg0DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg0TxAnt>4</radioCfg0TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg0RxAnt>4</radioCfg0RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg0RxAgc>0</radioCfg0RxAgc>
            <!--  Number of cells running on this port [1 - Cell , 2 - Cells ] -->
            <radioCfg0NumCell>1</radioCfg0NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg0Cell0PhyId>0</radioCfg0Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg0Cell1PhyId>1</radioCfg0Cell1PhyId>
        </RadioConfig0>
...
```

Refer to Reference Documents and Resources, Table 2, FlexRAN Reference Solution L1 XML Configuration User Guide for detailed explanations of all the phycfg.xml parameters.

4.3.2 1 Cell Non-CA LTE FDD Band 7 (OTA – Over-the-Air)

```
WR_TAG_NOS_OF_CELLS          = 1
WR_TAG_CELL_ID               = {1,2}
WR_TAG_OP_MODE               = 0
WR_TAG_PERIOD                = 0
WR_TAG_DUP_MODE              = 1
WR_TAG_TDD_ULDL_CFG_MODE     = 2
WR_TAG_TDD_SPCL_SF_CONFIG    = 7
WR_TAG_MAX_UE_SUPPORT        = 420
WR_TAG_MCC_0                 = 0
WR_TAG_MCC_1                 = 0
WR_TAG_MCC_2                 = 1
WR_TAG_MNC_0                 = 0
WR_TAG_MNC_1                 = 1
WR_TAG_MNC_2                 = -1
WR_TAG_TA_CODE               = {1,1}
WR_TAG_FREQ_BAND_IND         = {7,4}
WR_TAG_DL_EARFCN             = {3100,2175}
WR_TAG_UL_EARFCN             = {21100,20175}
WR_TAG_ENB_IP_ADDR           = 10.233.182.23
WR_TAG_PCI_SELECT_TYPE       = 0
WR_TAG_PRACH_SELECT_TYPE     = 1
WR_TAG_EARFCN_SELECT_TYPE    = 1
WR_TAG_PCI_LIST              = {1,2,35,36}
WR_TAG_DL_EARFCN_LIST        = {3100,2175}
WR_TAG_UL_EARFCN_LIST        = {21100,20175}
WR_TAG_ROOTSEQ_IDX_LIST      = {{22,10}}
WR_TAG_PRACHCFG_IDX_LIST     = {{8,8}}
WR_TAG_ZERO_CORR_ZONE_CFG_LIST    = {{5,5}}
WR_TAG_PRACH_FREQ_OFFSET_LIST     = {{43,43}}
```

```
WR_TAG_ROOTSEQ_IDX          = 22
WR_TAG_ZERO_CORR_ZONE_CFG   = 10
WR_TAG_PRACH_FREQ_OFFSET    = 3
WR_TAG_NO_OF_MME_INFO       = 1
WR_TAG_MME_INFO             = {{1,1,10.233.180.65}}
WR_TAG_SCTP_IP_ADDR         = 10.233.182.23
WR_TAG_HI_DBG               = 0
WR_TAG_SB_DBG               = 0
WR_TAG_SZ_DBG               = 0
WR_TAG_EG_DBG               = 0
WR_TAG_WR_DBG               = 1
WR_TAG_NH_DBG               = 0
WR_TAG_KW_DBG               = 0
WR_TAG_RG_DBG               = 0
WR_TAG_YS_DBG               = 0
WR_TAG_SM_DBG               = 0
WR_TAG_INACTIVITY_TIMER_VAL = 3000000
WR_TAG_END_MARKER_TIMER_VAL = 200
WR_TAG_MAX_EXPIRY           = 30
WR_TAG_CZ_DBG               = 0
WR_TAG_X2_PREP_TMR          = 5000
WR_TAG_X2_OVRALL_TMR        = 10000
WR_TAG_NO_OF_BRDCST_PLMN    = 1
WR_TAG_PLMN_ID_LST          = {00101}
WR_TAG_NO_OF_NGH_INFO       = INVLD
WR_TAG_NGH_INFO_CFG         = INVLD
WR_TAG_NO_OF_GU_GRP         = 1
WR_TAG_NUM_TX_ANTENNA       = 2
WR_TAG_S1_PREP_TMR          = 5000
WR_TAG_S1_OVRALL_TMR        = 10000
WR_TAG_MEAS_CFG_ENB         = 1
WR_TAG_RRM_RNTI_STRT        = {205,205}
WR_TAG_MAX_RRM_RNTIS        = {420,420}
WR_TAG_MAC_RNTI_STRT        = {61,511}
WR_TAG_MAX_MAC_RNTIS        = {420,420}
WR_TAG_RRM_NO_OF_DED_PREMBL = {10,10}
WR_TAG_RRM_DED_PREMBL_STRT  = {41,41}
WR_TAG_MAC_NO_OF_PREMBL     = {6,6}
WR_TAG_A1_RSRP_THRSHLD_VAL  = 90
WR_TAG_A2_RSRP_THRSHLD_VAL  = 6
WR_TAG_INTRA_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTRA_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTER_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTER_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTRA_HO_A3_OFFSET = 10
WR_TAG_INTRA_ANR_A3_OFFSET = 5
WR_TAG_INTER_ANR_A5_RSRP_THRSD1_VAL = 75
WR_TAG_INTER_ANR_A5_RSRP_THRSD2_VAL = 50
WR_TAG_ANR_REPORT_CFG_VAL = 0
WR_TAG_HO_REPORT_CFG_VAL = 1
WR_TAG_ANR_EPOC_TMR_VAL_IN_SECS = 1000
WR_TAG_ANR_TRICE_INTV_COUNT = 10
WR_TAG_UTRA_B2_RSRP_THRSD1_VAL = 70
WR_TAG_UTRA_FDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_UTRA_TDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_S_MEASURE_VAL        = 0
WR_TAG_INTRA_TTT_VAL        = 7
WR_TAG_INTRA_HYTERISIS      = 1
WR_TAG_NO_OF_NGH_ENB_CFG    = INVLD
WR_TAG_NGH_ENB_CFG          = INVLD
```

```
WR_TAG_PCI_VAL                = {1,2}
WR_TAG_DL_NUM_UE_PER_TTI      = 8
WR_TAG_UL_NUM_UE_PER_TTI      = 8
WR_TAG_MAX_DL_UE_PER_TTI      = 8
WR_TAG_MAX_UL_UE_PER_TTI      = 8
WR_TAG_DL_SCHD_TYPE           = 1
WR_TAG_UL_SCHD_TYPE           = 1
WR_TAG_DLFS_SCHD_TYPE         = 0
WR_TAG_PFS_DL_TPT_COEFFICIENT  = 10
WR_TAG_PFS_DL_FAIRNESS_COEFFICIENT = 10
WR_TAG_PFS_UL_TPT_COEFFICIENT  = 10
WR_TAG_PFS_UL_FAIRNESS_COEFFICIENT = 10
WR_TAG_DL_QCI_SCHD_WGT        = {8,6,7,5,9,4,3,2,1}
WR_TAG_UL_QCI_SCHD_WGT        = {8,6,7,5,9,4,3,2,1}
WR_TAG_TM_AUTO_CONFIG         = 0
WR_TAG_PREFERRED_TM           = 3
WR_TAG_MAX_X2_PEERS           = 5
WR_TAG_X2_TIME_TO_WAIT        = 200000
WR_TAG_SCTP_SRVC_TYPE         = 0
WR_TAG_DIAG_TUCL              = {{0,10}}
WR_TAG_DIAG_S1AP              = {{0,10}}
WR_TAG_DIAG_EGTP              = {{0,10}}
WR_TAG_DIAG_APP               = {{0,10}}
WR_TAG_DIAG_LTERRC            = {{0,10}}
WR_TAG_DIAG_LTERLC            = {{0,10}}
WR_TAG_DIAG_LTEPDCP           = {{0,10}}
WR_TAG_DIAG_LTECL             = {{0,10}}
WR_TAG_DIAG_LTEMAC            = {{0,10}}
WR_TAG_DIAG_X2AP              = {{0,10}}
WR_TAG_DIAG_SCTP              = {{0,10}}
WR_TAG_SCTP_RTO_MIN           = 100
WR_TAG_SCTP_RTO_MAX           = 1000
WR_TAG_SCTP_RTO_INITIAL       = 200
WR_TAG_SCTP_HRTBEAT_INTERVAL = 5000
WR_TAG_UL_ENABLE_TIME         = 1
WR_TAG_NUM_EUTRA_FREQ         = {2,2}
WR_TAG_EUTRA_FREQ_CFG         = {{3100,21100},{2175,20175},{3100,21100},{2175,20175}}
WR_TAG_NUM_UTRA_FDD_FREQ      = {1,1}
WR_TAG_UTRA_FDD_FREQ_CFG      = {{10713,23230},{10714,23231}}
WR_TAG_NUM_UTRA_TDD_FREQ      = {1,1}
WR_TAG_UTRA_TDD_FREQ_CFG      = {{10054,0,1},{9654,0,2}}
WR_TAG_CSG_SMCELL_PCI_START = 1
WR_TAG_CSG_SMCELL_PCI_RANGE = 100
WR_TAG_NO_OF_NGH_CFG          = {1,1}
WR_TAG_NGH_CELL_CFG           =
{{10.188.6.26,8,1,8,00102,3100,21100,0,1,0,2,2,7,0,0,60,40},{10.188.6.28,9,2,9,00102,2
175,20175,0,1,0,2,2,7,0,0,60,40}}
WR_TAG_NO_OF_UTRA_FDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_FDD_CELL_CFG     =
{{10,70,10713,23230,6,1,21901,145,45,0,1,1},{20,71,10714,23231,10,1,21901,150,50,0,1,1
}}
WR_TAG_NO_OF_UTRA_TDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_TDD_CELL_CFG     =
{{30,80,10054,145,100,60,1,21901,45,0},{40,81,9654,150,100,61,1,21901,50,0}}
WR_TAG_NUM_CDMA_1XRTT_BAND_CLS = {1,1}
WR_TAG_CDMA_1XRTT_BAND_CLS     = {{1,1,1,1},{1,1,1,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_FREQ = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_FREQ     = {{1,1000,1},{1,1000,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_CELL = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_CELL     = {{1,1000,1,1,1},{1,1000,1,1,1}}
```

```
WR_TAG_CSFB_UTRA_CFG_VAL          = 0
WR_TAG_CSFB_CDMA_CFG_VAL          = 0
WR_TAG_ECSFB_CFG_VAL          = 0
WR_TAG_DUAL_RX_SUPPORTED      = 1
WR_TAG_DUAL_RX_TX_SUPPORTED = 0
WR_TAG_AS_PRI_INTG_ALGO_LST = {1}
WR_TAG_AS_PRI_CIPH_ALGO_LST = {1}
WR_TAG_ABS_A3_OFFSET          = -6
WR_TAG_PICO_OFFSET            = 20
WR_TAG_ABS_PATTERN_TYPE       = 2
WR_TAG_ABS_PATTERN            = 01010101010101010101010101010101010101010101
WR_TAG_ABS_LOAD_PERIODICITY = 0
WR_TAG_SFR_START_RB           = 25
WR_TAG_SFR_END_RB             = 49
WR_TAG_SFR_POWER_LOW          = 4
WR_TAG_SFR_POWER_HIGH         = 5
WR_TAG_DRX_ENABLED            = 0
WR_TAG_DRX_INACTIVITY_TMR     = 10
WR_TAG_DRX_RETX_TMR           = 1
WR_TAG_DRX_LONG_CYCLE_GBR     = 1
WR_TAG_DRX_LONG_CYCLE_NON_GBR = 5
WR_TAG_ANR_DRX_LONG_CYCLE     = 11
WR_TAG_ANR_DRX_ON_DURATION_TMR = 7
WR_TAG_ANR_DRX_INACTIVITY_TMR = 8
WR_TAG_DEFAULT_PAGING_CYCLE = 0
WR_TAG_DEFAULT_PCCH_CFG_NB  = 7
WR_TAG_BANDWIDTH              = {20,20}
WR_TAG_BOOT_MODE              = 0
WR_TAG_PWS_ETWS_CMAS_CNTRL = 0
WR_TAG_WATCHDOG_SOFT_LIMIT  = 5
WR_TAG_WATCHDOG_HARD_LIMIT  = 15
WR_TAG_LOG_PATH               = /var/log
WR_TAG_LOG_FILE               = dbglog
WR_TAG_LOG_MAX_FILES          = 3
WR_TAG_LOG_FILESIZE_LIMIT     = 5
WR_TAG_LOG_LEVEL              = 0
WR_TAG_LOG_MASK               = 0
WR_TAG_LOG_PORT               = 9999
WR_TAG_LOG_REMOTE_LOGGING     = 1
WR_TAG_LOG_CIRBUF_SIZE        = 3000
WR_TAG_LOG_COREDUMP_FLAG      = 1
WR_TAG_INT_FREQ_MEAS_GAP      = 0
WR_TAG_ANR_MEAS_GAP_CONFIG    = 0
WR_TAG_SRC_HO_CANCEL_TMR      = 40000
WR_TAG_CNM_ENABLED            = 0
WR_TAG_TA_TMR_CMN             = 7
WR_TAG_TA_TMR_DED             = 7
WR_TAG_GRP_PUCCH_PWR_CTRL_ENABLE = 0
WR_TAG_GRP_PUSCH_PWR_CTRL_ENABLE = 0
WR_TAG_RRM_SR_PRDCTY          = {4,4}
WR_TAG_RRM_CQI_PRDCTY         = {6,6}
WR_TAG_RRM_NUM_SR_PER_TTI     = {8,8}
WR_TAG_RRM_NUM_CQI_PER_TTI    = {8,8}
WR_TAG_RRM_N1_PUCCH           = {18,18}
WR_TAG_LTE_PUCCH_PWR_FMT3A_ENABLE = 0
WR_TAG_LTE_PUSCH_PWR_FMT3A_ENABLE = 0
WR_TAG_DRX_QCI_SUPPORT_ENABLED = 0
WR_TAG_SPS_ENABLE_FLAG        = 0
WR_TAG_DL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_UL_NUM_SPS_UE_PER_TTI = 1
```

```
WR_TAG_MAX_SPS_RB            = 10
WR_TAG_DSCP_ENABLE           = 0
WR_TAG_QCI_DSCP_MAP          = {152,120,104,72,180,44,12,4,4}
WR_TAG_CSG_CSG_ID            = 1234567
WR_TAG_CSG_ACCESS_MODE       = 1
WR_TAG_CSG_CSG_PCI_START     = 1
WR_TAG_CSG_CSG_PCI_RANGE     = 5
WR_TAG_CSG_HENB_NAME         = "RADISYS"
WR_TAG_MAX_AVG_GBRPRB_USAGE = 99
WR_TAG_DCFI_ENABLE           = 0
WR_TAG_CFI                   = 1
WR_TAG_RIM_CFG               = {86400000,5000,5000,5000,2}
WR_TAG_NUM_GERAN_NEIGH_FREQ = {0,0}
WR_TAG_GERAN_NEIGH_FREQ      = INVLD
WR_TAG_NUM_GERAN_NEIGH_CELL = {0,0}
WR_TAG_GERAN_NEIGH_CELL      = INVLD
WR_TAG_GERAN_MEAS_CFG        = INVLD
WR_TAG_CELL_SIZE_TYPE        = 0
WR_TAG_ARP_EMER_SERV         = 1
WR_TAG_GERAN_B2_RED_RSRP_THRSD1_VAL = 70
WR_TAG_GERAN_B2_RED_THRSD2_VAL    = 40
WR_TAG_GERAN_B2_HO_RSRP_THRSD1_VAL = 60
WR_TAG_GERAN_B2_HO_THRSD2_VAL    = 30
WR_TAG_WIRESHARK_PORT        = 9999
WR_TAG_WIRESHARK_DST_IP_ADDR = 192.168.1.10
WR_TAG_ANR_CELL_VALID_AGE_VAL = 0
WR_TAG_ENABLE_CA             = 0
WR_TAG_CELL_FREQ_CONTIGUOUS = 0
WR_TAG_TENB_STATS            = {1,0,1,50,8989}
WR_TAG_A4_RSRP_THRSHLD_VAL   = 60
WR_TAG_MEAS_SCELL_ADD_REL    = 0
WR_TAG_RT_MAC_SCH_CL_THRD_CORE = 6
WR_TAG_NRT_PDCP_GTP_THRD_CORE = 6
WR_TAG_RRC_APP_S1AP_THRD_CORE = 6
WR_TAG_WLS_DEVICE_NAME = /dev/wls
CFGEND                       = 1
#This CFGEND has to be kept at the end and should not be moved as the configuration
#parameter reading ends once we read this tag. Any new configuration tag MUST be
#added above CFGEND
```

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```
WR_TAG_NOS_OF_CELLS          = 1
WR_TAG_CELL_ID               = {1,2}
WR_TAG_OP_MODE               = 0
WR_TAG_PERIOD                = 0
WR_TAG_DUP_MODE              = 2
WR_TAG_TDD_ULDL_CFG_MODE     = 2
WR_TAG_TDD_SPCL_SF_CONFIG    = 7
WR_TAG_MAX_UE_SUPPORT        = 64
WR_TAG_MCC_0                 = 0
WR_TAG_MCC_1                 = 0
WR_TAG_MCC_2                 = 1
WR_TAG_MNC_0                 = 0
WR_TAG_MNC_1                 = 1
WR_TAG_MNC_2                 = -1
WR_TAG_TA_CODE               = {1,1}
WR_TAG_FREQ_BAND_IND         = {40,40}
WR_TAG_DL_EARFCN             = {38750,38948}
```

```
WR_TAG_UL_EARFCN            = {38750,38948}
WR_TAG_ENB_IP_ADDR          = 10.233.182.23
WR_TAG_PCI_SELECT_TYPE      = 0
WR_TAG_PRACH_SELECT_TYPE    = 1
WR_TAG_EARFCN_SELECT_TYPE   = 1
WR_TAG_PCI_LIST             = {1,2,35,36}
WR_TAG_DL_EARFCN_LIST       = {38750,38948}
WR_TAG_UL_EARFCN_LIST       = {38750,38948}
WR_TAG_ROOTSEQ_IDX_LIST     = {{823,10,18}}
WR_TAG_PRACHCFG_IDX_LIST    = {{1,1,48}}
WR_TAG_ZERO_CORR_ZONE_CFG_LIST    = {{8,10,14}}
WR_TAG_PRACH_FREQ_OFFSET_LIST     = {{43,43}}
WR_TAG_ROOTSEQ_IDX          = 823
WR_TAG_ZERO_CORR_ZONE_CFG   = 10
WR_TAG_PRACH_FREQ_OFFSET    = 1
WR_TAG_NO_OF_MME_INFO       = 1
WR_TAG_MME_INFO             = {{1,1,10.233.180.160}}
WR_TAG_SCTP_IP_ADDR         = 10.233.182.23
WR_TAG_HI_DBG               = 0
WR_TAG_SB_DBG               = 0
WR_TAG_SZ_DBG               = 0
WR_TAG_EG_DBG               = 0
WR_TAG_WR_DBG               = 1
WR_TAG_NH_DBG               = 0
WR_TAG_KW_DBG               = 0
WR_TAG_RG_DBG               = 0
WR_TAG_YS_DBG               = 0
WR_TAG_SM_DBG               = 0
WR_TAG_INACTIVITY_TIMER_VAL = 3000000
WR_TAG_END_MARKER_TIMER_VAL = 200
WR_TAG_MAX_EXPIRY           = 30
WR_TAG_CZ_DBG               = 0
WR_TAG_X2_PREP_TMR          = 5000
WR_TAG_X2_OVRALL_TMR        = 10000
WR_TAG_NO_OF_BRDCST_PLMN    = 1
WR_TAG_PLMN_ID_LST          = {00101}
WR_TAG_NO_OF_NGH_INFO       = INVLD
WR_TAG_NGH_INFO_CFG         = INVLD
WR_TAG_NO_OF_GU_GRP         = 1
WR_TAG_NUM_TX_ANTENNA       = 2
WR_TAG_S1_PREP_TMR          = 5000
WR_TAG_S1_OVRALL_TMR        = 10000
WR_TAG_MEAS_CFG_ENB         = 1
WR_TAG_RRM_RNTI_STRT        = {205,205}
WR_TAG_MAX_RRM_RNTIS        = {32,32}
WR_TAG_MAC_RNTI_STRT        = {61,128}
WR_TAG_MAX_MAC_RNTIS        = {96,165}
WR_TAG_RRM_NO_OF_DED_PREMBL = {10,10}
WR_TAG_RRM_DED_PREMBL_STRT  = {41,41}
WR_TAG_MAC_NO_OF_PREMBL     = {6,6}
WR_TAG_A1_RSRP_THRSHLD_VAL  = 90
WR_TAG_A2_RSRP_THRSHLD_VAL  = 6
WR_TAG_INTRA_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTRA_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTER_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTER_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTRA_HO_A3_OFFSET = 10
WR_TAG_INTRA_ANR_A3_OFFSET = 5
WR_TAG_INTER_ANR_A5_RSRP_THRSD1_VAL = 75
WR_TAG_INTER_ANR_A5_RSRP_THRSD2_VAL = 50
```

```
WR_TAG_ANR_REPORT_CFG_VAL = 0
WR_TAG_HO_REPORT_CFG_VAL = 1
WR_TAG_ANR_EPOC_TMR_VAL_IN_SECS = 1000
WR_TAG_ANR_TRICE_INTV_COUNT = 10
WR_TAG_UTRA_B2_RSRP_THRSD1_VAL = 70
WR_TAG_UTRA_FDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_UTRA_TDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_S_MEASURE_VAL         = 0
WR_TAG_INTRA_TTT_VAL         = 7
WR_TAG_INTRA_HYTERISIS       = 1
WR_TAG_NO_OF_NGH_ENB_CFG     = INVLD
WR_TAG_NGH_ENB_CFG           = INVLD
WR_TAG_PCI_VAL               = {1,2}
WR_TAG_DL_NUM_UE_PER_TTI     = 8
WR_TAG_UL_NUM_UE_PER_TTI     = 8
WR_TAG_MAX_DL_UE_PER_TTI     = 8
WR_TAG_MAX_UL_UE_PER_TTI     = 8
WR_TAG_DL_SCHD_TYPE          = 2
WR_TAG_UL_SCHD_TYPE          = 2
WR_TAG_DLFS_SCHD_TYPE        = 0
WR_TAG_PFS_DL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_DL_FAIRNESS_COEFFICIENT = 0
WR_TAG_PFS_UL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_UL_FAIRNESS_COEFFICIENT = 0
WR_TAG_DL_QCI_SCHD_WGT       = {8,6,7,5,9,4,3,2,1}
WR_TAG_UL_QCI_SCHD_WGT       = {8,6,7,5,9,4,3,2,1}
WR_TAG_TM_AUTO_CONFIG        = 0
WR_TAG_PREFERRED_TM          = 3
WR_TAG_MAX_X2_PEERS          = 5
WR_TAG_X2_TIME_TO_WAIT       = 200000
WR_TAG_SCTP_SRVC_TYPE        = 0
WR_TAG_DIAG_TUCL             = {{0,10}}
WR_TAG_DIAG_S1AP             = {{0,10}}
WR_TAG_DIAG_EGTP             = {{0,10}}
WR_TAG_DIAG_APP              = {{0,10}}
WR_TAG_DIAG_LTERRC           = {{0,10}}
WR_TAG_DIAG_LTERLC           = {{0,10}}
WR_TAG_DIAG_LTEPDCP          = {{0,10}}
WR_TAG_DIAG_LTECL            = {{0,10}}
WR_TAG_DIAG_LTEMAC           = {{0,10}}
WR_TAG_DIAG_X2AP             = {{0,10}}
WR_TAG_DIAG_SCTP             = {{0,10}}
WR_TAG_SCTP_RTO_MIN          = 100
WR_TAG_SCTP_RTO_MAX          = 1000
WR_TAG_SCTP_RTO_INITIAL      = 200
WR_TAG_SCTP_HRTBEAT_INTERVAL = 5000
WR_TAG_UL_ENABLE_TIME        = 1
WR_TAG_NUM_EUTRA_FREQ        = {2,2}
WR_TAG_EUTRA_FREQ_CFG        =
{{38750,38750},{38948,38948},{38750,38750},{38948,38948}}
WR_TAG_NUM_UTRA_FDD_FREQ     = {1,1}
WR_TAG_UTRA_FDD_FREQ_CFG     = {{10713,23230},{10714,23231}}
WR_TAG_NUM_UTRA_TDD_FREQ     = {1,1}
WR_TAG_UTRA_TDD_FREQ_CFG     = {{10054,0,1},{9654,0,2}}
WR_TAG_CSG_SMCELL_PCI_START = 1
WR_TAG_CSG_SMCELL_PCI_RANGE = 100
WR_TAG_NO_OF_NGH_CFG         = {1,1}
WR_TAG_NGH_CELL_CFG          =
{{10.188.6.26,8,1,8,00102,38750,18900,0,1,0,2,2,7,0,0,60,40},{10.188.6.28,9,2,9,00102,
2175,20175,0,1,0,2,2,7,0,0,60,40}}
```

```
WR_TAG_NO_OF_UTRA_FDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_FDD_CELL_CFG     =
{{10,70,10713,23230,6,1,21901,145,45,0,1,1},{20,71,10714,23231,10,1,21901,150,50,0,1,1
}}
WR_TAG_NO_OF_UTRA_TDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_TDD_CELL_CFG     =
{{30,80,10054,145,100,60,1,21901,45,0},{40,81,9654,150,100,61,1,21901,50,0}}
WR_TAG_NUM_CDMA_1XRTT_BAND_CLS = {1,1}
WR_TAG_CDMA_1XRTT_BAND_CLS     = {{1,1,1,1},{1,1,1,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_FREQ = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_FREQ     = {{1,1000,1},{1,1000,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_CELL = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_CELL     = {{1,1000,1,1,1},{1,1000,1,1,1}}
WR_TAG_CSFB_UTRA_CFG_VAL         = 0
WR_TAG_CSFB_CDMA_CFG_VAL         = 0
WR_TAG_ECSFB_CFG_VAL          = 0
WR_TAG_DUAL_RX_SUPPORTED      = 1
WR_TAG_DUAL_RX_TX_SUPPORTED = 0
WR_TAG_AS_PRI_INTG_ALGO_LST = {1}
WR_TAG_AS_PRI_CIPH_ALGO_LST = {1}
WR_TAG_ABS_A3_OFFSET          = -6
WR_TAG_PICO_OFFSET            = 20
WR_TAG_ABS_PATTERN_TYPE       = 2
WR_TAG_ABS_PATTERN            = 01010101010101010101010101010101010101010101
WR_TAG_ABS_LOAD_PERIODICITY = 0
WR_TAG_SFR_START_RB           = 25
WR_TAG_SFR_END_RB             = 49
WR_TAG_SFR_POWER_LOW          = 4
WR_TAG_SFR_POWER_HIGH         = 5
WR_TAG_DRX_ENABLED            = 0
WR_TAG_DRX_INACTIVITY_TMR     = 10
WR_TAG_DRX_RETX_TMR           = 1
WR_TAG_DRX_LONG_CYCLE_GBR     = 1
WR_TAG_DRX_LONG_CYCLE_NON_GBR = 5
WR_TAG_ANR_DRX_LONG_CYCLE     = 11
WR_TAG_ANR_DRX_ON_DURATION_TMR = 7
WR_TAG_ANR_DRX_INACTIVITY_TMR = 8
WR_TAG_DEFAULT_PAGING_CYCLE = 0
WR_TAG_DEFAULT_PCCH_CFG_NB  = 7
WR_TAG_BANDWIDTH              = {20,20}
WR_TAG_BOOT_MODE              = 0
WR_TAG_PWS_ETWS_CMAS_CNTRL = 0
WR_TAG_WATCHDOG_SOFT_LIMIT  = 5
WR_TAG_WATCHDOG_HARD_LIMIT  = 15
WR_TAG_LOG_PATH               = /var/log
WR_TAG_LOG_FILE               = dbglog
WR_TAG_LOG_MAX_FILES          = 3
WR_TAG_LOG_FILESIZE_LIMIT     = 5
WR_TAG_LOG_LEVEL              = 3
WR_TAG_LOG_MASK               = 160
WR_TAG_LOG_PORT               = 9999
WR_TAG_LOG_REMOTE_LOGGING     = 1
WR_TAG_LOG_CIRBUF_SIZE        = 3000
WR_TAG_LOG_COREDUMP_FLAG      = 1
WR_TAG_INT_FREQ_MEAS_GAP      = 0
WR_TAG_ANR_MEAS_GAP_CONFIG    = 0
WR_TAG_SRC_HO_CANCEL_TMR      = 40000
WR_TAG_CNM_ENABLED            = 0
WR_TAG_TA_TMR_CMN             = 7
WR_TAG_TA_TMR_DED             = 7
```

```
WR_TAG_GRP_PUCCH_PWR_CTRL_ENABLE = 0
WR_TAG_GRP_PUSCH_PWR_CTRL_ENABLE = 0
WR_TAG_RRM_SR_PRDCTY        = {4,4}
WR_TAG_RRM_CQI_PRDCTY       = {6,6}
WR_TAG_RRM_NUM_SR_PER_TTI   = {8,8}
WR_TAG_RRM_NUM_CQI_PER_TTI  = {8,8}
WR_TAG_RRM_N1_PUCCH         = {64,64}
WR_TAG_LTE_PUCCH_PWR_FMT3A_ENABLE = 0
WR_TAG_LTE_PUSCH_PWR_FMT3A_ENABLE = 0
WR_TAG_DRX_QCI_SUPPORT_ENABLED = 0
WR_TAG_SPS_ENABLE_FLAG      = 0
WR_TAG_DL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_UL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_MAX_SPS_RB            = 10
WR_TAG_DSCP_ENABLE          = 0
WR_TAG_QCI_DSCP_MAP         = {152,120,104,72,180,44,12,4,4}
WR_TAG_CSG_CSG_ID           = 1234567
WR_TAG_CSG_ACCESS_MODE      = 1
WR_TAG_CSG_CSG_PCI_START    = 1
WR_TAG_CSG_CSG_PCI_RANGE    = 5
WR_TAG_CSG_HENB_NAME        = "RADISYS"
WR_TAG_MAX_AVG_GBRPRB_USAGE = 5
WR_TAG_DCFI_ENABLE          = 0
WR_TAG_CFI                  = 2
WR_TAG_RIM_CFG              = {86400000,5000,5000,5000,2}
WR_TAG_NUM_GERAN_NEIGH_FREQ = {0,0}
WR_TAG_GERAN_NEIGH_FREQ     = INVLD
WR_TAG_NUM_GERAN_NEIGH_CELL = {0,0}
WR_TAG_GERAN_NEIGH_CELL     = INVLD
WR_TAG_GERAN_MEAS_CFG       = INVLD
WR_TAG_CELL_SIZE_TYPE       = 0
WR_TAG_ARP_EMER_SERV        = 1
WR_TAG_GERAN_B2_RED_RSRP_THRSD1_VAL = 70
WR_TAG_GERAN_B2_RED_THRSD2_VAL   = 40
WR_TAG_GERAN_B2_HO_RSRP_THRSD1_VAL = 60
WR_TAG_GERAN_B2_HO_THRSD2_VAL   = 30
WR_TAG_SRS_ENABLE           = 0
WR_TAG_SRS_PERIODICITY      = 20
WR_TAG_SRS_CELL_BANDWIDTH   = 2
WR_TAG_SRS_CELL_SUBFRAME_CFG  = 0
WR_TAG_SRS_CELL_ACKNACK_SIMTX  = 0
WR_TAG_SRS_CELL_MAX_UPPTS      = 0
WR_TAG_SRS_UE_BANDWIDTH        = 0
WR_TAG_SRS_UE_HOPPING_BW       = 3
WR_TAG_WIRESHARK_PORT       = 9999
WR_TAG_WIRESHARK_DST_IP_ADDR = 192.168.1.10
WR_TAG_ANR_CELL_VALID_AGE_VAL = 0
WR_TAG_ENABLE_CA            = 0
WR_TAG_CELL_FREQ_CONTIGUOUS = 1
WR_TAG_TENB_STATS           = {1,0,1,30,8989}
WR_TAG_A4_RSRP_THRSHLD_VAL  = 60
WR_TAG_MEAS_SCELL_ADD_REL   = 0
WR_TAG_DL_MAX_ITBS          = 26
WR_TAG_UL_MAX_ITBS          = 26
WR_TAG_RT_MAC_SCH_CL_THRD_CORE = 6
WR_TAG_NRT_PDCP_GTP_THRD_CORE = 6
WR_TAG_RRC_APP_S1AP_THRD_CORE = 6
WR_TAG_WLS_DEVICE_NAME = /dev/wls
CFGEND                      = 1
#This CFGEND has to be kept at the end and should not be moved as the configuration
```

```
#parameter reading ends once we read this tag. Any new configuration tag MUST be added
above CFGEND
```

4.3.4 1 Cell CA LTE FDD Band 2 and Band4 (Inter-band)

```
WR_TAG_NOS_OF_CELLS          = 2
WR_TAG_CELL_ID               = {2,3}
WR_TAG_OP_MODE               = 0
WR_TAG_PERIOD                = 0
WR_TAG_DUP_MODE              = 1
WR_TAG_TDD_ULDL_CFG_MODE     = 2
WR_TAG_TDD_SPCL_SF_CONFIG    = 7
WR_TAG_MAX_UE_SUPPORT        = 420
WR_TAG_MCC_0                 = 0
WR_TAG_MCC_1                 = 0
WR_TAG_MCC_2                 = 1
WR_TAG_MNC_0                 = 0
WR_TAG_MNC_1                 = 1
WR_TAG_MNC_2                 = -1
WR_TAG_TA_CODE               = {1,1}
WR_TAG_FREQ_BAND_IND         = {2,4}
WR_TAG_DL_EARFCN             = {900,2175}
WR_TAG_UL_EARFCN             = {18900,20175}
WR_TAG_ENB_IP_ADDR           = 10.54.54.150
WR_TAG_PCI_SELECT_TYPE       = 0
WR_TAG_PRACH_SELECT_TYPE     = 1
WR_TAG_EARFCN_SELECT_TYPE    = 1
WR_TAG_PCI_LIST              = {1,2,35,36}
WR_TAG_DL_EARFCN_LIST        = {900,2175}
WR_TAG_UL_EARFCN_LIST        = {18900,20175}
WR_TAG_ROOTSEQ_IDX_LIST      = {{22,10}}
WR_TAG_PRACHCFG_IDX_LIST     = {{8,8}}
WR_TAG_ZERO_CORR_ZONE_CFG_LIST     = {{5,5}}
WR_TAG_PRACH_FREQ_OFFSET_LIST      = {{43,43}}
WR_TAG_ROOTSEQ_IDX           = 22
WR_TAG_ZERO_CORR_ZONE_CFG    = 10
WR_TAG_PRACH_FREQ_OFFSET     = 3
WR_TAG_NO_OF_MME_INFO        = 1
WR_TAG_MME_INFO              = {{1,1,10.54.54.17}}
WR_TAG_SCTP_IP_ADDR          = 10.54.54.150
WR_TAG_HI_DBG                = 0
WR_TAG_SB_DBG                = 0
WR_TAG_SZ_DBG                = 0
WR_TAG_EG_DBG                = 0
WR_TAG_WR_DBG                = 1
WR_TAG_NH_DBG                = 0
WR_TAG_KW_DBG                = 0
WR_TAG_RG_DBG                = 0
WR_TAG_YS_DBG                = 0
WR_TAG_SM_DBG                = 0
WR_TAG_INACTIVITY_TIMER_VAL  = 3000000
WR_TAG_END_MARKER_TIMER_VAL  = 200
WR_TAG_MAX_EXPIRY            = 30
WR_TAG_CZ_DBG                = 0
WR_TAG_X2_PREP_TMR           = 5000
WR_TAG_X2_OVRALL_TMR         = 10000
WR_TAG_NO_OF_BRDCST_PLMN     = 1
WR_TAG_PLMN_ID_LST           = {00101}
WR_TAG_NO_OF_NGH_INFO        = INVLD
```

```
WR_TAG_NGH_INFO_CFG          = INVLD
WR_TAG_NO_OF_GU_GRP          = 1
WR_TAG_NUM_TX_ANTENNA        = 2
WR_TAG_S1_PREP_TMR           = 5000
WR_TAG_S1_OVRALL_TMR         = 10000
WR_TAG_MEAS_CFG_ENB          = 1
WR_TAG_RRM_RNTI_STRT         = {205,205}
WR_TAG_MAX_RRM_RNTIS         = {420,420}
WR_TAG_MAC_RNTI_STRT         = {61,511}
WR_TAG_MAX_MAC_RNTIS         = {420,420}
WR_TAG_RRM_NO_OF_DED_PREMBL = {10,10}
WR_TAG_RRM_DED_PREMBL_STRT  = {41,41}
WR_TAG_MAC_NO_OF_PREMBL      = {6,6}
WR_TAG_A1_RSRP_THRSHLD_VAL  = 90
WR_TAG_A2_RSRP_THRSHLD_VAL  = 6
WR_TAG_INTRA_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTRA_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTER_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTER_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTRA_HO_A3_OFFSET = 10
WR_TAG_INTRA_ANR_A3_OFFSET = 5
WR_TAG_INTER_ANR_A5_RSRP_THRSD1_VAL = 75
WR_TAG_INTER_ANR_A5_RSRP_THRSD2_VAL = 50
WR_TAG_ANR_REPORT_CFG_VAL = 0
WR_TAG_HO_REPORT_CFG_VAL = 1
WR_TAG_ANR_EPOC_TMR_VAL_IN_SECS = 1000
WR_TAG_ANR_TRICE_INTV_COUNT = 10
WR_TAG_UTRA_B2_RSRP_THRSD1_VAL = 70
WR_TAG_UTRA_FDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_UTRA_TDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_S_MEASURE_VAL         = 0
WR_TAG_INTRA_TTT_VAL         = 7
WR_TAG_INTRA_HYTERISIS       = 1
WR_TAG_NO_OF_NGH_ENB_CFG     = INVLD
WR_TAG_NGH_ENB_CFG           = INVLD
WR_TAG_PCI_VAL               = {1,2}
WR_TAG_DL_NUM_UE_PER_TTI     = 8
WR_TAG_UL_NUM_UE_PER_TTI     = 8
WR_TAG_MAX_DL_UE_PER_TTI     = 8
WR_TAG_MAX_UL_UE_PER_TTI     = 8
WR_TAG_DL_SCHD_TYPE          = 2
WR_TAG_UL_SCHD_TYPE          = 2
WR_TAG_DLFS_SCHD_TYPE        = 0
WR_TAG_PFS_DL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_DL_FAIRNESS_COEFFICIENT = 0
WR_TAG_PFS_UL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_UL_FAIRNESS_COEFFICIENT = 0
WR_TAG_DL_QCI_SCHD_WGT       = {8,6,7,5,9,4,3,2,1}
WR_TAG_UL_QCI_SCHD_WGT       = {8,6,7,5,9,4,3,2,1}
WR_TAG_TM_AUTO_CONFIG        = 0
WR_TAG_PREFERRED_TM          = 3
WR_TAG_MAX_X2_PEERS          = 5
WR_TAG_X2_TIME_TO_WAIT       = 200000
WR_TAG_SCTP_SRVC_TYPE        = 0
WR_TAG_DIAG_TUCL             = {{0,10}}
WR_TAG_DIAG_S1AP             = {{0,10}}
WR_TAG_DIAG_EGTP             = {{0,10}}
WR_TAG_DIAG_APP              = {{0,10}}
WR_TAG_DIAG_LTERRC           = {{0,10}}
WR_TAG_DIAG_LTERLC           = {{0,10}}
```

```
WR_TAG_DIAG_LTEPDCP          = {{0,10}}
WR_TAG_DIAG_LTECL            = {{0,10}}
WR_TAG_DIAG_LTEMAC           = {{0,10}}
WR_TAG_DIAG_X2AP             = {{0,10}}
WR_TAG_DIAG_SCTP             = {{0,10}}
WR_TAG_SCTP_RTO_MIN          = 100
WR_TAG_SCTP_RTO_MAX          = 1000
WR_TAG_SCTP_RTO_INITIAL      = 200
WR_TAG_SCTP_HRTBEAT_INTERVAL = 5000
WR_TAG_UL_ENABLE_TIME        = 1
WR_TAG_NUM_EUTRA_FREQ        = {2,2}
WR_TAG_EUTRA_FREQ_CFG        = {{900,18900},{2175,20175},{900,18900},{2175,20175}}
WR_TAG_NUM_UTRA_FDD_FREQ     = {1,1}
WR_TAG_UTRA_FDD_FREQ_CFG     = {{10713,23230},{10714,23231}}
WR_TAG_NUM_UTRA_TDD_FREQ     = {1,1}
WR_TAG_UTRA_TDD_FREQ_CFG     = {{10054,0,1},{9654,0,2}}
WR_TAG_CSG_SMCELL_PCI_START = 1
WR_TAG_CSG_SMCELL_PCI_RANGE = 100
WR_TAG_NO_OF_NGH_CFG         = {1,1}
WR_TAG_NGH_CELL_CFG          =
{{10.188.6.26,8,1,8,00102,900,18900,0,1,0,2,2,7,0,0,60,40},{10.188.6.28,9,2,9,00102,21
75,20175,0,1,0,2,2,7,0,0,60,40}}
WR_TAG_NO_OF_UTRA_FDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_FDD_CELL_CFG     =
{{10,70,10713,23230,6,1,21901,145,45,0,1,1},{20,71,10714,23231,10,1,21901,150,50,0,1,1
}}
WR_TAG_NO_OF_UTRA_TDD_NGH_CFG    = {1,1}
WR_TAG_NGH_UTRA_TDD_CELL_CFG     =
{{30,80,10054,145,100,60,1,21901,45,0},{40,81,9654,150,100,61,1,21901,50,0}}
WR_TAG_NUM_CDMA_1XRTT_BAND_CLS = {1,1}
WR_TAG_CDMA_1XRTT_BAND_CLS     = {{1,1,1,1},{1,1,1,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_FREQ = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_FREQ     = {{1,1000,1},{1,1000,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_CELL = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_CELL     = {{1,1000,1,1,1},{1,1000,1,1,1}}
WR_TAG_CSFB_UTRA_CFG_VAL         = 0
WR_TAG_CSFB_CDMA_CFG_VAL         = 0
WR_TAG_ECSFB_CFG_VAL         = 0
WR_TAG_DUAL_RX_SUPPORTED     = 1
WR_TAG_DUAL_RX_TX_SUPPORTED = 0
WR_TAG_AS_PRI_INTG_ALGO_LST = {1}
WR_TAG_AS_PRI_CIPH_ALGO_LST = {1}
WR_TAG_ABS_A3_OFFSET         = -6
WR_TAG_PICO_OFFSET           = 20
WR_TAG_ABS_PATTERN_TYPE      = 2
WR_TAG_ABS_PATTERN           = 01010101010101010101010101010101010101010101
WR_TAG_ABS_LOAD_PERIODICITY = 0
WR_TAG_SFR_START_RB          = 25
WR_TAG_SFR_END_RB            = 49
WR_TAG_SFR_POWER_LOW         = 4
WR_TAG_SFR_POWER_HIGH        = 5
WR_TAG_DRX_ENABLED           = 0
WR_TAG_DRX_INACTIVITY_TMR    = 10
WR_TAG_DRX_RETX_TMR          = 1
WR_TAG_DRX_LONG_CYCLE_GBR    = 1
WR_TAG_DRX_LONG_CYCLE_NON_GBR = 5
WR_TAG_ANR_DRX_LONG_CYCLE    = 11
WR_TAG_ANR_DRX_ON_DURATION_TMR = 7
WR_TAG_ANR_DRX_INACTIVITY_TMR = 8
WR_TAG_DEFAULT_PAGING_CYCLE = 0
```

```
WR_TAG_DEFAULT_PCCH_CFG_NB  = 7
WR_TAG_BANDWIDTH            = {20,20}
WR_TAG_BOOT_MODE            = 0
WR_TAG_PWS_ETWS_CMAS_CNTRL = 0
WR_TAG_WATCHDOG_SOFT_LIMIT  = 5
WR_TAG_WATCHDOG_HARD_LIMIT  = 15
WR_TAG_LOG_PATH             = /var/log
WR_TAG_LOG_FILE             = dbglog
WR_TAG_LOG_MAX_FILES        = 3
WR_TAG_LOG_FILESIZE_LIMIT   = 5
WR_TAG_LOG_LEVEL            = 0
WR_TAG_LOG_MASK             = 0
WR_TAG_LOG_PORT             = 9999
WR_TAG_LOG_REMOTE_LOGGING   = 1
WR_TAG_LOG_CIRBUF_SIZE      = 3000
WR_TAG_LOG_COREDUMP_FLAG    = 1
WR_TAG_INT_FREQ_MEAS_GAP    = 0
WR_TAG_ANR_MEAS_GAP_CONFIG  = 0
WR_TAG_SRC_HO_CANCEL_TMR    = 40000
WR_TAG_CNM_ENABLED          = 0
WR_TAG_TA_TMR_CMN           = 7
WR_TAG_TA_TMR_DED           = 7
WR_TAG_GRP_PUCCH_PWR_CTRL_ENABLE = 0
WR_TAG_GRP_PUSCH_PWR_CTRL_ENABLE = 0
WR_TAG_RRM_SR_PRDCTY        = {4,4}
WR_TAG_RRM_CQI_PRDCTY       = {6,6}
WR_TAG_RRM_NUM_SR_PER_TTI   = {8,8}
WR_TAG_RRM_NUM_CQI_PER_TTI  = {8,8}
WR_TAG_RRM_N1_PUCCH         = {18,18}
WR_TAG_LTE_PUCCH_PWR_FMT3A_ENABLE = 0
WR_TAG_LTE_PUSCH_PWR_FMT3A_ENABLE = 0
WR_TAG_DRX_QCI_SUPPORT_ENABLED = 0
WR_TAG_SPS_ENABLE_FLAG      = 0
WR_TAG_DL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_UL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_MAX_SPS_RB            = 10
WR_TAG_DSCP_ENABLE          = 0
WR_TAG_QCI_DSCP_MAP         = {152,120,104,72,180,44,12,4,4}
WR_TAG_CSG_CSG_ID           = 1234567
WR_TAG_CSG_ACCESS_MODE      = 1
WR_TAG_CSG_CSG_PCI_START    = 1
WR_TAG_CSG_CSG_PCI_RANGE    = 5
WR_TAG_CSG_HENB_NAME        = "RADISYS"
WR_TAG_MAX_AVG_GBRPRB_USAGE = 5
WR_TAG_DCFI_ENABLE          = 0
WR_TAG_CFI                  = 2
WR_TAG_RIM_CFG              = {86400000,5000,5000,5000,2}
WR_TAG_NUM_GERAN_NEIGH_FREQ = {0,0}
WR_TAG_GERAN_NEIGH_FREQ     = INVLD
WR_TAG_NUM_GERAN_NEIGH_CELL = {0,0}
WR_TAG_GERAN_NEIGH_CELL     = INVLD
WR_TAG_GERAN_MEAS_CFG       = INVLD
WR_TAG_CELL_SIZE_TYPE       = 0
WR_TAG_ARP_EMER_SERV        = 1
WR_TAG_GERAN_B2_RED_RSRP_THRSD1_VAL = 70
WR_TAG_GERAN_B2_RED_THRSD2_VAL   = 40
WR_TAG_GERAN_B2_HO_RSRP_THRSD1_VAL = 60
WR_TAG_GERAN_B2_HO_THRSD2_VAL   = 30
WR_TAG_WIRESHARK_PORT       = 9999
WR_TAG_WIRESHARK_DST_IP_ADDR = 192.168.1.10
```

```
WR_TAG_ANR_CELL_VALID_AGE_VAL = 0
WR_TAG_ENABLE_CA              = 1
WR_TAG_CELL_FREQ_CONTIGUOUS = 0
WR_TAG_TENB_STATS             = {1,0,1,50,8989}
WR_TAG_A4_RSRP_THRSHLD_VAL  = 60
WR_TAG_MEAS_SCELL_ADD_REL   = 0
WR_TAG_RT_MAC_SCH_CL_THRD_CORE = 6
WR_TAG_NRT_PDCP_GTP_THRD_CORE = 6
WR_TAG_RRC_APP_S1AP_THRD_CORE = 6
WR_TAG_WLS_DEVICE_NAME = /dev/wls
CFGEND                        = 1
#This CFGEND has to be kept at the end and should not be moved as the configuration
#parameter reading ends once we read this tag. Any new configuration tag MUST be
#added above CFGEND
```

4.3.5 1 Cell CA LTE TDD Band 40 and Band40 (Intra-band Contiguous)

```
WR_TAG_NOS_OF_CELLS           = 2
WR_TAG_CELL_ID                = {1,2}
WR_TAG_OP_MODE                = 0
WR_TAG_PERIOD                 = 0
WR_TAG_DUP_MODE               = 2
WR_TAG_TDD_ULDL_CFG_MODE      = 2
WR_TAG_TDD_SPCL_SF_CONFIG     = 7
WR_TAG_MAX_UE_SUPPORT         = 64
WR_TAG_MCC_0                  = 0
WR_TAG_MCC_1                  = 0
WR_TAG_MCC_2                  = 1
WR_TAG_MNC_0                  = 0
WR_TAG_MNC_1                  = 1
WR_TAG_MNC_2                  = -1
WR_TAG_TA_CODE                = {1,1}
WR_TAG_FREQ_BAND_IND          = {40,40}
WR_TAG_DL_EARFCN              = {38750,38948}
WR_TAG_UL_EARFCN              = {38750,38948}
WR_TAG_ENB_IP_ADDR            = 10.233.182.23
WR_TAG_PCI_SELECT_TYPE        = 0
WR_TAG_PRACH_SELECT_TYPE      = 1
WR_TAG_EARFCN_SELECT_TYPE     = 1
WR_TAG_PCI_LIST               = {1,2,35,36}
WR_TAG_DL_EARFCN_LIST         = {38750,38948}
WR_TAG_UL_EARFCN_LIST         = {38750,38948}
WR_TAG_ROOTSEQ_IDX_LIST       = {{823,10,18}}
WR_TAG_PRACHCFG_IDX_LIST      = {{1,1,48}}
WR_TAG_ZERO_CORR_ZONE_CFG_LIST     = {{8,10,14}}
WR_TAG_PRACH_FREQ_OFFSET_LIST      = {{43,43}}
WR_TAG_ROOTSEQ_IDX            = 823
WR_TAG_ZERO_CORR_ZONE_CFG     = 10
WR_TAG_PRACH_FREQ_OFFSET      = 1
WR_TAG_NO_OF_MME_INFO         = 1
WR_TAG_MME_INFO               = {{1,1,10.233.180.160}}
WR_TAG_SCTP_IP_ADDR           = 10.233.182.23
WR_TAG_HI_DBG                 = 0
WR_TAG_SB_DBG                 = 0
WR_TAG_SZ_DBG                 = 0
WR_TAG_EG_DBG                 = 0
WR_TAG_WR_DBG                 = 1
WR_TAG_NH_DBG                 = 0
WR_TAG_KW_DBG                 = 0
```

```
WR_TAG_RG_DBG                = 0
WR_TAG_YS_DBG                = 0
WR_TAG_SM_DBG                = 0
WR_TAG_INACTIVITY_TIMER_VAL = 3000000
WR_TAG_END_MARKER_TIMER_VAL = 200
WR_TAG_MAX_EXPIRY            = 30
WR_TAG_CZ_DBG                = 0
WR_TAG_X2_PREP_TMR           = 5000
WR_TAG_X2_OVRALL_TMR         = 10000
WR_TAG_NO_OF_BRDCST_PLMN     = 1
WR_TAG_PLMN_ID_LST           = {00101}
WR_TAG_NO_OF_NGH_INFO        = INVLD
WR_TAG_NGH_INFO_CFG          = INVLD
WR_TAG_NO_OF_GU_GRP          = 1
WR_TAG_NUM_TX_ANTENNA        = 2
WR_TAG_S1_PREP_TMR           = 5000
WR_TAG_S1_OVRALL_TMR         = 10000
WR_TAG_MEAS_CFG_ENB          = 1
WR_TAG_RRM_RNTI_STRT         = {205,205}
WR_TAG_MAX_RRM_RNTIS         = {32,32}
WR_TAG_MAC_RNTI_STRT         = {61,128}
WR_TAG_MAX_MAC_RNTIS         = {96,165}
WR_TAG_RRM_NO_OF_DED_PREMBL = {10,10}
WR_TAG_RRM_DED_PREMBL_STRT  = {41,41}
WR_TAG_MAC_NO_OF_PREMBL      = {6,6}
WR_TAG_A1_RSRP_THRSHLD_VAL  = 90
WR_TAG_A2_RSRP_THRSHLD_VAL  = 6
WR_TAG_INTRA_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTRA_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTER_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTER_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTRA_HO_A3_OFFSET = 10
WR_TAG_INTRA_ANR_A3_OFFSET = 5
WR_TAG_INTER_ANR_A5_RSRP_THRSD1_VAL = 75
WR_TAG_INTER_ANR_A5_RSRP_THRSD2_VAL = 50
WR_TAG_ANR_REPORT_CFG_VAL = 0
WR_TAG_HO_REPORT_CFG_VAL = 1
WR_TAG_ANR_EPOC_TMR_VAL_IN_SECS = 1000
WR_TAG_ANR_TRICE_INTV_COUNT = 10
WR_TAG_UTRA_B2_RSRP_THRSD1_VAL = 70
WR_TAG_UTRA_FDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_UTRA_TDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_S_MEASURE_VAL         = 0
WR_TAG_INTRA_TTT_VAL         = 7
WR_TAG_INTRA_HYTERISIS       = 1
WR_TAG_NO_OF_NGH_ENB_CFG     = INVLD
WR_TAG_NGH_ENB_CFG           = INVLD
WR_TAG_PCI_VAL               = {1,2}
WR_TAG_DL_NUM_UE_PER_TTI     = 8
WR_TAG_UL_NUM_UE_PER_TTI     = 8
WR_TAG_MAX_DL_UE_PER_TTI     = 8
WR_TAG_MAX_UL_UE_PER_TTI     = 8
WR_TAG_DL_SCHD_TYPE          = 2
WR_TAG_UL_SCHD_TYPE          = 2
WR_TAG_DLFS_SCHD_TYPE        = 0
WR_TAG_PFS_DL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_DL_FAIRNESS_COEFFICIENT = 0
WR_TAG_PFS_UL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_UL_FAIRNESS_COEFFICIENT = 0
WR_TAG_DL_QCI_SCHD_WGT       = {8,6,7,5,9,4,3,2,1}
```

```
WR_TAG_UL_QCI_SCHD_WGT      = {8,6,7,5,9,4,3,2,1}
WR_TAG_TM_AUTO_CONFIG       = 0
WR_TAG_PREFERRED_TM         = 3
WR_TAG_MAX_X2_PEERS         = 5
WR_TAG_X2_TIME_TO_WAIT      = 200000
WR_TAG_SCTP_SRVC_TYPE       = 0
WR_TAG_DIAG_TUCL            = {{0,10}}
WR_TAG_DIAG_S1AP            = {{0,10}}
WR_TAG_DIAG_EGTP            = {{0,10}}
WR_TAG_DIAG_APP             = {{0,10}}
WR_TAG_DIAG_LTERRC          = {{0,10}}
WR_TAG_DIAG_LTERLC          = {{0,10}}
WR_TAG_DIAG_LTEPDCP         = {{0,10}}
WR_TAG_DIAG_LTECL           = {{0,10}}
WR_TAG_DIAG_LTEMAC          = {{0,10}}
WR_TAG_DIAG_X2AP            = {{0,10}}
WR_TAG_DIAG_SCTP            = {{0,10}}
WR_TAG_SCTP_RTO_MIN         = 100
WR_TAG_SCTP_RTO_MAX         = 1000
WR_TAG_SCTP_RTO_INITIAL     = 200
WR_TAG_SCTP_HRTBEAT_INTERVAL = 5000
WR_TAG_UL_ENABLE_TIME       = 1
WR_TAG_NUM_EUTRA_FREQ       = {2,2}
WR_TAG_EUTRA_FREQ_CFG       =
{{38750,38750},{38948,38948},{38750,38750},{38948,38948}}
WR_TAG_NUM_UTRA_FDD_FREQ    = {1,1}
WR_TAG_UTRA_FDD_FREQ_CFG    = {{10713,23230},{10714,23231}}
WR_TAG_NUM_UTRA_TDD_FREQ    = {1,1}
WR_TAG_UTRA_TDD_FREQ_CFG    = {{10054,0,1},{9654,0,2}}
WR_TAG_CSG_SMCELL_PCI_START = 1
WR_TAG_CSG_SMCELL_PCI_RANGE = 100
WR_TAG_NO_OF_NGH_CFG        = {1,1}
WR_TAG_NGH_CELL_CFG         =
{{10.188.6.26,8,1,8,00102,38750,18900,0,1,0,2,2,7,0,0,60,40},{10.188.6.28,9,2,9,00102,
2175,20175,0,1,0,2,2,7,0,0,60,40}}
WR_TAG_NO_OF_UTRA_FDD_NGH_CFG   = {1,1}
WR_TAG_NGH_UTRA_FDD_CELL_CFG    =
{{10,70,10713,23230,6,1,21901,145,45,0,1,1},{20,71,10714,23231,10,1,21901,150,50,0,1,1
}}
WR_TAG_NO_OF_UTRA_TDD_NGH_CFG   = {1,1}
WR_TAG_NGH_UTRA_TDD_CELL_CFG    =
{{30,80,10054,145,100,60,1,21901,45,0},{40,81,9654,150,100,61,1,21901,50,0}}
WR_TAG_NUM_CDMA_1XRTT_BAND_CLS = {1,1}
WR_TAG_CDMA_1XRTT_BAND_CLS     = {{1,1,1,1},{1,1,1,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_FREQ = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_FREQ     = {{1,1000,1},{1,1000,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_CELL = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_CELL     = {{1,1000,1,1,1},{1,1000,1,1,1}}
WR_TAG_CSFB_UTRA_CFG_VAL         = 0
WR_TAG_CSFB_CDMA_CFG_VAL         = 0
WR_TAG_ECSFB_CFG_VAL        = 0
WR_TAG_DUAL_RX_SUPPORTED    = 1
WR_TAG_DUAL_RX_TX_SUPPORTED = 0
WR_TAG_AS_PRI_INTG_ALGO_LST = {1}
WR_TAG_AS_PRI_CIPH_ALGO_LST = {1}
WR_TAG_ABS_A3_OFFSET        = -6
WR_TAG_PICO_OFFSET          = 20
WR_TAG_ABS_PATTERN_TYPE     = 2
WR_TAG_ABS_PATTERN          = 01010101010101010101010101010101010101010101
WR_TAG_ABS_LOAD_PERIODICITY = 0
```

```
WR_TAG_SFR_START_RB          = 25
WR_TAG_SFR_END_RB            = 49
WR_TAG_SFR_POWER_LOW         = 4
WR_TAG_SFR_POWER_HIGH        = 5
WR_TAG_DRX_ENABLED           = 0
WR_TAG_DRX_INACTIVITY_TMR    = 10
WR_TAG_DRX_RETX_TMR          = 1
WR_TAG_DRX_LONG_CYCLE_GBR    = 1
WR_TAG_DRX_LONG_CYCLE_NON_GBR = 5
WR_TAG_ANR_DRX_LONG_CYCLE    = 11
WR_TAG_ANR_DRX_ON_DURATION_TMR = 7
WR_TAG_ANR_DRX_INACTIVITY_TMR = 8
WR_TAG_DEFAULT_PAGING_CYCLE = 0
WR_TAG_DEFAULT_PCCH_CFG_NB  = 7
WR_TAG_BANDWIDTH             = {20,20}
WR_TAG_BOOT_MODE             = 0
WR_TAG_PWS_ETWS_CMAS_CNTRL = 0
WR_TAG_WATCHDOG_SOFT_LIMIT  = 5
WR_TAG_WATCHDOG_HARD_LIMIT  = 15
WR_TAG_LOG_PATH              = /var/log
WR_TAG_LOG_FILE              = dbglog
WR_TAG_LOG_MAX_FILES         = 3
WR_TAG_LOG_FILESIZE_LIMIT    = 5
WR_TAG_LOG_LEVEL             = 3
WR_TAG_LOG_MASK              = 160
WR_TAG_LOG_PORT              = 9999
WR_TAG_LOG_REMOTE_LOGGING    = 1
WR_TAG_LOG_CIRBUF_SIZE       = 3000
WR_TAG_LOG_COREDUMP_FLAG     = 1
WR_TAG_INT_FREQ_MEAS_GAP     = 0
WR_TAG_ANR_MEAS_GAP_CONFIG   = 0
WR_TAG_SRC_HO_CANCEL_TMR     = 40000
WR_TAG_CNM_ENABLED           = 0
WR_TAG_TA_TMR_CMN            = 7
WR_TAG_TA_TMR_DED            = 7
WR_TAG_GRP_PUCCH_PWR_CTRL_ENABLE = 0
WR_TAG_GRP_PUSCH_PWR_CTRL_ENABLE = 0
WR_TAG_RRM_SR_PRDCTY         = {4,4}
WR_TAG_RRM_CQI_PRDCTY        = {6,6}
WR_TAG_RRM_NUM_SR_PER_TTI    = {8,8}
WR_TAG_RRM_NUM_CQI_PER_TTI   = {8,8}
WR_TAG_RRM_N1_PUCCH          = {64,64}
WR_TAG_LTE_PUCCH_PWR_FMT3A_ENABLE = 0
WR_TAG_LTE_PUSCH_PWR_FMT3A_ENABLE = 0
WR_TAG_DRX_QCI_SUPPORT_ENABLED = 0
WR_TAG_SPS_ENABLE_FLAG       = 0
WR_TAG_DL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_UL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_MAX_SPS_RB             = 10
WR_TAG_DSCP_ENABLE           = 0
WR_TAG_QCI_DSCP_MAP          = {152,120,104,72,180,44,12,4,4}
WR_TAG_CSG_CSG_ID            = 1234567
WR_TAG_CSG_ACCESS_MODE       = 1
WR_TAG_CSG_CSG_PCI_START     = 1
WR_TAG_CSG_CSG_PCI_RANGE     = 5
WR_TAG_CSG_HENB_NAME         = "RADISYS"
WR_TAG_MAX_AVG_GBRPRB_USAGE = 5
WR_TAG_DCFI_ENABLE           = 0
WR_TAG_CFI                   = 2
WR_TAG_RIM_CFG               = {86400000,5000,5000,5000,2}
```

```
WR_TAG_NUM_GERAN_NEIGH_FREQ = {0,0}
WR_TAG_GERAN_NEIGH_FREQ     = INVLD
WR_TAG_NUM_GERAN_NEIGH_CELL = {0,0}
WR_TAG_GERAN_NEIGH_CELL     = INVLD
WR_TAG_GERAN_MEAS_CFG       = INVLD
WR_TAG_CELL_SIZE_TYPE       = 0
WR_TAG_ARP_EMER_SERV        = 1
WR_TAG_GERAN_B2_RED_RSRP_THRSD1_VAL = 70
WR_TAG_GERAN_B2_RED_THRSD2_VAL   = 40
WR_TAG_GERAN_B2_HO_RSRP_THRSD1_VAL = 60
WR_TAG_GERAN_B2_HO_THRSD2_VAL   = 30
WR_TAG_SRS_ENABLE           = 0
WR_TAG_SRS_PERIODICITY      = 20
WR_TAG_SRS_CELL_BANDWIDTH   = 2
WR_TAG_SRS_CELL_SUBFRAME_CFG  = 0
WR_TAG_SRS_CELL_ACKNACK_SIMTX  = 0
WR_TAG_SRS_CELL_MAX_UPPTS      = 0
WR_TAG_SRS_UE_BANDWIDTH        = 0
WR_TAG_SRS_UE_HOPPING_BW       = 3
WR_TAG_WIRESHARK_PORT       = 9999
WR_TAG_WIRESHARK_DST_IP_ADDR = 192.168.1.10
WR_TAG_ANR_CELL_VALID_AGE_VAL = 0
WR_TAG_ENABLE_CA            = 1
WR_TAG_CELL_FREQ_CONTIGUOUS = 1
WR_TAG_TENB_STATS           = {1,0,1,30,8989}
WR_TAG_A4_RSRP_THRSHLD_VAL  = 60
WR_TAG_MEAS_SCELL_ADD_REL   = 0
WR_TAG_DL_MAX_ITBS          = 26
WR_TAG_UL_MAX_ITBS          = 26
WR_TAG_RT_MAC_SCH_CL_THRD_CORE = 6
WR_TAG_NRT_PDCP_GTP_THRD_CORE = 6
WR_TAG_RRC_APP_S1AP_THRD_CORE = 6
WR_TAG_WLS_DEVICE_NAME = /dev/wls
CFGEND                      = 1
#This CFGEND has to be kept at the end and should not be moved as the configuration
parameter reading ends once we read this tag. Any new configuration tag MUST be added
above CFGEND
```

4.3.6 1 Cell 4x2 MIMO LTE FDD Band 2

```
WR_TAG_NOS_OF_CELLS         = 1
WR_TAG_CELL_ID              = {3,4}
WR_TAG_OP_MODE              = 0
WR_TAG_PERIOD               = 0
WR_TAG_DUP_MODE             = 1
WR_TAG_TDD_ULDL_CFG_MODE    = 2
WR_TAG_TDD_SPCL_SF_CONFIG   = 7
WR_TAG_MAX_UE_SUPPORT       = 420
WR_TAG_MCC_0                = 0
WR_TAG_MCC_1                = 0
WR_TAG_MCC_2                = 1
WR_TAG_MNC_0                = 0
WR_TAG_MNC_1                = 1
WR_TAG_MNC_2                = -1
WR_TAG_TA_CODE              = {1,1}
WR_TAG_FREQ_BAND_IND        = {2,4}
WR_TAG_DL_EARFCN            = {900,2175}
WR_TAG_UL_EARFCN            = {18900,20175}
WR_TAG_ENB_IP_ADDR          = 10.233.182.51
```

```
WR_TAG_PCI_SELECT_TYPE      = 0
WR_TAG_PRACH_SELECT_TYPE    = 1
WR_TAG_EARFCN_SELECT_TYPE   = 1
WR_TAG_PCI_LIST             = {1,2,35,36}
WR_TAG_DL_EARFCN_LIST       = {900,2175}
WR_TAG_UL_EARFCN_LIST       = {18900,20175}
WR_TAG_ROOTSEQ_IDX_LIST     = {{22,10}}
WR_TAG_PRACHCFG_IDX_LIST    = {{8,8}}
WR_TAG_ZERO_CORR_ZONE_CFG_LIST    = {{5,5}}
WR_TAG_PRACH_FREQ_OFFSET_LIST     = {{43,43}}
WR_TAG_ROOTSEQ_IDX          = 22
WR_TAG_ZERO_CORR_ZONE_CFG   = 10
WR_TAG_PRACH_FREQ_OFFSET    = 3
WR_TAG_NO_OF_MME_INFO       = 1
WR_TAG_MME_INFO             = {{1,1,10.233.180.160}}
WR_TAG_SCTP_IP_ADDR         = 10.233.182.51
WR_TAG_HI_DBG               = 0
WR_TAG_SB_DBG               = 0
WR_TAG_SZ_DBG               = 0
WR_TAG_EG_DBG               = 0
WR_TAG_WR_DBG               = 1
WR_TAG_NH_DBG               = 0
WR_TAG_KW_DBG               = 0
WR_TAG_RG_DBG               = 0
WR_TAG_YS_DBG               = 0
WR_TAG_SM_DBG               = 0
WR_TAG_INACTIVITY_TIMER_VAL = 3000000
WR_TAG_END_MARKER_TIMER_VAL = 200
WR_TAG_MAX_EXPIRY           = 30
WR_TAG_CZ_DBG               = 0
WR_TAG_X2_PREP_TMR          = 5000
WR_TAG_X2_OVRALL_TMR        = 10000
WR_TAG_NO_OF_BRDCST_PLMN    = 1
WR_TAG_PLMN_ID_LST          = {00101}
WR_TAG_NO_OF_NGH_INFO       = INVLD
WR_TAG_NGH_INFO_CFG         = INVLD
WR_TAG_NO_OF_GU_GRP         = 1
WR_TAG_NUM_TX_ANTENNA       = 4
WR_TAG_S1_PREP_TMR          = 5000
WR_TAG_S1_OVRALL_TMR        = 10000
WR_TAG_MEAS_CFG_ENB         = 1
WR_TAG_RRM_RNTI_STRT        = {205,205}
WR_TAG_MAX_RRM_RNTIS        = {420,420}
WR_TAG_MAC_RNTI_STRT        = {61,511}
WR_TAG_MAX_MAC_RNTIS        = {420,420}
WR_TAG_RRM_NO_OF_DED_PREMBL = {10,10}
WR_TAG_RRM_DED_PREMBL_STRT  = {41,41}
WR_TAG_MAC_NO_OF_PREMBL     = {6,6}
WR_TAG_A1_RSRP_THRSHLD_VAL  = 90
WR_TAG_A2_RSRP_THRSHLD_VAL  = 6
WR_TAG_INTRA_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTRA_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTER_A5_RSRP_THRSD1_VAL = 65
WR_TAG_INTER_A5_RSRP_THRSD2_VAL = 70
WR_TAG_INTRA_HO_A3_OFFSET = 10
WR_TAG_INTRA_ANR_A3_OFFSET = 5
WR_TAG_INTER_ANR_A5_RSRP_THRSD1_VAL = 75
WR_TAG_INTER_ANR_A5_RSRP_THRSD2_VAL = 50
WR_TAG_ANR_REPORT_CFG_VAL = 0
WR_TAG_HO_REPORT_CFG_VAL = 1
```

```
WR_TAG_ANR_EPOC_TMR_VAL_IN_SECS = 1000
WR_TAG_ANR_TRICE_INTV_COUNT = 10
WR_TAG_UTRA_B2_RSRP_THRSD1_VAL = 70
WR_TAG_UTRA_FDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_UTRA_TDD_B2_RSCP_THRSD2_VAL = 65
WR_TAG_S_MEASURE_VAL        = 0
WR_TAG_INTRA_TTT_VAL        = 7
WR_TAG_INTRA_HYTERISIS      = 1
WR_TAG_NO_OF_NGH_ENB_CFG    = INVLD
WR_TAG_NGH_ENB_CFG          = INVLD
WR_TAG_PCI_VAL              = {1,2}
WR_TAG_DL_NUM_UE_PER_TTI    = 8
WR_TAG_UL_NUM_UE_PER_TTI    = 8
WR_TAG_MAX_DL_UE_PER_TTI    = 8
WR_TAG_MAX_UL_UE_PER_TTI    = 8
WR_TAG_DL_SCHD_TYPE         = 2
WR_TAG_UL_SCHD_TYPE         = 2
WR_TAG_DLFS_SCHD_TYPE       = 0
WR_TAG_PFS_DL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_DL_FAIRNESS_COEFFICIENT = 0
WR_TAG_PFS_UL_TPT_COEFFICIENT  = 0
WR_TAG_PFS_UL_FAIRNESS_COEFFICIENT = 0
WR_TAG_DL_QCI_SCHD_WGT      = {8,6,7,5,9,4,3,2,1}
WR_TAG_UL_QCI_SCHD_WGT      = {8,6,7,5,9,4,3,2,1}
WR_TAG_TM_AUTO_CONFIG       = 0
WR_TAG_PREFERRED_TM         = 3
WR_TAG_MAX_X2_PEERS         = 5
WR_TAG_X2_TIME_TO_WAIT      = 200000
WR_TAG_SCTP_SRVC_TYPE       = 0
WR_TAG_DIAG_TUCL            = {{0,10}}
WR_TAG_DIAG_S1AP            = {{0,10}}
WR_TAG_DIAG_EGTP            = {{0,10}}
WR_TAG_DIAG_APP             = {{0,10}}
WR_TAG_DIAG_LTERRC          = {{0,10}}
WR_TAG_DIAG_LTERLC          = {{0,10}}
WR_TAG_DIAG_LTEPDCP         = {{0,10}}
WR_TAG_DIAG_LTECL           = {{0,10}}
WR_TAG_DIAG_LTEMAC          = {{0,10}}
WR_TAG_DIAG_X2AP            = {{0,10}}
WR_TAG_DIAG_SCTP            = {{0,10}}
WR_TAG_SCTP_RTO_MIN         = 100
WR_TAG_SCTP_RTO_MAX         = 1000
WR_TAG_SCTP_RTO_INITIAL     = 200
WR_TAG_SCTP_HRTBEAT_INTERVAL = 5000
WR_TAG_UL_ENABLE_TIME       = 1
WR_TAG_NUM_EUTRA_FREQ       = {2,2}
WR_TAG_EUTRA_FREQ_CFG       = {{900,18900},{2175,20175},{900,18900},{2175,20175}}
WR_TAG_NUM_UTRA_FDD_FREQ    = {1,1}
WR_TAG_UTRA_FDD_FREQ_CFG    = {{10713,23230},{10714,23231}}
WR_TAG_NUM_UTRA_TDD_FREQ    = {1,1}
WR_TAG_UTRA_TDD_FREQ_CFG    = {{10054,0,1},{9654,0,2}}
WR_TAG_CSG_SMCELL_PCI_START = 1
WR_TAG_CSG_SMCELL_PCI_RANGE = 100
WR_TAG_NO_OF_NGH_CFG        = {1,1}
WR_TAG_NGH_CELL_CFG         =
{{10.188.6.26,8,1,8,00102,900,18900,0,1,0,2,2,7,0,0,60,40},{10.188.6.28,9,2,9,00102,21
75,20175,0,1,0,2,2,7,0,0,60,40}}
WR_TAG_NO_OF_UTRA_FDD_NGH_CFG   = {1,1}
```

```
WR_TAG_NGH_UTRA_FDD_CELL_CFG    =
{{10,70,10713,23230,6,1,21901,145,45,0,1,1},{20,71,10714,23231,10,1,21901,150,50,0,1,1
}}
WR_TAG_NO_OF_UTRA_TDD_NGH_CFG   = {1,1}
WR_TAG_NGH_UTRA_TDD_CELL_CFG    =
{{30,80,10054,145,100,60,1,21901,45,0},{40,81,9654,150,100,61,1,21901,50,0}}
WR_TAG_NUM_CDMA_1XRTT_BAND_CLS = {1,1}
WR_TAG_CDMA_1XRTT_BAND_CLS     = {{1,1,1,1},{1,1,1,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_FREQ = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_FREQ     = {{1,1000,1},{1,1000,1}}
WR_TAG_NUM_CDMA_1XRTT_NEIGH_CELL = {1,1}
WR_TAG_CDMA_1XRTT_NEIGH_CELL     = {{1,1000,1,1,1},{1,1000,1,1,1}}
WR_TAG_CSFB_UTRA_CFG_VAL         = 0
WR_TAG_CSFB_CDMA_CFG_VAL         = 0
WR_TAG_ECSFB_CFG_VAL        = 0
WR_TAG_DUAL_RX_SUPPORTED    = 1
WR_TAG_DUAL_RX_TX_SUPPORTED = 0
WR_TAG_AS_PRI_INTG_ALGO_LST = {1}
WR_TAG_AS_PRI_CIPH_ALGO_LST = {1}
WR_TAG_ABS_A3_OFFSET        = -6
WR_TAG_PICO_OFFSET          = 20
WR_TAG_ABS_PATTERN_TYPE     = 2
WR_TAG_ABS_PATTERN          = 01010101010101010101010101010101010101010101
WR_TAG_ABS_LOAD_PERIODICITY = 0
WR_TAG_SFR_START_RB         = 25
WR_TAG_SFR_END_RB           = 49
WR_TAG_SFR_POWER_LOW        = 4
WR_TAG_SFR_POWER_HIGH       = 5
WR_TAG_DRX_ENABLED          = 0
WR_TAG_DRX_INACTIVITY_TMR   = 10
WR_TAG_DRX_RETX_TMR         = 1
WR_TAG_DRX_LONG_CYCLE_GBR   = 1
WR_TAG_DRX_LONG_CYCLE_NON_GBR = 5
WR_TAG_ANR_DRX_LONG_CYCLE   = 11
WR_TAG_ANR_DRX_ON_DURATION_TMR = 7
WR_TAG_ANR_DRX_INACTIVITY_TMR = 8
WR_TAG_DEFAULT_PAGING_CYCLE = 0
WR_TAG_DEFAULT_PCCH_CFG_NB  = 7
WR_TAG_BANDWIDTH            = {20,20}
WR_TAG_BOOT_MODE            = 0
WR_TAG_PWS_ETWS_CMAS_CNTRL = 0
WR_TAG_WATCHDOG_SOFT_LIMIT  = 5
WR_TAG_WATCHDOG_HARD_LIMIT  = 15
WR_TAG_LOG_PATH             = /var/log
WR_TAG_LOG_FILE             = dbglog
WR_TAG_LOG_MAX_FILES        = 3
WR_TAG_LOG_FILESIZE_LIMIT   = 5
WR_TAG_LOG_LEVEL            = 0
WR_TAG_LOG_MASK             = 0
WR_TAG_LOG_PORT             = 9999
WR_TAG_LOG_REMOTE_LOGGING   = 1
WR_TAG_LOG_CIRBUF_SIZE      = 3000
WR_TAG_LOG_COREDUMP_FLAG    = 1
WR_TAG_INT_FREQ_MEAS_GAP    = 0
WR_TAG_ANR_MEAS_GAP_CONFIG  = 0
WR_TAG_SRC_HO_CANCEL_TMR    = 40000
WR_TAG_CNM_ENABLED          = 0
WR_TAG_TA_TMR_CMN           = 7
WR_TAG_TA_TMR_DED           = 7
WR_TAG_GRP_PUCCH_PWR_CTRL_ENABLE = 0
```

```
WR_TAG_GRP_PUSCH_PWR_CTRL_ENABLE = 0
WR_TAG_RRM_SR_PRDCTY         = {4,4}
WR_TAG_RRM_CQI_PRDCTY        = {6,6}
WR_TAG_RRM_NUM_SR_PER_TTI    = {8,8}
WR_TAG_RRM_NUM_CQI_PER_TTI   = {8,8}
WR_TAG_RRM_N1_PUCCH          = {8,8}
WR_TAG_LTE_PUCCH_PWR_FMT3A_ENABLE = 0
WR_TAG_LTE_PUSCH_PWR_FMT3A_ENABLE = 0
WR_TAG_DRX_QCI_SUPPORT_ENABLED = 0
WR_TAG_SPS_ENABLE_FLAG       = 0
WR_TAG_DL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_UL_NUM_SPS_UE_PER_TTI = 1
WR_TAG_MAX_SPS_RB             = 10
WR_TAG_DSCP_ENABLE           = 0
WR_TAG_QCI_DSCP_MAP          = {152,120,104,72,180,44,12,4,4}
WR_TAG_CSG_CSG_ID            = 1234567
WR_TAG_CSG_ACCESS_MODE       = 1
WR_TAG_CSG_CSG_PCI_START     = 1
WR_TAG_CSG_CSG_PCI_RANGE     = 5
WR_TAG_CSG_HENB_NAME         = "RADISYS"
WR_TAG_MAX_AVG_GBRPRB_USAGE = 5
WR_TAG_DCFI_ENABLE           = 0
WR_TAG_CFI                   = 2
WR_TAG_RIM_CFG               = {86400000,5000,5000,5000,2}
WR_TAG_NUM_GERAN_NEIGH_FREQ = {0,0}
WR_TAG_GERAN_NEIGH_FREQ      = INVLD
WR_TAG_NUM_GERAN_NEIGH_CELL = {0,0}
WR_TAG_GERAN_NEIGH_CELL      = INVLD
WR_TAG_GERAN_MEAS_CFG        = INVLD
WR_TAG_CELL_SIZE_TYPE        = 0
WR_TAG_ARP_EMER_SERV         = 1
WR_TAG_GERAN_B2_RED_RSRP_THRSD1_VAL = 70
WR_TAG_GERAN_B2_RED_THRSD2_VAL    = 40
WR_TAG_GERAN_B2_HO_RSRP_THRSD1_VAL = 60
WR_TAG_GERAN_B2_HO_THRSD2_VAL    = 30
WR_TAG_WIRESHARK_PORT        = 9999
WR_TAG_WIRESHARK_DST_IP_ADDR = 192.168.1.10
WR_TAG_ANR_CELL_VALID_AGE_VAL = 0
WR_TAG_ENABLE_CA             = 0
WR_TAG_CELL_FREQ_CONTIGUOUS = 0
WR_TAG_TENB_STATS            = {1,0,1,50,8989}
WR_TAG_A4_RSRP_THRSHLD_VAL   = 60
WR_TAG_MEAS_SCELL_ADD_REL    = 0
WR_TAG_RT_MAC_SCH_CL_THRD_CORE = 6
WR_TAG_NRT_PDCP_GTP_THRD_CORE = 6
WR_TAG_RRC_APP_S1AP_THRD_CORE = 6
WR_TAG_WLS_DEVICE_NAME = /dev/wls
CFGEND                       = 1
#This CFGEND has to be kept at the end and should not be moved as the configuration
parameter reading ends once we read this tag. Any new configuration tag MUST be added
above CFGEND
```

Refer to Table 2, *Total eNodeB User Guide* provides detailed information on the configuration parameters available. Contact Radisys Customer support for a copy.

4.4 EPC*

Polaris EPC* v10.2.0-17 is used for the FlexRAN setup. An example configuration is provided below. Refer to Table 2, *Polaris EPC User Guides* for more information.

```
namespace eval ::config {

        variable version 10.2.0-17

        array set 10.233.180.160:5680 {
                emulatorType HSS
                expiry Perpetual
                hss,0x7f60f802a080 {intfSWm p4p1 portDiaSWd 3868 netmaskSWm 23
ipaddrSWm 10.233.180.163 portDiaSTa 3868 portDiaS6a 3868 portDiaZh 3868 ipaddrZh
10.233.180.163 portDiaCx 3868 host hss1.polaris-phy portDiaS6b 3868
HSSExtensiveDiameterValidation 0 intfSWd p4p1 ipaddrCx 10.233.180.163 ipaddress
10.233.180.163 netmaskSWd 23 intfSTa p4p1 realm epc.mnc001.mcc001.3gppnetwork.org intf
p4p1 ipaddrSWd 10.233.180.163 portDiaSWm 3868 netmaskSTa 23 intfZh p4p1 intfS6a p4p1
netmask 23 ipaddrSTa 10.233.180.163 intfS6b p4p1 intfCx p4p1 netmaskZh 23 netmaskS6a
23 netmaskS6b 23 netmaskCx 23 ipaddrS6a 10.233.180.163 ipaddrS6b 10.233.180.163 plmn
TestNetwork}
                hssSPRService,TestNetwork:1 {plmn TestNetwork serviceName Service-
IMS-Signalling1 serviceId 1 qci 5 precedence 1 ulMBR 0 dlMBR 0 ulGBR 0 dlGBR 0
piggybacked 0 pl 1 pci 0 pvi 0}
                hssSPRService,TestNetwork:2 {plmn TestNetwork serviceName Service-
Voice-2 serviceId 2 qci 1 precedence 4 sdfIdList 1 ulMBR 1024 dlMBR 1024 ulGBR 1024
dlGBR 1024 pl 2 pci 0 pvi 0 piggybacked 0}
                hssSPRServices {TestNetwork:1 TestNetwork:2}
                hsspdncontext,TestNetwork:PDN_Context_1 {pdnContextName PDN_Context_1
plmn TestNetwork apn intel.com pdnType 1 allowIMSService 1 imsDomainName TestNetwork
preferredSCSCF sip:scscf.TestNetwork:6060 pdnGw 10.233.180.162 apnAMBRUL 60000
apnAMBRDL 140000 defaultQCI 5 pl 1 pci 0 pvi 0 vPLMNAddressAllowed 0 ipv4AddressStart
10.10.10.1 ipv4AddressEnd 10.10.12.253 chargingCharacteristics 1 allowedServiceIdList
{1 2} serviceNameList {Service-IMS-Signalling1 Service-Voice-2}}
                hsspdncontexts TestNetwork:PDN_Context_1
                hsss,
                hsssdffilter,TestNetwork:1 {plmn TestNetwork serviceId 2 direction 3
flowDescription {permit out ip from 0.0.0.0/0  to 0.0.0.0/0 } sdfId 1 fcOctets
{{{Remote IPv4 Address} 0.0.0.0/0}}}
                hsssdffilters TestNetwork:1
                hssueprofile,TestNetwork:Subscription-Profile-1 {profileName
Subscription-Profile-1 plmn TestNetwork epsSubscribedCharging 2 epsambrul 60000
epsambrdl 140000 subscribedPDNList PDN_Context_1 defaultPDN PDN_Context_1
networkAccessMode 0 dataCapTotal 0 rateCutter 0 mpsPriorityLevel 0 relayNode 0
currency 840 accessRestriction 0 rfspId 0}
                hssueprofiles TestNetwork:Subscription-Profile-1
                hssuereg,TestNetwork:Subscription-Profile-1:1234567850
{operatorVariant dbc59adcb6f9a0ef735477b7fadf8374 allowedServiceIdList {1 2} nues 420
sharedKeyIncrement 0 sharedKeyStart 5e4ab35891375d2aee812e67c309a629 maximumCredit 50
opType 0 profileName Subscription-Profile-1 msisdnIncrement 1 chargingMethod 2
msinIncrement 1 msisdnStart 8800000001 msinStart 1234567850 mdtUserConsent 0 balance 0
plmn TestNetwork authAlgoType 0}
                hssueregs TestNetwork:Subscription-Profile-1:1234567850
                logLevel Information
                logSize 20
                plmn,TestNetwork {name TestNetwork mcc 001 mnc 01}
                plmns TestNetwork
                spr,TestNetwork:10.233.180.160:5680 {sprPort 5680 sprIP
10.233.180.160 mnc 01 mcc 001 plmn TestNetwork}
                sprs TestNetwork:10.233.180.160:5680
                version 10.2.0-17
        }

        array set 10.233.180.160:5682 {
                emulatorType MME
```

```
                expiry Perpetual
                logLevel Information
                logSize 20
                mme,0x7fb744007eb0 {MMEExtensiveDiameterValidation 0 intfM3 p4p1
netmaskSm 23 pgwRestart 1 serviceRestoration 1 intfS1MME p4p1 preferIPv4Address 1
netmaskS1MME 23 ipaddrS1MME 10.233.180.160 imsSupportIndication 1 nbrPGW
{{10.233.180.162 TestNetwork 2}} netmaskS3 23 intf p4p1 partialPathFailure 1 intfS10
p4p1 netmaskS6a 23 nodeIdType 0 intfS11 p4p1 nodeIdValue 10.233.180.160 intfS13 p4p1
{MME Group ID} 32768 ipaddrS102 10.233.180.160 netmaskM3 23 intfSGs p4p1 portSctp
36412 intfSBc p4p1 netmaskS102 23 modifyAccessBearer 1 portSBcAP 29168 plmn
TestNetwork ipaddrS10 10.233.180.160 ipaddrS11 10.233.180.160 {MME Code} 1 relayNode 1
ipaddrS13 10.233.180.160 ipaddress 10.233.180.160 intfS102 p4p1 nbrHSS {{TestNetwork
10.233.180.163 3868 0 epc.mnc001.mcc001.3gppnetwork.org}} ipaddrSGs 10.233.180.160
name mmec01.mmegi8000.mme intfS6a p4p1 ipaddrSBc 10.233.180.160 ipaddrSm
10.233.180.160 netmaskS10 23 netmaskS11 23 intfSm p4p1 netmaskS13 23 ipaddrS3
10.233.180.160 diaProxyPA2 0 intfS3 p4p1 netmaskSGs 23 relativeCapacity 1 nbrSGW
{{10.233.180.161 TestNetwork 1 2}} netmask 23 netmaskSBc 23 ipaddrM3 10.233.180.160
ipaddrS6a 10.233.180.160 diaRealm epc.mnc001.mcc001.3gppnetwork.org}
                mmes,
                plmn,TestNetwork {name TestNetwork mnc 01 poolAreas {poolArea,32768
{tacList 1 id 32768 mme 0x7fb744007eb0}} mcc 001}
                plmns TestNetwork
                version 10.2.0-17
        }

        array set 10.233.180.160:5683 {
                emulatorType PCRF
                expiry Perpetual
                logLevel Information
                logSize 20
                pcrf,0x7f5bb0000c00 {intfGx p4p1 netmaskGx 23 portDiaGxx 3868
diaProxyPA2 0 intfRx p4p1 PCRFExtensiveDiameterValidation 0 netmaskRx 23 sprIP
10.233.180.160 ipaddress 10.233.180.164 portDiaS9 3868 intfGxx p4p1 ipaddrS9
10.233.180.164 intf p4p1 netmaskGxx 23 portDiaGx 3868 sprPort 5680
imsConfigurationPresent 0 ipaddrGxx 10.233.180.164 ipaddrGx 10.233.180.164 netmask 23
diaHost pcrf1.ubuntu intfS9 p4p1 portDiaRx 3868 ipaddrRx 10.233.180.164 netmaskS9 23
plmn TestNetwork diaRealm epc.mnc001.mcc001.3gppnetwork.org}
                pcrfs,
                plmn,TestNetwork {name TestNetwork mcc 001 mnc 01}
                plmns TestNetwork
                version 10.2.0-17
        }

        array set 10.233.180.160:5684 {
                associatedpdnprofiles,0x7fe588000ca0 intel.com:TestNetwork
                emulatorType PGW
                expiry Perpetual
                logLevel Information
                logSize 20
                pdnprofile,intel.com@TestNetwork {plmn TestNetwork apn intel.com
pdnType 1 dhcpIPv4 10.233.180.162 primaryDnsIPv4 127.0.0.1 secondaryDnsIPv4 0.0.0.0
pcscfIPv4 10.233.180.164 imsiAuthRequired 0 apnType 2 subscriptRequired 0}
                pdnprofiles intel.com@TestNetwork
                pgw,0x7fe588000ca0 {interfaceSGi p4p1 preferIPv4Address 1 netmaskS5c
23 intfS2a p4p1 intf p4p1 ipaddrS5u 10.233.180.162 partialPathFailure 1 ipaddrGx
10.233.180.162 nodeIdType 0 netmaskSgi 23 netmaskS6b 23 pcrfDiaPort 3868 intfGx p4p1
nodeIdValue 10.233.180.162 intfS8u p4p1 ipaddrS8c 10.233.180.162 enableSGiNat 0
netmaskS5u 23 otherPolicy,0x7fe588000ca0 {bearerBindingOptions 0} ipaddrS2a
10.233.180.162 diaHost pgw1.polaris-phy nbrPCRF {{10.233.180.164 3868 132 1 1
epc.mnc001.mcc001.3gppnetwork.org}} peerRealm epc.mnc001.mcc001.3gppnetwork.org plmn
```

```
TestNetwork netmaskS8c 23 netmaskGx 23 pcrfNodeType 1 intfS5c p4p1 ipaddrS8u
10.233.180.162 portDiaS6b 3868 ipaddress 10.233.180.162 dhcpClientPortIPv6 546
netmaskS2a 23 pcrfProtocolID 132 intfSgi p4p1 intfS6b p4p1 netmaskS8u 23 diaProxyPA2 0
intfS5u p4p1 PGWModify {enableLoopback 1 enableFragmentation 1}
PGWExtensiveDiameterValidation 0 ipaddrS5c 10.233.180.162 portDiaGx 3868 netmaskv6Sgi
64 dhcpClientPort 67 netmask 23 ipaddrv6Sgi 1001:c023:9c17:9209::a02:de06 pcrfIP
10.233.180.164 intfS8c p4p1 ipaddrSgi 10.233.180.162 ipaddrS6b 10.233.180.162 diaRealm
epc.mnc001.mcc001.3gppnetwork.org}
                pgws,
                plmn,TestNetwork {name TestNetwork mcc 001 mnc 01}
                plmns TestNetwork
                version 10.2.0-17
        }
        array set 10.233.180.160:5685 {
                emulatorType SGW
                expiry Perpetual
                logLevel Information
                logSize 20
                plmn,TestNetwork {name TestNetwork mcc 001 mnc 01}
                plmns TestNetwork
                sgw,0x7fb9f0002a40 {nodeIdValue 10.233.180.161 intfS5S8u p4p1
netmaskS5S8c 23 SGWExtensiveDiameterValidation 0 ipaddrS1S4S12u 10.233.180.161
ipaddrS5S8c 10.233.180.161 pcrfNodeType 1 serviceRestoration 1 diaProxyPA2 0
pgwRestart 1 intfGxc p4p1 netmaskS5S8u 23 ipaddrS11S4c 10.233.180.161 ipaddrS5S8u
10.233.180.161 netmaskGxc 23 preferIPv4Address 1 ipaddrGxc 10.233.180.161 intfS1S4S12u
p4p1 ipaddress 10.233.180.161 intfS11S4c p4p1 realm epc.mnc001.mcc001.3gppnetwork.org
netmaskS1S4S12u 23 intf p4p1 pcrfProtocolID 132 netmaskS11S4c 23 partialPathFailure 1
netmask 23 modifyAccessBearer 1 pcrfIP 10.233.180.164 diaHost sgw1.ubuntu nbrPCRF
{{10.233.180.164 3868 132 1 1 epc.mnc001.mcc001.3gppnetwork.org}} nodeIdType 0
pcrfDiaPort 3868 intfS5S8c p4p1 plmn TestNetwork diaRealm
epc.mnc001.mcc001.3gppnetwork.org}
                sgws,
                version 10.2.0-17
        }

        variable emulators {{5680 10.233.180.160} {5682 10.233.180.160} {5683
10.233.180.160} {5684 10.233.180.160} {5685 10.233.180.160}}
}
```

4.5 File Transfer Protocol (FTP)

Use any regular File Transfer Protocol (FTP) server for FTP traffic generation between the UE and the core network. When setting up a TM500 emulator, the FTP server should allow many simultaneous connections. For example, the default configuration of the TM500 with the script provided below is 400 UEs that are RRC connected and 256 UEs running full-duplex traffic.

The FTP server must be configured to allow at least 256 FTP connections at the same time.

Alternatively, the D500* data generation and analysis tool can be used for traffic scenarios simulation.

NOTE: Additional information for configuring the D500 generation and analysis tool is out of the scope of this document and can be found in the D500 User Guide and corresponding documentation. The D500 User Guide is only available with the purchase of the D500 data generation and analysis.

4.6 Commercial UE (CUE)

Samsung S10 5GNR/LTE Band 2/13 TDD/FDD model #SM-G977U UEs are used for running scenarios with commercial UEs (CUE) (non-CA). All tests were conducted Over the Air (OTA).

The installation and configuration of the UEs are outside the scope of this document. A test SIM card is required, and its corresponding parameters must be added/updated to the EPC configuration file (for example, the IMSI and Authentication Key, etc.)

4.7 RRH

For FlexRAN 4G end-to-end demonstration, AceAxis* ART Radio test units are used. This section provides details of the physical set-up and configuration of these units for our supported scenarios.

4.7.1 2x2 RRH

Using a "null modem" cable connected to the front panel, configure the AceAxis* ART Radio (refer to Figure 7).

Figure 7. Front Panel 2x2 RRH

The serial port settings used are:

- Baud Rate: 115200 bps
- Data: 8 bits, no parity, 1 stop bit
- No flow control.

To log in, enter the following information:

- User: root
- Password: axis

The `tif` command processor should be used to specify the radio configuration.

For the 20 MHz Band 7* configuration with DL= 2655 MHz and UL=2535 MHz, the following script must be executed every time after power cycling the RRH:

```
# Set up for B7 LTE20, DL=2655 MHz, UL=2535 MHz
.rx.setEnable 1 off
.rx.setEnable 2 off
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.tx.setFreq 1 2655000
.tx.setFreq 2 2655000
.rx.setFreq 1 2535000
.rx.setFreq 2 2535000
```

```
.carrier.set 0 LTE20 TxPower=0 TxFreq=2655000 RxFreq=2535000 GroupUp=8 GroupDown=8
TxScaling=-14 TxContainer[0]=1 TxContainer[1]=9 RxContainer[0]=1 RxContainer[1]=9
.carrier.set 0 state=ENABLE

.tx.setIfatten 1 0
.tx.setRfatten 1 6
.tx.setEnable 1 on
.tx.setIfatten 2 0
.tx.setRfatten 2 6
.tx.setEnable 1 on
.tx.setEnable 2 on

.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on

.carrier.showall
```

If a different band is used, then the corresponding frequencies for the DL and UL must be adjusted. Refer to Table 2, ART Radio User Guide for additional information regarding the configuration of the radio.

NOTE: This radio is used for 1 Cell Non-CA scenarios only. It cannot be used with CA or 4x4 MIMO scenarios.

4.7.2 4x4 RRH

The 4x4 RRH consists of two radios connected to a multi-hop CPRI link (refer to Figure 8).

- The left side is radio 0
- The right side is radio 1

Figure 8. Front Panel 4x4 RRH

They are controlled and configured separately, in the same way as the 2x2 unit in Section 4.7.1., 2x2 RRH.

AceAxis ART Radio configuration is performed using a “null modem” cable connected to the rear panel (refer to Figure 9).

Figure 9. Rear Panel 4x4 RRH

To log in, enter the following information:

- User: **root**
- Password: **axis**

The `tif` command processor should be used to specify the radio configuration.

4.7.2.1 FDD CA with Two CCs (Component Carrier): 20 MHz Band2 and Band4

For the 20 MHz Band2 configuration with DL=1960 MHz, UL=1880 MHz, execute the following script once after power cycling the RRH on Radio 0:

```
# Set up for LTE20, DL=1960 MHz, UL=1880 MHz Radio 0
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=1960000 RxFreq=1880000 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=1 TxContainer[1]=9 RxContainer[0]=1 RxContainer[1]=9
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on
.carrier.showall
```

For the 20 MHz Band4 configuration with DL=2132.5 MHz, UL=1732.5 MHz, execute the following script once after power cycling the RRH on Radio 1:

```
# Set up for LTE10, DL=2132.5 MHz, UL=1732.5 MHz Radio 1
.rx.setEnable 1 off
.rx.setEnable 2 off
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=2132500 RxFreq=1732500 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=17 TxContainer[1]=25 RxContainer[0]=17
RxContainer[1]=25
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
```

```
.rx.setEnable 2 on
.carrier.showall
```

Refer to, Table 2, ART Radio User Guide for additional information regarding the radio configuration.

4.7.2.2 TDD CA with Two CC: 20 MHz Band40 and Band40

For the 20 MHz Band40 configuration with DL=2130 MHz, UL=2310 MHz, execute the following script once after power cycling the RRH on Radio 0:

```
# Set up for LTE20 TDD PCC, DL=2310 MHz, UL=2310 MHz Radio 0
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=2310000 RxFreq=2310000 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=1 TxContainer[1]=9 RxContainer[0]=1 RxContainer[1]=9
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on
.carrier.showall
```

For the 20 MHz Band40 configuration with DL=2323.8 MHz, UL=2329.8 MHz, execute the following script once after power cycling the RRH on Radio 1:

```
# Set up for LTE20 TDD CA SCC, DL=2329.8 MHz, UL=2329.8 MHz Radio 1
.rx.setEnable 1 off
.rx.setEnable 2 off
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=2329800 RxFreq=2329800 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=17 TxContainer[1]=25 RxContainer[0]=17
RxContainer[1]=25
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
```

```
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on
.carrier.showall
```

Additional information regarding the radio configuration can be found in Table 2, ART Radio User Guide.

4.7.2.3 FDD 4x2 MIMO: 20 MHz Band2

For the 20 MHz Band2 configuration with DL=1960 MHz, UL=1880 MHz, execute the following script once after power cycling the RRH on Radio 0:

```
# Set up for LTE20, DL=1960 MHz, UL=1880 MHz Radio 0
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=1960000 RxFreq=1880000 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=1 TxContainer[1]=9 RxContainer[0]=1 RxContainer[1]=9
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on
.carrier.showall
```

For the 20 MHz Band2 configuration with DL=1960 MHz, UL=1880 MHz, execute the following script once after power cycling the RRH on Radio 1:

```
# Set up for LTE10, DL=1960 MHz, UL=1880 MHz Radio 1
.rx.setEnable 1 off
.rx.setEnable 2 off
.tx.setEnable 1 off
.tx.setEnable 2 off
.carrier.set 0 state=DISABLE
.carrier.showall
.tx.setmode 1 modulated
.tx.setmode 2 modulated
.tx.resetFIFO 1
.tx.resetFIFO 2
.carrier.set 0 LTE20 TxPower=-25 TxFreq=1960000 RxFreq=1880000 GroupUp=8 GroupDown=8
TxScaling=-13.97 TxContainer[0]=17 TxContainer[1]=25 RxContainer[0]=17
RxContainer[1]=25
.carrier.set 0 state=ENABLE
.rx.setManAttenMode 1
.rx.setManAttenMode 2
.tx.setEnable 1 on
.tx.setEnable 2 on
.rx.setRfatten 1 0
.rx.setIfatten 1 10
```

```
.rx.setEnable 1 on
.rx.setRfatten 2 0
.rx.setIfatten 2 10
.rx.setEnable 1 on
.rx.setEnable 2 on
.carrier.showall
```

Additional information regarding the radio configuration can be found in Table 2, ART Radio User Guide.

The configuration of the RRH assumes that a cable connection between the eNodeB and UEs exists as described below. If different cable connections are used, additional changes in the radio configuration scripts above may be required to adjust the signal level.

4.7.2.4 Recommended 4x4 RRH Start-up Sequence after Power Cycle

1. Be sure the RRH and Ferry Bridge have power cycled.
2. Start the L1 and Start L2 applications.
3. Wait for the CPRI link and L1 TTIs prints.
4. Run the configuration radio script on Radio 0 and Radio 1.
5. Attach the UEs and start traffic as per the targeted LTE scenario.

   4x4 RRH does not require reconfiguration or power cycling between sessions of the eNodeB application.

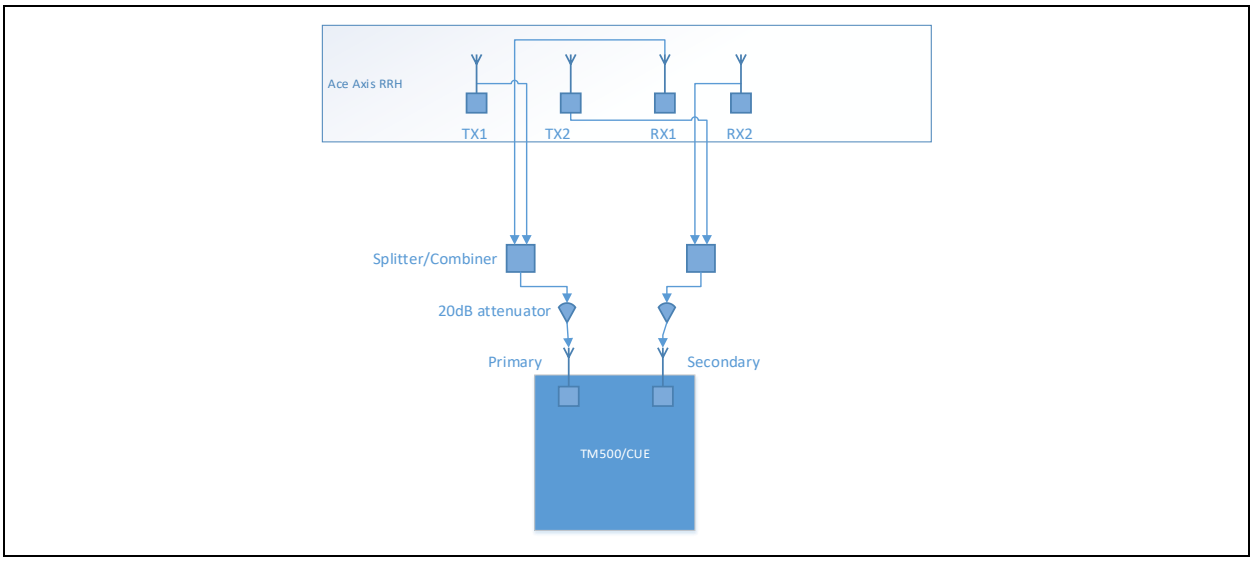
4.8 Cable Connections

This section provides recommended RF cable connections to run the LTE scenarios supported by FlexRAN successfully.

4.8.1 Single Cell 2x2 RRH with TM500/CUE

Figure 10 shows a single-cell cabled connection to either a TM500* emulator or one commercial UE.

Figure 10. FlexRAN RF Connection for 1 Cell Non-CA (2x2 RRH)

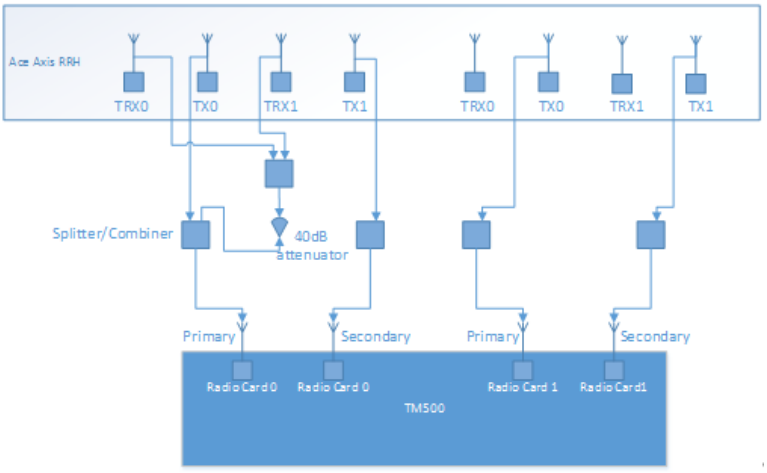


NOTE: The attenuation of 20 dB is required For a connection to a Commercial UE only.

4.8.2 CA Cell or 4x2 MIMO with 4x4 RRH with TM500*

A Carrier Aggregation (CA) or 4x2 MIMO cabled connection to a TM500* emulator is shown in Figure 11.

Figure 11. FlexRAN RF Connections for CA and 4x2 MIMO (4x4 RRH)



4.9 Viavi* TM500 Emulator

Notes:

1. The TM500* test scenario scripts used with the FlexRAN base code are too big to be included in this User Manual.
2. The user is expected to be familiar with the Viavi* TM500 system and have a good understanding of the configuration principles.

It is important to note specific items relating to the TM500 settings when compared to the default call procedure, which is provided with the equipment listed below:

1. PUSCH/PUCCH/RACH UL Power Offset has to be 80 dB.
2. UE Path loss has to be 10 dB.
3. UE TA has to be driven from UE0.
4. PRACH attempts should be limited to 1 per TTI.
5. For 4x2 `MIMO L1_DL_DATA_SYM_NORMALISE_METOD` set to 1.
6. PUCCH power control is off.

   Refer to Table 2, TM500 LTE TEST Mobile Application User Guide. If needed, reference the TM500 scripts used with the FlexRAN base code, which are available from your Intel Field Sales representative.

4.10 Recommended Start-up Sequence

The FlexRAN application performs the LTE eNodeB functionality in terms of the LTE Network. The following is the recommended start-up sequence for setup.

4.10.1 Setup Network Components Except for eNodeB

Set up and enable all the network components that are external to the LTE eNodeB according to the configurations described in the previous sections:

- EPC
- FTP server
- TM500/CUEs
- RRH
- Ferry Bridge

4.10.1.1 Start eNodeB

Refer to Section 4.4, EPC*, to start the EPC first before starting the eNodeB.

Enter the following commands to start eNodeB:

1. Start the VM.
2. Connect via SSH to VM and start L1.
3. Connect via SSH to VM and start L2.
4. Wait for the TTI ticks to be printed on the L1 console.
5. While the eNodeB is running, perform an attach procedure for all UEs.
6. Start the traffic scenario according to your requirements.

§

5.0 Packet Processing Hardware Offload

Hardware Offload was introduced in FlexRAN v1.4 to enable packet filtering on the NIC and facilitate separating packets based not only on the PCP field in VLAN Tag but primarily on the packet subtype. Filtering packets based on their subtypes allows for separating different types of control packets as well as all types of data packets existing in one mode. Packets of different subtypes are directed to separate queues.

Hardware Offload in FlexRAN v1.4 works in the CPRI and LTE modes. In the CPRI mode, two types of data packets are separated on the NIC: Timing and CPRI packets. In the LTE mode, three data packet types are distinguished on the NIC and sent to separate queues (Timing, PUSCH, and PRACH).

This filtering can be achieved with the application of a Fortville Dynamic Device Personalization (DDP) profile called DPR-009 Radio Fronthaul that was generated strictly for this purpose. The profile adds new `PCTYPES` to Fortville, one PCTYPE per packet subtype. As a result, 13 new `PCTYPES` are added. The profile must be installed on a Fortville DDP so it can perform packet filtering based on the new `PCTYPES`.

Table 3. Packet Subtypes Filtered in CPRI Mode

CPRI Mode Packet Sub-Type	Sub-Type
Timing Packet	0x0003
CPRI Data Packet	0x0006
Control Specific Register Packet	0x0008
Present Broadcast Packet	0x0009

Table 4. Packet Subtypes Filtered in LTE Normal Mode

CPRI Mode Packet Sub-Type	Sub-Type
Timing Packet	0x0003
Control Specific Register Packet	0x0008
Present Broadcast Packet	0x0009
PUSCH Packet	0x000B
PRACH Packet	0x000C

5.1 NIC Offload, Legacy Implementation, and Single Queue Mode

There are three alternatives for handling packet filtering:

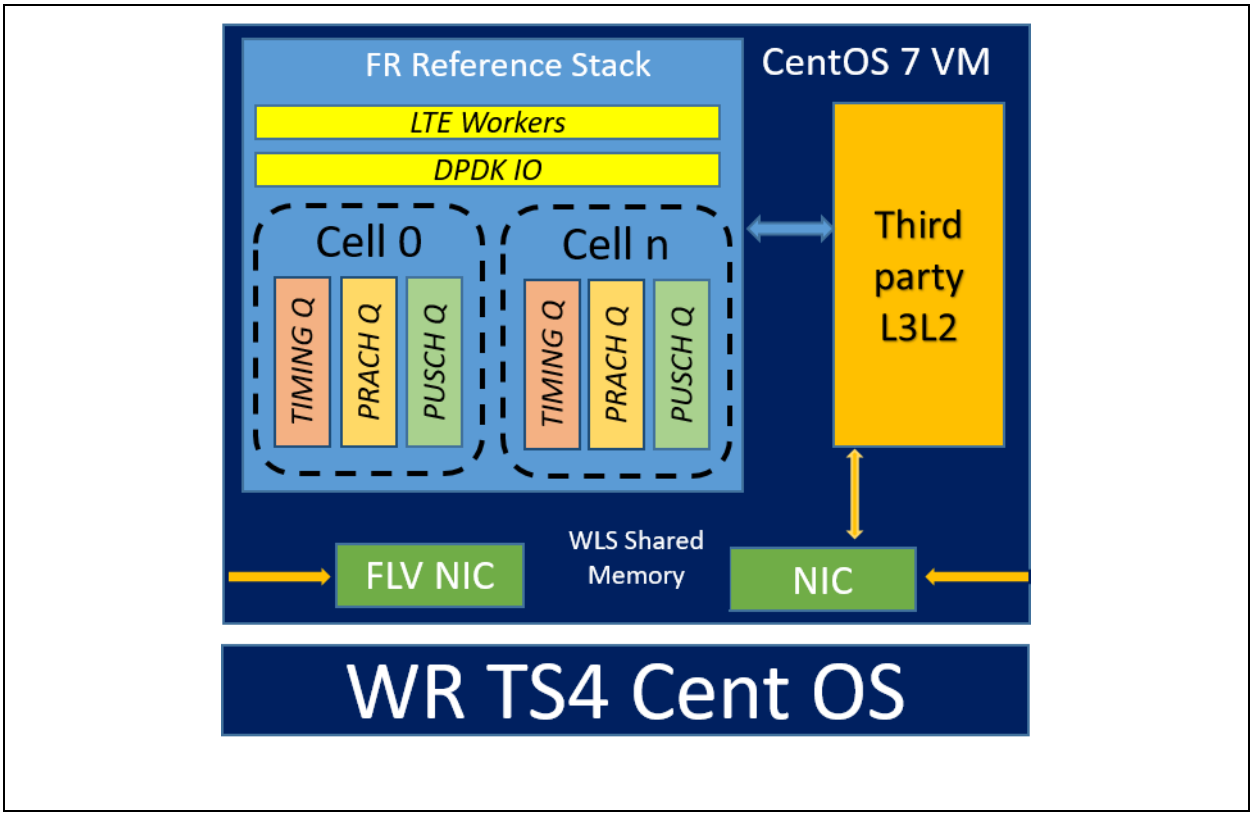
- NIC Offload
- Legacy implementation
- Single Queue Mode

5.1.1 Flexibility and Scalability Support with NIC Offload

- Pre-Classification on the NIC was done compared to CPU
- Support for 13 Fronthaul (FH) packet types which maps to individual queues per cell: `PDSCH, PDCCH, PBCH, TIMING, PSS, RS, CPRI_DATA, TIME_DOMAIN, CONTROL, BROADCAST, MANAGEMENT, PUSCH` and `PRACH`
- Efficient Scaling of FH I/O core is still maintaining Real-time and high bandwidth.

- Using FLV DDP profile and `rte_flow()`.
- Support for Ferry Bridge-based FH.
- Paves the way for 5G NR FH, Backhaul, and MEC deployments.
- Profile not distributed as part of the package.

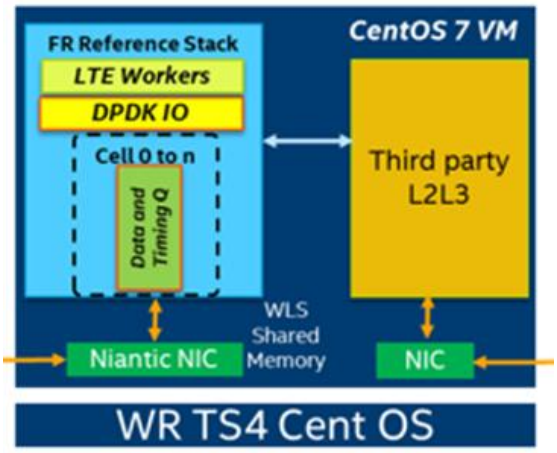
Figure 12. Packet Subtype-based Filtering with Fortville DDP Profile, Offloaded to NIC



5.1.2 Legacy Implementation

- Single Port/Queue servicing data and timing of all cells
- DPDK IO core executes classification
- Chances of the head of the line blocking and Max latency jitter when there are many cells and mix loaded cells
- Support for the 10 G Niantic NIC

Figure 13. Packet Type-based Filtering Performed on CPU



5.1.3 Single Queue Mode

In FlexRAN v18.09, a Single Queue mode was introduced next to the Hardware Offload and Legacy Implementation. The Single Queue mode allows the L1 application to send/receive all types of packets using a single Tx/Rx queue. The Single Queue L1 is supported on both the Niantic and Fortville NIC. The Single Queue mode disables packet filtering both through the NIC offload and `VMDQ_DCB`.

5.2 Hardware Offload Prerequisites

FlexRAN setup for Hardware Offload has the following requirements:

- Intel Fortville 10/40 Gigabit Ethernet Controller NIC v6.
- DPDK v19.11
- Fortville DDP Profile (DPR-009 Radio FH)

5.2.1 Update NVM Image on Intel® Fortville 10/40 to v6

Check the NVM image version on the network card.

5.2.2 Restarting System eNodeB

1. Exit from the L2 application (type "**q**" on the L2 console).
2. Exit from the L1 application (type "**exit**" on L1 console).
3. Power on Ferry Bridge.
4. Start eNodeB again as per item.

NOTE: It is not necessary to restart the VM between running eNodeB sessions. Restarting the L2 and L1 applications is sufficient.

```
ethtool -i ethX
driver: i40e
version: 1.5.10-k
firmware-version: 6.01 0x80003484 1.1747.0
```

```
expansion-rom-version:
bus-info: 0000:07:00.0
supports-statistics: yes
supports-test: yes
supports-eeprom-access: yes
supports-register-dump: yes
supports-priv-flags: yes
```

If the firmware version is below 6.xx, it needs to be updated.

5. Get the Node Version Manager (NVM) v6.01 update for Intel Ethernet Adapters—Linux* from the following: https://downloadcenter.intel.com/download/25791/Non-Volatile-Memory-NVM-Update-Utility-for-Intel-Ethernet-Adapters-Linux-.

   The NVM v6.01 update is packed into the `NVMUpdatePackage.zip` folder. Extract the files into the NVM folder. Then, (for Linux* x64 systems) inside the NVM folder, find and extract `XL710_NVMUpdatePackage_v6_01_Linux.tar.gz` file. Next, go to `./XL710/Linux_x64` and change the permissions on the `nvmupdate64e` file:

```
chmod 755 nvmupdate64e
```

6. Then, run the file:

```
./nvmupdate64e
```

   It lists all identified NIC devices on the system and their firmware versions.

```
Intel(R) Ethernet NVM Update Tool
NVMUpdate version 1.30.2.11
Copyright (C) 2013 - 2017 Intel Corporation.

WARNING: To avoid damage to your device, do not stop the update or reboot or power
off the system during this update.
Inventory in progress. Please wait [.+********]

Num Description                                 Ver.  DevId S:B    Status
=== ========================================= ===== ===== ====== ===============
01) Intel(R) 82599 10 Gigabit Dual Port      48.20  10FB 00:002 Update not
available
                     Network Connection
02) Intel(R) I350 Gigabit Network Connection  1.99  1521 00:004 Update not
available
03) Intel(R) Ethernet Converged Network       5.05  1572 00:007 Update available
    Adapter X710-4
```

7. Verify the Intel® Ethernet Converged Network Adapter X710's version is at least v6.01.

   If the version is older than v6.01, the words "*update available*" should be displayed next to it. Then, follow the prompts to update the NVM image on the device.

8. Once finished, power off the system. Remove the power cable for several seconds and power it on again.

   To verify that the firmware was updated successfully, use the above ethtool command, or rerun this: `./NVM/XL710/Linux_x64/nvmupdate64e`.

```
Num Description                                 Ver.  DevId S:B    Status
=== ========================================= ===== ===== ====== ===============
01) Intel(R) 82599 10 Gigabit Dual Port      48.20  10FB 00:002 Update not
available
                     Network Connection
02) Intel(R) I350 Gigabit Network Connection  1.99  1521 00:004 Update not
available
03) Intel(R) Ethernet Converged Network       6.01  1572 00:007 Update available
```

```
    Adapter X710-4
```

5.2.3 DDP Profile

To get the required DDP profile, contact your local Intel representative.

The DPR-009 Radio FH profile needs to be loaded into Fortville.

5.2.3.1 Loading/unloading DDP Profile

The DDP profile can be loaded onto the NIC using the DPDK `testpmd` application.

1. Start `testpmd`, for example:
   ```
   sudo ./testpmd -l 0-3 -n 4 -- -i --portmask=0x3 --nb-cores=2
   ```
2. Stop port(s) you want to load the profile to, using command "`port stop (port_id|all)`" to stop one or all ports, for example:
   ```
   testpmd>port stop 0
   ```
   The DDP profile is stored in `radiofh4g.pkgo` and the original configuration is stored in the `radiofh4g.bak` file.
3. Use the command ddp add (`port_id`) (`profile_path[,output_path]`) to load the profile, for example:
   ```
   testpmd>ddp add 0 radiofh4g.pkgo, radiofh4g.bak
   ```
4. Verify the profile was loaded successfully with the command "`ddp get list (port_id)`", for example:
   ```
   testpmd>ddp get list 0
   ```
   The `ddp` profile should appear within the output.
5. Close the `testpmd` application:
   ```
   testpmd>quit
   ```
   To unload the profile, start the `testpmd` application as above, stop the ports again, and use the command "`ddp del (port_id) (profile_path)`":
   ```
   testpmd>ddp del 0 "/root/radiofh4g.pkgo"
   ```

5.3 Test Setup for FlexRAN with Hardware Offload

Hardware Offload in FlexRAN was tested on a setup built of a Broadwell server with the X710 NIC connected through the PCI to Ferry Bridge (refer to Figure 14). In this setup, Ferry Bridge is connected to the optical loopback interface. The Broadwell server is sending the Ethernet traffic through Fortville to Ferry Bridge, and Ferry Bridge is changing it to CPRI and sending it back to the server through the loopback (refer to Figure 15).

In the test scenarios, Ferry Bridge used 4x4 `rec_re` and `rec_rec` images (`fbr_fpga_wrap_4x4_rec_re.jic` and `fbr_fpga_wrap_4x4_rec_rec.jic`).

Figure 14. Test Setup for Hardware Offload

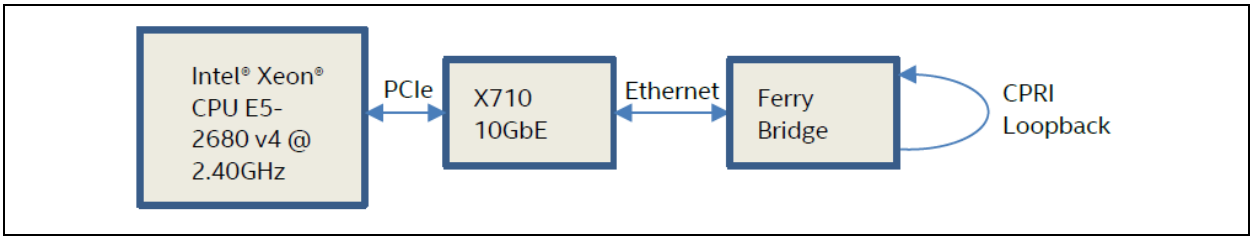
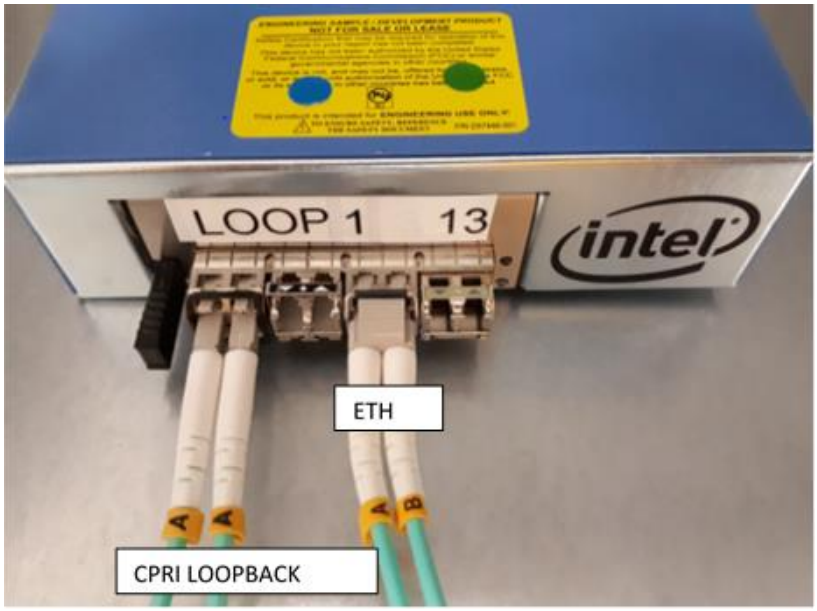


Figure 15. Ferry Bridge Cabling



The setup was tested in two modes: CPRI mode and LTE normal mode.

NOTE: The CPRI mode should be tested with the 4x4 `rec_rec` image installed on the Ferry Bridge. The LTE normal mode should be tested with the 4x4 `rec_re` image.

Before running the tests, the configuration file used with the radio mode "phycfg.xml" stored in the "`./lte_phy`" directory must be amended following the instructions given in the following sections. Then, build the FlexRAN with hardware offload (Section 5.4, Build FlexRAN for Hardware Offload, Build FlexRAN for Hardware Offload) or without the hardware offload, in the legacy mode (Section5.5, Build FlexRAN in the Legacy Mode) and the run tests (Section 5.7, Test Examples).

5.3.1 Testing Configuration for CPRI Mode

Adjust the configuration in the `phycfg.xml` file. Change `ferryBridgeMode` to **1** and `ferryBridgeOptCableLoopback` to **1**. If using port 0, leave `ferryBridgeEthPort` set to **1**.

```
<radioEnable>1</radioEnable>           <!-- Enable/disable radio [0 - disable
(external app control radio), 1 - use Lib-Radio, 2 - use phy app (obsolete)] -->
 <dpdkMemorySize>6144</dpdkMemorySize> <!--  DPDK memory size allocated from hugepages
[MB]  [default: 2048] -->
 <dpdkIrqMode>0</dpdkIrqMode>          <!--  DPDK Interrupt mode enable        [0 -
disabled, PMD is used, 1 - enabled, uio irq is used] -->
<ferryBridgeMode>1</ferryBridgeMode>   <!--  Ferry Bridge (FB) mode [0 - LTE MODE, 1 -
CPRI BYPASS MODE] -->
 <ferryBridgeEthPort>1</ferryBridgeEthPort> <!--  Number of Ethernet ports on FB    [0
- DPDK port 0, 1 - DPDK port 1, 2 - both DPDK port 0 and port 1 (CA mode with two
ETH)] -->
 <ferryBridgeSyncPorts>0</ferryBridgeSyncPorts> <!--  FB Synchronized CPRI ports
[0 - no reSync REC & RE FPGA, 1 - reSync REC & REC FPGA] -->
 <ferryBridgeOptCableLoopback>1</ferryBridgeOptCableLoopback>  <!--  FB Loopback Mode
[0 - no optical loopback connected REC<->RE, 1 - optical loopback connected REC<->RE]
-->
```

For RadioConfig0, change RadioCfg0PCIeEthDev so it matches the DPDK device to be used in the test.

```
<RadioConfig0>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg0PCIeEthDev>0000:09:00.0</radioCfg0PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg0DpdkRx>1</radioCfg0DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg0DpdkTx>2</radioCfg0DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg0TxAnt>4</radioCfg0TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg0RxAnt>4</radioCfg0RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg0RxAgc>0</radioCfg0RxAgc>
            <!--  Number of cells running on this port [1 - Cell , 2 - Cells ] -->
            <radioCfg0NumCell>1</radioCfg0NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg0Cell0PhyId>0</radioCfg0Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg0Cell1PhyId>1</radioCfg0Cell1PhyId>
         </RadioConfig0>
```

5.3.2 Testing Configuration for LTE mode

Use Ferry Bridge 4x4 `rec_re` image.

Adjust the configuration in the file `phycfg.xml`. Change `ferryBridgeMode` to **0** and `ferryBridgeOptCableLoopback` to **1**. If using port 0 leave `ferryBridgeEthPort` set to **1**.

```
<radioEnable>1</radioEnable>          <!-- Enable/disable radio [0 - disable (external
app control radio), 1 - use Lib-Radio, 2 - use phy app (obsolete)] -->
<dpdkMemorySize>6144</dpdkMemorySize> <!--  DPDK memory size allocated from hugepages
[MB]  [default: 2048] -->
<dpdkIrqMode>0</dpdkIrqMode>          <!--  DPDK Interrupt mode enable        [0 -
disabled, PMD is used, 1 - enabled, uio irq is used] -->
<ferryBridgeMode>0</ferryBridgeMode>  <!--  Ferry Bridge (FB) mode            [0 - LTE
MODE, 1 - CPRI BYPASS MODE] -->
<ferryBridgeEthPort>1</ferryBridgeEthPort> <!--  Number of Ethernet ports on FB    [0
- DPDK port 0, 1 - DPDK port 1, 2 - both DPDK port 0 and port 1 (CA mode with two
ETH)] -->
<ferryBridgeSyncPorts>0</ferryBridgeSyncPorts> <!--  FB Synchronized CPRI ports
[0 - no reSync REC & RE FPGA, 1 - reSync REC & REC FPGA] -->
<ferryBridgeOptCableLoopback>1</ferryBridgeOptCableLoopback>  <!--  FB Loopback Mode
[0 - no optical loopback connected REC<->RE, 1 - optical loopback connected REC<->RE]
-->
```

5.4 Build FlexRAN for Hardware Offload

Build the l1 app:

```
cd ./build/lte/l1app
./build.sh xclean && ./build.sh AVX2 HO_ENABLED
```

5.5 Build FlexRAN in the Legacy Mode

Rebuild the l1 app to work in the legacy mode:

```
cd ./build/lte/l1app
./build.sh xclean && ./build.sh AVX2
```

5.6 Build FlexRAN in Single Queue Mode

Rebuild the l1 app in Single Queue Mode:

```
cd ./build/lte/l1app
./build.sh xclean && ./build.sh AVX2 SINGLE_QUEUE
```

5.7 Test Examples

NOTE: To test FlexRAN in legacy mode, use the Niantic network card. Testing the hardware offload requires a Fortville NIC.

5.7.1 CPRI Mode

1. Navigate to `/bin/lte/l1` and start the script:
   ```
   ./l1.sh
   ```
2. Wait for the command line to appear on the screen. Then choose the test to run:
   ```
   frbtest 1000
   ```
3. Wait for the test to finish, and exit the command line:
   ```
   exit
   ```

5.7.2 LTE Mode

1. Navigate to . /bin/lte/l1 and start the script:
   ```
   ./l1.sh
   ```
2. Wait for the command line to appear on the screen. Then, choose the test to run:
   ```
   frblte 1000
   ```
3. Wait for the test to finish, and exit the command line:
   ```
   Exit
   ```

§

Appendix A Other FlexRAN Configuration

This section provides the setup of the DPDK and possibly flash a new FPGA image to FerryBridge Front Haul.

A.1 DPDK v19.11 for FlexRAN Configuration

This section contains an example of the `dpdk.sh` file included in the release package.

Configuration of DPDK v19.11 for FlexRAN application:

```
#cat  /opt/vm/dpdk.sh

#! /bin/bash
export RTE_SDK=/opt/dpdk-19.11
export RTE_TARGET=x86_64-native-linuxapp-icc

#
# Unloads igb_uio.ko.
#
remove_igb_uio_module()
{
    echo "Unloading any existing DPDK UIO module"
    /sbin/lsmod | grep -s igb_uio > /dev/null
    if [ $? -eq 0 ] ; then
        sudo /sbin/rmmod igb_uio
    fi
}

#
# Loads new igb_uio.ko (and uio module if needed).
#
load_igb_uio_module()
{
    if [ ! -f $RTE_SDK/$RTE_TARGET/kmod/igb_uio.ko ];then
        echo "## ERROR: Target does not have the DPDK UIO Kernel Module."
        echo "       To fix, please try to rebuild target."
        return
    fi

    remove_igb_uio_module

    /sbin/lsmod | grep -s uio > /dev/null
    if [ $? -ne 0 ] ; then
        if [ -f /lib/modules/$(uname -r)/kernel/drivers/uio/uio.ko ] ; then
            echo "Loading uio module"
            sudo /sbin/modprobe uio
        fi
    fi

    # UIO may be compiled into kernel, so it may not be an error if it can't
    # be loaded.

    echo "Loading DPDK UIO module"
```

```
    sudo /sbin/insmod $RTE_SDK/$RTE_TARGET/kmod/igb_uio.ko
    if [ $? -ne 0 ] ; then
        echo "## ERROR: Could not load kmod/igb_uio.ko."
        quit
    fi
}

load_igb_uio_module

CPU_FEATURES_DETECT=`cat /proc/cpuinfo |grep hypervisor | wc -l`

if [ "$CPU_FEATURES_DETECT" -eq "0" ]
then
VM_DETECT='HOST'
echo ${VM_DETECT}
else
VM_DETECT='VM'
echo ${VM_DETECT}
fi

$RTE_SDK/usertools/dpdk-devbind.py --status
if [ ${VM_DETECT} == 'HOST' ]; then
    #HOST
    $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:09:00.0
#   $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:03:00.1
#   $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:05:00.0
#   $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:05:00.1
else
    #VM
    $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:00:04.0
    $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:00:05.0
    $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:00:06.0
    $RTE_SDK/usertools/dpdk-devbind.py --bind=igb_uio 0000:00:07.0
fi

$RTE_SDK/usertools/dpdk-devbind.py --status
```

A.2 Updating FPGA Image

The Electronically Erasable Programmable Read-Only Memory (EEPROM) that stores the FPGA image in the Ferry Bridge module can be updated using the embedded USB-Blaster* functionality on the FPGA and the Altera® Quartus* programming tool. The Intel® Quartus® Programmer can be installed on the server. Intel uses v13.1.

A.2.1 Obtain the Intel® Quartus ® Programmer Installer

The Intel® Quartus® Programmer can be downloaded for free from the Altera website at the following location:

http://dl.altera.com/?product=qprogrammer#tabs-4

To download the tool, you must first register with Altera®.

1. On the download portal, click the Additional Software tab.
2. Select **Intel® Quartus® II Programmer and Tools** and **save** the `QuartusProgrammerSetup-13.1.0.162.run file`. (Download a later version. Intel uses v13.1.)
3. Log in to the Host UE server (make sure you are not logged in to VM.)

4. Create the directory `/opt/altera/`.
5. Copy the `QuartusProgrammerSetup-13.1.0.162.run` file to the `/opt/altera` directory on the Host UE server.
6. Enter `cd /opt/altera`.
7. Enter "`chmod 755 QuartusProgrammerSetup-13.1.0.162.run`".
8. Install the software:
   a. Enter"`./QuartusProgrammerSetup-13.1.0.162.run`".
   b. Press **Enter** several times to scroll through the license agreement and enter **accept** at the final prompt.
9. Select the install directory to be `/opt/altera/`.

The command-line version of the Altera tool is now installed at `/opt/altera/`.

§

Appendix B Upgrade the FPGA Image

The R1. v1.0 FPGA image is located at `/opt/altera/fpga_bin`.

To upgrade the FPGA EEPROM image on the Ferry Bridge perform the following procedure:

1. Connect the USB cable to the micro-USB port at the rear of the Ferry Bridge.
2. Connect the USB cable to the USB port on the host.
3. The `.jic` image file is located in the `/opt/intel/fpga_bin` directory on the host eNodeB server.

   Edit the `AMC_EEPROM.cdf` file to point to the updated `.jic` image file.

```
/opt/altera/fpga_bin# cat ./AMC_EEPROM.cdf
/* Quartus II 64-Bit Version 13.1.4 Build 182 03/12/2014 SJ Full Version */
JedecChain;
Altera is a trademark of Intel Corporation or its subsidiaries.
        FileRevision(JESD32A);
        DefaultMfr(6E);

        P ActionCode(Cfg)
                Device PartName(5SGXEA7K2) Path("/opt/altera/fpga_bin/")
File("new_image.jic") MfrSpec(OpMask(1) SEC_Device(EPCQ256) Child_OpMask(1 1));

ChainEnd;
```

4. Execute the following command to verify connectivity with the FPGA and identify the USB port utilized. (USB-Blaster [1-1.4] is shown in the example below.)

```
/opt/altera/qprogrammer/bin/quartus_pgm -a
```

5. Execute the Intel® Quartus® programming command:

```
/opt/altera/qprogrammer/bin/quartus_pgm -c \"USB-Blaster [1-1.4]\"
/opt /intel/fpga_bin/AMC_EEPROM.cdf
```

   The programming process takes approximately 15 minutes.

```
/opt/altera/13.1/qprogrammer/bin/quartus_pgm -c \"USB-Blaster [1-1.4]\"
/opt/altera/fpga_bin/AMC_EEPROM.cdf
/opt/altera/13.1/qprogrammer/adm/qenv.sh: line 83: warning: setlocale: LC_CTYPE:
cannot change locale (en_US.UTF-8): No such file or directory
Info: ******************************************************************
Info: Running Quartus II 32-bit Programmer
    Info: Version 13.1.0 Build 162 10/23/2013 SJ Full Version
    Info: Copyright (C) 1991-2013 Altera Corporation. All rights reserved.
    Info: Your use of Altera Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Altera Program License
    Info: Subscription Agreement, Altera MegaCore Function License
    Info: Agreement, or other applicable license agreement, including,
    Info: without limitation, that your use is for the sole purpose of
    Info: programming logic devices manufactured by Altera and sold by
    Info: Altera or its authorized distributors.  Please refer to the
    Info: applicable agreement for further details.
    Info: Processing started: Wed Sep 28 01:36:12 2016
```

```
Info: Command: quartus_pgm -c "USB-Blaster [1-1.4]"
/opt/altera/fpga_bin/AMC_EEPROM.cdf
Info (213045): Using programming cable "USB-Blaster [3-2]"
Info (213011): Using programming file /opt/altera/fpga_bin/new_image.jic with
checksum 0x6D73E974 for device 5SGXEA7K2@1
Info (209060): Started Programmer operation at Wed Sep 28 01:36:46 2016
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x029030DD
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209018): Device 1 silicon ID is 0x19
Info (209044): Erasing ASP configuration device(s)
Info (209023): Programming device(s)
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Wed Sep 28 01:41:07 2016
Info: Quartus II 32-bit Programmer was successful. 0 errors, 0 warnings
    Info: Peak virtual memory: 974 megabytes
    Info: Processing ended: Wed Sep 28 01:41:07 2016
    Info: Elapsed time: 00:04:55
    Info: Total CPU time (on all processors): 00:00:43
```

6. Once completed, remove the USB cable, and power-cycle the FPGA to load the updated configuration from the EEPROM to the FPGA.

§