FlexRAN 5G New Radio Reference Solution L1

User Guide

March 2021

Intel Confidential

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Revision History

Revision	Description	Date
9.0	Updates for FlexRAN Software Release v21.03 • Added Section 4.4, Wilson City Server with icelake-SP Setting	March 2021
8.0	Updates for FlexRAN Software Release v20.11 • Updated location of MSR-Tools source code in Section 1.3. • Updated explanation about TDP setting in BIOS in Section 4.1.1. • Updated Section 4.1.3, Check OS Version. • Updated Section 4.3.2, Cmdline Setting.	November 2020
7.0	Updates for FlexRAN Software Release v20.04: • Section 3.0, updated with xRAN FH connection. • Section 4.1.3, Step 6, updated.	April 2020
6.0	Updates for FlexRAN Software Release v20.02: • Updated Section 2.0 with a new configuration. • Updated Section 4.1 with more specific headings and instructions for a new configuration. A new accompanying code for new configuration has been included. • Added Section 4.2, Wolf Pass Server with Cascade Lake-SP Settings. • Updated Section 4.3 with more specific headings and instructions for the new configuration.	February 2020
5.0	Updates for FlexRAN Software Release v19.10: • Added Section 4.2, SuperMicro Server Setting • Added Section 4.2.1. GUI BIOS Settings • Added Figure 22 through Figure 30	October 2019
4.0	Update for release v19.06: Section 2.0 Updated references for release features	July 2019
3.0	Update for release v19.03	April 2019
2.0	Update for release v18.12	December 2018
1.0	Initial release	October 2018

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1.0 Introduction

This document introduces the FlexRAN 5G New Radio (NR) system architecture and describes how to set up the system. The document scope is limited to describing the NR stand-alone setup only and is not intended to explain how to connect to a Remote Radio Unit (RRU).

1.1 Intended Audience

The intended audience for this document is designers and engineers working with the FlexRAN 5G NR release.

1.2 Terminology

Table 1. Terminology

Term	Description
DPDK	Data Plane Development Kit
FEC	Forward Error Correction
FH	Front Haul
FPGA	Field Programmable Gate Array
GRUB	GRand Unified Bootloader
GUI	Graphical User Interface
ICC	Intel C++ Compiler
MmWave	Millimeter-Wave
MSR	Model-Specific Register
NR	New Radio
OS	Operating System
PCIe*	Peripheral Component Interconnect express*
QSFP	Quad Small Form Factor Pluggable
RAS	Reliability, availability, and serviceability
RRU	Remote Radio Unit
TUB	Timing and UART Board
UEFI	Unified Extensible Firmware Interface
xRAN	Extensible Radio Access Network

1.3 References and Resources

Table 2. References and Resources

Document Title	Document No. /Location
FlexRAN Reference Solution Software Release Notes	575822
FlexRAN and Mobile Edge Compute (MEC) Platform Setup Guide	576898
FlexRAN 5G NR Reference Solution L2-L1 API	603575
FlexRAN 5G NR Reference Solution RefPHY (Doxygen)	603577
FlexRAN 5G New Radio FPGA User Guide	603578
xRAN Front Haul Software Architecture Specification	611268
Intel® Quartus® Prime Pro Edition Version 18.1 Software and Device Support Release Notes (Doc # RN-01082-18.1.0)	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/rn/archives/rn-qts-pro-dev-support-18.1.pdf
MSR-Tools Source Code	https://github.com/intel/msr-tools
Quartus Prime Standard Edition	http://fpgasoftware.intel.com/18.1/?edition=standard&platform=windows&download_manager=dlm3

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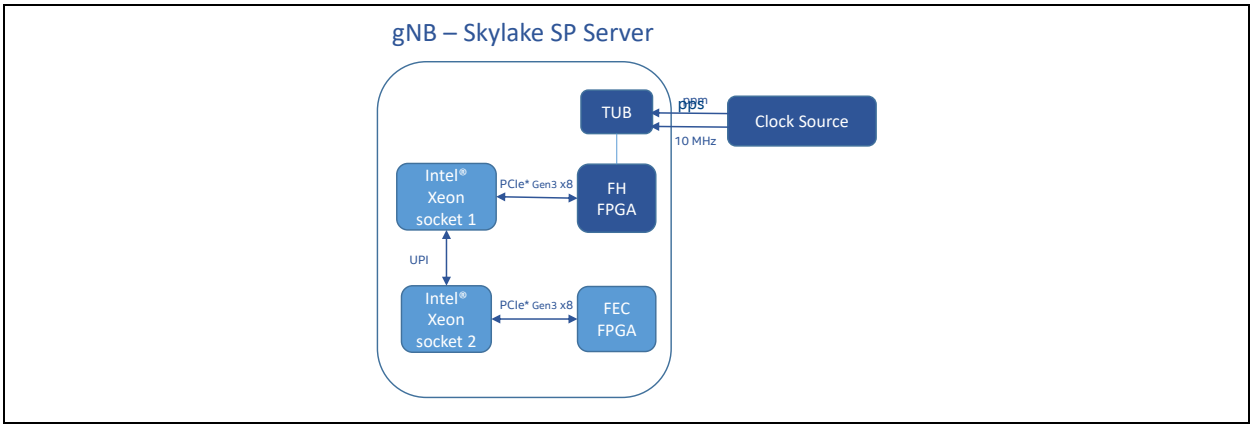
2.0 System Overview

For the FlexRAN 5G NR release features, refer to *FlexRAN Reference Solution Software Release Notes*, Section 2, in Table 2.

2.1 Front Haul Connection with FPGA

Figure 1 illustrates the system configuration for the Millimetre Wave (MmWave) system.

Figure 1. MmWave System Configuration

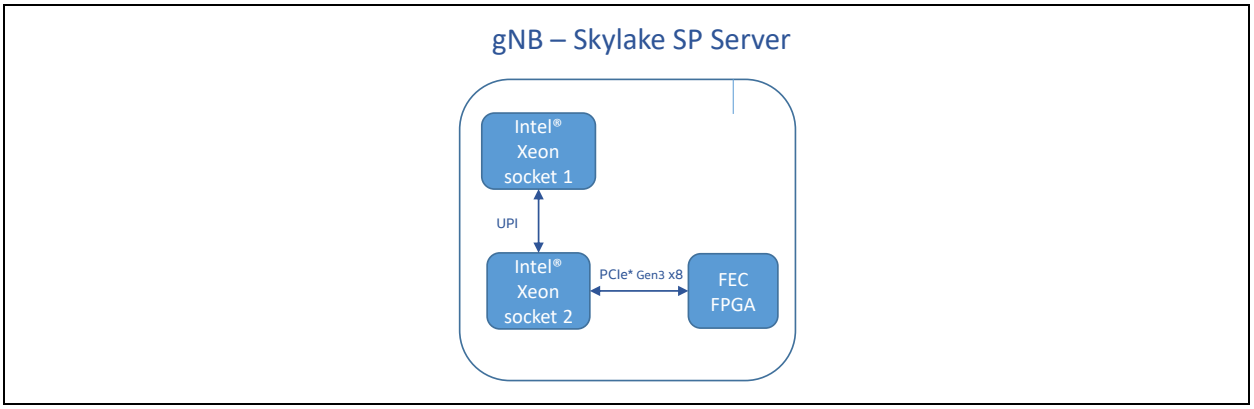


The Front Haul (FH) Field Programmable Gate Array (FPGA) is responsible for data transferring and time synchronization.

Note: FH FPGA is connected to CPU through Peripheral Component Interconnect express* (PCIe*), and it is connected to the external clock source TUB through COM. Refer to the FlexRAN 5G New Radio FPGA User Guide in Table 2 as the FPGA configuration is not in the scope of this document.

Figure 2 illustrates the system configuration for a sub 6 GHz setup.

Figure 2. Sub-6 GHz System Configuration

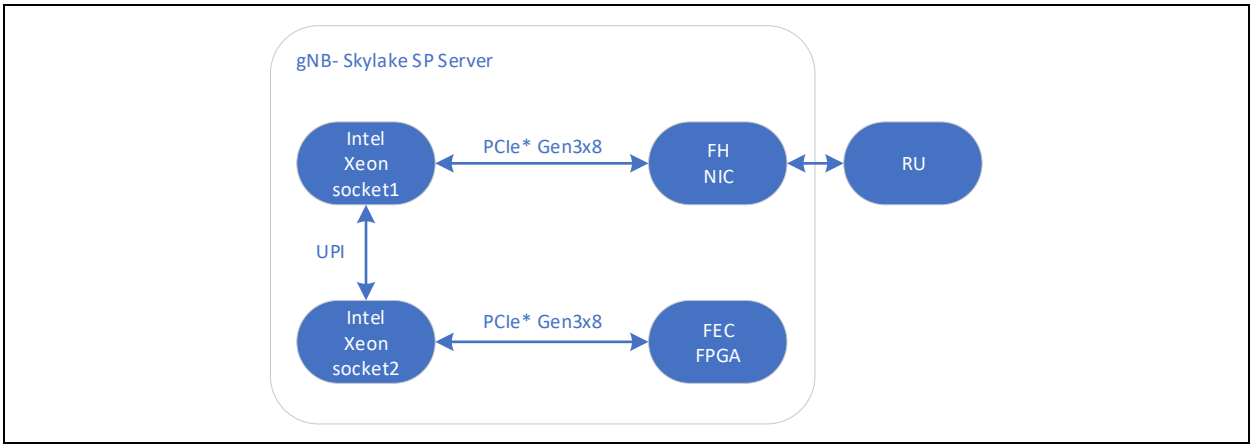


The current sub-6 GHz system does not support FH FPGA.

2.1.1 FH connection with xRAN

Figure 3 illustrates the system configuration with the xRAN FH.

Figure 3. System Configuration with xRAN FH



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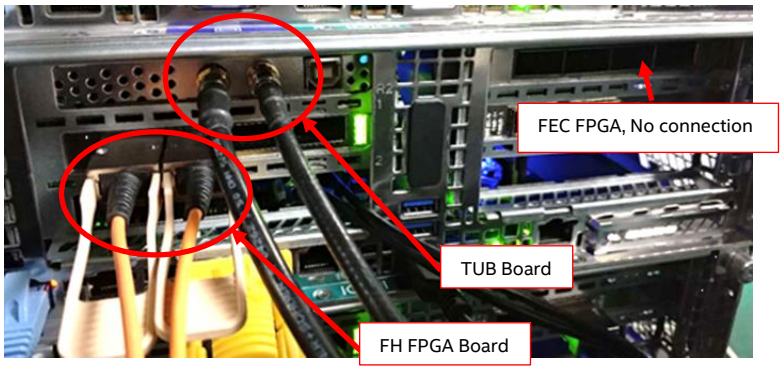
3.0 System Setup

Assume all hardware components are installed correctly, including the server, FPGAs, and TUB* (supplied by Terasic*). Install the system by matching the setup shown in Figure 3.

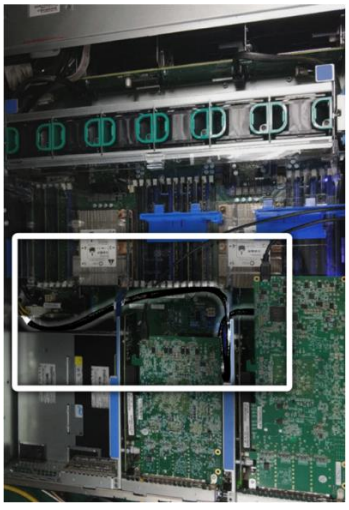
Figure 3. System Cable Connections



The Quad Small Form-Factor Pluggable (QSFP)+ Modules should be installed in left to right order, with the left module connecting to the leftmost FH FPGAs and the module on the right connecting to the rightmost FH FPGAs. The QSFP+ ports are connected to the RRU, which is outside the scope of this document.

Each FPGA card needs to have a dedicated USB cable, which is used to program the FPGA. See Figure 4, FPGA USB cable connection.

Figure 4. FPGA USB Cable Connection



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4.0 System Environment Configuration

This section describes how to configure the BIOS and check the Operating System (OS) settings. These configurations are required for the initial setup. If the system is already set up, refer to this section to check each configuration.

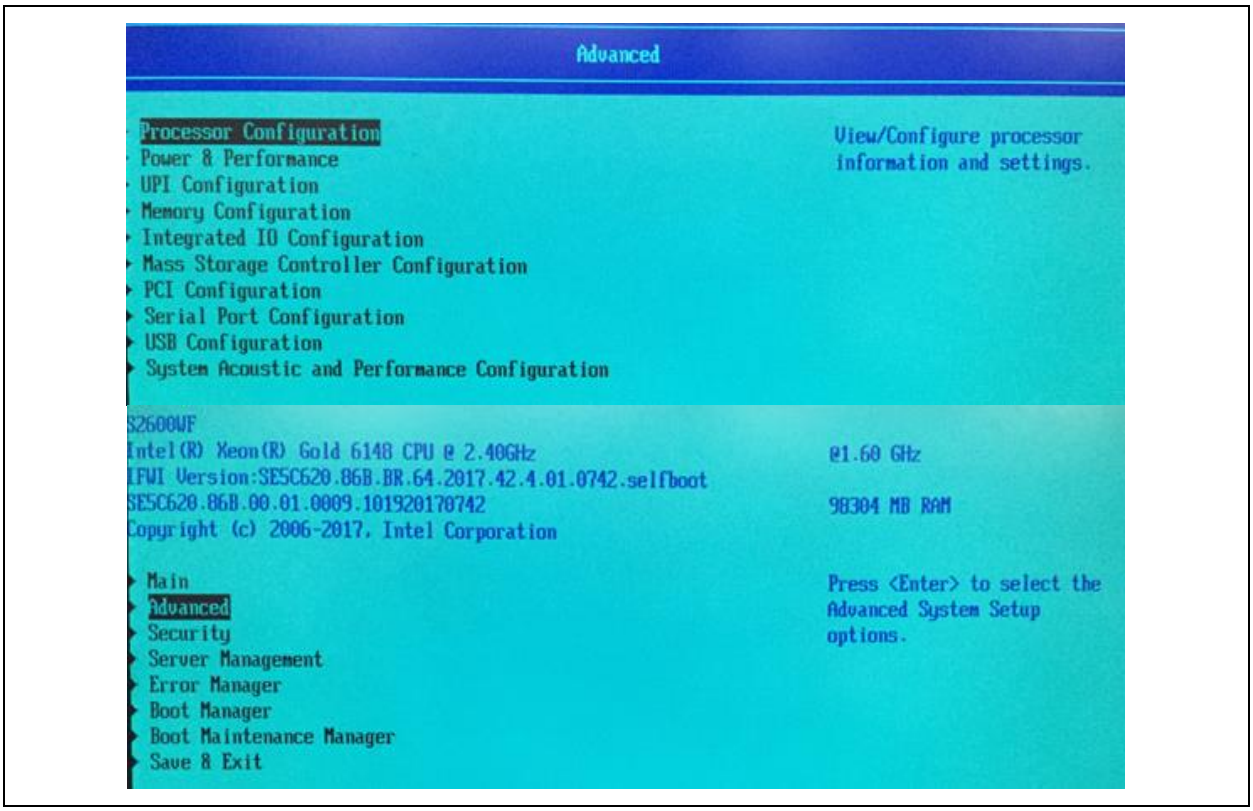
4.1 Wolf Pass Server with Skylake-SP Setting

This section describes how to set the BIOS. If the BIOS is already set, refer to the rest of this section for options to check and validate.

4.1.1 Graphical User Interface (GUI) BIOS Setting

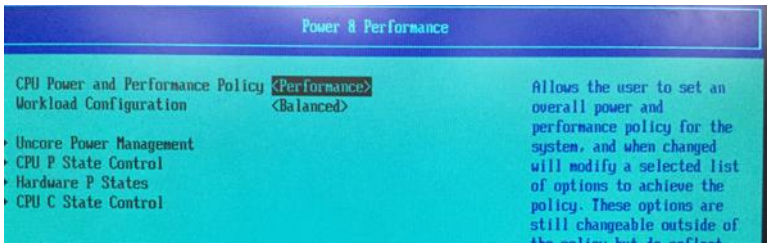
1. Connect the Skylake-SP server with a monitor and keyboard.
2. Select **F2** during server boot phase to enter the BIOS setup Graphical User Interface (GUI).
3. Select **F9** to load the default BIOS settings.
4. Select **Advanced ->Power & Performance** (refer to Figure 5).

Figure 5. BIOS Settings – Advanced Page



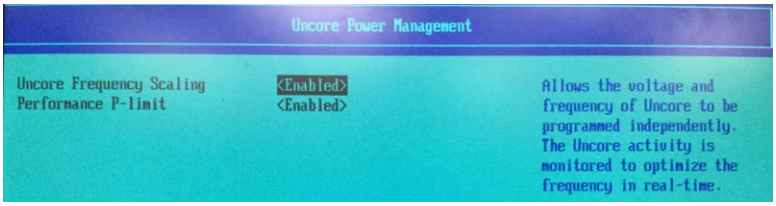
5. Set CPU Power and Performance Policy to **Performance**. Then select **Uncore Power Management** (refer to Figure 6).

Figure 6. BIOS Settings – Power & Performance Page



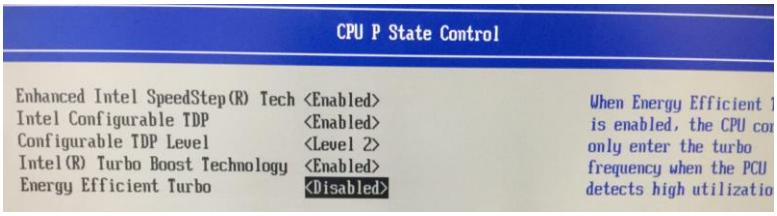
6. Set **Uncore Power Management** to match Figure 7.

Figure 7. BIOS Settings – Uncore Power Management Page



7. Set **CPU P State** to match Figure 8.

Figure 8. BIOS Settings – CPU P State Control Page

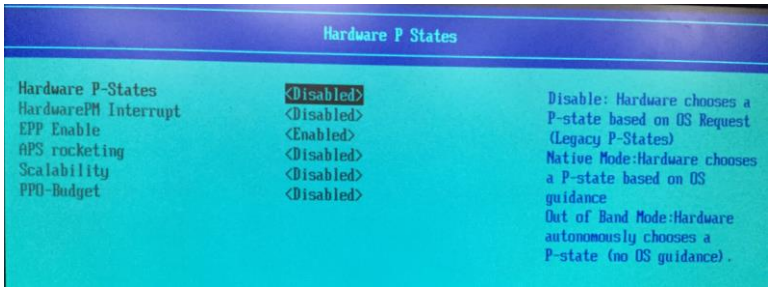


When a core needs to run any AVX instruction, there is a process of requesting for a frequency license grant. This grant process can take up to tens of microseconds and is very undeterministic. Once the grant is provided, the core has a hysteresis period (~500 µs) after which it will release this grant (if no more AVX code is running) on the core.

The FlexRAN code is what the BIOS team terms as sparse AVX512, which means this process of license grant and release happens often. This process can be disabled from BIOS (shown above) under the Intel Configurable TDP setting. The draw back of disabling this process is that the core frequency cannot go beyond a certain frequency. However, the performance loss caused by lower frequency is negligible compared to the gains due to the AVX512 optimization.

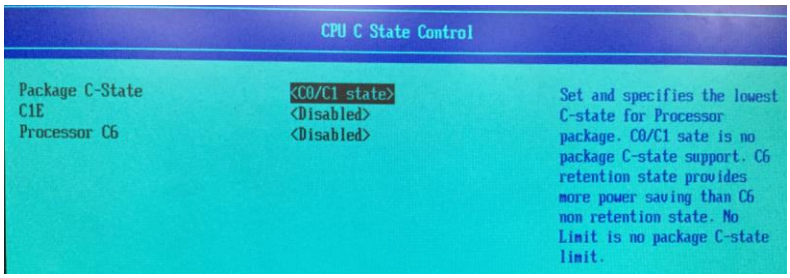
8. Set **Hardware P States** to disabled (refer to Figure 9)

Figure 9. BIOS Settings – Hardware P State Page



9. Set **CPU C State Control** to match Figure 10.

Figure 10. BIOS Settings- CPU C State Control Page



10. Return to Advanced and select **Memory Configuration**. Set **Memory Reliability Availability and Serviceability (RAS),** and **Performance Configuration** to match Figure 11 and Figure 12.

Figure 11. BIOS Settings- Memory Configuration Page

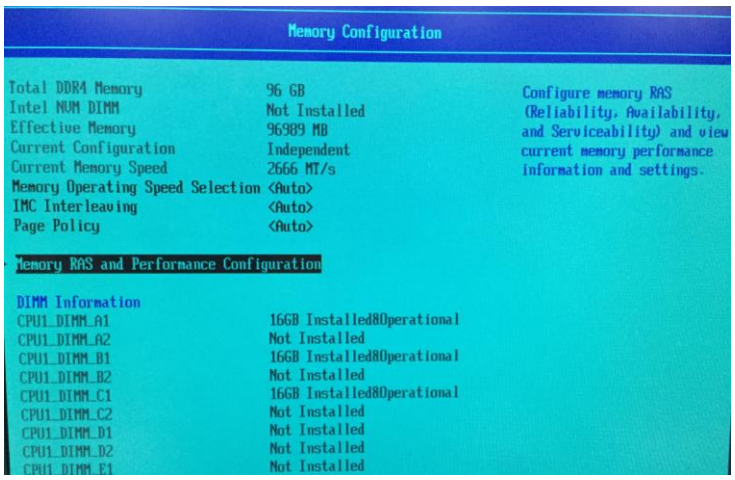
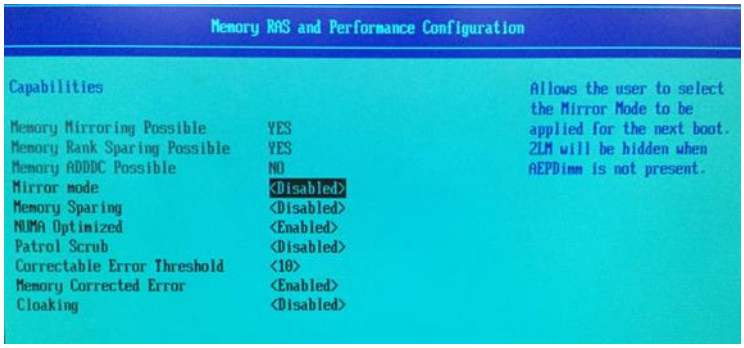


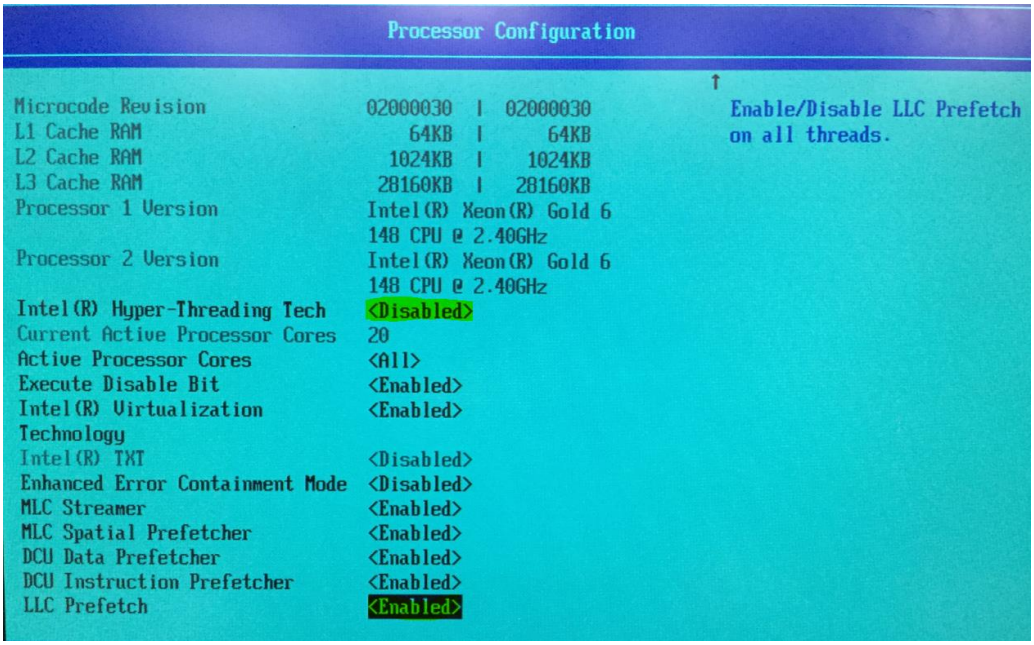
Figure 12. BIOS Settings- Memory RAS and Performance Configuration Page



11. Return to Advanced and set **Processor Configuration** to match Figure 13. Intel® Hyper-Threading Technology (Intel® HT Technology) is currently set to **Disabled**.

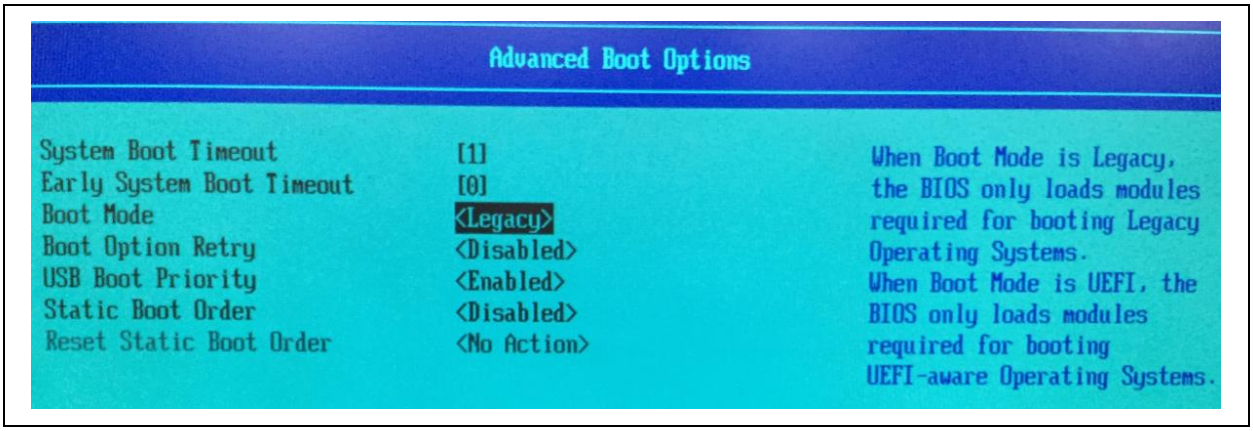
Note: Previous setting changes may affect Intel® HT Technology settings. Confirm this change before quitting the BIOS setting.

Figure 13. BIOS Settings- Processor Configuration Page



12. Return to Advanced and select **Boot Maintenance Manager**->**Advanced Boot Option** to set the Boot Mode to Legacy (refer to Figure 14).

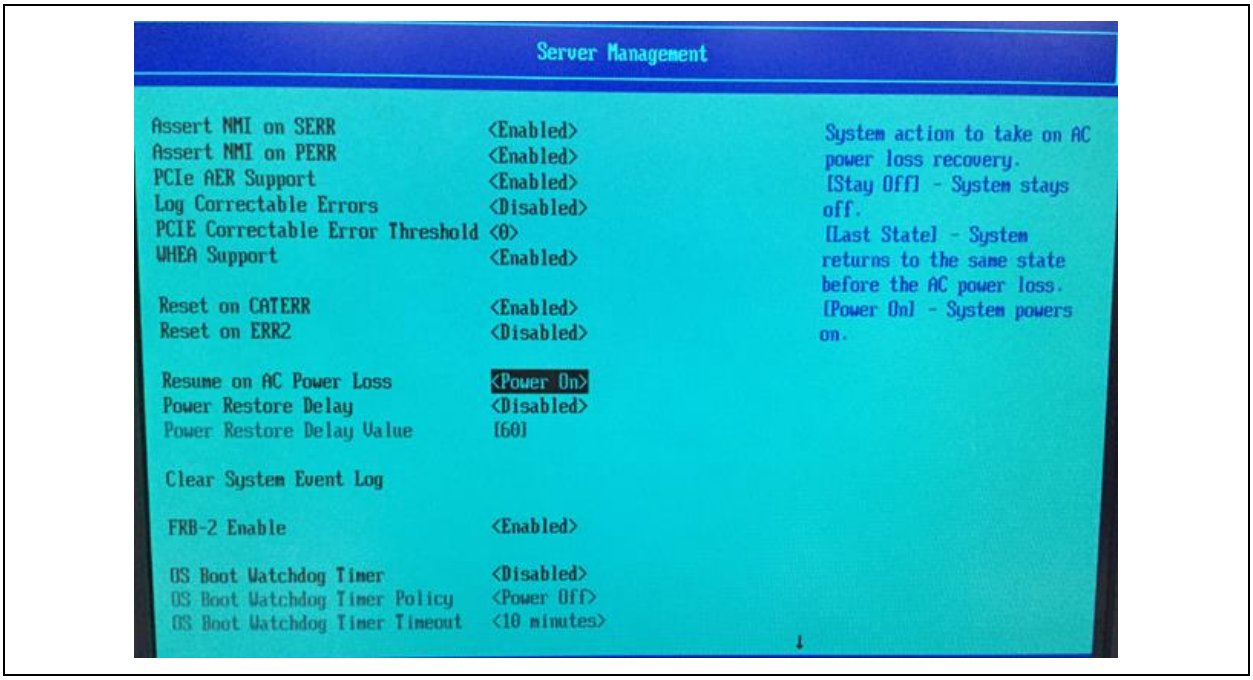
Figure 14. BIOS Settings- Advanced Boot Options Page



Note: Users can also use the Unified Extensible Firmware Interface (UEFI) boot mode instead of Legacy mode.

13. Return to Advanced and select **Server Management**. Set **Resume** to on and AC Power Loss to **Power On** (refer to Figure 15).

Figure 15. BIOS Settings-Server Management Page



14. After setting BIOS, select **F10** to save and reboot the server.

4.1.2 CPU Frequency Setting

To set the CPU frequency setting, follow this procedure:

1. When the OS boots, login with username root.
2. To check the CPU frequency, use the following command:

```
cat/proc/cpuinfo/grep MHz
```

If the output on the screen does not match Figure 16, run this command:

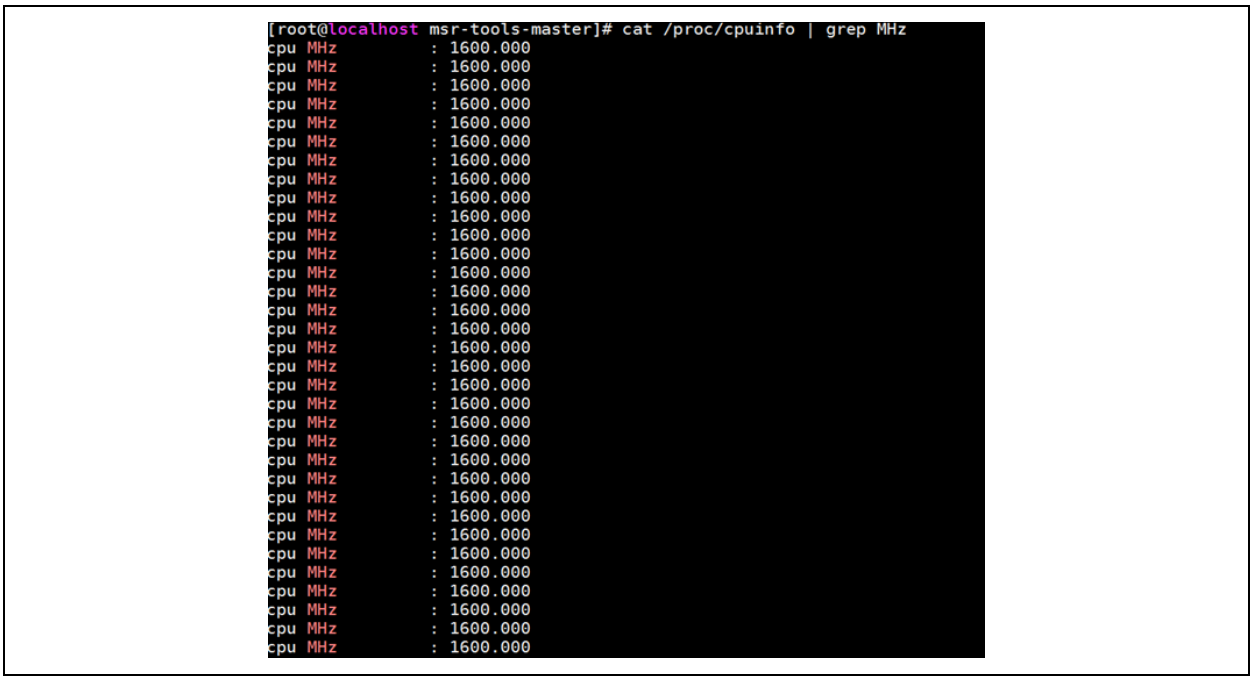
```
cpupower frequency-set -g performance
```

Also, use the following command to check the CPU frequency.

```
cat/proc/cpuinfo |grep MHz
```

They should be all fixed to 1.6 GHz (refer to Figure 16).

Figure 16. Correct CPU Frequency Number



3. Boost the CPU frequency to 2.2 GHz.
   a. Download the Model-Specific Register (MSR) tool found in MSR-Tools (refer to Table 2).
   b. Copy and extract msr-tools-1.3.zip to the Skylake-sp server and put it in the /home path.
   c. In the /home/msr-tools-master, run gcc wrmsr.c -o wrmsr to compile. Then, add the following commands into a new .sh file:

```
#!/bin/bash
for i in {0..39}
do
/home/msr-tools-master/wrmsr -p $i 0x199 0x1600
done
#Set Uncore to Max
/home/msr-tools-master/wrmsr -p 0 0x620 0x1e1e
/home/msr-tools-master/wrmsr -p 39 0x620 0x1e1e
```

For example:

Copy the above commands into tubo2200.sh file, then save and quit.

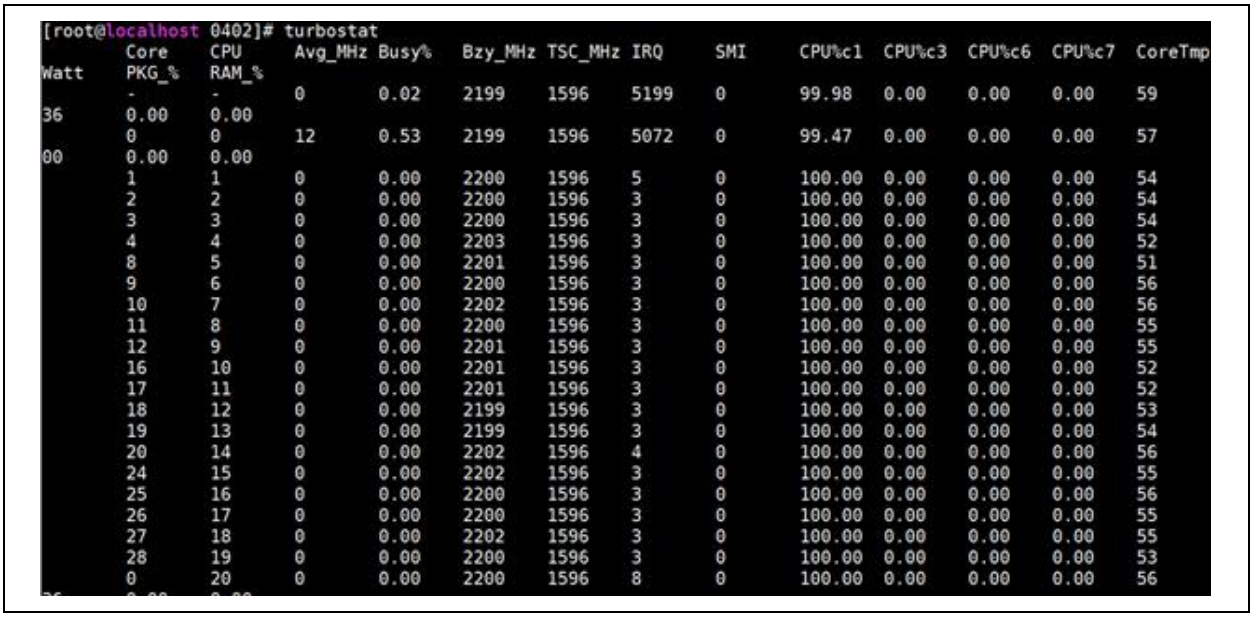
Run the saved (.sh) file:

```
sh tubo2200.sh
```

Enter the following command to check the configuration is applied correctly. "Bzy_MHz" should be around 2.2 GHz (2200, refer to Figure 17):

```
# turbostat
```

Figure 17. Turbostat to Show CPU Frequency



```
[root@localhost 0402]# turbostat
        Core    CPU     Avg_MHz Busy%   Bzy_MHz TSC_MHz IRQ     SMI     CPU%c1  CPU%c3  CPU%c6  CPU%c7  CoreTmp
Watt    PKG_%   RAM_%
        -       -       0       0.02    2199    1596    5199    0       99.98   0.00    0.00    0.00    59
36      0.00    0.00
        0       0       12      0.53    2199    1596    5072    0       99.47   0.00    0.00    0.00    57
00      0.00    0.00
        1       1       0       0.00    2200    1596    5       0       100.00  0.00    0.00    0.00    54
        2       2       0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    54
        3       3       0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    54
        4       4       0       0.00    2203    1596    3       0       100.00  0.00    0.00    0.00    52
        8       5       0       0.00    2201    1596    3       0       100.00  0.00    0.00    0.00    51
        9       6       0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    56
        10      7       0       0.00    2202    1596    3       0       100.00  0.00    0.00    0.00    56
        11      8       0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    55
        12      9       0       0.00    2201    1596    3       0       100.00  0.00    0.00    0.00    55
        16      10      0       0.00    2201    1596    3       0       100.00  0.00    0.00    0.00    52
        17      11      0       0.00    2201    1596    3       0       100.00  0.00    0.00    0.00    52
        18      12      0       0.00    2199    1596    3       0       100.00  0.00    0.00    0.00    53
        19      13      0       0.00    2199    1596    3       0       100.00  0.00    0.00    0.00    54
        20      14      0       0.00    2202    1596    4       0       100.00  0.00    0.00    0.00    56
        24      15      0       0.00    2202    1596    3       0       100.00  0.00    0.00    0.00    55
        25      16      0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    56
        26      17      0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    55
        27      18      0       0.00    2202    1596    3       0       100.00  0.00    0.00    0.00    55
        28      19      0       0.00    2200    1596    3       0       100.00  0.00    0.00    0.00    53
        0       20      0       0.00    2200    1596    8       0       100.00  0.00    0.00    0.00    56
```

If Turbostat does not display 2.2 GHz, use the following procedure to modify kernel boot options:

1. Open GRand Unified Bootloader (GRUB) configuration (/etc/default/grub) and add following options to kernel boot argument (GRUB_CMDLINE_LINUX)

   ```
   processor.max_cstate=1
   intel_idle.max_cstate=0
   ```

2. After saving the changes, the GRUB needs to be updated using one of the following commands, depending on the boot mode used.

- For UEFI boot:

  ```
  grub2-mkconfig -o /boot/efi/EFI/centos/grub.cfg
  ```

- For Legacy boot:

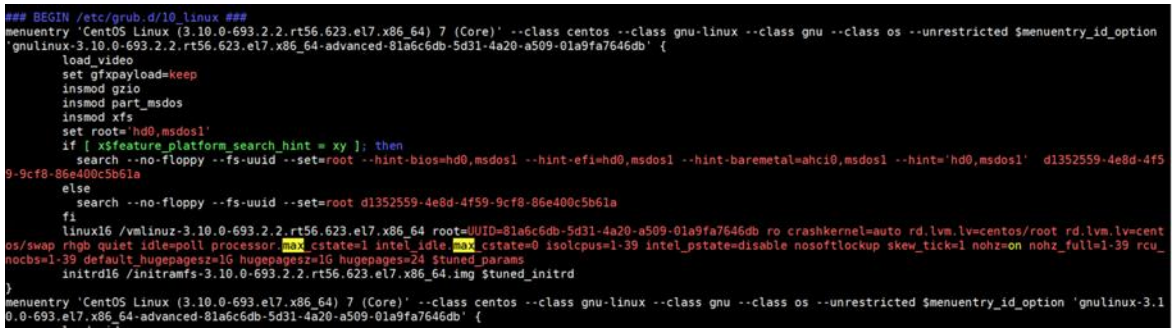
  ```
  grub2-mkconfig -o /boot/grub2/grub.cfg
  ```

3. After reboot, rerun the following:

   ```
   cpupower frequency-set -g performance
   ```

```
cd /home/msr-tools-master
sh tubo2200.sh
turbostat
```

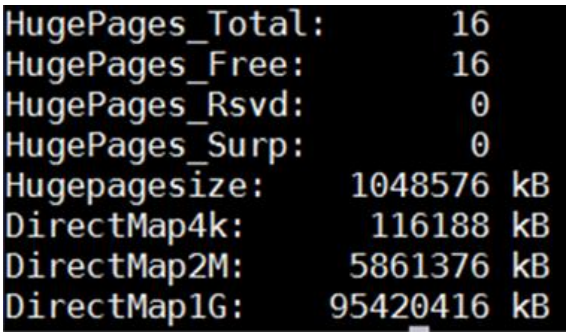
Figure 18. GRUB Script



4.1.3 Check OS Version

1. When the OS boots, login with username root.
2. Use command uname –a to check the OS version, and it should be similar to the OS version in Section 4.1, *Compilation* of *FlexRAN 5G NR Reference Solution RefPHY (Doxygen)* [Doc ID: 603577]. If the OS version is different, reboot and select the correct OS image in OS boot time.
3. Use command cat /proc/meminfo to check memory information. The HugePage size should be 1 GB, and the total number of pages should be at least 16 GB (refer to Figure 19).

Figure 19. Hugepage Memory Status



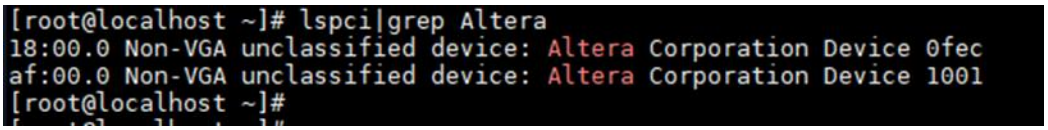
4. Use command lspci|grep Altera®[1] to check the FPGA status. Typically, it will show "Altera® Corporation Device 0fec and Altera® Corporation Device 1001."

   Device 0fec is the FPGA with an FEC image, 1001, which is related to the FH image. These prints help to check whether the FPGAs are installed and flashed correctly. If they are installed and

[1] Altera® is a trademark of Intel® Corporation or its subsidiaries

flashed correctly, the display will resemble Figure 20. If the FPGA has not flashed correctly, reflash the FPGA.

Figure 20. PCI FPGA Status



5. Check the Intel C++ Compiler (ICC) version using the command icc –v.

   The ICC version will show as written in the Release Notes in Table 2 (which will state each release dependency).

6. Check the DPDK status.

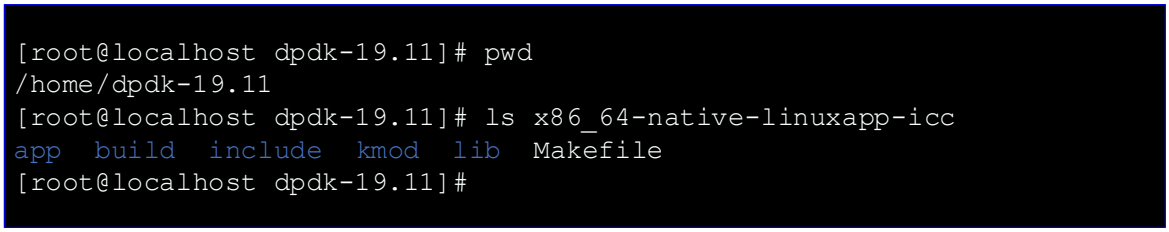
   DPDK version refers to each Release Notes, and the following is an example.

   For example, if DPDK is installed at /home/dpdk-19.11, run the following commands:

```
#cd /home/dpdk-19.11
#ls x86_64-native-linuxapp-icc
```

   If the display matches Figure 21, the DPDK v19.11 is installed.

Figure 21. DPDK v19.11 Status



Otherwise, refer to the following link for DPDK compiling and building instructions:

http://doc.dpdk.org/guides-19.11/linux_gsg/index.html

4.2 Wolf Pass Server with Cascade Lake-SP Setting

All of Wolf Pass with Cascade Lake's-SP server settings (except for the CPU frequency) should be the same as Wolf Pass with Skylake-SP.

4.2.1 CPU Frequency Setting

To set the CPU frequency setting, follow this procedure:

1. When the OS boots, login with username **root**.
2. To check the CPU frequency, use the following command:

```
cat/proc/cpuinfo/grep MHz
```

If the output on the screen does not match Figure 22, run this command:

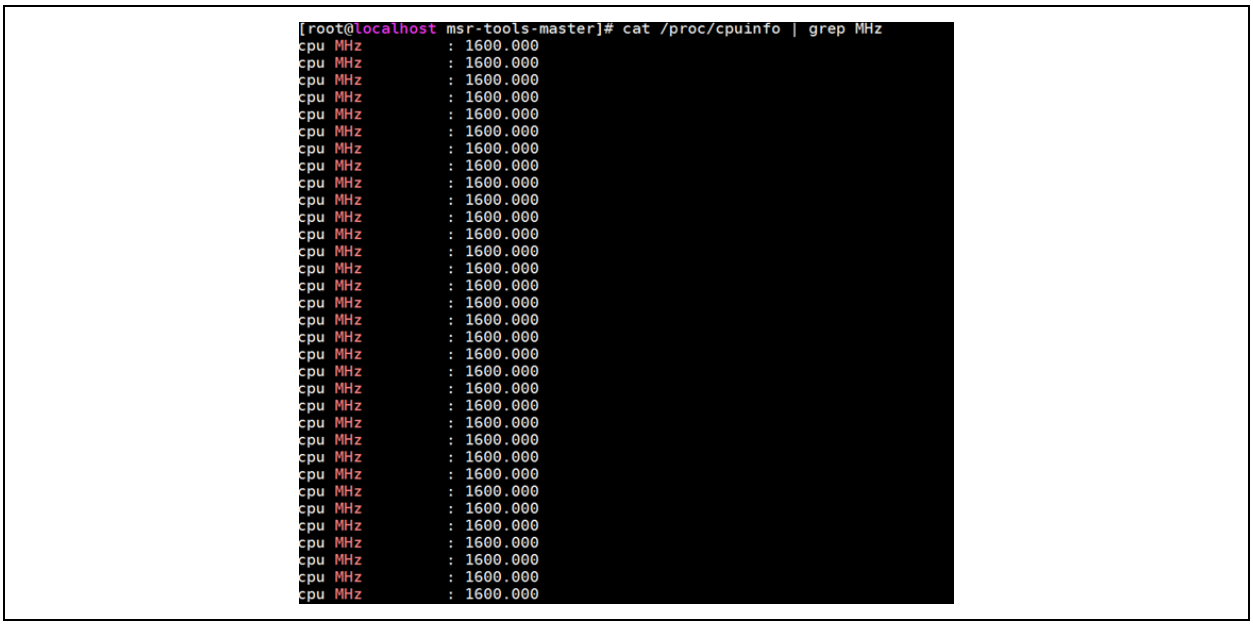
```
cpupower frequency-set -g performance
```

Use the following command to check the CPU frequency:

```
cat/proc/cpuinfo |grep MHz
```

They should be all fixed to 1.6 GHz (refer to Figure 22).

Figure 22. Correct CPU Frequency Number



3. Boost CPU frequency to 2.5 GHz.
   a. Download the MSR tool found in MSR-Tools (refer to Table 2).
   b. Copy and extract msr-tools-1.3.zip to the Skylake-SP server and put it in the /home path.
   c. In /home/msr-tools-master, run gcc wrmsr.c -o wrmsr to compile. Then Add the following commands into a new .sh file:

```
#!/bin/bash
for i in {0..39}
do
/home/msr-tools-master/wrmsr -p $i 0x199 0x1900
done
```

```
#Set Uncore to Max
/home/msr-tools-master/wrmsr -p 0 0x620 0x1e1e
/home/msr-tools-master/wrmsr -p 39 0x620 0x1e1e
```

4.3 Supermicro* Server with Skylake-D Setting

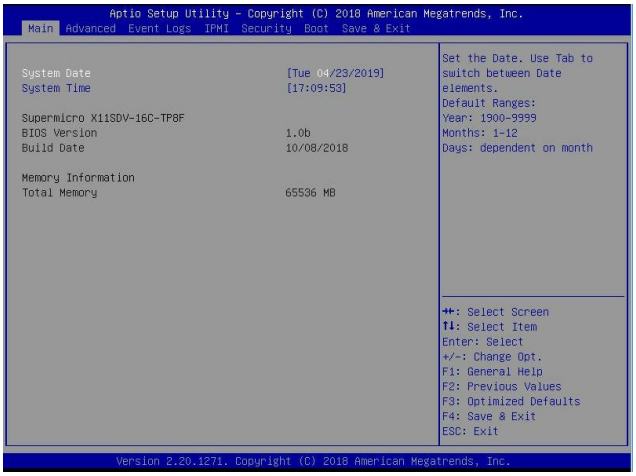
This section lists the Supermicro* BIOS, cmdline, and CPU frequency setting reference.

4.3.1 GUI BIOS Setting

The following is a procedure for setting the GUI BIOS.

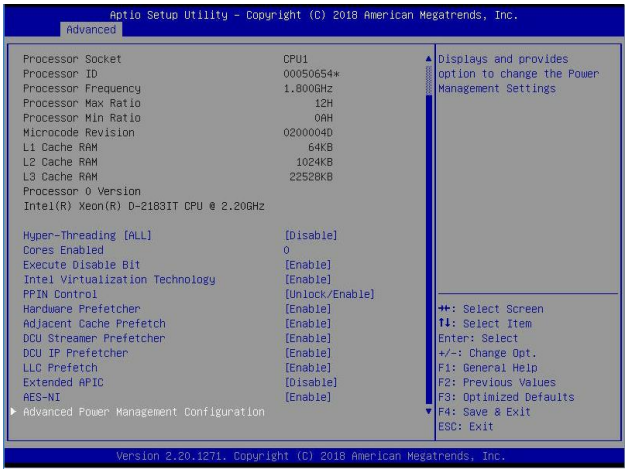
1. Press **Del** during the server boot phase and enter the BIOS setup GUI.
2. Check the BIOS version in the Main menu (refer to Figure 23).
3. Refer to Figure 26 through Figure 30 to verify the correct settings.

Figure 23. BIOS Version – Check Date



4. Select **Advanced** to check CPU Configuration (refer to Figure 24).

Figure 24. Check CPU Configuration



5. Enter the Advanced Power Management Configuration (refer to Figure 25).

Figure 25. Advanced Power Management Configuration

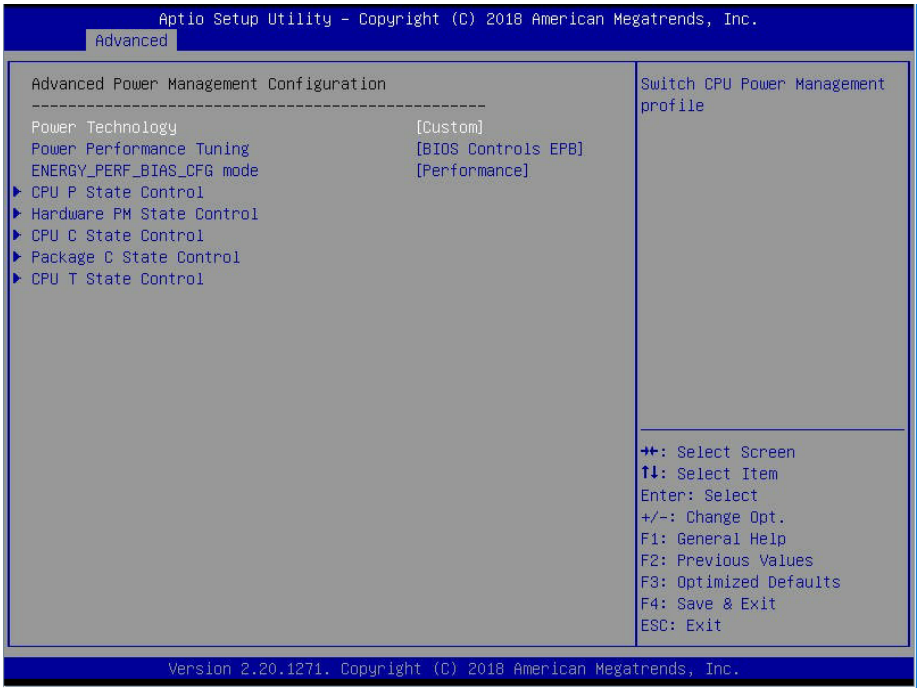


Figure 26. CPU C State Control Settings

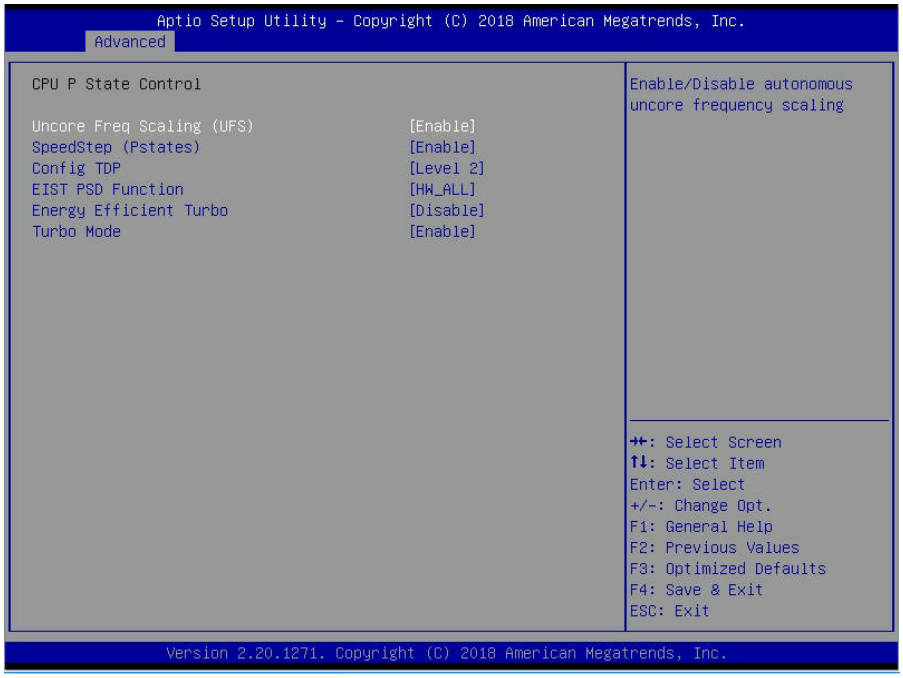


Figure 27. Hardware PM State Control

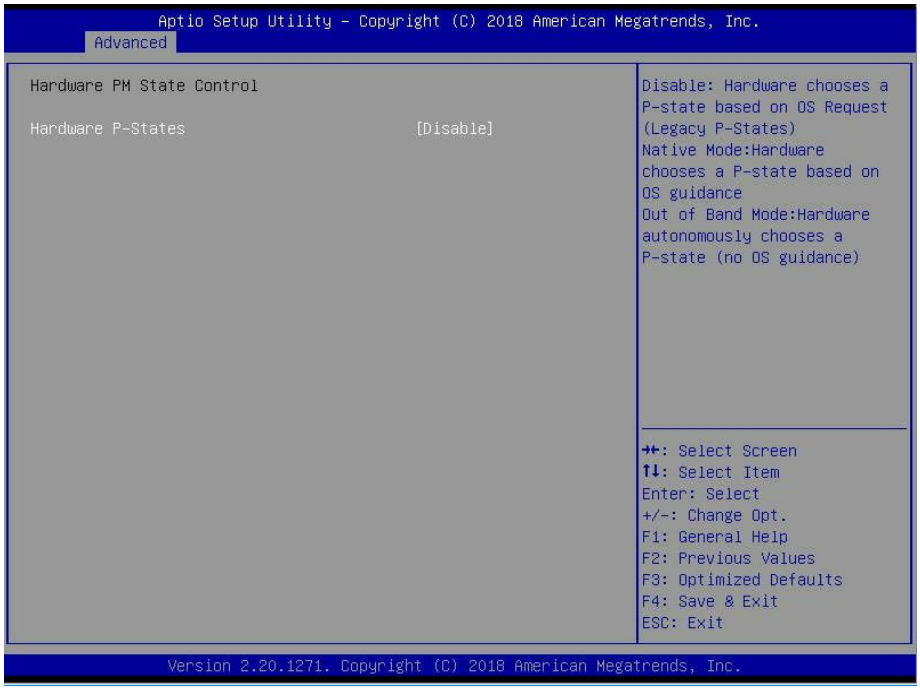


Figure 28. CPU C State Control Settings

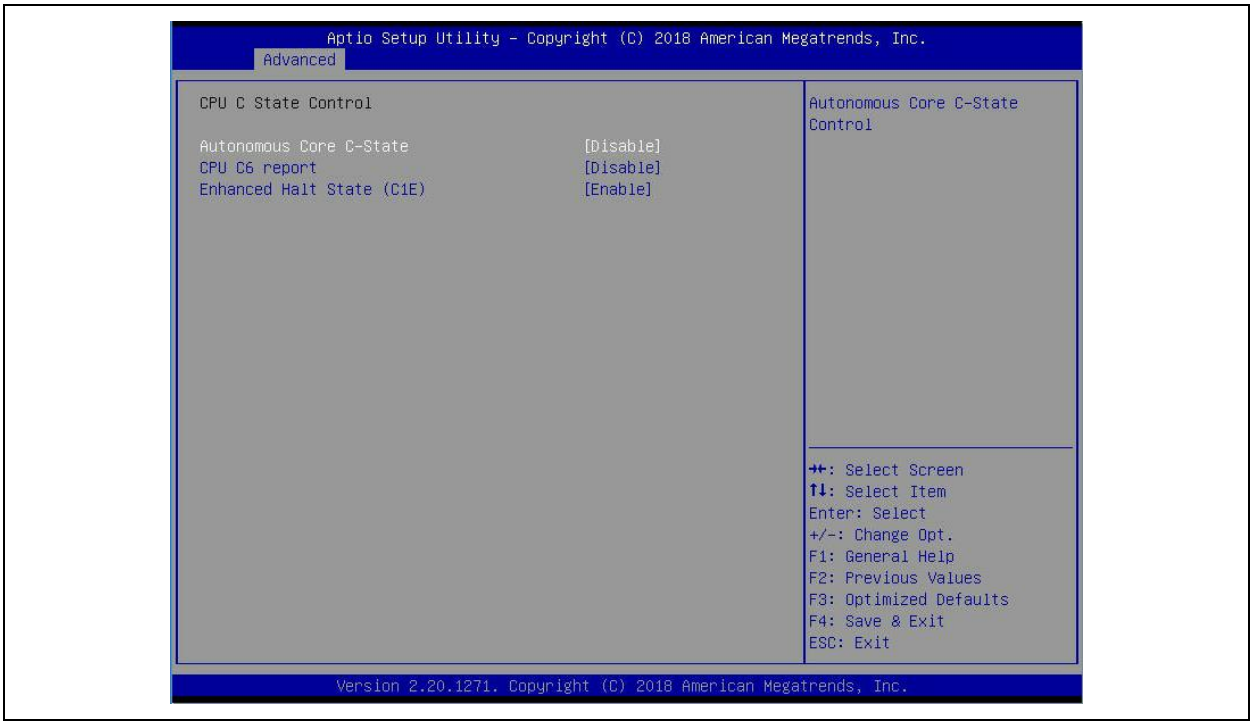


Figure 29. Package C State Control Settings

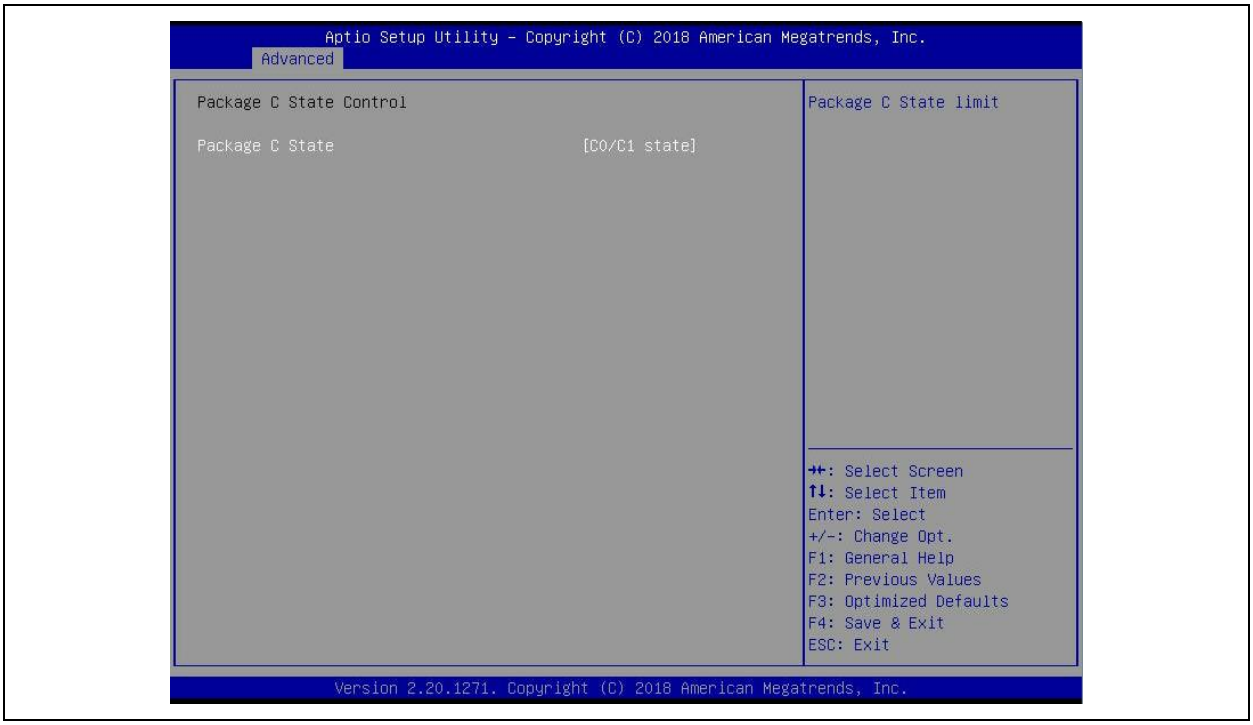
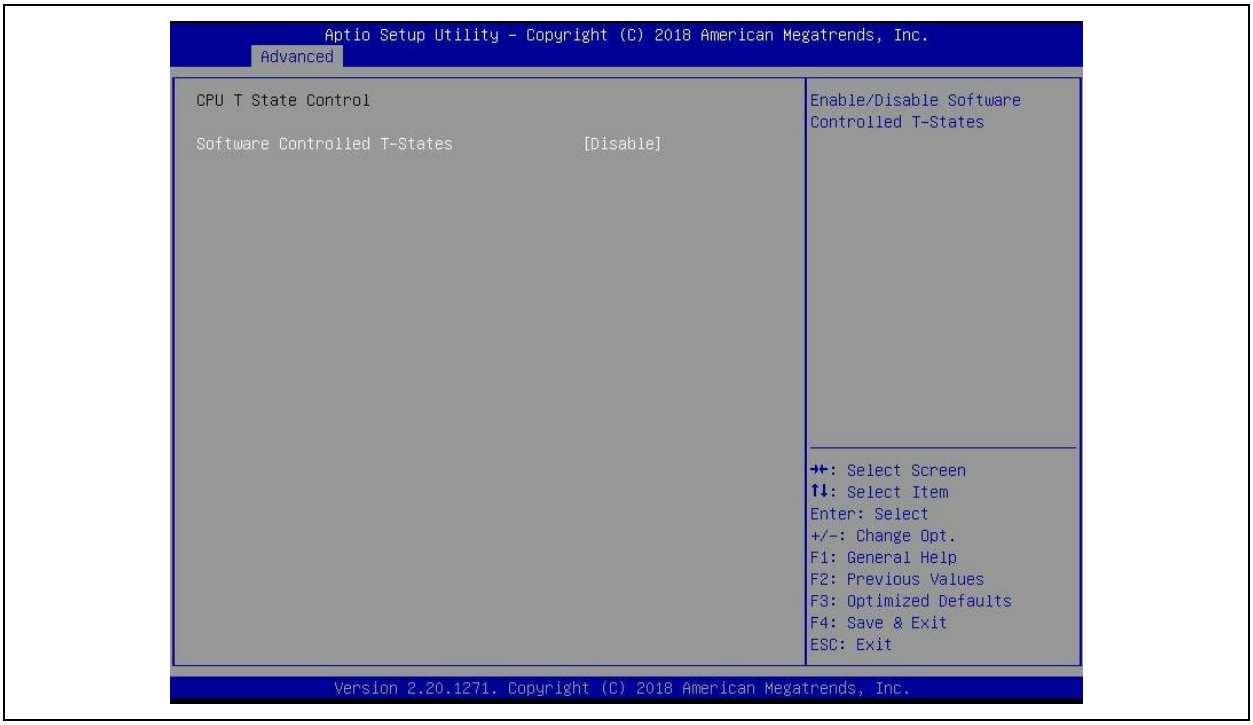


Figure 30. CPU T State Control Settings



If there are modifications to the settings referred to in Figure 26 through Figure 30, press **F4** to save and exit.

4.3.2 Cmdline Setting

Check the CMD line:

```
[root@localhost ~]# cat /proc/cmdline
BOOT_IMAGE=/vmlinuz-3.10.0-693.2.2.rt56.623.el7.x86_64 root=UUID=8734d476-ec28-434e-880d-0d804ce80fcd ro crashkernel=auto rd.lvm.lv=centos/root rd.lvm.lv=centos/swap rhgb quiet processor.max_cstate=1 intel_idle.max_cstate=0 idle=poll isolcpus=1-15,17-31 nosoftlockup skew_tick=1 nohz=on nohz_full=1-15,17-31 rcu_nocbs=1-15,17-31 default_hugepagesz=1G hugepagesz=1G hugepages=16 intel_pstate=disable
```

Modify the GRUB if any parameter was different, and reboot.

4.3.3 CPU Frequency Setting

Use the "turbostat" command to check the CPU frequency in Linux*.

Figure 31. CPU frequency in Linux*

```
Core     CPU      Avg_MHz  Busy%    Bzy_MHz  TSC_MHz
RAM_%
-        -        1995     100.00   2000     1796
0.00
0        0        1995     100.00   2000     1796
0.00
1        1        1995     100.00   2000     1796
2        2        1995     100.00   2000     1796
3        3        1995     100.00   2000     1796
4        4        1995     100.00   2000     1796
5        5        1995     100.00   2000     1796
6        6        1995     100.00   2000     1796
7        7        1995     100.00   2000     1796
8        8        1995     100.00   2000     1796
9        9        1995     100.00   2000     1796
10       10       1995     100.00   2000     1796
11       11       1995     100.00   2000     1796
12       12       1995     100.00   2000     1796
13       13       1995     100.00   2000     1796
14       14       1995     100.00   2000     1796
15       15       1995     100.00   2000     1796
```

If the frequency is not stable, run the command:

```
"cpupower frequency-set -g performance"
```

4.4 Wilson City Server with icelake-SP Setting

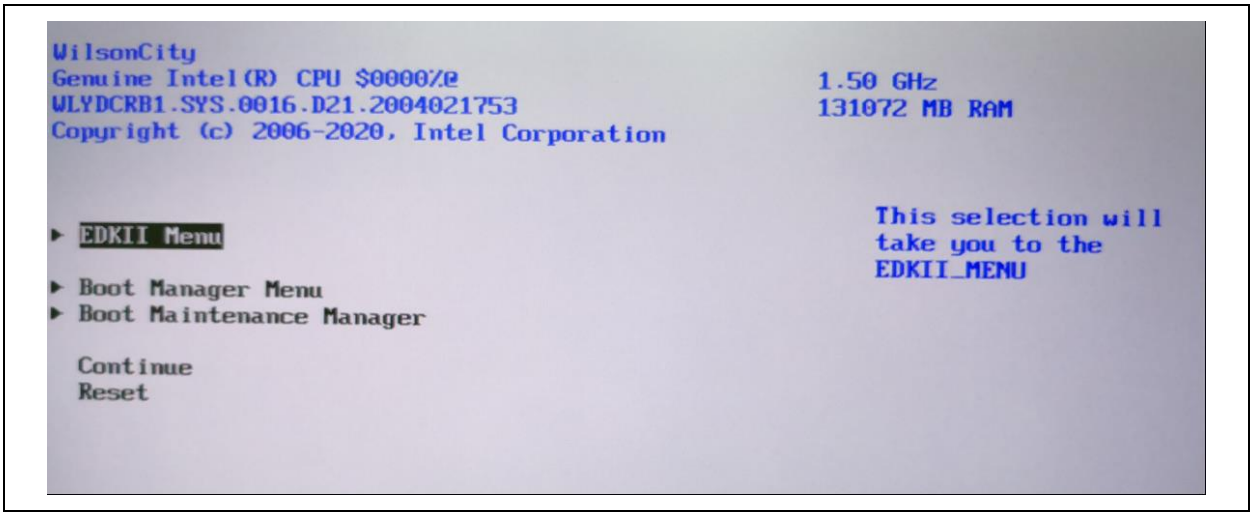
This section lists the Wilson City BIOS, cmdline, and CPU frequency setting reference.

4.4.1 GUI BIOS Setting

The following is a procedure for setting the GUI BIOS.

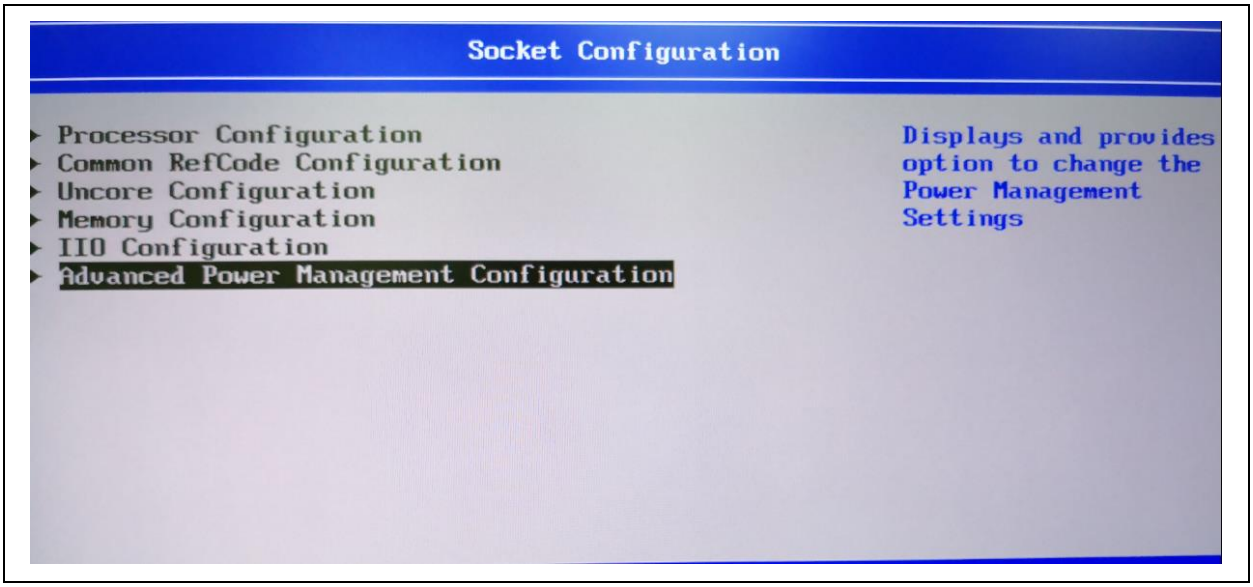
6. Press **F2** during the server boot phase and enter the BIOS setup GUI.
7. Check the BIOS version in the Main menu (refer to Figure 32).
8. Refer to through to verify the correct settings.

Figure 32. BIOS Setting



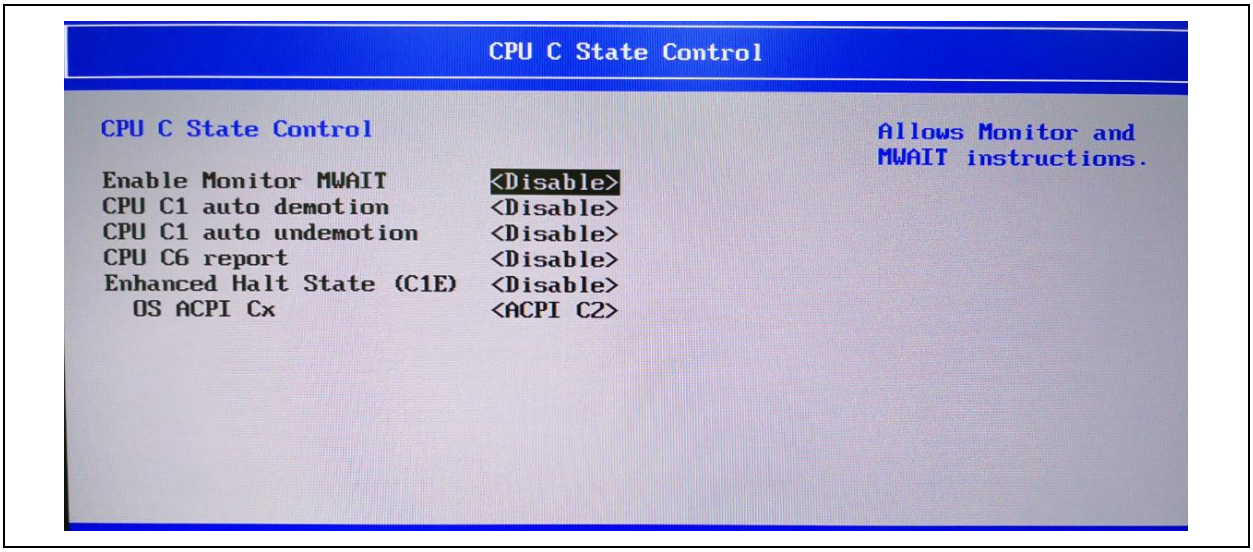
9. Enter the Advanced Power Management Configuration (refer to Figure 33).

Figure 33. Advanced Power Management Configuration



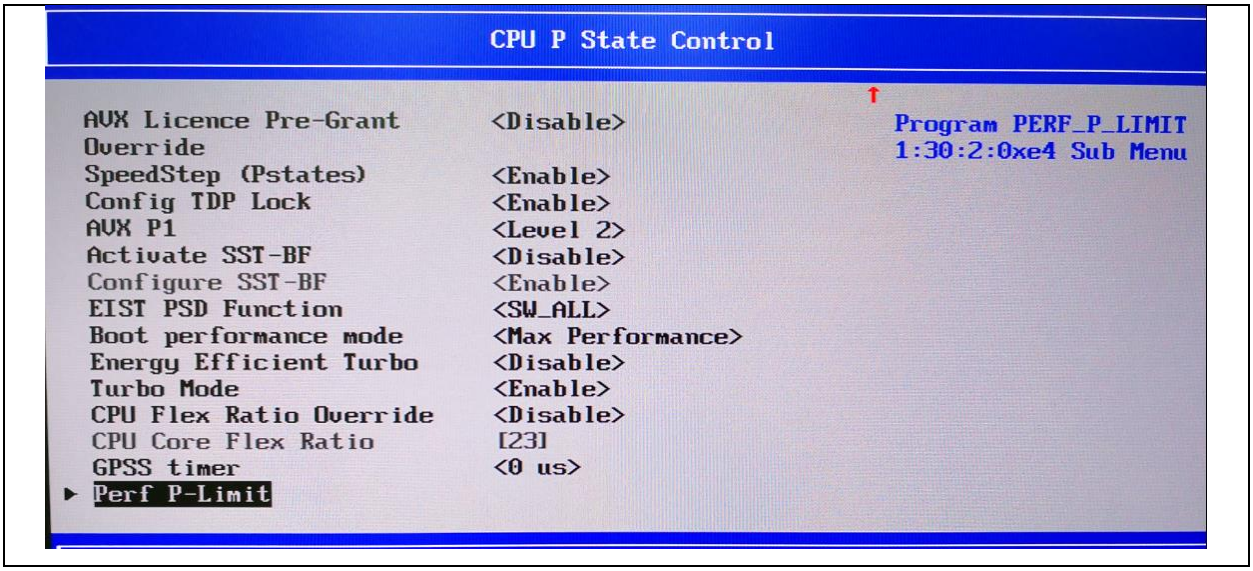
10. Enter CPU C State Control Setting (refer to Figure 34).

Figure 34. CPU C State Control Settings



11. Enter CPU P State Control Setting (refer to Figure 34).

Figure 35.CPU P State Control Settings



12. Enter Hardware PM State Control (refer to Figure 36).

Figure 36. Hardware PM State Control

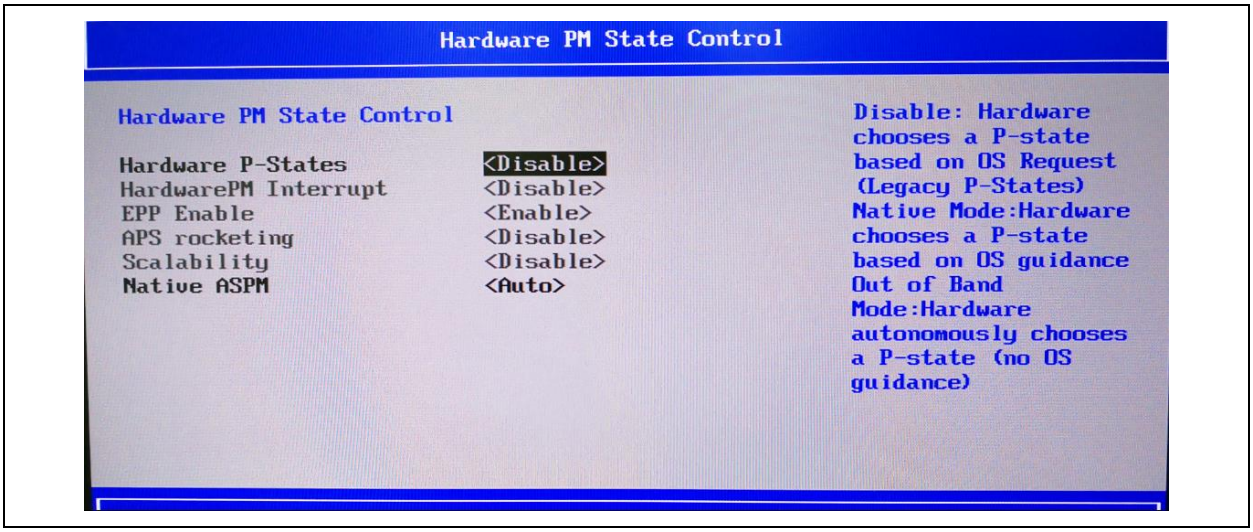
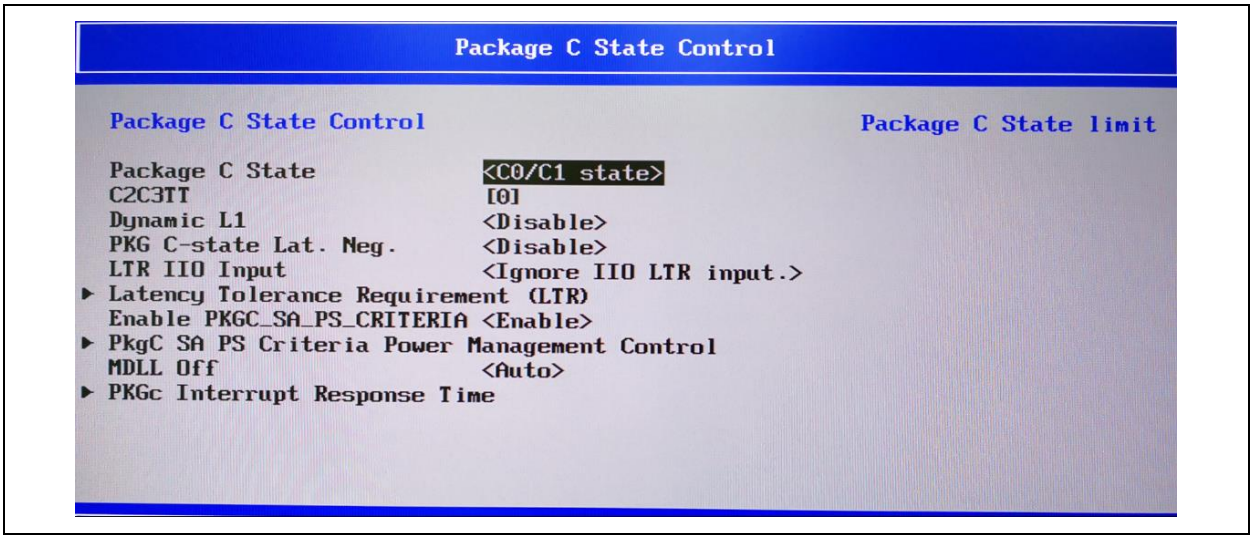
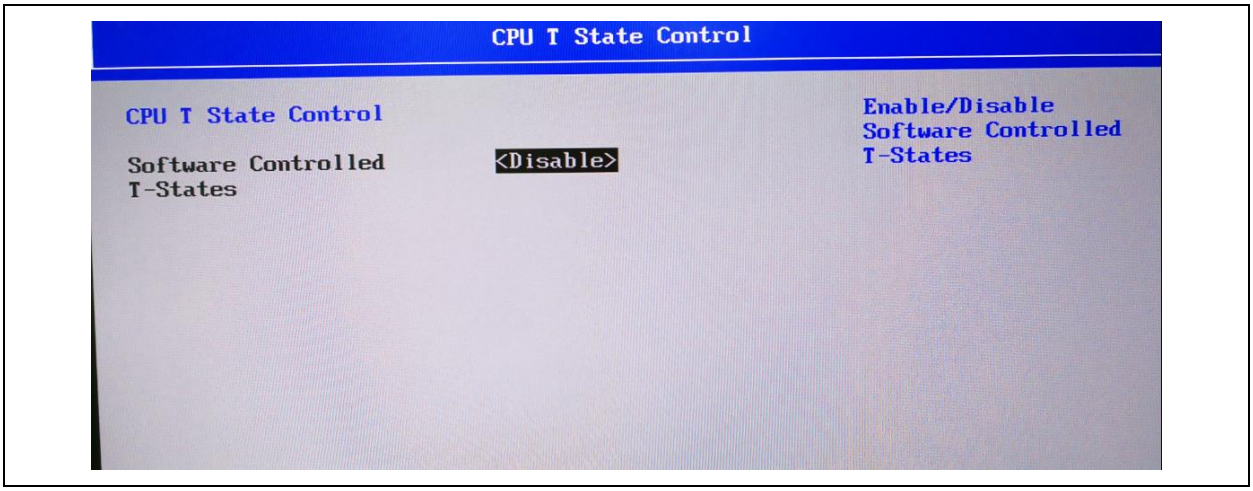


Figure 37. Package C State Control Settings

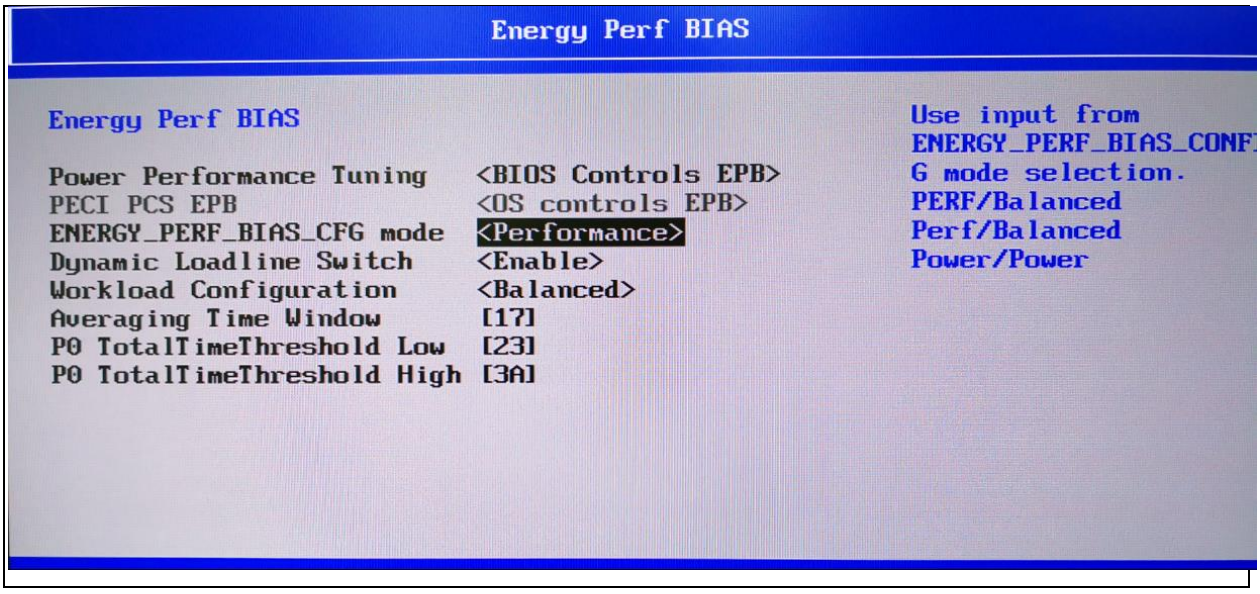


13. Enter CPU T State Control Setting (refer to Figure 37)



14. Enter CPU – Advance PM Tuning > Energy Perf BIAS (refer to Figure 38), set “Power Performance Tuning” as “BIOS Controls EPB” and set “ENERGEY_PERF_BIAS_CFG mode” as “Performance”.

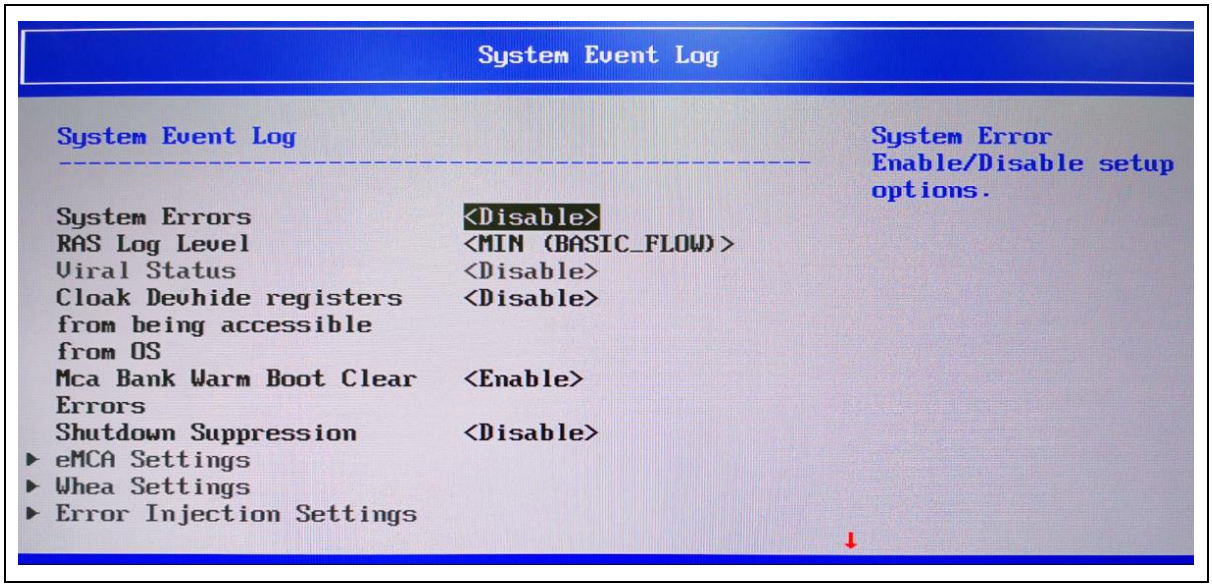
Figure 38. CPU - Advance PM Tuning Settings



In order to use MountBryce (ACC100), following BIOS items should be set:

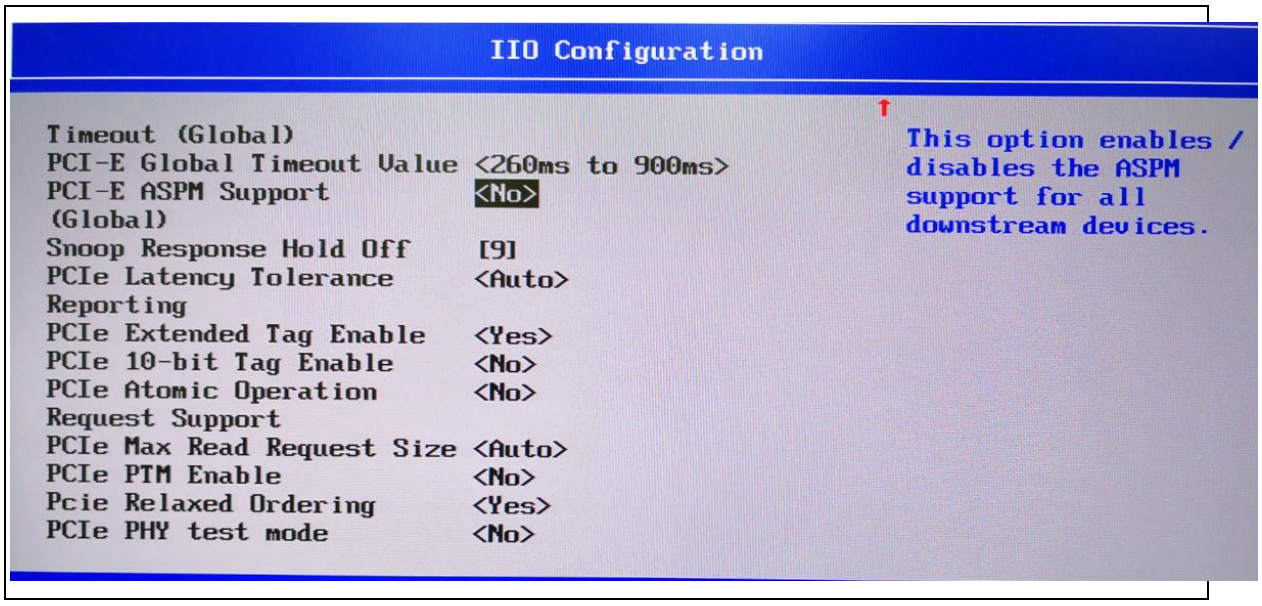
15. Enter System Event Log (refer to Figure 39), set “System Errors” as “Disable”.

Figure 39. System Even Log



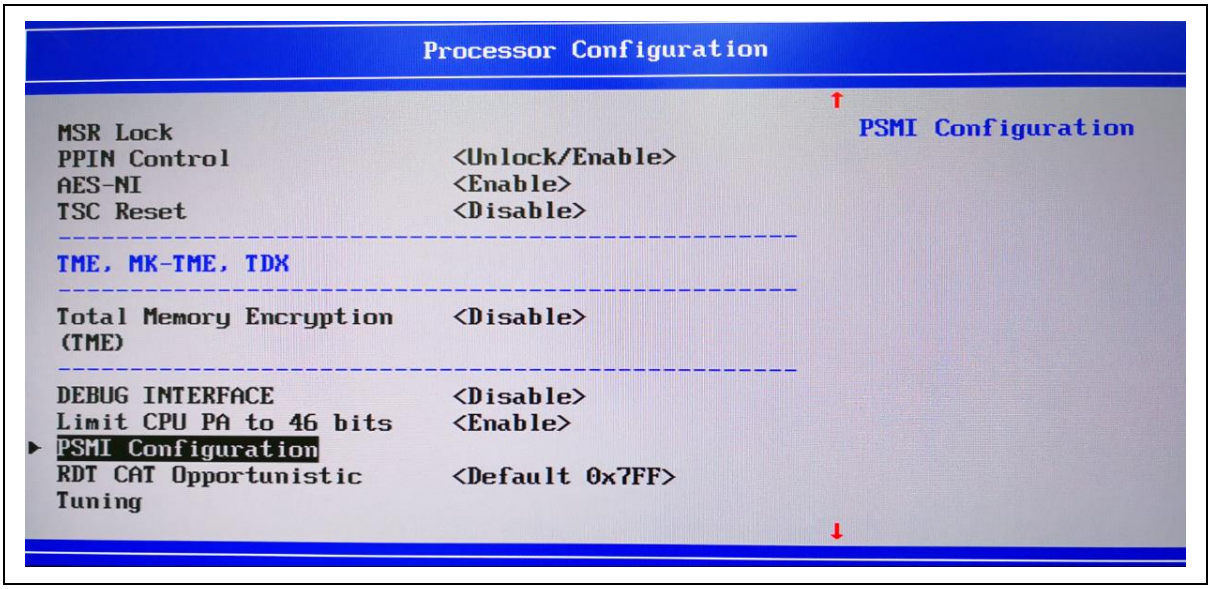
16. Enter IIO configuration (refer to Figure 40), to diable IIO PCIE global ASPM

Figure 40. IIO configuration



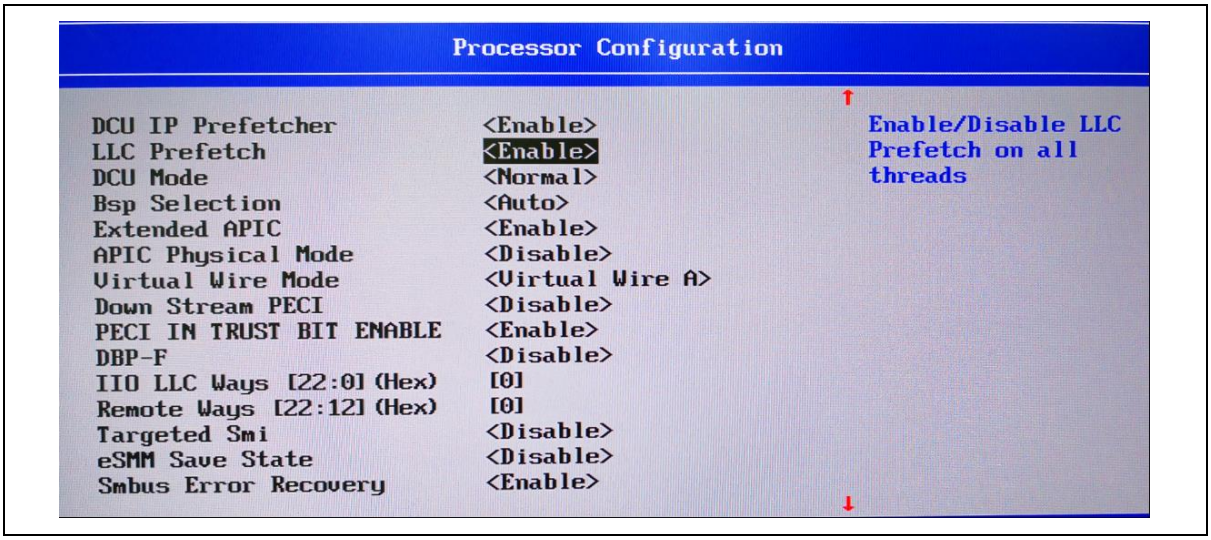
17. Enter Processor configuration (refer to Figure 41), to limit Processor PA to 46 bits

Figure 41. Processor configuration > limit processor PA



18. Enter Processor configuration (refer to Figure 42), to enabled extended APIC for processor

Figure 42. Processor configuration > enable extended APIC for Processor



If there are modifications to the settings referred to in Figure 32 through Figure 42, press **F10** to save and exit.

4.4.2 Cmdline Setting

Check the CMD line:

```
[root@icelake-scs1-1 ~]# cat /proc/cmdline

BOOT_IMAGE=/vmlinuz-3.10.0-957.10.1.rt56.921.el7.x86_64 root=/dev/mapper/centos-root
ro crashkernel=auto rd.lvm.lv=centos/root rd.lvm.lv=centos/swap rhgb quiet
intel_iommu=off usbcore.autosuspend=-1 selinux=0 enforcing=0 nmi_watchdog=0 idle=poll
```

```
softlockup_panic=0 audit=0 intel_pstate=disable cgroup_disable=memory mce=off
hugepagesz=1G hugepages=40 hugepagesz=2M hugepages=0 default_hugepagesz=1G isolcpus=1-
23,25-47 rcu_nocbs=1-23,25-47 kthread_cpus=0 irqaffinity=0 nohz_full=1-23,25-47
```

Modify the grub as following if any parameter is different, and then reboot.

1. Edit /etc/tuned/realtime-virtual-host-variables.conf to change isolated_cores=1-23, 25-47:

```
# Examples:

isolated_cores=1-23,25-47
```

2. Edit /boot/efi/EFI/centos/grub.cfg (for UEFI) or /etc/default/grub (for Lagecy) if any other cmdline parameter is different. After change, you need run following command and then reboot to make it effective:

```
grub2-mkconfig -o /boot/grub2/grub.cfg
```

4.4.3 CPU Frequency Setting

Use the same method as SKL-SP to change the CPU frequency and Uncore frequency. The difference is to set CPU frequency for icelake-SP as 2.5GHz.

Use the "turbostat" command to check the CPU frequency in Linux*.

Figure 43. CPU frequency in Linux*

Core	CPU	Avg_MHz	Busy%	Bzy_MHz	TSC_MHz	IRQ
-	-	2494	100.00	2500	1497	5116
0	0	2494	100.00	2500	1497	5044
1	1	2494	100.00	2500	1497	3
2	2	2494	100.00	2500	1497	3
3	3	2494	100.00	2500	1497	3
4	4	2494	100.00	2500	1497	3
5	5	2494	100.00	2500	1497	3
6	6	2494	100.00	2500	1497	3
7	7	2494	100.00	2500	1497	3
8	8	2494	100.00	2500	1497	3
9	9	2494	100.00	2500	1497	3
10	10	2494	100.00	2500	1497	3
11	11	2494	100.00	2500	1497	3
12	12	2494	100.00	2500	1497	3
13	13	2494	100.00	2500	1497	3
14	14	2494	100.00	2500	1497	3
15	15	2494	100.00	2500	1497	3
16	16	2494	100.00	2500	1497	3
17	17	2494	100.00	2500	1497	3
18	18	2494	100.00	2500	1497	3
19	19	2494	100.00	2500	1497	3
20	20	2494	100.00	2500	1497	3
21	21	2494	100.00	2500	1497	3
22	22	2494	100.00	2500	1497	3
23	23	2494	100.00	2500	1497	6

If the frequency is not stable, run the command:

```
"cpupower frequency-set -g performance"
```

§

5.0 Test Case Running Method

Refer to *FlexRAN 5G NR Reference Solution RefPHY Doxygen*, Table 2 for a full list of test cases, instructions, and how to run them.

§