Ferry Bridge

Release Notes

October 2018

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Contents

Figures

Tables

Revision History

Date	Revision	Description
31 May 2014	0.1.0	Ferry Bridge R0.1.0 Release (BBU Pool Reference SW).
25 Aug. 2014	0.1.1	Ferry Bridge R0.1.1 Release, release patch for R1.0.0
13 Jan. 2015	1.0.0	Ferry Bridge R1.0.0 Release
9 April 2015	1.1.0	Ferry Bridge R1.1.0 Release
Aug. 2015	1.2.0	Ferry Bridge R1.2.0 Release (BBU Pool Reference SW with Waddell Creek integrated).
May. 2016	1.3.0	Ferry Bridge R1.3.0 PRACH & Control Channel Release
December 2016	1.3.1	4x4 antenna support with PRACH & Control Channels. Added functionality to bypass AGC. NCO calculation update based on integration to RRH.
March 2017	1.4	Posted document rev. 1.4 to CDI.
April 2017	1.5	Document rev 1.5 supports Ferry Bridge R1.3.2. Multiple REC images per FPGA and synchronization.
June 2017	1.6	Document rev 1.6 supports Ferry Bridge R1.3.3.
August 2017	1.7	Document rev 1.7 supports Ferry Bridge R1.4.0.
October 2018	1.8	Document rev 1.8 supports Ferry Bridge R1.4.1.

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1 Introduction

This document provides system improvement compared to previous releases, system requirements, installation instructions, issues and limitations, and legal information for BBU.

This document contains a very high level overview of the Control Channel and PRACH functionality that has been added into the FBR design. The document highlights the key registers that are used in setting up and controlling the features.

The software package that is provided with this release is limited to the Sample Application. This updated Sample Application exercises the PRACH functionality that is implemented.

The document is not intended to provide a detailed overview of the IP design / hierarchy of the FBR IP.

1.1 Intended Audience

The target audience is Telecom Equipment Manufacturers (TEMs) and operators, software developers, test and validation engineers, and system integrators.

1.2 Customer Support

For technical support, including answers to questions not addressed in this product, visit the technical support forum, FAQs, and other support information at http://www.intel.com/software/products/support/. For NDA customers, contact your Intel Field Application Engineer (FAE) or the equivalent.

Note: If your distributor provides technical support for this product, contact your distributor, rather than Intel, for support.

1.3 Terminology

Table 1. Terminology

Term	Description
ARQ	Automatic Repeat Request
BBU	Base Band Unit
BW	Bandwidth
CE	Channel Estimation
CPRI	Common Public Radio Interface

Term	Description
CQI	Channel Quality Indication
CTC	Convolutional Turbo Code
DCI	Display Control Interface
DMRS	Demodulation Reference Signal
ECC	Error Checking and Correction
FBR	Ferry Bridge
FE	Front End
HARQ	Hybrid ARQ
LTE	Long Term Evolution
MAC	Media Access Control
MIMO	Multiple In Multiple Out
MMSE	Minimum Mean Squared Error
OVP	Open Virtualization Platform
PMI	Precoding Matrix Indicator
PRACH	Physical Random Access Channel
RLC	Radio Link Control
RS	Reference Signals
TEM	Telecom Equipment Manufacturer
UE	User Equipment
UL	Up Link

Table 2. Related Documentation

Title	Intel Document Number	Description
Intel® FlexRAN Ferry Bridge User Guide	548166	Describes operation of the Ferry Bridge unit.

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2 Changes for R1.4.1

2.1 New Feature

2.1.1 DPDK 18.08 Compatibility

Ferry Bridge drivers have been updated to be compatible with DPDK 18.08.

2.1.2 Intel® Ethernet Controller Support

Support for Intel® Ethernet Controller XL710 10/40 GbE has been added.

2.2 Resolved Issues for R1.4.1

2.2.1 Bug Fixes

None

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3 Changes Added for Previous Releases

3.1 Features Added for FBR 1.4.0

3.1.1 Images for the Terasic* FPGA card

R1.4.0 and later releases include support for the Terasic* FPGA card.

The Terasic images files are located in directories as below and each of those directories contains files necessary for installation:

- ferrybridge/fpga_terasic_images/DEV_CARD_4x4_REC_RE_6.1G
- ferrybridge/fpga_terasic_images/DEV_CARD_4x4_REC_REC_4.9G
- ferrybridge/fpga_terasic_images/DEV_CARD_2x2_REC_REC_2.4G
- ferrybridge/fpga_terasic_images/DEV_CARD_4x4_REC_REC_6.1G
- ferrybridge/fpga_terasic_images/DEV_CARD_2x2_REC_RE_2.4G

These images match the original AMC images listed below:

- ferrybridge/fpga_images/fbr_fpga_wrap_4x4_rec_re.jic
- ferrybridge/fpga_images/fbr_fpga_wrap_2x2_rec_rec.jic
- ferrybridge/fpga_images/fbr_fpga_wrap_2x2_rec_re.jic
- ferrybridge/fpga_images/fbr_fpga_wrap_4x4_4G9_rec_rec.jic
- ferrybridge/fpga_images/fbr_fpga_wrap_4x4_rec_rec.jic

3.1.2 MXG Feature (AMC card only)

The MXG feature contains the new 10MHz clock, implemented via a new PLL in the design.

3.1.3 Update to the REV_ID register

Each image can now be identified uniquely via reading of the REV_ID register.

3.2 Features Added for FBR 1.3.3

3.2.1 New Maximum Number of Instances

The maximum number of Ferry Bridge instances in the library has been increased from 2 to 8.

3.3 Features Added for FBR 1.3.2

3.3.1 Multiple Ports Per FBR

Release 1.3.2 and later releases support FBR images that support two REC instances per FBR device.

- fbr_fpga_wrap_2x2_rec_re.jic
- fbr_fpga_wrap_2x2_rec_rec.jic - New feature supported with 2 REC
- fbr_fpga_wrap_4x4_rec_re.jic
- fbr_fpga_wrap_4x4_rec_rec.jic – New feature supported with 2 REC

Figure 1 FBR R1.3.0 and Previous Release

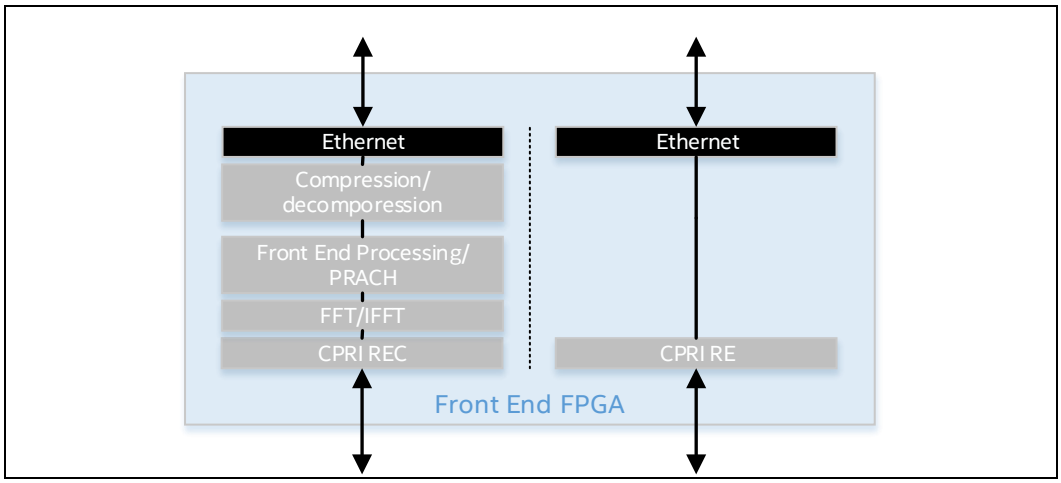
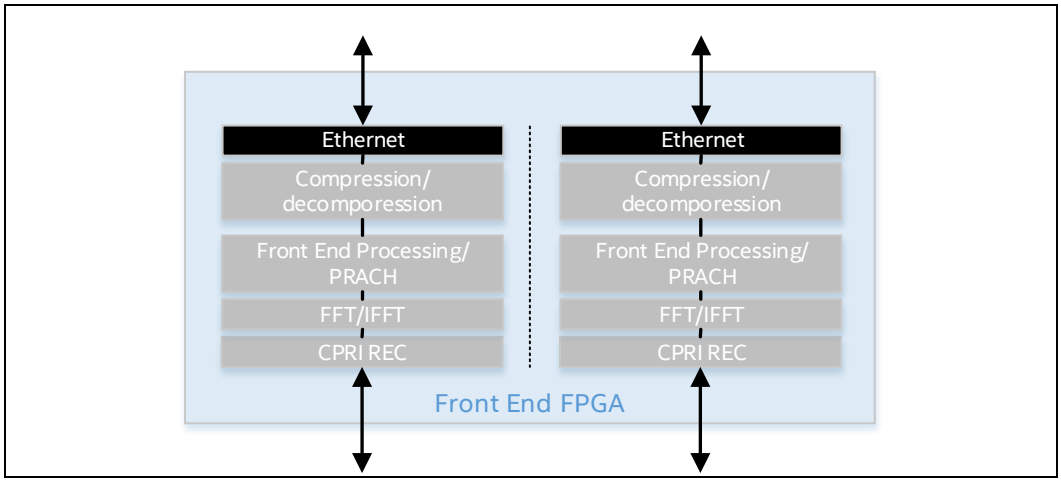


Figure 2 Features Added in FBR R1.3.2 Release



For the feature added in FBR R1.3.2, the SW uses two Ethernet ports to connect and configure both instances.

3.3.2 Synchronization Feature

R1.3.2 and later releases support two CPRI interfaces that can be used by a single application. It may be useful for the application to synchronize these CPRI interfaces so they use the same Radio Frame Pulse.

The CPRI IP can have its Hyper Frame number reset by toggling the `aux_tx_data_mask[64]` register of the CPRI IP. This feature is described in greater detail in the CPRI IP user guide.

Without describing the internal functionality of the CPRI IP here in this document, this section describes how the FBR facilitates toggling the `aux_tx_data_mask[64]` register on the CPRI IP. The register FRAME_SYNC_EN is used for this purpose.

3.3.2.1 How the Feature Works

There are 2 FBR cores in the design, FBR_CORE_0 and FBR_CORE_1. Each core has its own CPRI IP that it interacts with. When software writes to enable the frame sync feature in either of the cores, it is recognized as a request to synchronize both cores at the same time.

Thus to trigger this feature, all SW needs to do is enable it. However, SW needs to do this at a point in time where both CPRI IP's are alive and running. If either of the CPRI IP's are not actively running, then enabling this feature will not obtain the desired effect. An API is provided to perform this synchronization in the correct sequence as described in section 3.3.2.2.

This synchronization feature is supported in FBR R1.3.2 and later releases.

Code Extract 1: Register Definition to Enable the Synchronization Feature

```
#define RPE_FRAME_SYNC_EN (0x5024)
/**< @ingroup rpe_ferrybridge
 * Register value to enable the RFP Frame re-synchronisation. */
```

3.3.2.2 SW API to Enable Two Instance Handles and Synchronize

Code Extract 2: API Defined to Synchronize Multiple Instance Handles

```
/**
 ******************************************************************************
 * @ingroup rpe_common
 *
 * @description
 *      API to start the RPE Instance. Note starting the RPE instance means
 *      that any IO's associated with the instance will start communication.
 *      In the case of CPRI IO the communication will start at the radio frame
 *      boundary unless otherwise specified in feature setup.
 *      All configuration and setup of the instance must be complete before
 *      starting the instance.
 *
 * @context
 *         This function may be called from any context.
 *
 * @assumptions
```

```
 *         Instance Configuration complete.
 *
 * @sideEffects
 *         None
 *
 * @reentrant
 *        Yes
 *
 * @threadsafe
 *         No
 *
 * @param[in] handle               Array of Instance Handles associated with
the
 *                                 linked remote devices.
 *
 * @param[in] num_handles       The number of handles in the array
 *
 * @retval RPE_STATUS_SUCCESS       Function executed successfully.
 * @retval RPE_STATUS_FAIL          Function failed to read the register
 *                                  successfully.
 * @retval RPE_INVALID_PARAMETER    Invalid parameter used as input.
 *
 * @pre
 *         None
 *
 * @post
 *         None
 *
 * @note
 *         This function is blocking.
 *
 * @see
 *
 ******************************************************************************/
RpeStatus rpeStartAndSyncInstances(RpeInstanceHandle *handle, uint8_t
num_handles);
```

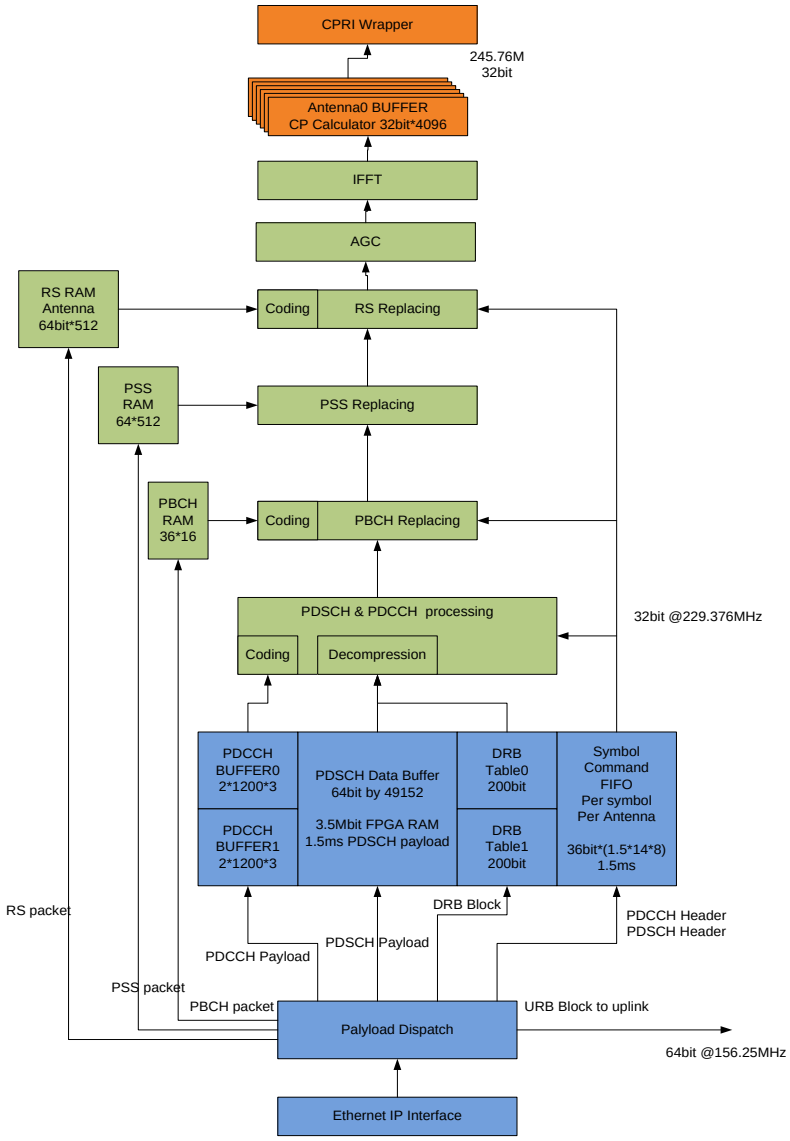
3.4 Features Added for FBR 1.3.1

The R1.3.1 release builds on the previous one by adding support for 4 antenna configurations. The control channel functionality is the same for both 2 antenna and 4 antenna. The latest release contains two FPGA RTL images one for 2 antenna and a separate one for 4 antenna.

3.4.1 Control Channels

Figure 3 illustrates the Ferry Bridge downlink IP path.

Figure 3 FBR Downlink Path



In the diagram, there are 3 IP blocks named:

- RS Replacing
- PSS Replacing
- PBCH Replacing

These 3 IP blocks contain the RTL code which has been upgraded to implement the feature as required by the LTE standard.

The following registers are used to enable the features.

1. PBCH Antenna Control

   Register Name: **PBCH_ANTx_CTRL** (where x ranges 0 to 7. Thus 1 per Antenna)

   Address: **0x2300 – 0x231C**
   Register Name: **PBCH_QPSK Vector**
   Address: **0x2340**

2. PSS Antenna Control

   Register Name: **PSS_ANTx_CTRL** (where x ranges 0 to 7. Thus 1 per Antenna)

   Address: **0x2000 – 0x201C**

3. RS Antenna Control

   Register Name: **RS_ANTx_CTRL** (where x ranges 0 to 7. Thus 1 per Antenna)

   Address: **0x2100 – 0x211C**
   Register Name: **RS_QPSK Vector**
   Address: **0x2140**

These registers are described in more detail in the MAS documentation. In terms of exact values to put in the registers in order to implement various functionality, please refer to section 2.3.5 in the MAS document.

The SAS document describes detailed information in sections 4.2.3.6, 4.2.3.7, and 4.2.3.8 with regard to the packets that are used to load up the RAM memories that are used in part to make the features work. We will not describe them any further in this document, just highlight them as something which is needed in order to make the feature work.

In terms of a general overview of the functionality, the control channel features are implemented inside the LTE grid in different subframes / time slots. For a very brief overview of where they are implemented in our RTL design, please refer to the following website and choose 20MHZ Bandwidth Channel. http://niviuk.free.fr/lte_resource_grid.html

The grid has a color coordinated picture, which highlights which subframes / time slots that each part of the feature is implemented in. It should be relatively straight forward to see from that diagram where the control channels will have data inserted into the LTE grid based on the function being enabled.

3.4.1.1 Configuring and Enabling Control Channels

In terms of enabling and using the control channels, the user must do the following when attempting to enable and use all 3 features together.

Step 1. Preload the PBCH memory by utilizing the PBCH_PACKET
Step 2. Preload the PSS memory by utilizing the PSS_PACKET
Step 3. Preload the RS memory by utilizing the RS_PACKET
Step 4. Enable the PBCH feature per Antenna by using registers PBCH_ANTx_CTRL. There is 1 register per Antenna
Step 5. Enable the PSS feature per Antenna by using registers PSS_ANTx_CTRL. There is 1 register per Antenna
Step 6. Enable the RS feature per Antenna by using registers RS_ANTx_CTRL. There is 1 register per Antenna

These 6 steps should be included in the general setup routine that SW implements to prepare the FBR design before any PDCCH / PDSCH samples are transmitted into the design.

At this point in the configuration setup, the 3 Control channels will have their RAM memories preloaded and the register space setup.

Once the CPRI IP has reported it is synchronized (as was already the case in past releases of the FBR design), the user can now attempt to send down PDCCH and PDSCH packets to trigger the functionality to be implemented in the downlink path.

Note that in the case of the PSS and PBCH, there is an extra control bit in the PDCCH packet that is used as an additional enable for those features. This is described in section 4.2.3.5 of the SAS document.

Thus, the PBCH and PSS features can be enabled in the design but they only come into effect when the SW controlled PDCCH packet tells the system that there is actual PBCH and or PSS information contained within the subframe. This allows the SW routines maintain control over the primary and secondary synchronization control feature without having to reconfigure the design each time.

It is important to note that each feature can be enabled independently of each other. The configuration scenario described here is just to show how all 3 would be enabled together.

Control Channels registers are setup as:

Register name	Address	Value
PBCH_ANT0_CTRL	0x2300	0x1
PBCH_ANT1_CTRL	0x2304	0x1
PBCH_QPSK_VECTOR	0x2340	0xEE02EE01
PSS_ANT0_CTRL	0x2000	0x1
PSS_ANT1_CTRL	0x2004	0x1
RS_ANT0_CTRL	0x2100	0x1
RS_ANT1_CTRL	0x2104	0x1
RS_QPSK_VECTOR	0x2140	0x1234ABCD

This configuration implements a 2 Antenna scenario using PBCH, PSS/SSS and RS Control Channels.

For 4 antenna scenario please update the appropriate configuration to enable all 4 antennas.

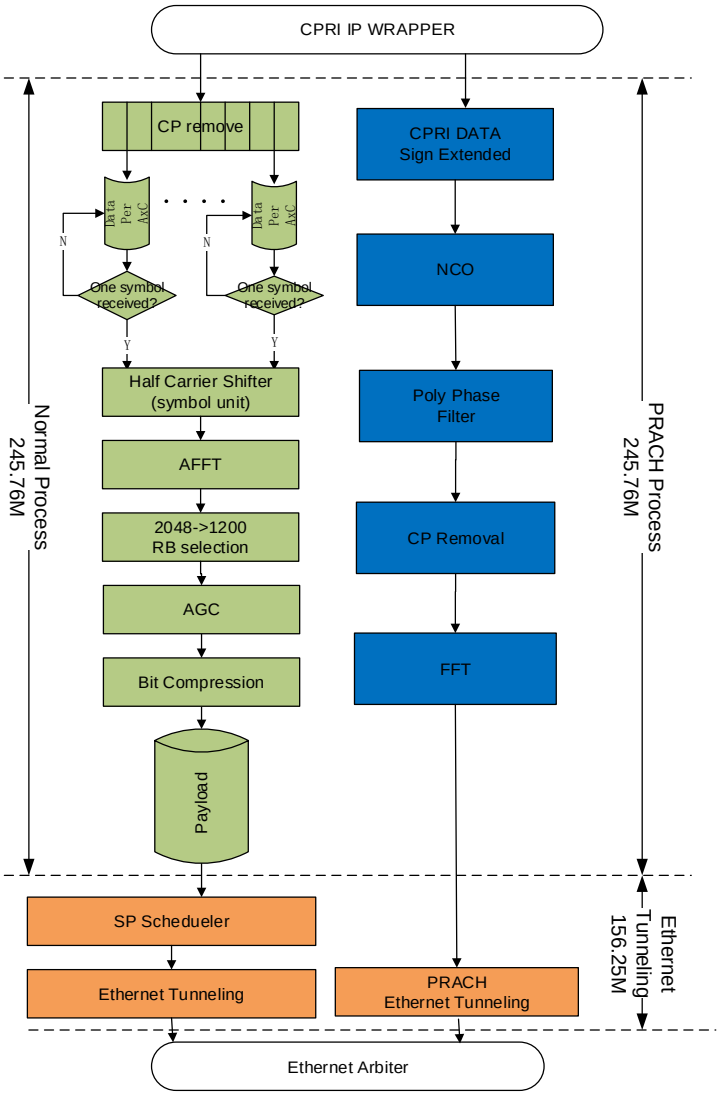
3.4.2 PRACH

Support for PRACH was also added in the 4x4 RTL image provided in the package. PRACH can be configured in the same way as previous releases.

Note the NCO calculation in the library has been updated based on feedback from RRH integration testing.

Figure 4 illustrates the FerryBridge uplink IP path. It is described in detail in the MAS document.

Figure 4 FBR Uplink Path



The PRACH path on the right hand side of the diagram is newly added to the FBR design. It maintains an uplink path feature which runs in parallel to the PUSCH feature. Note that the PUSCH feature has always been in the FBR design and no changes were implemented to that part of the design.

In the diagram, there are a number of sub IP blocks inside the PRACH path, namely:

- NCO
- Polyphase Filter
- CP Removal
- FFT

These IP blocks and their functionality are described in greater detail in section 2.3.6.3 on the MAS document.

The following registers are used to enable the feature:

1. Highest level PRACH Control Registers

   Register Name: FE_PRACH_CONFIG

   Address: 0x7000
   Register Name: FE_PRACH_CONFIG_INDEX

   Address: 0x7008

2. Second level PRACH Control Registers

   Register Name: FE_PRACH_NCO_PHASE
   Address: 0x700C

   Register Name: FE_PRACH_NCO_PHI_INC
   Address: 0x7010

   Register Name: FE_PRACH_STATUS
   Address: 0x7014

3.4.2.1 Configuring and Controlling the PRACH Function

In terms of enabling and using the PRACH function, the user must setup the highest level PRACH control registers as depicted above. The register setup steps should be included in the general setup routine that SW implements to prepare the FBR design before any PDCCH / PDSCH samples are transmitted into the design.

The PRACH is enabled via the FE_PRACH_CONFIG register and its PRACH implementation behavior is controlled via the FE_PRACH_CONFIG_INDEX register. This information is described in much greater detail in the MAS document. The FE_PRACH_CONFIG_REGISTER controls the reporting of PRACH packets based on the subframe setup that's done in that register.

The second level registers are used more to control internal operating behavior in the design, which whilst important to the feature itself, it's at a lower level and thus outside the scope of this document in terms of setting up the design to trigger some functional behavior.

Once the CPRI IP has reported it is synchronized (as was already the case in past releases of the FBR design), the user can now attempt to send down PDCCH and PDSCH packets to trigger the functionality to be implemented.

The PRACH related registers are setup as:

Register name	Address	Value
FE_PRACH_CONFIG	0x7000	0x3
FE_PRACH_CONFIG_INDEX	0x7008	0x0
FE_PRACH_NCO_PHASE	0x700C	0x0

This configuration turns on PRACH packets capturing during test scenario number 7.

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4 Known and Resolved Issues in Previous Releases

4.1 Known Issues

4.1.1 Known Issues for Release 1.3.1, 1.4.0, and 1.4.1

- SCSY:763 - PRACH issues with latest Ferry Bridge Release

  Problem happens with TM500 and CUE. On some runs PRACH is not detected at all. On the next restart/power cycle of Ferry Bridge, PRACH detection could be ok.

  Workaround is to enable PRACH on all 4 antennas.

4.2 Resolved Issues

4.2.1 Bug Fixes for R1.3.3

- SCSY:765 - 4.9G image shows error on AxC

  This was fixed by updating the CPRI_MAP_CONFIG value.

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5 Release Content and Dependencies

5.1 Release Content

The following table identifies the release content and revision numbers for the components in this release.

Table 3. Release Content

Component	Revision
BBU Pool Reference Software provided	R1.4.1

5.2 Dependencies

The following components are required for the Ferry Bridge reference software.

5.2.1 Dependencies for R1.4.1

Table 4. Dependencies for R1.4.1

Component	Revision
Intel® DPDK	18.08
Wind River* Linux* OVP	6.0.0.13
Intel® C++ Composer	18.0.1

5.2.2 Dependencies for R1.4.0

Table 5. Dependencies for R1.4.0

Component	Revision
Intel® DPDK	16.11
Wind River* Linux* OVP	6.0.0.13
Intel® C++ Composer	17.0.0

5.2.3 Dependencies for R1.3.3

Table 6. Dependencies for R1.3.3

Component	Revision
Intel® DPDK	16.11
Wind River* Linux* OVP	6.0.0.13
Intel® C++ Composer	17.0.0

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6 Hardware and Software Compatibility

6.1 Hardware Platform Configuration

The following hardware platform configuration has been verified for the Ferry Bridge R1.4.1 release.

Please refer to user guide for Ferry Bridge configuration.

Table 7. Canoe Pass System

Item	Description	Quantity
Motherboard	Intel® S2600CP2 Dual Socket Server Board Intel® C600-J Chipset Intel® Ethernet I350 10/100/1000 LAN Controller 2 ports (back panel) 1 DB-15 video connector (back panel) Integrated Matrox* G200 2D 1 DB9 serial port connector (back panel) 6 USB ports 4 (back panel), 2 (front panel) Codename = Canoe Pass	1
Chassis	Intel® Server Chassis P4000M 4U Pedestal Chassis with dual 750W PSU 4 SATA Hot-Swap bays (empty) 8 bays total but 4 are non-functional 5 Redundant hot-swap fans Codename = Union Peak M	1
CPU	Intel® Xeon® E5-2650 processor 8C, 95W, 2.0 GHz, 20M Cache. 8.0 GT/s Intel® QuickPath Interconnect (Intel® QPI) Technology Intel® Hyper-Threading Technology (Intel® HT), Intel® Virtualization Technology (Intel® VT), DDR3, Intel® Turbo Boost Technology Codename = Sandy Bridge-EP	2
System Memory	4GB DDR3 1333 RDIMMS with ECC 4GB DIMM per channel, 4 channels per CPU, 2 CPUs per board = total 8 RDIMMs per board Total System Memory = 32 GB	8
SATA Hard Drive	Western Digital* WD1002FAEX – 1.0 TB Capacity 64MB Cache Connected to SATA port 0	1

Item	Description	Quantity
Ethernet NIC	Intel® Ethernet Server Adapter X520-SR2 (2 ports) PCIe* (Dual 10 GbE) add-in card Codename = Niantic 25W Max Populated in slot 1 (CPU1)	1

6.2 Software Compatibility

6.2.1 Software Compatibility for R1.4.1

The LTE Reference stack software should be updated to R18.09 as this version supports DPDK 18.08.

6.2.2 Software Compatibility for R1.4.0

The LTE Reference stack software remains unchanged from R1.2.0. The previous software is compatible with the R1.4.0 FPGA.

6.2.3 Software Compatibility for R1.3.3

The LTE Reference stack software remains unchanged from R1.2.0. The previous software is compatible with the R1.3.3 FPGA.

6.2.4 Software Compatibility for R1.3.2

The LTE Reference stack software remains unchanged from R1.2.0. The previous software is not compatible with the R1.3.2 FPGA. It needs to be updated to use the version of DPDK labeled (16.11).

6.3 How to Update FPGA Image

Please refer to the section "Appendix A: Updating FPGA Image" in the *Intel® FlexRAN Ferry Bridge User Guide*.

6.4 Supported Operating Systems

The Wind River® Linux* OVP environment is supported.

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