FLEXRAN 5G NR FPGA OFFLOAD

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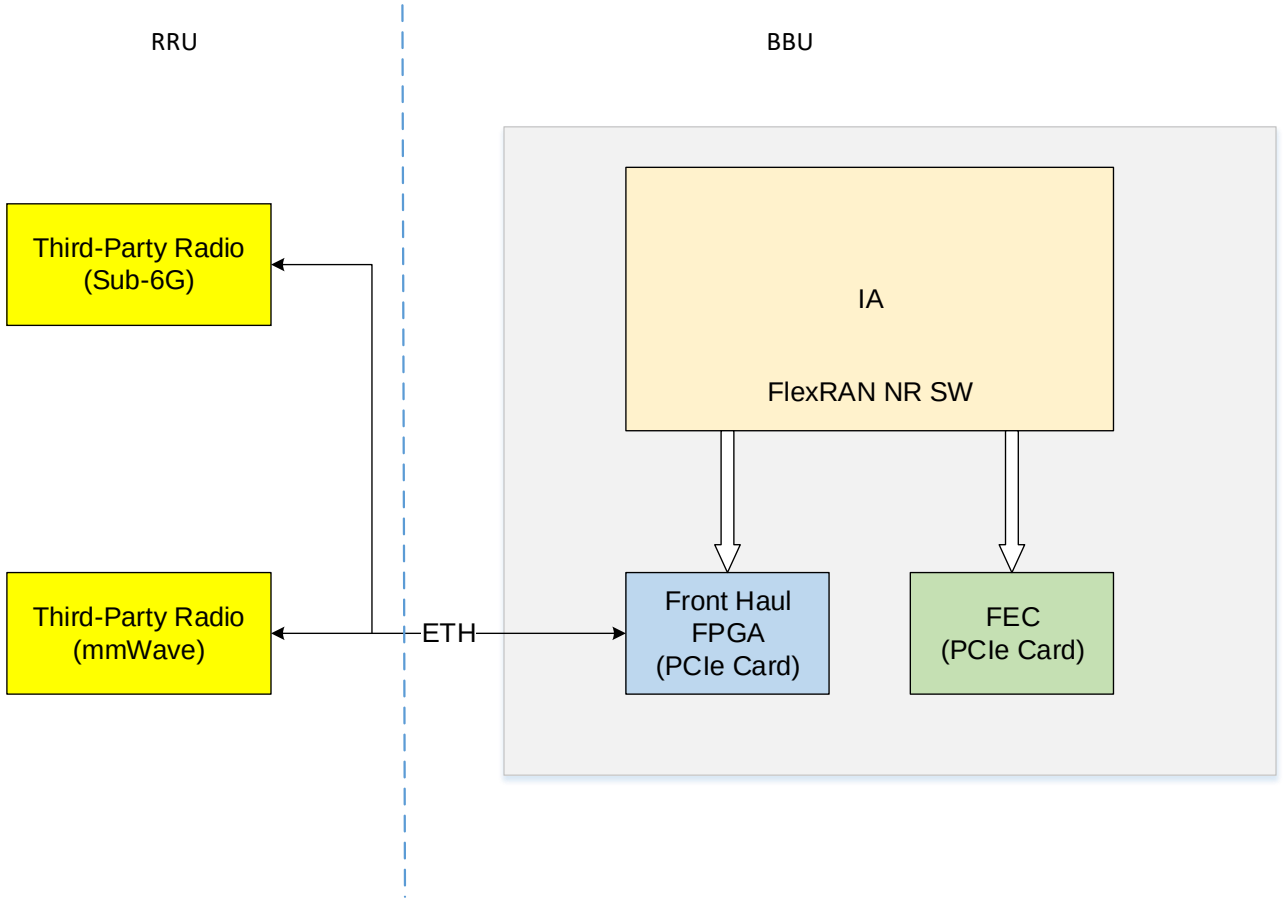
Agenda

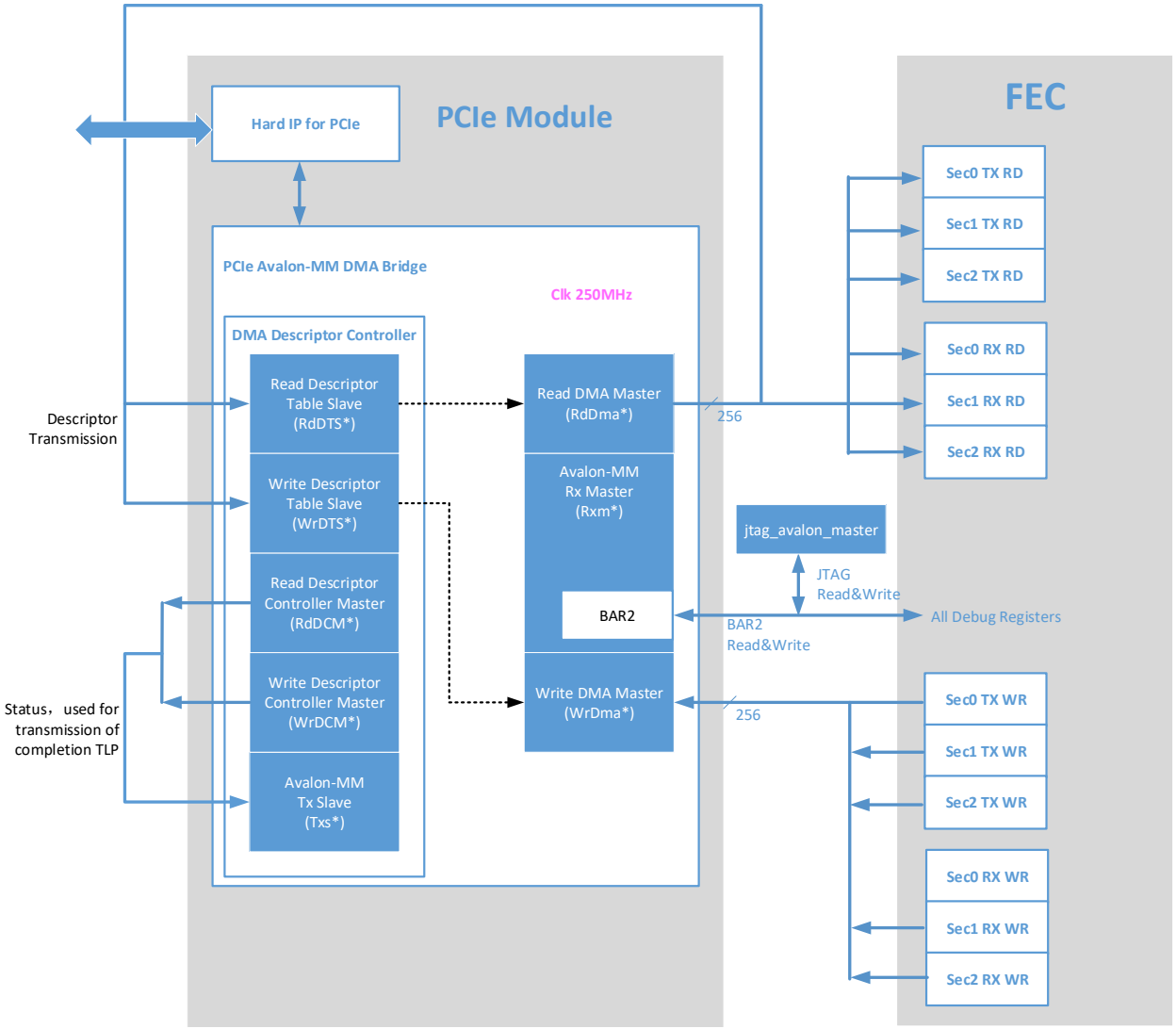
- SYSTEM ARCHITECTURE
- FEC FPGA ARCHITECTURE AND PROCESSING
- FRONT HAUL FPGA ARCHITECTURE AND PROCESSING

SYSTEM ARCHITECTURE



- Two FPGA cards
  - Front Hual
  - FEC
- Connection to IA by 8x PCIe interface
- Connection to Thrid-Party RF by ETH

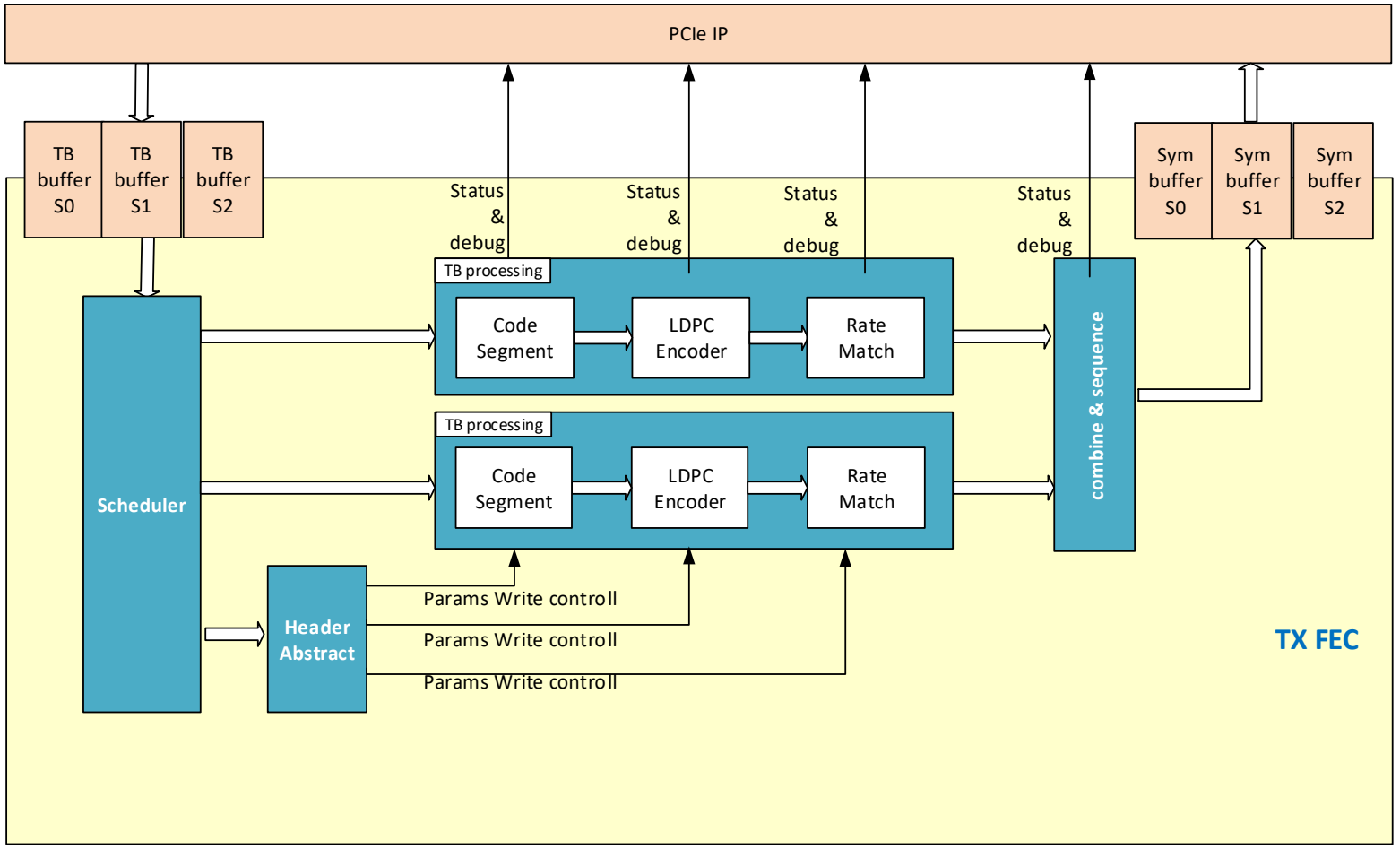
FEC PCIE DMA INTERFACE



- Avalon-MM DMA interface
- Single-Channel DMA
- 8x bandwidth, support read/write simultaneously with maximum 47Gbps
- 256 bit and 250MHz clock

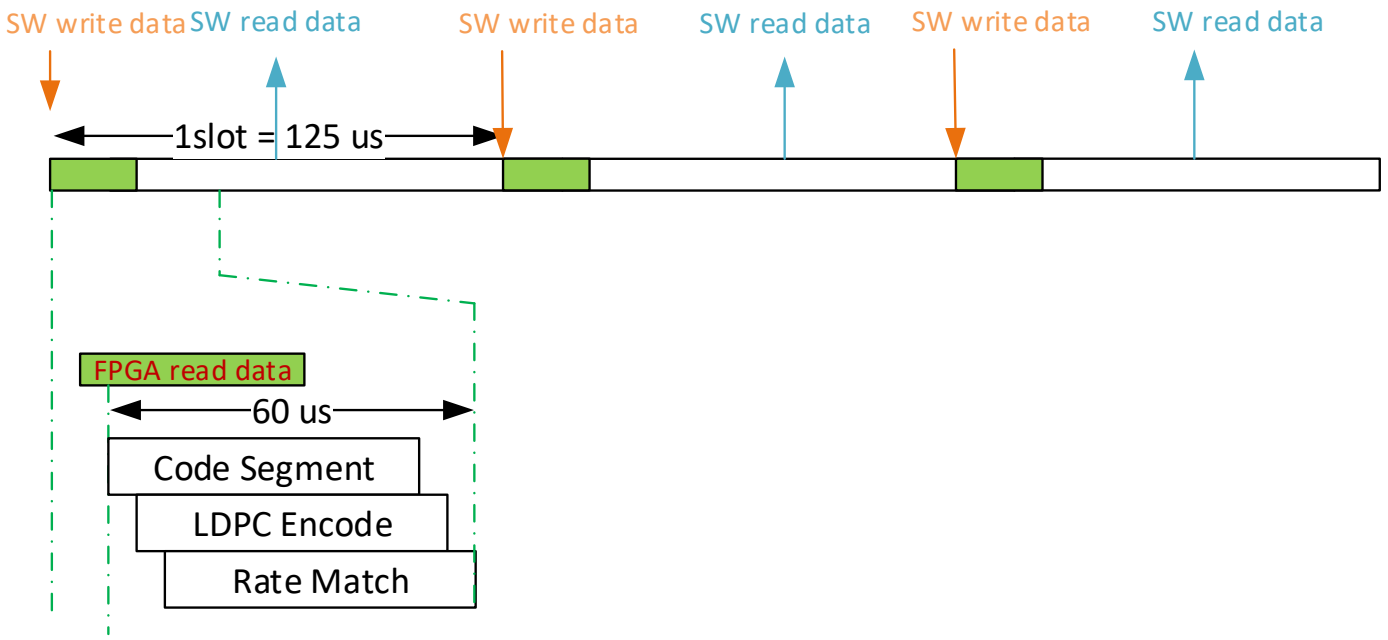
SW		PCIE/FPGA
TX_DMA	=	DMA READ
RX_DMA	=	DMA WRITE

FEC TX ARCHITECTURE



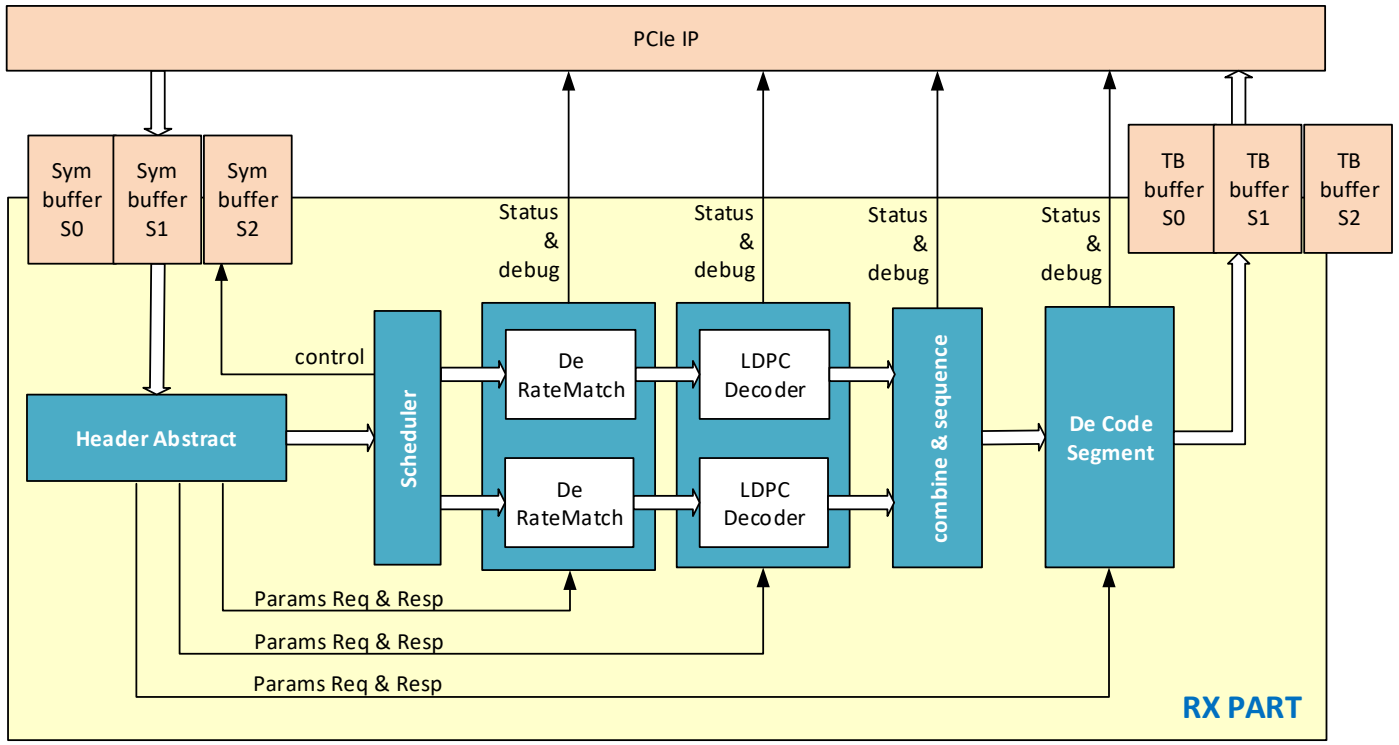
- 66RB*12SC*11Symbols*256QAM*4Layers*3Sectors
- Control information and TX TB data are in one TB package for each TB
- Block Function
  - TB CRC
  - Code Block Segment
  - CB CRC
  - LDPC Encoder
  - LDPC Rate Match
- Each sector has separate buffer space
- None DMA buffer is pingpong buffer

TX FEC Processing Pipeline



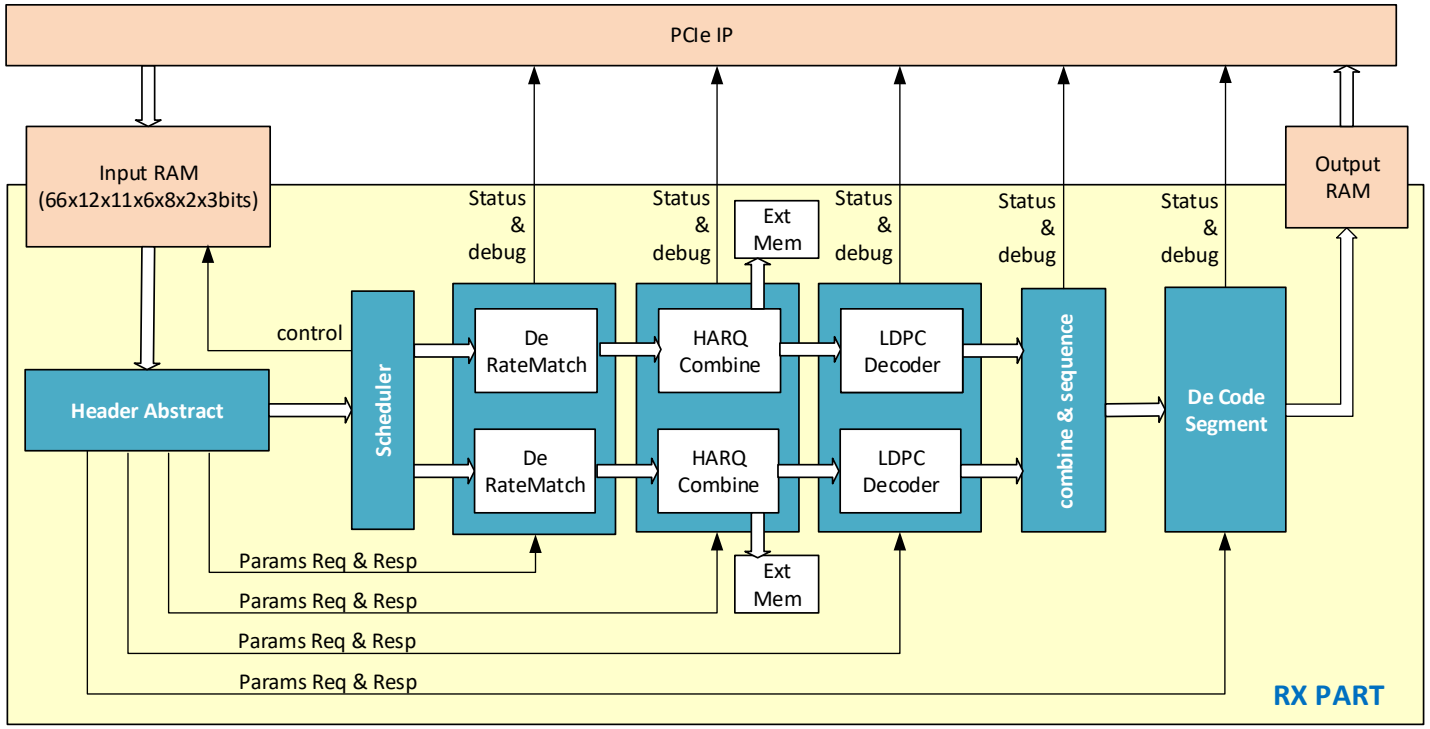
- TB level processing
- Pipeline based on code block
- Processing timing target is 50% of slot time

FEC RX ARCHITECTURE WITHOUT HARQ



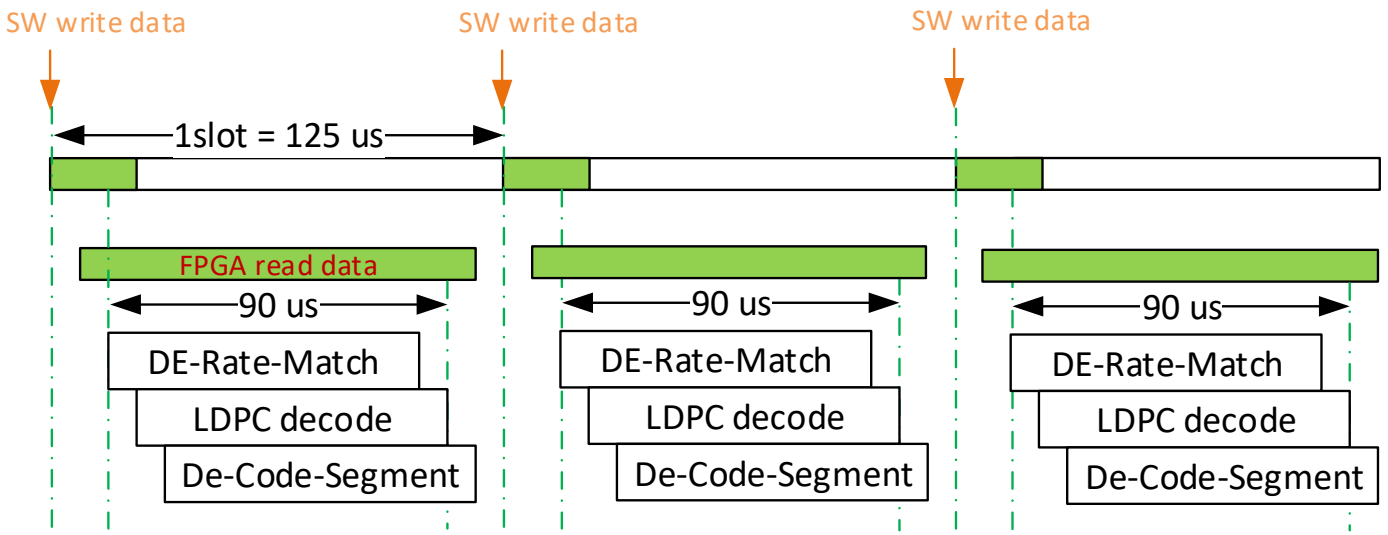
- 66RB*12SC*11Symbols*6QAM*8LLRbits*2Layers*3Sectors
- Block Function
  - De-RateMatch
  - LDPC Decoder
  - De-CodeBlock Segement
  - CB CRC
  - TB CRC
- 2 decoder core pingpong working for each link
- PingPang buffer at Output side

FEC RX ARCHITECTURE WITH HARQ



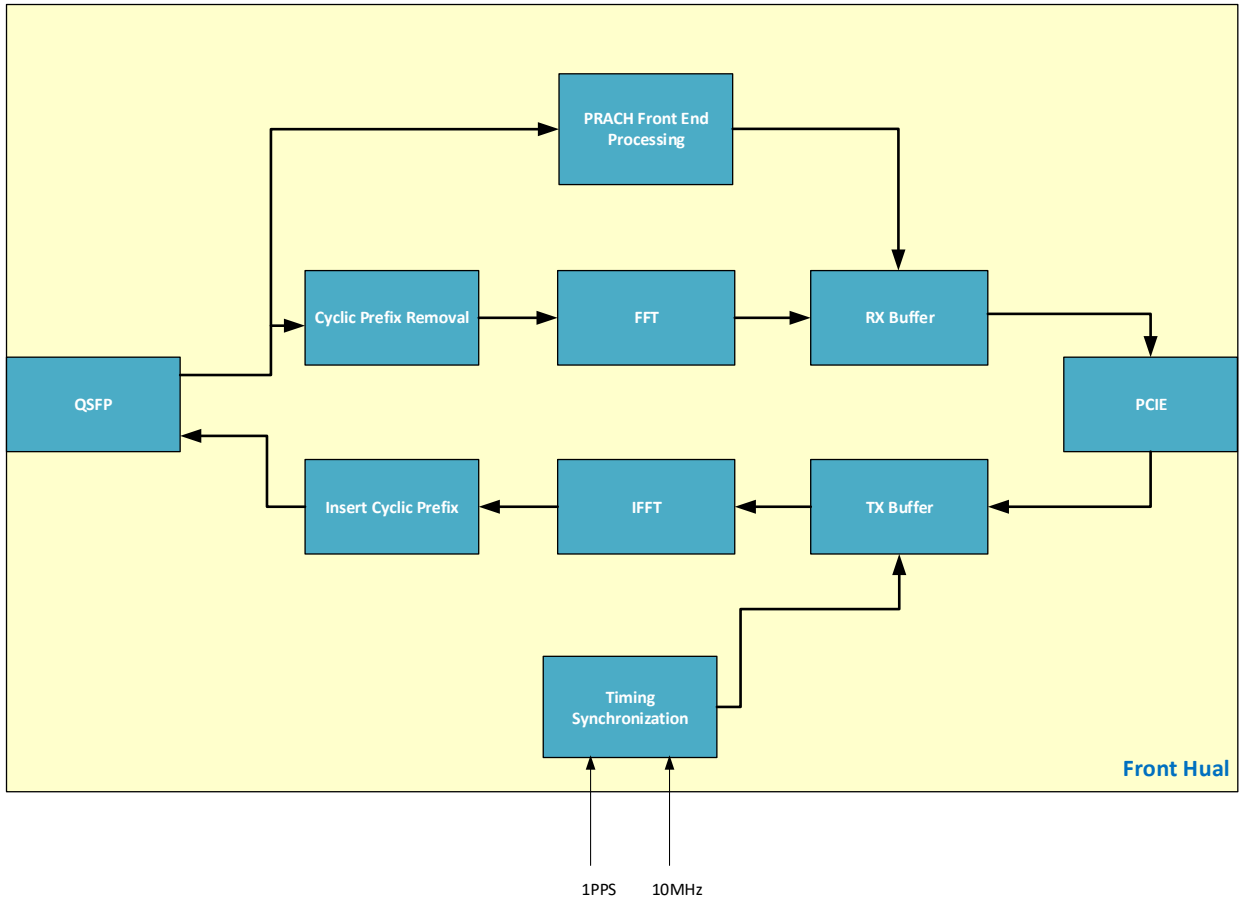
- HARQ combine and external Memory interface are added
- High speed external memory
- HARQ function based on code block

RX Processing Pipeline



- Code Block Level processing
- Pipeline based on code block
- Processing timing target is ~80% of slot time at 8 iteration

FRONTHAUL FPGA ARCHITECTURE



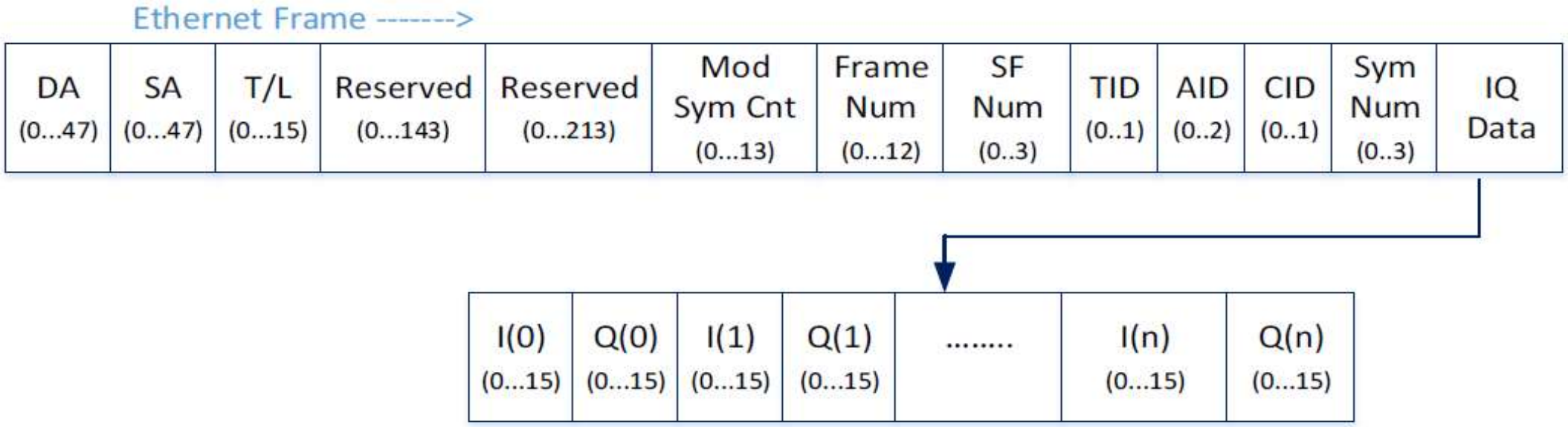
- FH Function
  - FFT/IFFT and CP Insert/remove
  - Timing synchronization
  - PRACH RX front processing
  - QSFP and PCIE interface

40Gbps Ethernet in QSFP Interface

- **1 Ethernet Packet contain data for 1 Sector & 1 Antenna & 1 Symbol**

  CP=136 -> Ethernet Packet length 4672 Bytes

  CP=72 -> Ethernet Packet length 4416 Bytes



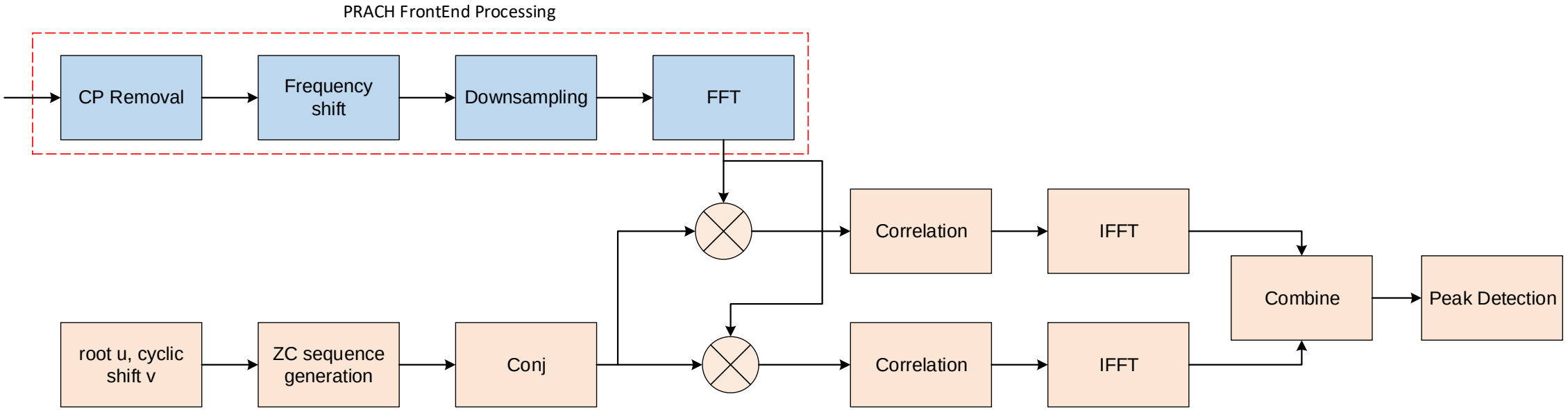
- **Control information is embedded in Ethernet Packet**
- **Plan move to standard specification (xRAN, 1914.3, .etc)**

Timing synchronization

- Input 1PPS and 10MHz from external source
- Slot/Subframe/Frame number generation to IA
- Align 1PPS and adjust start point of transmission

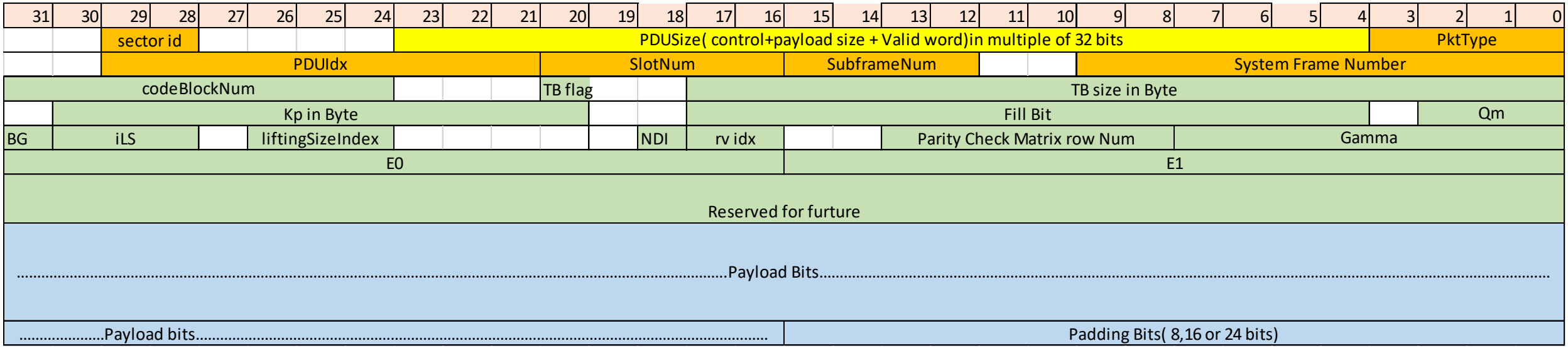
PRACH FrontEnd Processing

- LTE like PRACH format: Long sequence format
- New Format in NR: A1, A2, A3, B1, B2, B3, B4, C0, C2

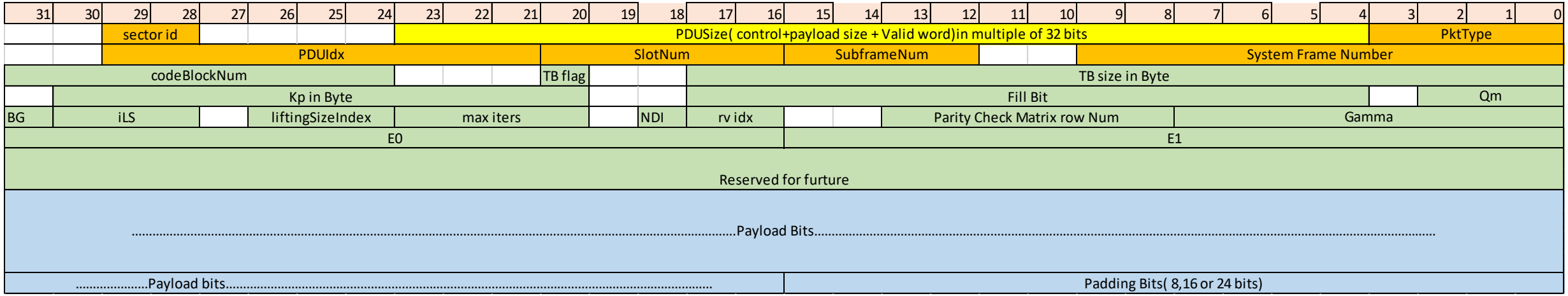


Backup

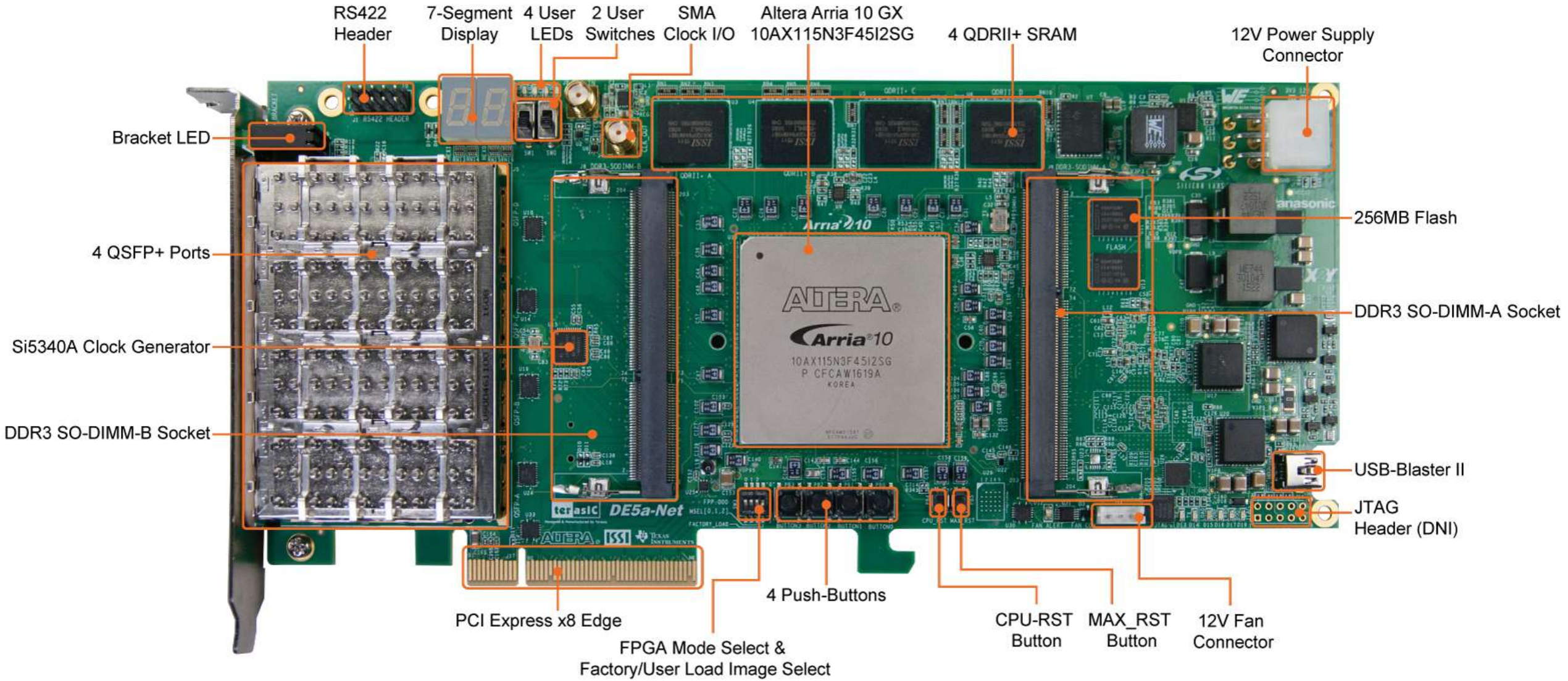
TX FEC TB package format



RX FEC Symbol package format



Terasic DE5a-Net board



TR10a-HL board