FlexRAN Reference Solution L1 XML Configuration

User Guide - Software Release v21.03

March 2021

Revision 1.9.4

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Revision History

Date	Revision	Description
March 2021	1.9.4	Changes for FlexRAN Software release v21.03: • Revised Table 15, Radio ConfigX Parameters • Revised Table 17, PHY Variables - PDSCH • Revised Table 18, PHY Variables - PUSCH • Revised Table 21, PHY Variables - PRACH • Revised Table 23, PHY Variables - Common • Revised Table 26, BBU Pooling Configuration Options • Updated Section 11.0, xRAN Configuration • Revised Section 13.0, Typical File Content
November 2020	1.9.3	Changes for FlexRAN Software release v20.11: • Updated Table 8, DPDK Parameters • Updated Table 18, PHY Variables - PUSCH • Added Section 6.6, PHY Variables – URLLC • Revised Section 13.0, Typical File Content
April 2020	1.9.2	Changes for FlexRAN Software release v20.04: • Updated Table 1, Terminology • Updated Table 5, API Delivery Scheme • Revised Table 8, Debug Log Parameters • Replaced Section 4.0, Power Options with DPDK Parameters • Revised Table 9, Radio Parameters DPDK memory Size • Revised Table 19, PHY Variables – PDSCH • Revised Table 20, PHY Variables – PUSCH • Revised Table 21, PHY Variables – PUCCH • Added Table 22, PHY Variables – SRS • Revised Table 23, PHY Variables – PRACH removed 4G only • Section 8.0, Corrected cross-reference and updated Table 26, CPY Binding Parameters • Revised Table 27, BBU Pooling Configuration Options • Section 10.0 FPGA Configuration added 5G only • Revised Table 29, xRAN Configuration Options (Only supported in 5GNR) • Section 12.0, Table 30, Stream Status Options revised • Section 13.0, Typical File Content revised
February 2020	1.9.1	FlexRAN Software release v20.02: • Added PdschSymbolSplit, IrcEnableThreshold, srsCeSplit, and • massiveMimoSrsCores to PHY variables in Chapter 6.

Date	Revision	Description
		• Added three variables in Chapter 11.
September 2019	1.9	Added FPGA version numbers, LLR output resolution, and WLS memory size, updated document for release 19.10.
July 2019	1.8	Added FPGA and xRAN configuration sections, updated document for release 19.06.
October 2018	1.7	Added Power Options table, removed Waddell Creek support, added updates for software release 18.09.
July 2018	1.6	Updated document with Radio Over Ethernet functionality for release 1.5.1.
April 2018	1.5	Covers software release 1.5.0. Added `fecEncBypass` and `fecDecBypass` to PHY variables. Removed some `IqLogDumpToFile` bit map parameters. Radio ports 0-7 now have parameter listings.
December 2017	1.4	Covers software release 1.4.0.
September 2017	1.3	Covers software release 1.3.0.
June 2017	1.2	Covers software release 1.1.2.
July 2017	1.1	OOC version that covers software release 1.1.1.
April 2017	1.0	Fourth release with the addition of mlogs, variables, system and timer thread entries, and some default value changes. Covers software release 1.1.0.
March 2017	0.3	Third release with additional configuration entries for DPDK, radio configuration, and wireless subsystem. Covers software release 0.5.1.
December 2016	0.2	Second release to clean up unused entries and add other updates. Covers software release 0.5.0.
October 2016	0.1	Initial release

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1.0 Introduction

This document describes the physical layer (PHY) configuration parameters intended to control Layer 1 (L1) operations for the FlexRAN L1. These parameters are stored in a configuration file using a subset of XML format, which is passed as an argument to the FlexRAN L1 application at startup.

For example, `./l1app -cfgfile=phycfg.xml`.

1.1 Terminology

Table 1. Terminology

Term	Description
API	Application Programming Interface
BBDEV	Baseband Device
BBU	Base Band Unit
CPRI	Common Public Radio Interface
DPDK	Data Plane Development Kit
DU	Data Unit
FEC	Forward Error Correction
FIFO	First-In, First-Out
FPGA	Field-Programmable Gate Array
FFT	Fast Fourier Transform
5GNR	Fifth Generation New Radio
IQ	In-Phase Quadrature
L1	Layer 1
MAC	Media Access Control
MMSE	Minimum Mean Square Error
ORAN	Open Radio Access Network
PHY	Physical Layer
PMD	Poll Mode Driver
PRACH	Physical Random Access Channel
PDSCH	Physical Downlink Shared Channel

Term	Description
PUCCH	Physical Uplink Control Channel
PUSCH	Physical Uplink Shared Channel
ROE	Radio over Ethernet IEEE 1914.3
RU	Radio Unit
SRS	Sounding Reference Signal
TTI	Transmission Time Interval
WLS	Wireless Subsystem Interface
xRAN	Extensible Radio Access Network

1.2 Reference Documents

Table 2. References

Title	Document Number
FlexRAN Reference Solution L2-L1 API Specification	571742
FlexRAN Reference Solution L1 User Guide	570228
FlexRAN Reference Solution Software Release Notes	575822
O-RAN Fronthaul Working Group Control, User and Synchronization Plane Specification (ORAN-WG4.CUS.0-v02.00)	https://www.o-ran.org/specifications

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2.0 Definitions

Note: In this guide, the column "Influence on PHY Perf." indicates the parameter affects processing time.

2.1 Internal Parameters

Table 3. Internal Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
Version	ASCII String	No	XML version string (for example, 1.0). Needs to match the internal PHY XML version.	19.06

2.2 API Delivery Scheme

Table 4. API Delivery Scheme

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
successiveNoApi	Integer	No	A maximum number of successive missing APIs during a TTI from the L2+ allowed before triggering a PHY stop.	15
wls_dev_name	String	No	Full path to wls device used for transport of MAC-PHY API (for example, /dev/wls0).	/dev/wls
wlsMemorySize	Hex Integer	Yes	WLS Memory Size. The default is 1GB. Leaves for 10 MB for the structure that is shared within this 1 GB.	0x3F600000

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3.0 PHY Logging Parameters

3.1 Iq Logs

Table 5. Iq Log Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
dlIqLog	Single Digit	Yes	Enable Dl Iq logging. 0 = Disabled 1 = Enabled	0
ulIqLog	Single Digit	Yes	Enable Ul Iq logging. 0 = Disabled 1 = Enabled	0
iqLogDumpToFile	Unsigned Integer	Yes	Enable iq log dump to a file. Twenty-three files can be enabled or disabled, as explained in phycfg.xml, which defines the bit fields used for this purpose.	0

Table 6. IqLogDumpToFile Bit Map

Bit	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
0	Single Bit	Yes	Enable/Disable the creation of the gDlIfftInxp-x.bin file(s) that contain the frequency domain input samples to the DL IFFT for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
1	Single Bit	Yes	Enable/Disable the creation of gDlIqAntp-x.bin file(s) that contain the DL IFFT Output time-domain iq samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0

Bit	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
2	Single Bit	Yes	Enable/Disable the creation of the `gUlIqAntp-x.bin` file(s) that contain the UL time-domain FFT input iq samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
3	Single Bit	Yes	Reserved.	0
4	Single Bit	Yes	Enable/Disable the creation of the `gULFFTAlawp-x.bin` file(s) that contain the UL `FFTAlaw` encoded FFT frequency domain output IQ samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
5	Single Bit	Yes	Enable/Disable the creation of the `gUlFFTOutp-x.bin` file(s) that contain the UL FFT OUT frequency-domain IQ samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
6	Single Bit	Yes	Reserved.	0
7	Single Bit	Yes	Enable/Disable the creation of the `gUlFFTOutAntExpp-x.bin` file(s) that contain the UL FFT OUT Exponent and the AGC value samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
8	Single Bit	Yes	Enable/Disable the creation of the `gUlPrachAntp-x.bin` file(s) that contain the PRACH input samples for DPDK port p and each antenna x in binary format. 0 = Disabled 1 = Enabled	0
9-15	Single Bit	Yes	Reserved.	0

Bit	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
16	Single Bit	Yes	Enable/Disable the creation of the gDlIfftInxp-x.txt file(s) that contain the input samples to the DL IFFT for DPDK port p and each antenna x in ASCII format. 0 = Disabled 1 = Enabled	0
17	Single Bit	Yes	Enable/Disable the creation of gDlIqAntp-x.txt file(s) that contain the DL iq samples for DPDK port p and each antenna x in ASCII format. 0 = Disabled 1 = Enabled	0
18	Single Bit	Yes	Enable/Disable the creation of the gUlIqAntp-x.txt file(s) that contain the UL iq samples for DPDK port p and each antenna x in ASCII format. 0 = Disabled 1 = Enabled	0
19	Single Bit	Yes	Reserved.	0
20	Single Bit	Yes	Enable/Disable the creation of the gULFFTAlawp-x.txt file(s) that contain the UL FFTAlaw samples for DPDK port p and each antenna x in ASCII format. 0 = Disabled 1 = Enabled	0
21	Single Bit	Yes	Enable/Disable the creation of the gUlFFTOutp-x.txt file(s) that contain the UL FFT OUT samples for DPDK port p and each antenna x in ASCII format. 0 = Disabled 1 = Enabled	0
22-31	Single Bit	Yes	Reserved.	0

3.2 Debug Logs

Table 7. Debug Log Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
phyMLog	Single Digit	No	Dump the last MLog history information automatically at the PHY stop.	1
phyStats	Single Digit	No	Save PHY statistics in a file.	1

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4.0 DPDK Parameters

Table 8. DPDK Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
dpdkFilePrefix	String	N/A	name of DPDK memory zone, needs to align between primary and secondary process	gnb0
dpdkMemorySize	Integer	N/A	DPDK memory size allocated from hugepages [MB].	2048
dpdkIrqMode	Single Digit	N/A	DPDK Interrupt mode enabled. 0 = Disabled, PMD is used 1 = Enabled, uio irq is used	1
dpdkBasebandFecMode	Integer	Yes	DPDK FEC BBDEV to use [0 - SW, 1 – FEC Hardware Accelerator, 2 – Allow both SW and FEC Hardware Accelerator]	1
dpdkBasebandDevice	String	No	DPDK BBDev name added to the whitelist. The argument format is <[domain:]bus:devid.func>	0000:0e:00.0

4.1 DPDKSharedResource

Table 9. DPDK Shared Resource Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
numSharedResource	Integer	N/A	number of the set of shared ports and corresponding memory, maximum 4, if none, set to 0	0

4.1.1 SharedResource0 (5G only)

Table 10. Shared Resource0 Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
mempoolName0	String	N/A	DPDK memory pool name, if don't want to init memory pool, set name to 0	fast_pkt

numElement0	Integer	N/A	The number of elements in the mempool. The optimum size for a mempool is when n is a power of two minus one: n = (2^q - 1)	65535
elementSize0	Integer	N/A	The size of each element	2048
privateDataSize0	Integer	N/A	The size of the private data appended after the mempool structure	64
ringName0	String	N/A	DPDK ring pool name, if don't want to init ring, set name to 0	0
ringSize0	Integer	N/A	The size of the ring (must be a power of 2)	1024
portAddr0	String	N/A	DPDK port pci-e address, if don't want to init port, set number to 0	0000:af:00.0
portSocketIdx0	Integer	N/A	DPDK port socket index	1
txQueueNum0	Integer	N/A	Number of Tx queue	1
txQueueDesc0	Integer	N/A	Tx queue description	512
rxQueueNum0	Integer	N/A	Number of Rx queue	1
rxQueueDesc0	Integer	N/A	Rx queue description	128
maxPayloadSize0	Integer	N/A	Max payload size, if larger than 1500Bytes, Jumbo frame will be enabled	9728

4.1.2 SharedResource1 (5G only)

Table 11. Shared Resource1 Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
mempoolName1	String	N/A	DPDK memory pool name, if don't want to init memory pool, set name to 0	header_pkt
numElement1	Integer	N/A	The number of elements in the mempool. The optimum size for a mempool is when n is a power of two minus one: n = (2^q - 1)	65535
elementSize1	Integer	N/A	The size of each element	2048
privateDataSize1	Integer	N/A	The size of the private data appended after the mempool structure	64

ringName1	String	N/A	DPDK ring pool name, if don't want to init ring, set name to 0	0
ringSize1	Integer	N/A	The size of the ring (must be a power of 2)	1024
portAddr1	String	N/A	DPDK port pci-e address, if don't want to init port, set number to 0	0000:af:00.1
portSocketIdx1	Integer	N/A	DPDK port socket index	1
txQueueNum1	Integer	N/A	Number of Tx queue	2
txQueueDesc1	Integer	N/A	Tx queue description	512
rxQueueNum1	Integer	N/A	Number of Rx queue	1
rxQueueDesc1	Integer	N/A	Rx queue description	128
maxPayloadSize1	Integer	N/A	Max payload size, if larger than 1500Bytes, Jumbo frame will be enabled	9728

4.1.3 SharedResource2 (5G only)

Table 12. Shared Resource2 Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
mempoolName2	String	N/A	DPDK memory pool name, if don't want to init memory pool, set name to 0	clone_pkt
numElement2	Integer	N/A	The number of elements in the mempool. The optimum size for a mempool is when n is a power of two minus one: n = (2^q - 1)	65535
elementSize2	Integer	N/A	The size of each element	2048
privateDataSize2	Integer	N/A	The size of the private data appended after the mempool structure	64
ringName2	String	N/A	DPDK ring pool name, if don't want to init ring, set name to 0	0
ringSize2	Integer	N/A	The size of the ring (must be a power of 2)	1024
portAddr2	String	N/A	DPDK port pci-e address, if don't want to init port, set number to 0	0
portSocketIdx2	Integer	N/A	DPDK port socket index	0

txQueueNum2	Integer	N/A	Number of Tx queue	1
txQueueDesc2	Integer	N/A	Tx queue description	512
rxQueueNum2	Integer	N/A	Number of Rx queue	1
rxQueueDesc2	Integer	N/A	Rx queue description	128
maxPayloadSize2	Integer	N/A	Max payload size, if larger than 1500Bytes, Jumbo frame will be enabled	9728

4.1.4 SharedResource3 (5G only)

Table 13. Shared Resource3 Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
mempoolName3	String	N/A	DPDK memory pool name, if don't want to init memory pool, set name to 0	pdu3
numElement3	Integer	N/A	The number of elements in the mempool. The optimum size for a mempool is when n is a power of two minus one: n = (2^q - 1)	65535
elementSize3	Integer	N/A	The size of each element	2048
privateDataSize3	Integer	N/A	The size of the private data appended after the mempool structure	64
ringName3	String	N/A	DPDK ring pool name, if don't want to init ring, set name to 0	sdu3
ringSize3	Integer	N/A	The size of the ring (must be a power of 2)	1024
portAddr3	String	N/A	DPDK port pci-e address, if don't want to init port, set number to 0	0
portSocketIdx3	Integer	N/A	DPDK port socket index	0
txQueueNum3	Integer	N/A	Number of Tx queue	1
txQueueDesc3	Integer	N/A	Tx queue description	512
rxQueueNum3	Integer	N/A	Number of Rx queue	1
rxQueueDesc3	Integer	N/A	Rx queue description	128

maxPayloadSize3	Integer	N/A	Max payload size, if larger than 1500Bytes, Jumbo frame will be enabled	9728

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5.0 Radio Parameters

Table 14. Radio Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
radioEnable	Single Digit	N/A	Enable radio interface. Emulation mode is activated if the radio is disabled. 0 = Disabled 1 = Enabled Ferry Bridge 2 = Enabled ROE	1
ferryBridgeMode	Single Digit	N/A	FerryBridge operation mode. 0 = LTE MODE 1 = CPRI BYPASS MODE	0
ferryBridgeEthPort	Single Digit	N/A	Number of Ethernet ports in FerryBridge. 0 = DPDK Port 0 1 = DPDK Port 1 2 = Both DPDK port 0 and port 1 (CA mode with two ETH)	1
ferryBridgeSyncPorts	Single Digit	N/A	FerryBridge Synchronized CPRI Ports. 0 = No reSync REC and RE FPGA 1 = reSync REC and REC FPGA	0
ferryBridgeOptCableLoopback	Single Digit	N/A	FerryBridge Loopback mode. 0 = No optical loopback connected Rec<->RE 1 = Optical loopback connected REC<->RE	0

5.1 Radio Configuration Parameters

5.1.1 Radio Config 0 - 7 Parameters

For each Radio Config, replace the “X” in radioCfgX with the configured radio.

For example for Radio Config 3:

radioCfgX -> radioCfg3

Table 15. Radio ConfigX Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
radioCfgXPCIeEthDev	String	No	DPDK: Add a PCI device in whitelist. The argument format is: <[domain:]bus:devid.func>	0000:08:00.0
radioCfgXDpdkRx	Integer	No	DPDK: RX thread core ID [0-max-core]	1
radioCfgXDpdkTx	Integer	No	DPDK: TX thread core ID. [0-max-core]	2
radioCfgXTxAnt	Integer	Yes	The number of TX antennas-1, 2, 4. For ROE: 8 or 12	4
radioCfgXRxAnt	Integer	Yes	The number of RX antennas-1, 2, or 4. For ROE: 8 or 12	4
radioCfgXRxAgc	Integer	Yes	RX AGC configuration. 0 = RX AGC disabled 1 = RX AGC enabled (default for FPGA release 1.3.1)	0
radioCfgXRxAntVertical	Integer	Yes	Number of Rx Antenna Vertical Elements. Range: [1 -> 64]	1
radioCfgXRxAntHorizontal	Integer	Yes	Number of Rx Antenna Horizontal Elements. Range: [1 -> 64]	1
radioCfgXRxAntPolarization	Integer	Yes	Number of Rx Antenna Polarization settings. Range: [1, 2]	1
radioCfgXNumCell	Integer	Yes	The number of cells running on this port. 1 – 4 cells	1
radioCfgXCell0PhyId	Integer	No	Phy Instance ID mapped to the first CPRI port.	0
radioCfg0Cell1PhyId	Integer	No	Phy Instance ID mapped to the second CPRI port.	1
radioCfgXCell2PhyId	Integer	No	Phy Instance ID mapped to the third CPRI port.	2

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
radioCfgXCell3PhyId	Integer	No	Phy Instance ID mapped to the fourth CPRI port.	3
radioCfgXCell4PhyId	Integer	No	Phy Instance ID mapped to the fifth CPRI port.	4
radioCfgXCell5PhyId	Integer	No	Phy Instance ID mapped to the sixth CPRI port.	5
radioCfgXriuMac	String	No	Radio Interface Unit Mac address for ROE.	11:22:33:44:55:66

5.1.2 Radio Port Selection

Table 16. Radio Port Selection Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
radioPort0	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort0	0
radioPort1	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort1	1
radioPort2	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort2	2
radioPort3	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort3	3
radioPort4	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort4	4
radioPort5	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort5	5
radioPort6	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort6	6
radioPort7	Integer	No	Selects Radio Config n where *n* is ∈[0,1,2,3,4,5,6,7] for radioPort7	7

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6.0 PHY Variables

6.1 PHY Variables - PDSCH

Table 17. PHY Variables - PDSCH

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
fecEncBypass	Single Digit	No	**(4G only)** Bypass FEC Encoder to simulate offload of FEC to FPGA. Used for profiling only. 0 = Encoder runs 1 = Bypass Encoder	0
fecEncSplit	Single Digit	Yes	The Max number of parallel tasks the DL FEC Encoder is split into. The range is 1 to 4. If the wrong value is entered, it defaults to 1. If fecEncBypass is set to 1, fecEncSplit is forced to 1.	4
PdschOfdmSplitEnable	Single Digit	Yes	**(5G Only)** Enable splitting PDSCH symbol processing into symbols instead of splitting by UE groups and UEs. 0 = PDSCH symbol processing split by UE groups and UEs, 1 = PDSCH symbol processing split by symbols	0
PdschSymbolSplit	Integer	Yes	**(5G only)** Split processing for PDSCH symbol processing to do parallel processing. NOTE: Valid value 0~8. The pipeline first splits the processing by MU-groups; if it were not sufficient, it would split by UE until reaching the total split number, which is set here.	0
PdschDlWeightSplit	Integer	Yes	**(5G only)** Split processing for PDSCH Downlink beamforming weights to do parallel processing.	0

			NOTE: Valid value 0~8. The pipeline first splits the processing by MU-groups; if it were not sufficient, it would split by RB until reaching the total split number, which is set here. The splitting by RB considers the workload distribution equality as well as cache alignment.	

6.2 PHY Variables - PUSCH

Table 18. PHY Variables - PUSCH

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
taFiltEnable	Single Digit	No	**(4G only)** TA filtering. 0 = Disabled 1 = Enabled	1
ircEnable	Single Digit	Yes	**(4G only)** IRC enable (always disabled in this release). 0 = Disabled 1 = Enabled	0
mmseDisable	Single Digit	Yes	**(4G only)** Minimum mean square error (MMSE) symbol equalizer disable. 0 = MMSE enabled 1 = MMSE disabled	0
chanEstSplit	Single Digit	Yes	**(5G only)** Split processing for Channel Estimation for PUSCH to do parallel processing. NOTE: Valid value 0,1,2,4. The pipeline flexibly decides to split the processing by MU-group, UE, or layer. It depends on how many UEs/layers it schedules in each TTI.	0
CEInterpMethod	Integer	Yes	**(5G only)** Frequency interpolation method for PUSCH Channel Estimation. Bit 0 = 0: 1 RB sinc interpolation 1: 4 RB sinc interpolation	0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
			Bit 1 = 0: Apply timing advance compensation post frequency interpolation. 1: Apply timing advance compensation pre frequency interpolation.	
mmseSplit	Single Digit	Yes	**(5G only)** Split processing for the MMSE algorithm for PUSCH to do parallel processing. NOTE: Valid value 0~8. The pipeline first splits the processing by MU-groups; if it were not sufficient, it would split by RB until reaching the total split number, which is set here. The splitting by RB considers the workload distribution equality as well as cache alignment.	0
PuschUlWeightSplit	Integer	Yes	**(5G only)** Split processing for PUSCH Uplink beamforming weights to do parallel processing. NOTE: Valid value 0~8. The pipeline first splits the processing by MU-groups; if it were not sufficient, it would split by RB until reaching the total split number, which is set here. The splitting by RB considers the workload distribution equality as well as cache alignment.	0
PuschDecompSplit	Integer	Yes	**(5G Only)** Split processing for Pusch xRAN/ORAN Decompression processing. Valid value 0~8. Will split by ports.	0
PuschLlrRxSplit	Integer	Yes	**(5G only)** Split processing for PUSCH LLR processing to do parallel processing.	0
fecDecBypass	Single Digit	Yes	**(4G only)** Bypass FEC Decoder to simulate offload of FEC to FPGA. Used for profiling only. 0 = Decoder runs 1 = Bypass Decoder	0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
fecDecSplit	Single Digit	Yes	**(4G only)** Max number of parallel tasks that the UL FEC Decoder is split into. The range is 1 to 4. If the wrong value is entered, it defaults to 1. If fecDecBypass is set to 1, fecDecSplit is forced to 1.	4
fecDecEarlyTermDisable	Integer	Yes	Software FEC Decoder Early Termination disabled. If 1, then programmed number of iterations are run from MAC PHY API regardless of CRC PASS	0
fecDecNumHalfIter	Integer	Yes	**Software FEC 4G** Decoder Number of half iterations. If 0, then the Number of half iterations is set to 6. Else this value is used	0
fecDecNumIter	Integer	Yes	**Software FEC 5G** Decoder number of iterations. If 0, then the number of iterations is set to 10. Else this value is used	0
llrOutDecimalDigit	Integer	Yes	(**5G Only**) Several decimal digits of LLR fixed-point output. If 0, then this value is set to **2**, which means LLR is symmetric 8S2 (range=-31 to 31). Else this value is used. Valid range 0~7.	2
IrcEnableThreshold	Integer	Yes	**(5G Only)** SNR Threshold to turn on 5GNR IRC equalizer. If set to -100, then IRC will be disabled.	-10
PuschNoiseScale	Integer	Yes	**(5G Only)** Scale factor used to scale measured noise to account for ChanEst errors for mu=0 and 2 layers. Valid Range: 1,2,3,4	2
CEFocEnable	Integer	Yes	**(5G Only)** Frequency Offset Compensation 0 = disable, 1= enable	0
CEFocGranularity	Integer	Yes	**(5G Only)**	768

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
			Frequency Offset Compensation granularity. Number of Resource Elements using the same frequency offset measurements. Valid Value: 1 – 3276	
PuschLinearInterpEnable	Integer	Yes	**(5G Only)** Enable/Disable time domain linear interpolation for PUSCH Channel Estimation 0 – Disable 1 – Enable	0
PuschLinearInterpGranularity 0->11	String	Yes	**(5G Only)** Setting of Time Domain Linear Interpolation type for each cell and for each Multi-User MIMO UE group. A maximum of MAX_MUMIMO_GROUP_NUM(16) for each cell. Valid Values: 99 = Nearest Neighbor 0 = Linear 1 = Linear 2 2 = Linear 3 3 = Linear 4 4 = Linear 6 Meaning of these methods are described in the Algorithms Release Document (610016). Example Input: 0, 3, 4, 99, 1 This will set UE group 0 to use Linear, UE Group 1 to use Linear 4, UE Group 2 to use Nearest Neighbor, etc...	99
DFTBfWeightGenEnable	Integer	Yes	**(5G Only)** Beamforming Weight generation algorithm choice. 0: Zero-Forcing based weight generation 1: DFT CodeBook based weight generation	0
BfWeightGenGranularity	Integer	Yes	**(5G Only)** Beamforming weight matrix generation RB pick granularity.	2

6.3 PHY Variables - PUCCH

Table 19. PHY Variables - PUCCH

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
pucchFormat2DetectThreshold	Integer	No	(**4G Only**) PUCCH Format 2 Detection Threshold for 4G	0
PucchSplit	Integer	Yes	(**5G Only**) Allow splitting of 5G PUCCH tasks to run in multiple cores. If 0 or 1, do not split; 2 = split to two sub-tasks; 4 = split to four sub-tasks	0

6.4 PHY Variables – SRS

Table 20. PHY Variables – SRS

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
SrsCeSplit	Integer	Yes	(**5G only**) Enable split processing for SRS channel estimation to do parallel processing	0

6.5 PHY Variables - PRACH

Table 21. PHY Variables - PRACH

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
prachDetectThreshold	Integer	No	Prach Detection Threshold	100
prachDetectFoCheck	Single Digit	Yes	Enable/Disable PRACH Frequency Offset detection. 0: Disable 1: Enable	0

6.6 PHY Variables – URLLC

Table 22. PHY Variables - URLLC

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
UrllcPuschFecSplit	Integer	Yes	**(5G Only)** For URLLC cells. 0 – FEC LDPC Decoder task will run in mode specified in <dpdkBasebandFecMode> field. (If dpdkBasebandFecMode = 1 means hardware, if 0 or 2, then software.) 1 - Split FEC LDPC Decoder task by 2 (half in software, half in FEC Accelerator hardware). Requires a value of 2 to be set for <dpdkBasebandFecMode>	0
UrllcBbdevIdEnd	Integer	Yes	**(5G Only)** For URLLC cells and only for Mt. Bryce (ACC100) FEC hardware accelerator. Valid Values: 0 – 11. 0: Do not allocate specific bbdev queues for URLLC Cells. 1-11: Allocate specific number of bbdev queues for URLLC cells. For this to work, dpdkBasebandFecMode must be 2. Both software and hardware must be enabled from dpdk.	0

6.7 PHY Variables - Common

Table 23. PHY Variables - Common

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
TimerModeFreqDomain	Integer	No	**(4G Only)** If set to 1, in timer mode, frequency-domain IQ samples are used for L1 processing during runtime. IFFT and FFT will not be run during runtime to simulate IFFT, and FFT offloaded to FPGA.	0

MemInitThEnable	Single Digit	Yes	**(5G Only)** Enable/disable memory initialization of resource grid scheme. 0: disable, 1: Enable	0
MemInitThInLoad	Integer	Yes	**(5G Only)** Unoccupied RBs threshold to decide if entire resource block grid should be memset vs. only memsetting un-used RB locations. Range: 1 -> 99	70

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7.0 Mlog Variables

Table 24. Mlog Variables

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
MlogSubframes	Integer	No	Several subframes logged into Mlog. Needs to be a power of 2	128
MlogCores	Integer	No	Number of Cores logged into Mlog	10
MlogSize	Integer	No	Size of each subframe (in bytes)	3084

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8.0 CPU Binding to Application Threads

Note: Most of the parameters in this chapter will not work if L1 has been built with the BBU pooling framework. If L1 is built with the BBU pooling framework, use the parameters in Chapter 9.0, BBU Pooling Configuration, instead.

Note: Most thread parameter values have three parts:

- CPU Core # (0 to number of cores on the system)
- Priority (0-99, where higher numbers give higher priority to thread)
- Policy (0 = FIFO scheduling, 1 = Round Robin scheduling)

Table 25. CPU Binding Parameters

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
radioDpdkMaster	Integer	No	DPDK Radio Master Thread. Single-core value. See the note above for format.	2, 99, 0
systemThread	Integer	No	System thread. Single-core value. See the note above for format.	0, 0, 0
timerThread	Integer	No	Timer thread. Single-core value. See the note above for format.	0, 96, 0
FpgaDriverCpuInfo	Integer	No	(**5G only**) FPGA polling thread for FEC on Terasic card. Single-core value. See the note above for format.	3, 96, 0
FrontHaulCpuInfo	Integer	No	(**5G only**) FPGA non-xRAN Front Haul(ifft/fft) polling thread. This thread can be on the same core as the FEC polling core. Single-core value. See the note above for format.	3, 96, 0

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9.0 BBU Pooling Configuration

Table 26. BBU Pooling Configuration Options

Name	Type	Influence on PHY Perf.	Description	Default
BbuPoolSleepEnable	Integer	No	If set to 1, BBU pool cores will return control to kernel tasks when the task is complete. If set to 0, BBU pool cores will always be in userspace, never going to sleep. eBBUPool also uses this indication as same usage of BBU pool.	1
BbuPoolThreadCorePriority	Integer	Yes	The priority of all BBU cores configured below. eBBUPool also uses this indication as same usage of BBU pool.	94
BbuPoolThreadCorePolicy	Integer	Yes	The policy of all BBU cores configured below. [0: SCHED_FIFO (first in first out), 1: SCHED_RR (round robin]. eBBUPool also uses this indication as same usage of BBU pool.	0
BbuPoolThreadDefault_0_63	Integer	Yes	The default number of cores for Task Scheduler. A decimal number will represent the number of cores. Setting for the first 64 cores on the system. When a decimal number is translated to a bitfield, it will show which cores are used. For example, 12 => 0000 1100, this means cores 2 and 3 will be used for Task Scheduler. eBBUPool also uses this indication as same usage of BBU pool. Same rule applies to at most 256 cores.	0xf0
BbuPoolThreadDefault_64_127	Integer	Yes	The default number of cores for Task Scheduler. A decimal number will represent the number of cores. Setting for the second set of 64 cores on the system. When a decimal number is translated to a bitfield, it will show which cores are used. For example, 12 => 0000 1100, this means cores 64+2 and 64+3 will be used for Task Scheduler.	0x0
BbuPoolThreadDefault_128_191	Integer	Yes	The default number of cores for Task Scheduler. A decimal number will represent the number of cores. Setting for the third set of 64 cores on the system. When a decimal number is translated to a bitfield, it will show which cores are used. For example, 12 => 0000 1100, this means cores 128+2 and 128+3 will be used for Task Scheduler.	0x0

Name	Type	Influence on PHY Perf.	Description	Default
BbuPoolThreadDefault_192_255	Integer	Yes	The default number of cores for Task Scheduler. A decimal number will represent the number of cores. Setting for the fourth set of 64 cores on the system. When a decimal number is translated to a bitfield, it will show which cores are used. For example, 12 => 0000 1100, this means cores 192+2 and 192+3 will be used for Task Scheduler.	0x0
BbuPoolThreadSRS_0_63	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_0_63. BBUPool worker thread dedicated to SRS processing in case of Massive MIMO scenarios. eBBUPool also uses this indication as same usage of BBU pool. Same rule applies to at most 256 cores for SRS process.	0x80
BbuPoolThreadSRS_64_127	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_64_127. BBUPool worker thread dedicated to SRS processing in case of Massive MIMO scenarios.	0x0
BbuPoolThreadSRS_128_191	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_128_191. BBUPool worker thread dedicated to SRS processing in case of Massive MIMO scenarios.	0x0
BbuPoolThreadSRS_192_255	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_192_255. BBUPool worker thread dedicated to SRS processing in case of Massive MIMO scenarios.	0x0
BbuPoolThreadDlBeam_0_63	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_0_63. BBUPool worker thread dedicated for Downlink Beamforming processing in case of Massive MIMO scenarios. eBBUPool also uses this indication as same usage of BBU pool. Same rule applies to at most 256 cores for DL beamforming process.	0x40
BbuPoolThreadDlBeam_64_127	Integer	Yes	(**5G only**)	0x0

Name	Type	Influence on PHY Perf.	Description	Default
			Same format as BbuPoolThreadDefault_64_127. BBUPool worker thread dedicated for Downlink Beamforming processing in case of Massive MIMO scenarios.	
BbuPoolThreadDlBeam_128_191	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_128_191. BBUPool worker thread dedicated for Downlink Beamforming processing in case of Massive MIMO scenarios.	0x0
BbuPoolThreadDlBeam_191_255	Integer	Yes	(**5G only**) Same format as BbuPoolThreadDefault_191_255. BBUPool worker thread dedicated for Downlink Beamforming processing in case of Massive MIMO scenarios.	0x0
eBbuPoolNumQueue	Integer	Yes	The number of elements per queue for new eBBUPool task scheduler. Values need to be separated by a comma to indicate each queue.. Supports up a maximum of 10 queues. Valid range: 0 -> 1024	512,512,512,512
eBbuPoolNumContext	Integer	Yes	Number of ping pong context for eBBUPool task scheduler. Used to TDD scenarios to prioritize UL tasks from older slots over current DL tasks in current slot. Range: 1 to 4	1
eBbuPoolMaxContextFetch	Integer	Yes	Maximum number of contexts to fetch by each consumer thread for eBBUPool task scheduler. Parameter only used if eBbuPoolNumContext is greater than 1. Range: 1 to eBbuPoolNumContext	1
eBbuPoolPrintFlag	Integer	Yes	Enable internal print of statistics from eBBUPool task scheduler. 0 => Off, 1 = On	0

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10.0 FPGA Configuration (5G Only)

Table 27. FPGA Configuration Options (Only supported in 5GNR)

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
FrontHaulTimeAdvance	Integer	No	Time Advance added in FPGA from PPS is used to sync with RRU.	9450
nEthPorts	Integer	No	The number of ports used from FPGA. 4 Ports: 462607 (0x70f0F) 2 Ports: 459523 (0x70303)	459523
nPhaseCompFlag	Integer	Yes	Phase compensation enables the flag. 0: Disable Phase Compensation in Front Haul FPGA. 1: Enable Phase Compensation in Front Haul FPGA.	1
nFecFpgaVersionMu3	Hex Integer	Yes	The version number for FPGA tested with this release. FEC Version for mmWave (mu=3).	0xFC060601
nFecFpgaVersionMu0_1	Hex Integer	Yes	Version number for FPGA tested with this release. FEC Version for sub6 (mu=0,1).	0x0816D405
nFhFpgaVersionMu3	Hex Integer	Yes	The version number for FPGA tested with this release. Front Haul Version for mmWave (mu=3).	0x8001000F
nFhFpgaVersionMu0_1	Hex Integer	Yes	The version number for FPGA tested with this release. Front Haul Version for sub6 (mu=0,1).	0x90010008

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11.0 xRAN Configuration

All xRAN configuration parameters have been moved to separate file. Depending on how the L1 shell script is invoked, a specific combination of phycfg.xml and xran.xml will be loaded and parsed. Please refer to Table 3.

Note: Most thread parameter values have three parts:

- CPU Core # (0 to number of cores on the system)
- Priority (0-99, where higher numbers give higher priority to thread)
- Policy (0 = FIFO scheduling, 1 = Round Robin scheduling)

Note: `oRu0PrbElemDlXX`and `oRu0PrbElemUlXX` parameters have eleven fields. For example:

< `oRu0PrbElemDl1`> 0,50,0,14,1,1,0,16,1,0,0<`/oRu0PrbElemDl1`>

- `nRBStart` – First resource block to send in this chunk
- `nRBSize` – Number of resource blocks to send in this chunk
- `nStartSymb` – First symbol to send in this chunk
- `nNumSymb` – Number of symbols to send in this chunk
- `nBeamIndex` – Beam index to send in this chuck
- `bf_weight_update` – Beamforming weight update. 0 = no update, 1 = update
- `compMethod` – Compression method. 0 = no compression, 1 = block floating-point compression.
- `iqWidth` – Number of bits in block floating-point compression.
- `BeamFormingType` – 0=xRAN Beam ID Based, 1=xRAN Beam Weight; 2=xRAN Beam Attribute
- `ScaleFactor` – Scale factor used to scale the input to xRAN.
- `REMask` – Block floating point resource element mask.

Table 28. xRAN Configuration Options (Only supported in 5GNR)

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
`xRANThread`	Integer	Yes	xRAN thread (core where the xRAN polling function is pinned). Thread will include: • Timing source • Polling of hardware (NIC and BBDEV FPGA devices) • Packet generation on DL for C-plane and U-plane • Packet parsing for U-plane • Callbacks to L1 Refphy • Triggering of L1 BBU Tasks	19, 96, 0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
			• TTI events. Single-core value. See the note above for format.	
xRANWorker	Integer	Yes	xRAN worker thread. If xRAN worker thread is created by putting a non-zero value in the core mask, additional cores will be assigned for xRAN. Work load will be split between xRAN worker and xRAN thread. xRAN worker will take over functionality of: • Polling of hardware (NIC and BBDEV FPGA devices) • Pacekt parsing for U-plane • Callbacks to L1 RefPhy • Triggering of L1 BBU Tasks • TTI Events • Part of C-plane generation for Massive MIMO scenario. Hex core mask value. See the note above for format.	0x8000000000, 96, 0
oRuNum	Integer	No	Numbers of O-RU connected to O-DU. All O-RUs are the same capabilities. Max O-RUs is per XRAN_PORTS_NUM i.e. 4. Valid Values: 1, 2, 3, 4	1
oRuEthLinkSpeed	Integer	Yes	10G, 25G, 40G, or 100G speed of Physical connection on O-RU. Valid Values: 10, 25, 40, 100	25
oRuLinesNumber	Integer	Yes	Total number of links per O-RU (Fronthaul Ethernet link in IOT spec). Valid Values: 1 2, 3	1
PciBusAddoRu0Vf0	String	No	PCI Bus address of RU 0 for VF 0	0000:51:01.0
PciBusAddoRu0Vf1	String	No	PCI Bus address of RU 0 for VF 1	0000:51:01.1
PciBusAddoRu0Vf2	String	No	PCI Bus address of RU 0 for VF 2	0000:51:01.2
PciBusAddoRu0Vf3	String	No	PCI Bus address of RU 0 for VF 3	0000:51:01.3
PciBusAddoRu1Vf0	String	No	PCI Bus address of RU 1 for VF 0	0000:51:01.4
PciBusAddoRu1Vf1	String	No	PCI Bus address of RU 1 for VF 1	0000:51:01.5
PciBusAddoRu1Vf2	String	No	PCI Bus address of RU 1 for VF 2	0000:51:01.6

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
PciBusAddoRu1Vf3	String	No	PCI Bus address of RU 1 for VF 3	0000:51:01.7
PciBusAddoRu2Vf0	String	No	PCI Bus address of RU 2 for VF 0	0000:51:02.0
PciBusAddoRu2Vf1	String	No	PCI Bus address of RU 2 for VF 1	0000:51:02.1
PciBusAddoRu2Vf2	String	No	PCI Bus address of RU 2 for VF 2	0000:51:02.2
PciBusAddoRu2Vf3	String	No	PCI Bus address of RU 2 for VF 3	0000:51:02.3
PciBusAddoRu3Vf0	String	No	PCI Bus address of RU 3 for VF 0	0000:00:00.0
PciBusAddoRu3Vf1	String	No	PCI Bus address of RU 3 for VF 1	0000:00:00.0
PciBusAddoRu3Vf2	String	No	PCI Bus address of RU 3 for VF 2	0000:00:00.0
PciBusAddoRu3Vf3	String	No	PCI Bus address of RU 3 for VF 3	0000:00:00.0
oRuRem0Mac0	String	No	MAC Address for Remote O-RU 0 Ethernet Link 0 for VF 0	00:11:22:33:00:01
oRuRem0Mac1	String	No	MAC Address for Remote O-RU 0 Ethernet Link 0 for VF 0	00:11:22:33:00:11
oRuRem0Mac2	String	No	MAC Address for Remote O-RU 0 Ethernet Link 1 for VF 2	00:11:22:33:00:21
oRuRem0Mac3	String	No	MAC Address for Remote O-RU 0 Ethernet Link 1 for VF 3	00:11:22:33:00:31
oRuRem1Mac0	String	No	MAC Address for Remote O-RU 1 Ethernet Link 0 for VF 4	00:11:22:33:01:01
oRuRem1Mac1	String	No	MAC Address for Remote O-RU 1 Ethernet Link 0 for VF 5	00:11:22:33:01:11
oRuRem1Mac2	String	No	MAC Address for Remote O-RU 1 Ethernet Link 1 for VF 6	00:11:22:33:01:21
oRuRem1Mac3	String	No	MAC Address for Remote O-RU 1 Ethernet Link 1 for VF 7	00:11:22:33:01:31
oRuRem2Mac0	String	No	MAC Address for Remote O-RU 2 Ethernet Link 0 for VF 8	00:11:22:33:02:01
oRuRem2Mac1	String	No	MAC Address for Remote O-RU 2 Ethernet Link 0 for VF 9	00:11:22:33:02:11

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
oRuRem2Mac2	String	No	MAC Address for Remote O-RU 2 Ethernet Link 1 for VF 10	00:11:22:33:02:21
oRuRem2Mac3	String	No	MAC Address for Remote O-RU 2 Ethernet Link 1 for VF 11	00:11:22:33:02:31
oRuRem3Mac0	String	No	MAC Address for Remote O-RU 3 Ethernet Link 0 for VF 12	00:11:22:33:03:01
oRuRem3Mac1	String	No	MAC Address for Remote O-RU 3 Ethernet Link 0 for VF 13	00:11:22:33:03:11
oRuRem3Mac2	String	No	MAC Address for Remote O-RU 3 Ethernet Link 1 for VF 14	00:11:22:33:03:21
oRuRem3Mac3	String	No	MAC Address for Remote O-RU 3 Ethernet Link 1 for VF 15	00:11:22:33:03:31
oRu0NumCc	Integer	Yes	Number of cells (CCs) running on O-RU 0. Total number of cells supported by L1 is equal to 12. This means that the total number of cells for all O-RUs must be less than or equal to 12. (oRu0NumCc + oRu1NumCc + oRu2NumCc + oRu3NumCc) <= 12. Valid Values: 0 -> 12	12
oRu0Cc0PhyId -> oRu0Cc11PhyId	Integer	No	PHY Instance IDs running on O-RU 0. If there are 12 component carriers on this O-RU, then all 12 of these fields must be defined. If, for example, there only are 2 CCs for this O-RU, then only oRu0Cc0PhyId and oRu0Cc1PhyId need to be defined.	0->11
Category	Integer	No	xRAN Category of O-RU: 0 – Category A 1 – Category B	1
xranPmdSleep	Integer	Yes	Enable sleep on PMD cores	1
MTU	Integer	No	Maximum Transmission Unit. It will be used for application-layer fragmentation for U-plane packets.	9600
T1a_min_cp_dl	Integer	No	Minimum of the transmission window for the Last C-Plane message in the Downlink Direction (the end of transmission windows for C-Plane DL) for O-DU. Units in micro-seconds	70

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
T1a_max_cp_dl	Integer	No	Maximum of the transmission window for First C-Plane message in the Downlink Direction (the start of transmission windows for C-Plane DL) for O-DU. Units in micro-seconds	140
T1a_min_cp_ul	Integer	No	Minimum of the transmission window for the Last C-Plane message in the Uplink Direction (the end of transmission windows for C-Plane UL) for O-DU. Units in micro-seconds	70
T1a_max_cp_ul	Integer	No	Maximum of the transmission window for First C-Plane message in the Uplink Direction (the start of transmission windows for C-Plane UL) for O-DU. Units in micro-seconds	80
T1a_min_up	Integer	No	Minimum of the transmission window for U-Plane (the end of transmission windows for U-plane DL) for O-DU. Units in micro-seconds	35
T1a_max_up	Integer	No	Maximum of the transmission window for U-Plane (the start of transmission windows for U-plane DL) for O-DU. Units in micro-seconds	35
Ta4_min	Integer	No	Minimum reception window for U-Plane (the start of reception windows for U-plane UL) for O-DU. Units in micro-seconds	0
Ta4_max	Integer	No	Maximum reception window for U-Plane (the end of reception windows for U-plane UL) for O-DU. Units in micro-seconds	45
Tadv_cp_dl	Integer	No	Time in advance that C-plane message must arrive at the O-RU before the corresponding U-plane message for O-RU. Units in micro-seconds.	25
T2a_min_cp_dl	Integer	No	Minimum of the reception window for the Last C-Plane message in the Downlink Direction (the end of transmission windows for C-Plane DL) for O-RU. Units in micro-seconds	285
T2a_max_cp_dl	Integer	No	Maximum of the reception window for First C-Plane message in the Downlink Direction (the start of transmission windows for C-Plane DL) for O-RU. Units in micro-seconds	429

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
T2a_min_cp_ul	Integer	No	Minimum of the reception window for the Last C-Plane message in the Uplink Direction (the end of transmission windows for C-Plane UL) for O-RU. Units in micro-seconds	285
T2a_max_cp_ul	Integer	No	Maximum of the reception window for First C-Plane message in the Uplink Direction (the start of transmission windows for C-Plane UL) for O-RU. Units in micro-seconds	429
T2a_min_up	Integer	No	Minimum of the transmission window for U-Plane (the end of transmission windows for U-plane DL) for O-RU. Units in micro-seconds	71
T2a_max_up	Integer	No	Maximum of the transmission window for U-Plane (the start of transmission windows for U-plane DL) for O-RU. Units in micro-seconds	428
Ta3_min	Integer	No	Minimum reception window for U-Plane (the start of reception windows for U-plane UL) for O-RU. Units in micro-seconds	20
Ta3_max	Integer	No	Maximum reception window for U-Plane (the end of reception windows for U-plane UL) for O-RU. Units in micro-seconds	32
DynamicSectionEna	Single Digit	No	If set to 0, C-Plane for Downlink will have static configuration (full RBs with a single section). If set to 1, C-Plane for Downlink will have multiple sections as configured by L1	0
DynamicSectionEnaUL	Single Digit	No	If set to 0, C-Plane for Uplink will have static configuration (full RBs with a single section). If set to 1, C-Plane for Uplink will have multiple sections as configured by L1	0
xRANSFNWrap	Single Digit	No	When set, SFN will wrap back around when the maximum SFN is reached depending on numerology.	1
xRANNumDLPRBs	Integer	No	Total Number of DL PRBs per symbol (starting from RB 0) that is transmitted (used for testing. If 0, then value is used from PHY_CONFIG_REQ_API)	0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
xRANNumULPRBs	Integer	No	Total Number of UL PRBs per symbol (starting from RB 0) that is received (used for testing. If 0, then value is used from PHY_CONFIG_REQ_API)	0
Gps_Alpha	Integer	No	Alpha value as defined in Section 9.7.2 of ORAN spec, refer to Table 2. Value should be alpha * (1/1.2288ns), range 0 – 1e7 (ns)	0
Gps_Beta	Integer	No	Beta value as defined in Section 9.7.2 of ORAN spec, refer to Table 2. range -32767 – 32767	0
xranCompMethod	Integer	No	xRAN compression mode on O-DU <-> O-RU. 0 – no compression 1 – Block Floating point compression	0
xraniqWidth	Integer	No	IQ width when DynamicSectionEna and BFP Compression enabled.	16
xranModCompEna	Single Digit	No	Modulation Compression mode is enabled or not. (for DL only) 0 – Disabled 1 - Enabled	0
oRu0nPrbElemDl	Integer	Yes	Several different RB chunks are used as specified in C-plane in the Downlink direction. 0 – send all resource blocks as one section and 1 chunk. 1 -> 8: send resource blocks as specified by following oRu0PrbElemDlXX.	2
oRu0PrbElemDl0	Integer	Yes	Configuration for the 1st RB chunk to be sent in Downlink Direction. See the note above for format.	0,50,0,14,1,1,0,16,1,0,0
oRu0PrbElemDl1	Integer	Yes	Configuration for the 2nd RB chunk to be sent in Downlink Direction. See the note above for format.	50,25,0,14,1,1,0,16,1,0,0
oRu0PrbElemDl2	Integer	Yes	Configuration for the 3rd RB chunk to be sent in Downlink Direction. See the note above for format.	72,36,0,14,3,1,1,9,1,0,0
oRu0PrbElemDl3	Integer	Yes	Configuration for the 4th RB chunk to be sent in Downlink Direction. See the note above for format.	144,48,0,14,4,1,1,9,1,0,0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
oRu0PrbElemDl4	Integer	Yes	Configuration for the 5th RB chunk to be sent in Downlink Direction. See the note above for format.	144,36,0,14,5,1,1,9,1,0,0
oRu0PrbElemDl5	Integer	Yes	Configuration for the 6th RB chunk to be sent in Downlink Direction. See the note above for format.	180,36,0,14,6,1,1,9,1,0,0
oRu0PrbElemDl6	Integer	Yes	Configuration for the 7th RB chunk to be sent in Downlink Direction. See the note above for format.	216,36,0,14,7,1,1,9,1,0,0
oRu0PrbElemDl7	Integer	Yes	Configuration for 8th RB chunk to be sent in Downlink Direction. See the note above for format.	252,21,0,14,8,1,1,9,1,0,0
oRu0nPrbElemUl	Integer	Yes	Several different RB chunks are used as specified in C-plane in the Uplink direction. 0 – send all resource blocks as one section and 1 chunk. 1 -> 8: send resource blocks as specified by following oRu0PrbElemUlXX.	2
oRu0PrbElemUl0	Integer	Yes	Configuration for the 1st RB chunk to be sent in Uplink Direction. See the note above for format.	0,50,0,14,1,1,0,16,1,0,0
oRu0PrbElemUl1	Integer	Yes	Configuration for the 2nd RB chunk to be sent in Uplink Direction. See the note above for format.	50,25,0,14,1,1,0,16,1,0,0
oRu0PrbElemUl2	Integer	Yes	Configuration for the 3rd RB chunk to be sent in Uplink Direction. See the note above for format.	72,36,0,14,3,1,1,9,1,0,0
oRu0PrbElemUl3	Integer	Yes	Configuration for the 4th RB chunk to be sent in Uplink Direction. See the note above for format.	144,48,0,14,4,1,1,9,1,0,0
oRu0PrbElemUl4	Integer	Yes	Configuration for the 5th RB chunk to be sent in Uplink Direction. See the note above for format.	144,36,0,14,5,1,1,9,1,0,0
oRu0PrbElemUl5	Integer	Yes	Configuration for the 6th RB chunk to be sent in Uplink Direction. See the note above for format.	180,36,0,14,6,1,1,9,1,0,0

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
oRu0PrbElemUl6	Integer	Yes	Configuration for the 7th RB chunk to be sent in Uplink Direction. See the note above for format.	216,36,0,14,7,1,1,9,1,0,0
oRu0PrbElemUl7	Integer	Yes	Configuration for the 8th RB chunk to be sent in Uplink Direction. See the note above for format.	252,21,0,14,8,1,1,9,1,0,0

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12.0 Stream Stats Options

Table 29. Stream Stats Options

Name	Type	Influence on PHY Perf.	Description	Default (phycfg.xml)
StreamStats	Integer	No	(**5G only**) If set to 1, L1 statistics are streamed over UDP to the destination address and port specified.	0
StreamIp	String	No	The destination IP address to stream the L1 statistics	127.0.0.1
StreamPort	Integer	No	IP Port used to create UDP socket	2000

§

13.0 Typical File Content

This is the default `phycfg_xran.xml` file included in the FlexRAN 21.03 release.

```
<?xml version="1.0"?>
<!--
-->
<!--   <COPYRIGHT_TAG>
-->
<!--
-->
<PhyConfig>
    <version>21.03</version>

    <Api>
        <!--  Maximum number of successive missing API allowed before triggering PHY
stop (-1 is infinite) -->
        <successiveNoApi>15</successiveNoApi>
        <!--  Full path to wls device used for transport of MAC-PHY API (e.g. wls0 )--
>
        <wls_dev_name>wls0</wls_dev_name>
        <!-- MAC managed WLS Memory size. This is used for all API buffer allocations
-->
        <wlsMacMemorySize>0x3EA80000</wlsMacMemorySize>
        <!-- L1 managed WLS Memory size. This is used for SRS weight storage. For
64x64 usecase and 6 cells (with 512 users per cell) use 0x18000000 -->
        <wlsPhyMemorySize>0x18000000</wlsPhyMemorySize>
    </Api>

    <PhyLogs>
        <IqLogs>
            <dlIqLog>0</dlIqLog>
            <ulIqLog>0</ulIqLog>
            <!--  Write IQ Logs to File. This is a bit field where each bit has
following interpretation. If bit is 1, then file is written -->
            <!--  Bit 0: DlIfftIn.bin -->
            <!--  Bit 1: UlFftOut.bin -->
            <!--  Bit 16: DlIfftIn.txt -->
            <!--  Bit 17: UlFftOut.txt -->
            <iqLogDumpToFile>0</iqLogDumpToFile>
        </IqLogs>
        <DebugLogs>
            <phyMlog>1</phyMlog>
            <phyStats>1</phyStats>
        </DebugLogs>
    </PhyLogs>

    <!-- This section defines all DPDK related parameters used for DPDK initialization
-->
    <DPDK>
        <!--  name of DPDK memory zone, needs to align between primary and secondary
process -->
        <dpdkFilePrefix>gnb0</dpdkFilePrefix>
        <!--  DPDK memory size allocated from hugepages [MB]  [default: 2048] -->
        <dpdkMemorySize>20480</dpdkMemorySize>
```

```
        <!--  DPDK IOVA Mode used for DPDK initialization. If 0, then PA mode. Else VA
Mode -->
        <dpdkIovaMode>0</dpdkIovaMode>
        <!--  DPDK FEC BBDEV to use             [0 - SW, 1 - HW accelerator, 2 - Both]
-->
        <dpdkBasebandFecMode>1</dpdkBasebandFecMode>
        <!--  DPDK BBDev name added to the passlist. The argument format is
<[domain:]bus:devid.func> -->
        <dpdkBasebandDevice>0000:92:00.0</dpdkBasebandDevice>
        <!-- This section is used to init DPDK shared ports and memory with secondary
process  -->
        <DPDKSharedResource>
            <!-- number of the set of shared ports and corresponding memory, maximum
4, if none, set to 0 -->
            <numSharedResource>0</numSharedResource>

            <!--  Shared Resource Config 0 -->
            <SharedResource0>
                <!-- DPDK memory pool name, if don't want to init memory pool, set
name to 0 -->
                <mempoolName0>fast_pkt</mempoolName0>
                <!-- The number of elements in the mempool. The optimum size for a
mempool is when n is a power of two minus one: n = (2^q - 1) -->
                <numElement0>65535</numElement0>
                <!-- The size of each element -->
                <elementSize0>2048</elementSize0>
                <!-- The size of the private data appended after the mempool
structure-->
                <privateDataSize0>64</privateDataSize0>
                <!-- DPDK ring pool name, if don't want to init ring, set name to 0 --
>
                <ringName0>0</ringName0>
                <!-- The size of the ring (must be a power of 2) -->
                <ringSize0>1024</ringSize0>
                <!-- DPDK port pci-e address, if don't want to init port, set number
to 0 -->
                <portAddr0>0000:af:00.0</portAddr0>
                <!-- DPDK port socket index -->
                <portSocketIdx0>1</portSocketIdx0>
                <!-- Number of Tx queue -->
                <txQueueNum0>1</txQueueNum0>
                <!-- Tx queue description -->
                <txQueueDesc0>512</txQueueDesc0>
                <!-- Number of Rx queue -->
                <rxQueueNum0>1</rxQueueNum0>
                <!-- Rx queue description -->
                <rxQueueDesc0>128</rxQueueDesc0>
                <!-- Max payload size, if larger than 1500Bytes, Jumbo frame will be
enabled -->
                <maxPayloadSize0>9728</maxPayloadSize0>
            </SharedResource0>

            <!--  Shared Resource Config 1 -->
            <SharedResource1>
                <!-- DPDK memory pool name, if don't want to init memory pool, set
name to 0 -->
                <mempoolName1>header_pkt</mempoolName1>
```

```
                <!-- The number of elements in the mempool. The optimum size for a
mempool is when n is a power of two minus one: n = (2^q - 1) -->
                <numElement1>65535</numElement1>
                <!-- The size of each element -->
                <elementSize1>2048</elementSize1>
                <!-- The size of the private data appended after the mempool
structure-->
                <privateDataSize1>64</privateDataSize1>
                <!-- DPDK ring pool name, if don't want to init ring, set name to 0 --
>
                <ringName1>0</ringName1>
                <!-- The size of the ring (must be a power of 2) -->
                <ringSize1>1024</ringSize1>
                <!-- DPDK port pci-e address, if don't want to init port, set number
to 0 -->
                <portAddr1>0000:af:00.1</portAddr1>
                <!-- DPDK port socket index -->
                <portSocketIdx1>1</portSocketIdx1>
                <!-- Number of Tx queue -->
                <txQueueNum1>2</txQueueNum1>
                <!-- Tx queue description -->
                <txQueueDesc1>512</txQueueDesc1>
                <!-- Number of Rx queue -->
                <rxQueueNum1>1</rxQueueNum1>
                <!-- Rx queue description -->
                <rxQueueDesc1>128</rxQueueDesc1>
                <!-- Max payload size, if larger than 1500Bytes, Jumbo frame will be
enabled -->
                <maxPayloadSize1>9728</maxPayloadSize1>
            </SharedResource1>

            <!--  Shared Resource Config 2 -->
            <SharedResource2>
                <!-- DPDK memory pool name, if don't want to init memory pool, set
name to 0 -->
                <mempoolName2>clone_pkt</mempoolName2>
                <!-- The number of elements in the mempool. The optimum size for a
mempool is when n is a power of two minus one: n = (2^q - 1) -->
                <numElement2>65535</numElement2>
                <!-- The size of each element -->
                <elementSize2>2048</elementSize2>
                <!-- The size of the private data appended after the mempool
structure-->
                <privateDataSize2>64</privateDataSize2>
                <!-- DPDK ring pool name, if don't want to init ring, set name to 0 --
>
                <ringName2>0</ringName2>
                <!-- The size of the ring (must be a power of 2) -->
                <ringSize2>1024</ringSize2>
                <!-- DPDK port pci-e address, if don't want to init port, set number
to 0 -->
                <portAddr2>0</portAddr2>
                <!-- DPDK port socket index -->
                <portSocketIdx2>0</portSocketIdx2>
                <!-- Number of Tx queue -->
                <txQueueNum2>1</txQueueNum2>
                <!-- Tx queue description -->
                <txQueueDesc2>512</txQueueDesc2>
```

```
                <!-- Number of Rx queue -->
                <rxQueueNum2>1</rxQueueNum2>
                <!-- Rx queue description -->
                <rxQueueDesc2>128</rxQueueDesc2>
                <!-- Max payload size, if larger than 1500Bytes, Jumbo frame will be
enabled -->
                <maxPayloadSize2>9728</maxPayloadSize2>
            </SharedResource2>

            <!--  Shared Resource Config 3 -->
            <SharedResource3>
                <!-- DPDK memory pool name, if don't want to init memory pool, set
name to 0 -->
                <mempoolName3>pdu3</mempoolName3>
                <!-- The number of elements in the mempool. The optimum size for a
mempool is when n is a power of two minus one: n = (2^q - 1) -->
                <numElement3>65535</numElement3>
                <!-- The size of each element -->
                <elementSize3>2048</elementSize3>
                <!-- The size of the private data appended after the mempool
structure-->
                <privateDataSize3>64</privateDataSize3>
                <!-- DPDK ring pool name, if don't want to init ring, set name to 0 --
>
                <ringName3>sdu3</ringName3>
                <!-- The size of the ring (must be a power of 2) -->
                <ringSize3>1024</ringSize3>
                <!-- DPDK port pci-e address, if don't want to init port, set number
to 0 -->
                <portAddr3>0</portAddr3>
                <!-- DPDK port socket index -->
                <portSocketIdx3>0</portSocketIdx3>
                <!-- Number of Tx queue -->
                <txQueueNum3>1</txQueueNum3>
                <!-- Tx queue description -->
                <txQueueDesc3>512</txQueueDesc3>
                <!-- Number of Rx queue -->
                <rxQueueNum3>1</rxQueueNum3>
                <!-- Rx queue description -->
                <rxQueueDesc3>128</rxQueueDesc3>
                <!-- Max payload size, if larger than 1500Bytes, Jumbo frame will be
enabled -->
                <maxPayloadSize3>9728</maxPayloadSize3>
              </SharedResource3>
        </DPDKSharedResource>
    </DPDK>

    <!-- This section is used with FerryBridge FPGA and 5GNR code -->
    <Radio>
        <!-- Enable/disable radio              [0 - disable (external app control
radio), 1 - use Ferry Bridge, 4 - use xRAN -->
        <radioEnable>4</radioEnable>
        <!--  Ferry Bridge (FB) mode           [0 - LTE MODE, 1 - CPRI BYPASS MODE] -
->
        <ferryBridgeMode>1</ferryBridgeMode>
        <!--  Number of Ethernet ports on FB    [0 - DPDK port 0, 1 - DPDK port 1, 2 -
both DPDK port 0 and port 1 (CA mode with two ETH)] -->
        <ferryBridgeEthPort>1</ferryBridgeEthPort>
```

```
        <!--  FB Synchronized CPRI ports        [0 - no reSync REC & RE FPGA, 1 -
reSync REC & REC FPGA] -->
        <ferryBridgeSyncPorts>0</ferryBridgeSyncPorts>
        <!--  FB Loopback Mode                  [0 - no optical loopback connected
REC<->RE, 1 - optical loopback connected REC<->RE] -->
        <ferryBridgeOptCableLoopback>0</ferryBridgeOptCableLoopback>

        <!--  Radio Config 0 -->
        <RadioConfig0>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg0PCIeEthDev>0000:19:00.0</radioCfg0PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg0DpdkRx>1</radioCfg0DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg0DpdkTx>2</radioCfg0DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg0TxAnt>2</radioCfg0TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg0RxAnt>2</radioCfg0RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg0RxAgc>0</radioCfg0RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg0RxAntVertical>1</radioCfg0RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg0RxAntHorizontal>1</radioCfg0RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg0RxAntPolarization>1</radioCfg0RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells, 3 -
Cells , 4 - Cells ] -->
            <radioCfg0NumCell>1</radioCfg0NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg0Cell0PhyId>0</radioCfg0Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port   [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg0Cell1PhyId>1</radioCfg0Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg0Cell2PhyId>2</radioCfg0Cell2PhyId>
            <!-- Forth Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg0Cell3PhyId>3</radioCfg0Cell3PhyId>
            <!--  Fifth Phy instance ID mapped to this port       [0-7 - valid range
of PHY instance for third cell ] -->
            <radioCfg0Cell4PhyId>4</radioCfg0Cell4PhyId>
            <!--  Sixth Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg0Cell5PhyId>5</radioCfg0Cell5PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg0riuMac>11:22:33:44:55:66</radioCfg0riuMac>
            </ROE>
        </RadioConfig0>

        <!--  Radio Config 1 -->
```

```
        <RadioConfig1>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg1PCIeEthDev>0000:03:00.1</radioCfg1PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg1DpdkRx>1</radioCfg1DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg1DpdkTx>1</radioCfg1DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg1TxAnt>4</radioCfg1TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg1RxAnt>4</radioCfg1RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg1RxAgc>0</radioCfg1RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg1RxAntVertical>1</radioCfg1RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg1RxAntHorizontal>1</radioCfg1RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg1RxAntPolarization>1</radioCfg1RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg1NumCell>1</radioCfg1NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg1Cell0PhyId>2</radioCfg1Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg1Cell1PhyId>3</radioCfg1Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg1Cell2PhyId>2</radioCfg1Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg1Cell3PhyId>3</radioCfg1Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg1riuMac>ac:1f:6b:2c:9f:07</radioCfg1riuMac>
            </ROE>
        </RadioConfig1>

        <!--  Radio Config 2 -->
        <RadioConfig2>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg2PCIeEthDev>0000:05:00.0</radioCfg2PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg2DpdkRx>10</radioCfg2DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg2DpdkTx>11</radioCfg2DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg2TxAnt>4</radioCfg2TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg2RxAnt>4</radioCfg2RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg2RxAgc>0</radioCfg2RxAgc>
```

```
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg2RxAntVertical>1</radioCfg2RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg2RxAntHorizontal>1</radioCfg2RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg2RxAntPolarization>1</radioCfg2RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg2NumCell>2</radioCfg2NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg2Cell0PhyId>4</radioCfg2Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg2Cell1PhyId>5</radioCfg2Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg2Cell2PhyId>2</radioCfg2Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg2Cell3PhyId>3</radioCfg2Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg2riuMac>ac:1f:6b:2c:9f:07</radioCfg2riuMac>
            </ROE>
        </RadioConfig2>

        <!--  Radio Config 3 -->
        <RadioConfig3>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg3PCIeEthDev>0000:05:00.1</radioCfg3PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg3DpdkRx>12</radioCfg3DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg3DpdkTx>13</radioCfg3DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg3TxAnt>4</radioCfg3TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg3RxAnt>4</radioCfg3RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg3RxAgc>0</radioCfg3RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg3RxAntVertical>1</radioCfg3RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg3RxAntHorizontal>1</radioCfg3RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg3RxAntPolarization>1</radioCfg3RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg3NumCell>2</radioCfg3NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg3Cell0PhyId>6</radioCfg3Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg3Cell1PhyId>7</radioCfg3Cell1PhyId>
```

```
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg3Cell2PhyId>2</radioCfg3Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg3Cell3PhyId>3</radioCfg3Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg3riuMac>ac:1f:6b:2c:9f:07</radioCfg3riuMac>
            </ROE>
        </RadioConfig3>

        <!--  Radio Config 4 -->
        <RadioConfig4>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg4PCIeEthDev>0000:00:08.0</radioCfg4PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg4DpdkRx>14</radioCfg4DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg4DpdkTx>15</radioCfg4DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg4TxAnt>4</radioCfg4TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg4RxAnt>4</radioCfg4RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg4RxAgc>0</radioCfg4RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg4RxAntVertical>1</radioCfg4RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg4RxAntHorizontal>1</radioCfg4RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg4RxAntPolarization>1</radioCfg4RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg4NumCell>2</radioCfg4NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg4Cell0PhyId>8</radioCfg4Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg4Cell1PhyId>9</radioCfg4Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg4Cell2PhyId>2</radioCfg4Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg4Cell3PhyId>3</radioCfg4Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg4riuMac>ac:1f:6b:2c:9f:07</radioCfg4riuMac>
            </ROE>
        </RadioConfig4>

        <!--  Radio Config 5 -->
        <RadioConfig5>
```

```
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg5PCIeEthDev>0000:08:00.0</radioCfg5PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg5DpdkRx>16</radioCfg5DpdkRx>
            <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg5DpdkTx>16</radioCfg5DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg5TxAnt>4</radioCfg5TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg5RxAnt>4</radioCfg5RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg5RxAgc>0</radioCfg5RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg5RxAntVertical>1</radioCfg5RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg5RxAntHorizontal>1</radioCfg5RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg5RxAntPolarization>1</radioCfg5RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg5NumCell>2</radioCfg5NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg5Cell0PhyId>10</radioCfg5Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg5Cell1PhyId>11</radioCfg5Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg5Cell2PhyId>2</radioCfg5Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg5Cell3PhyId>3</radioCfg5Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg5riuMac>ac:1f:6b:2c:9f:07</radioCfg5riuMac>
            </ROE>
        </RadioConfig5>

        <!--  Radio Config 6 -->
        <RadioConfig6>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg6PCIeEthDev>0000:00:05.0</radioCfg6PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg6DpdkRx>16</radioCfg6DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg6DpdkTx>16</radioCfg6DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg6TxAnt>4</radioCfg6TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg6RxAnt>4</radioCfg6RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg1RxAgc>0</radioCfg1RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
```

```
            <radioCfg6RxAntVertical>1</radioCfg6RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg6RxAntHorizontal>1</radioCfg6RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg6RxAntPolarization>1</radioCfg6RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg6NumCell>2</radioCfg6NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg6Cell0PhyId>12</radioCfg6Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg6Cell1PhyId>13</radioCfg6Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
            <radioCfg6Cell2PhyId>2</radioCfg6Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg6Cell3PhyId>3</radioCfg6Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg6riuMac>ac:1f:6b:2c:9f:07</radioCfg6riuMac>
            </ROE>
        </RadioConfig6>

        <!--  Radio Config 7 -->
        <RadioConfig7>
            <!-- DPDK: Add a PCI device in white list The argument format is
<[domain:]bus:devid.func> -->
            <radioCfg7PCIeEthDev>0000:00:06.0</radioCfg7PCIeEthDev>
            <!-- DPDK: RX Thread core id [0-max core] -->
            <radioCfg7DpdkRx>16</radioCfg7DpdkRx>
             <!-- DPDK: TX Thread core id [0-max core] -->
            <radioCfg7DpdkTx>16</radioCfg7DpdkTx>
            <!--  Number of Tx Antenna         [1, 2, 4] -->
            <radioCfg7TxAnt>4</radioCfg7TxAnt>
            <!--  Number of Rx Antenna         [1, 2, 4] -->
            <radioCfg7RxAnt>4</radioCfg7RxAnt>
            <!--  Rx AGC configuration         [0 - Rx AGC disabled, 1 - Rx AGC
enabled (default for fpga release 1.3.1)] -->
            <radioCfg7RxAgc>0</radioCfg7RxAgc>
            <!--  Number of Rx Antenna Vertiacl elements    [4, 8, 64] -->
            <radioCfg7RxAntVertical>1</radioCfg7RxAntVertical>
            <!--  Number of Rx Antenna Horizontal elements  [4, 8, 64] -->
            <radioCfg7RxAntHorizontal>1</radioCfg7RxAntHorizontal>
            <!--  Number of Rx Antenna Polarization Setting [1, 2] -->
            <radioCfg7RxAntPolarization>1</radioCfg7RxAntPolarization>
            <!--  Number of cells running on this port   [1 - Cell , 2 - Cells ] -->
            <radioCfg7NumCell>2</radioCfg7NumCell>
            <!-- First Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for first cell ] -->
            <radioCfg7Cell0PhyId>14</radioCfg7Cell0PhyId>
            <!-- Second Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for second cell ] -->
            <radioCfg7Cell1PhyId>15</radioCfg7Cell1PhyId>
            <!-- Third Phy instance ID mapped to this port    [0-7 - valid range of
PHY instance for third cell ] -->
```

```
            <radioCfg7Cell2PhyId>2</radioCfg7Cell2PhyId>
            <!-- Forth Fourth instance ID mapped to this port    [0-7 - valid range of
PHY instance for fourth cell ] -->
            <radioCfg7Cell3PhyId>3</radioCfg7Cell3PhyId>
            <!--  Radio Over Ethernet IEEE 1914.3 -->
            <ROE>
                <!-- ROE: Mac address of RIU -->
                <radioCfg7riuMac>ac:1f:6b:2c:9f:07</radioCfg7riuMac>
            </ROE>
        </RadioConfig7>

        <!-- Select Radio Config Option (from above) for Port 0 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort0>0</radioPort0>

        <!-- Select Radio Config Option (from above) for Port 1 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort1>1</radioPort1>

        <!-- Select Radio Config Option (from above) for Port 2 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort2>2</radioPort2>

        <!-- Select Radio Config Option (from above) for Port 3 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort3>3</radioPort3>

        <!-- Select Radio Config Option (from above) for Port 4 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort4>4</radioPort4>

        <!-- Select Radio Config Option (from above) for Port 5 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort5>5</radioPort5>

        <!-- Select Radio Config Option (from above) for Port 6 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort6>6</radioPort6>

        <!-- Select Radio Config Option (from above) for Port 7 [0: RadioConfig0, 1:
RadioConfig1 ... 7: RadioConfig7] -->
        <radioPort7>7</radioPort7>
    </Radio>

    <PhyVars>
        <!-- The below variables can be modified in file here and it will take effect
when PHY is brought up after reboot of system -->
        <Pdsch>
            <!-- Split PDSCH symbol processing -->
            <PdschSymbolSplit>0</PdschSymbolSplit>

            <!-- Enable the PDSCH symbol process to OFDM symbol based split, otherwise
UE group/UE based split. 0 disable, 1 enable -->
            <PdschOfdmSplitEnable>0</PdschOfdmSplitEnable>

            <!-- Split PDSCH DL beamforiming weight generation processing -->
            <PdschDlWeightSplit>0</PdschDlWeightSplit>
```

```
            <!-- Max number of parallel tasks that the DL FEC Encoder is split into.
Number needs to be between 1 and 4. If wrong value entered, it will be defaulted to 1.
-->
            <!-- For hardware offload (using fpga / eAsic) it will be defaulted to 1.
-->
            <FecEncSplit>4</FecEncSplit>
        </Pdsch>
        <Pusch>
            <!-- Split processing for Channel Estimation for PUSCH -->
            <PuschChanEstSplit>0</PuschChanEstSplit>

            <!-- Split processing for MMSE for PUSCH -->
            <PuschMmseSplit>0</PuschMmseSplit>

            <!-- Split processing for LLR Rx for PUSCH -->
            <PuschLlrRxSplit>0</PuschLlrRxSplit>

            <!-- Split PUSCH UL beamforiming weight generation processing -->
            <PuschUlWeightSplit>0</PuschUlWeightSplit>

            <!-- Software FEC Decoder Early Termination disabled. If 1, then
programmed number of iterations are run from MAC PHY API regardless of CRC PASS -->
            <FecDecEarlyTermDisable>0</FecDecEarlyTermDisable>

            <!-- FEC LDPC Decoder Number of iterations. If 0 then Number of iterations
is set to 10. Else this value is used -->
            <FecDecNumIter>12</FecDecNumIter>

            <!-- Max number of parallel tasks that the UL FEC Decoder is split into.
Number needs to be between 1 and 4. If wrong value entered, it will be defaulted to 1.
-->
            <!-- For hardware offload (using fpga / eAsic) it will be defaulted to 1.
-->
            <FecDecSplit>4</FecDecSplit>

            <!-- Only for terasic. Number of decimal digits of LLR fixed point output.
If 0 then this value is set to 2, which means LLR is 8S2. Else this value is used -->
            <llrOutDecimalDigit>2</llrOutDecimalDigit>

            <!-- SNR Threshold for IRC. If -100, then IRC will be disabled -->
            <IrcEnableThreshold>-100</IrcEnableThreshold>

            <!-- PUSCH Noise Scaling -->
            <!-- Used to scale measured noise to account for ChanEst errors for mu=0
and 2 layers. -->
            <!-- Valid values = 1, 2, 3, 4 -->
            <PuschNoiseScale>2</PuschNoiseScale>

            <!-- frequency interpolation method for PUSCH CE -->
            <!-- bit 0: 0: 1RB sinc interpolation 1: 4RB sinc interpolation -->
            <!-- bit 1: 0: disable pre - interpolation 1: enable pre - interpolation -
->
            <CEInterpMethod>0</CEInterpMethod>

            <!-- frequency offset compensation -->
            <!-- 0: disable, 1: enable -->
            <CEFocEnable>0</CEFocEnable>
```

```
            <!-- frequency offset compensation granularity in terms of RE-->
            <CEFocGranularity>768</CEFocGranularity>

            <!-- time domain linear interpolation for PUSCH enable = 1, disable = 0-->
            <PuschLinearInterpEnable>0</PuschLinearInterpEnable>

            <!-- time domain linear interpolation granularity for PUSCH cell0, cell1
and cell2 respectively -->
            <!-- 0 - Linear, 1 - Linear2 ... 4 - Linear6, 99 - nearest -->
            <!-- use comma to separte the values if want to apply differnt granularity
for differnt UE groups -->
            <PuschLinearInterpGranularity0>99</PuschLinearInterpGranularity0>
            <PuschLinearInterpGranularity1>0,1,2,3,4</PuschLinearInterpGranularity1>
            <PuschLinearInterpGranularity2>0,1,2,3,4</PuschLinearInterpGranularity2>
            <PuschLinearInterpGranularity3>0,1,2,3,4</PuschLinearInterpGranularity3>

            <!-- beamforming weight matrix gen algo choose-->
            <!-- 0: ZF based weight gen algo, 1: dftcodebook based weight gen algo-->
            <DFTBfWeightGenEnable>0</DFTBfWeightGenEnable>

            <!-- beamforming weight matrix gen RB pick granularity-->
            <BfWeightGenGranularity>2</BfWeightGenGranularity>
        </Pusch>
        <Pucch>
            <!-- Split processing for PUCCH -->
            <PucchSplit>0</PucchSplit>
        </Pucch>
        <Srs>
            <!-- Split processing for SRS CE -->
            <SrsCeSplit>0</SrsCeSplit>
        </Srs>
        <Prach>
            <!-- Prach Detection Threshold. If non zero, computed value is used. -->
            <prachDetectThreshold>0</prachDetectThreshold>
            <!-- prach detect fo check -->
            <!-- 0: disable, 1: enable -->
            <prachDetectFoCheck>0</prachDetectFoCheck>
        </Prach>

        <Urllc>
            <!-- For URLLC cells, setting this field to 1 will split the FEC
processing by 2 (half in software and half in hardware). Default: 0 Disabled -->
            <UrllcPuschFecSplit>0</UrllcPuschFecSplit>

            <!-- If there are URLLC Cells, this field indicates how many BBDEV Queue
Ids to allocate for URLLC. All others are for eMBB. Default: 0 Disabled -->
            <!-- The lower the queue ID, the higher the priority to process these -->
            <UrllcBbdevIdEnd>0</UrllcBbdevIdEnd>
        </Urllc>
    </PhyVars>

    <MlogVars>
        <!-- Number of subframes are logged into Mlog. Needs to be a power of 2 -->
        <MlogSubframes>128</MlogSubframes>
        <!-- Number of Cores being logged into Mlog -->
        <MlogCores>40</MlogCores>
        <!-- Size of each subframe (in bytes) -->
        <MlogSize>10000</MlogSize>
```

```
    </MlogVars>

    <!-- CPU Binding to Application Threads -->
    <Threads>
        <!-- System Threads (Single core id value): Core, priority, Policy [0:
SCHED_FIFO 1: SCHED_RR] -->
        <systemThread>2, 0, 0</systemThread>

        <!-- Timer Thread (Single core id value): Core, priority, Policy [0:
SCHED_FIFO 1: SCHED_RR] -->
        <timerThread>0, 96, 0</timerThread>

        <!-- FPGA for LDPC Thread (Single core id value): Core, priority, Policy [0:
SCHED_FIFO 1: SCHED_RR] -->
        <FpgaDriverCpuInfo>3, 96, 0</FpgaDriverCpuInfo>

        <!-- FPGA for Front Haul (FFT / IFFT) Thread (Single core id value): Core,
priority, Policy [0: SCHED_FIFO 1: SCHED_RR] -->
        <!-- This thread should be created for timer mode and hence can be same core
as LDPC polling core -->
        <FrontHaulCpuInfo>3, 96, 0</FrontHaulCpuInfo>

        <!-- DPDK Radio Master Thread (Single core id value): Core, priority, Policy
[0: SCHED_FIFO 1: SCHED_RR] -->
        <radioDpdkMaster>2, 99, 0</radioDpdkMaster>
    </Threads>

    <BbuPoolConfig>
        <!-- If set to 1, BBU Pool cores, return control to kernel after task is
completed. Else it will always be in user space without going to sleep -->
        <!-- It is mainly used when setting core to harware sleep mode and latency of
sleep is not very deterministic -->
        <BbuPoolSleepEnable>1</BbuPoolSleepEnable>

        <!-- Priority Of All BBU Cores -->
        <BbuPoolThreadCorePriority>94</BbuPoolThreadCorePriority>
        <!-- Policy for All BBU Cores [0: SCHED_FIFO 1: SCHED_RR] -->
        <BbuPoolThreadCorePolicy>0</BbuPoolThreadCorePolicy>

        <!-- BBUPool Worker Thread Cores (Bit mask of all cores that are used for BBU
Pool in Decimal or Hex [needs to start with "0x"]) -->
        <BbuPoolThreadDefault_0_63>0xF0</BbuPoolThreadDefault_0_63>
        <BbuPoolThreadDefault_64_127>0x0</BbuPoolThreadDefault_64_127>
        <BbuPoolThreadDefault_128_191>0x0</BbuPoolThreadDefault_128_191>
        <BbuPoolThreadDefault_192_255>0x0</BbuPoolThreadDefault_192_255>

        <!-- BBUPool Worker Thread Cores dedicated for SRS processing in case of
Massive MIMO Configs. Mask needs to be a subset of BbuPoolThreadDefault_0_63 or
BbuPoolThreadDefault_64_127 -->
        <!-- (Bit mask of all cores that are used for BBU Pool in Decimal or Hex
[needs to start with "0x"]) -->
        <BbuPoolThreadSrs_0_63>0x0</BbuPoolThreadSrs_0_63>
        <BbuPoolThreadSrs_64_127>0x0</BbuPoolThreadSrs_64_127>
        <BbuPoolThreadSrs_128_191>0x0</BbuPoolThreadSrs_128_191>
        <BbuPoolThreadSrs_192_255>0x0</BbuPoolThreadSrs_192_255>
```

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        <!-- BBUPool Worker Thread Cores dedicated for DL beam  processing in case of
Massive MIMO Configs. Mask needs to be a subset of BbuPoolThreadDefault_0_63 or
BbuPoolThreadDefault_64_127 -->
        <!-- (Bit mask of all cores that are used for BBU Pool in Decimal or Hex
[needs to start with "0x"]) -->
        <BbuPoolThreadDlbeam_0_63>0x0</BbuPoolThreadDlbeam_0_63>
        <BbuPoolThreadDlbeam_64_127>0x0</BbuPoolThreadDlbeam_64_127>
        <BbuPoolThreadDlbeam_128_191>0x0</BbuPoolThreadDlbeam_128_191>
        <BbuPoolThreadDlbeam_192_255>0x0</BbuPoolThreadDlbeam_192_255>

        <!-- URLLC Processing Thread (Bit mask of all cores that are used in Decimal
or Hex [needs to start with "0x"]) -->
        <BbuPoolThreadUrllc>0x100</BbuPoolThreadUrllc>
    </BbuPoolConfig>

    <Fpga>
        <!-- Time advance added in FPGA from PPS. This is to sync with RRU -->
        <FrontHaulTimeAdvance>7450</FrontHaulTimeAdvance>

        <!-- Number of ports used from FPGA. 4Ports: 462607 (0x70F0F) 2Ports: 459523
(0x70303) -->
        <nEthPorts>462607</nEthPorts>
        <!-- phase compensation enable flag 0:disablle 1:enable -->
        <nPhaseCompFlag>0</nPhaseCompFlag>

        <!-- Version Numbers on FPGA tested with each release -->
        <!-- FEC Version for mmWave -->
        <nFecFpgaVersionMu3>0x20010900</nFecFpgaVersionMu3>

        <!-- FEC Version for sub3 and sub6 -->
        <nFecFpgaVersionMu0_1>0x0423D420</nFecFpgaVersionMu0_1>

        <!-- Front Haul Version for mmWave -->
        <nFhFpgaVersionMu3>0x8001000F</nFhFpgaVersionMu3>

        <!-- Front Haul Version for sub3 and sub6 -->
        <nFhFpgaVersionMu0_1>0x90010008</nFhFpgaVersionMu0_1>
    </Fpga>

    <StreamStats>
        <!-- If this is set to 1, L1 statistics are streamed over UDP to the
desitnation address and port -->
        <StreamStats>0</StreamStats>

        <!-- Destination IP Address to stream the stats -->
        <StreamIp>127.0.0.1</StreamIp>

        <!-- IP Port used to create UDP socket -->
        <StreamPort>2000</StreamPort>
    </StreamStats>

</PhyConfig>
```

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