EXIMIUS
Excellence Everyday

SHIP IP User Guide

Channel Alignment IP

Revision: 0.1

26 August 2021

Table of Contents

Table of Figures

Table of Tables

Revision History

Revision	Date	Author	Summary of Changes
0.1	8/26/21	Art Arizpe	Initial draft

Table 1 Revision History

1. Overview

The Channel Alignment module interfaces to a Protocol Adapter IP and to one or multiple AIB PHYs.

Its function, in multi-channel configurations, is to remove the channel-to-channel skew in the received AIB data. This is required because transport through the AIB can introduce skew between AIB channels.

Each AIB channel has a strobe bit, used to align all the channels. The strobe bit is normally zero and pulses high for one clock cycle. The receiving side uses RX Alignment FIFOs to align the strobe bits and the associated data bits.

1.1 TX Path Operations

The module can generate the alignment strobes at the same selectable bit location for each channel. The strobe bit generation can be enable or disabled. If it is disabled, it is up to the application to generate the alignment strobes. The number of clock cycles between strobes, or the strobe interval, is selectable.

1.2 RX Path Operations

The module removes the channel-to-channel skew in the AIB data. The module supports performing the alignment once, at the start of operation or performing it all the time. The module provides status output to indicate alignment done and alignment error detected. It also provides RX Alignment FIFOs full, partially full, empty, and partially empty flags, with selectable thresholds.

An example of the module's usage in a a basic chiplet system follows. The system consists of lead and follower chiplets. There are 24 channel AIB subsytems connecting 3 dies in this diagram. The Channel Alignment module can be used in any of the chiplets as shown. The AIB subsytems may have different frequencies and data path widths. The module will operate in all these cases. Although the module is targeted at AIB 2.0 operation, it will also work with AIB 1.0, AIB-O, and other general applications.

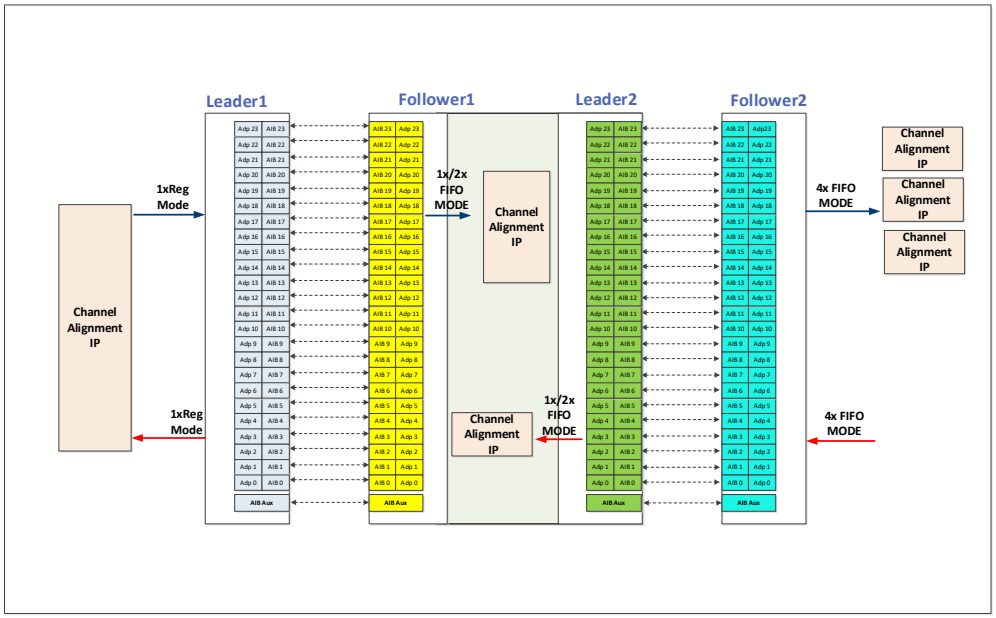

Figure 1 Channel Alignment IP in AIB Chiplet System

2. Features

2.1 Channel Alignment

- The module supports aligning from 2 to 24 channels. For AIB 1.0 and AIB 2.0, each channel can have 40 to 320 data bits. For AIB-O, each channel can have as few as 20 data bits.
- The Channel Alignment strobe bit location is selectable.
- The number of clock cycles between strobe bits, or the strobe bit interval, is selectable.
- Each channel contains an RX Alignment FIFO.
- The RX Alignment FIFO depth is configurable. All channels have the same FIFO depth. The RX Alignment FIFO provides full, partially full, empty, and partially empty flags.
- After channel alignment is locked, the module can continue operating without inspecting the strobe bits again or it can continuously monitor the strobe bits.

2.2 Online Synchronization

The tx_online and rx_online signals can be driven from system level signals allowing for an automated Online Synchronization SM to perform the sequencing of the various online bits in the system. This also automates recovery of non-persistent Strobes and some markers, allowing them to be recovered to be used as data. It also allows for the receive logic to differentiate post-calibrated data from pre-calibration garbage from the PHY.

2.3 Errors

- Alignment error
- Strobe bit position error
- Strobe bit encoding error

3. Block Diagram

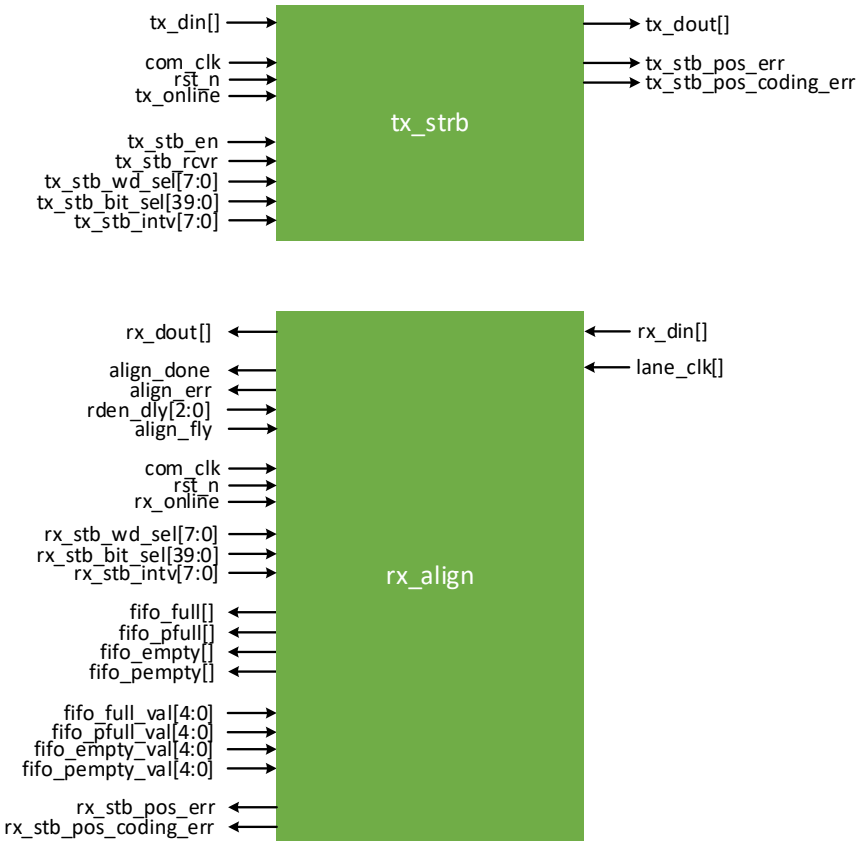

Figure 2 Channel Alignment Block Diagram

The module contains two sub-blocks, txp_strb, for TX strobe generation and rx_align for RX channel alignment.

3.1 tx_strb

The tx_strb block generates the TX channel alignment strobes at the selected bit location and interval. The target latency through tx_strb is one clock cycle.

3.2 rx_align

The rx_align uses the channel alignment strobe bits to remove the channel-to-channel skew.

The following conditions cause align_err to assert.

- Alignment is not detected before the RX Alignment FIFOs overflow
- A strobe is not detected where specified by rx_stb_intv
    - If align_fly is asserted and alignment has completed

The latency through the rx_align depends on the worst skew of a single channel.

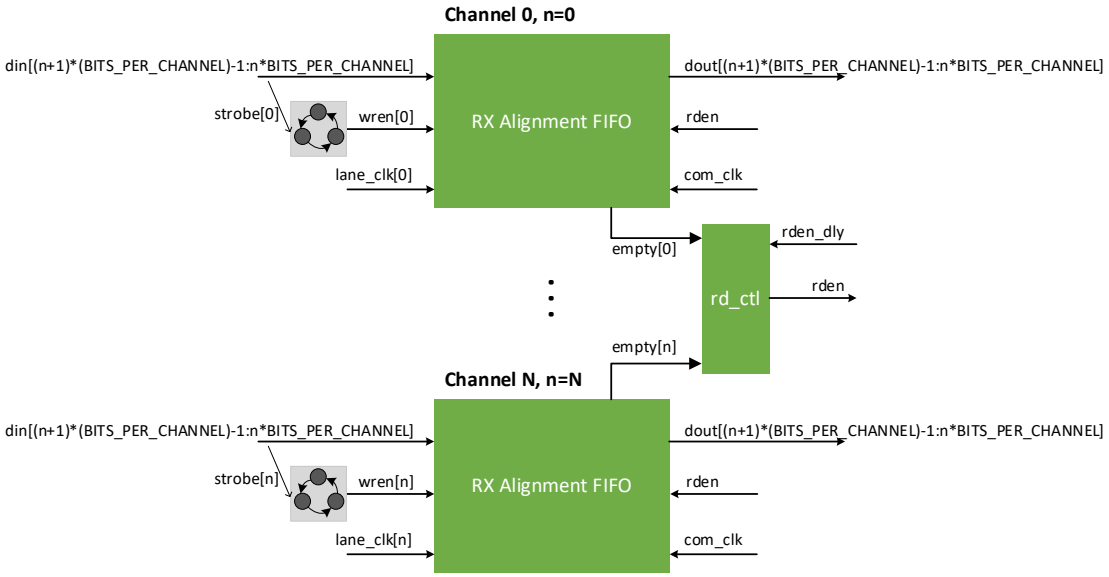

Figure 3 RX Alignment FIFO

The module uses FIFOs to implement the alignment function. There is an RX Alignment FIFO for each channel.

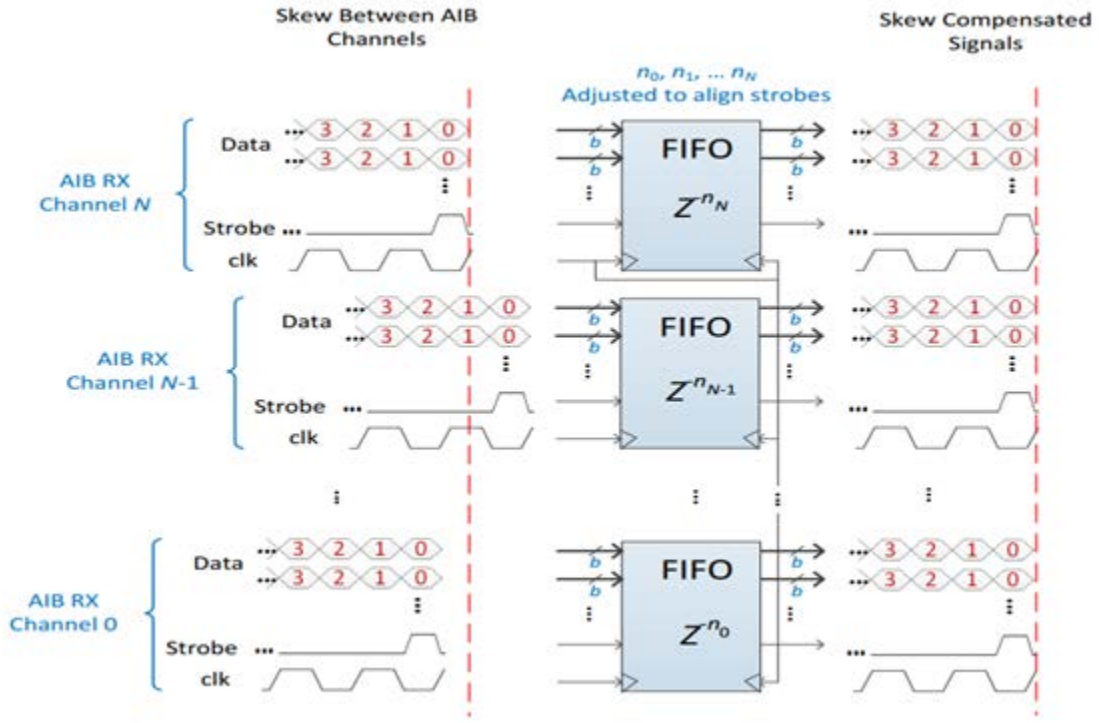

Figure 4 FIFO-based alignment

The RX Alignment FIFO operation is:

- On the TX side, a strobe bit with the correct interval is written to all channels simultaneously. The strobe bit is normally 1'b0 and pulses to 1'b1 for one cycle.
- When the RX side logic detects the first strobe bit, the channel's data, including the strobe bit, is written to the RX Alignment FIFO. Subsequent words are written to the RX Alignment FIFO.
- When all channel's RX Alignment FIFOs are not empty, the read logic will start reading the RX Alignment FIFOs. This guarantees the words read from all the RX Alignment FIFOs are aligned.
- Status bits are provided to indicate when alignment is done or when an alignment error is detected.

The strobe bit position is selectable for both TX and RX. The rden signal can be delayed with respect to all the RX Alignment FIFOs not being empty by the rden_dly input port.

3.3 AIB 2.0 and 1.0 Data Rate Modes

The module supports operating in the Full, Half, and Quarter data rate modes of AIB 2.0 and also in AIB 1.0 data rate. The following table and figure show examples.

Mode	**Data Width**	**FMax**
Full Rate AIB 2.0	80	2 GHz
Half Rate AIB 2.0	160	1 GHz
Quarter Rate AIB 2.0	320	500 MHz
Full Rate AIB 1.0	40	1 GHz
Half Rate AIB 1.0	80	500 MHz

Table 2 Supported Data Rates

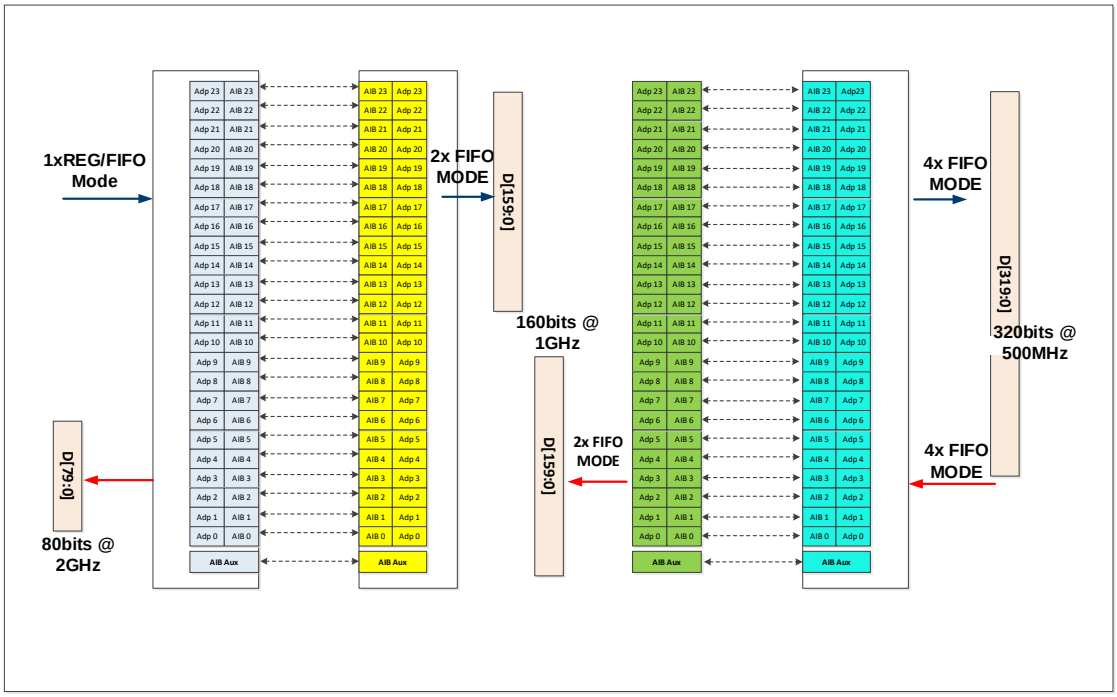

Figure 5 Data Rates and Widths

3.4 Channel Alignment Strobe Generation

The module supports selectable alignment strobe bit position. It is important to be aware that the strobe bit position needs to be considered as a system specification instead of one only for a single instance of the module.

The selection is straightforward for symmetric data width operation, but not for asymmetric data widths. The alignment strobe bit location interacts with the gearbox marker bit as shown in the following examples.

3.4.1 2:1 Data Rate Conversion

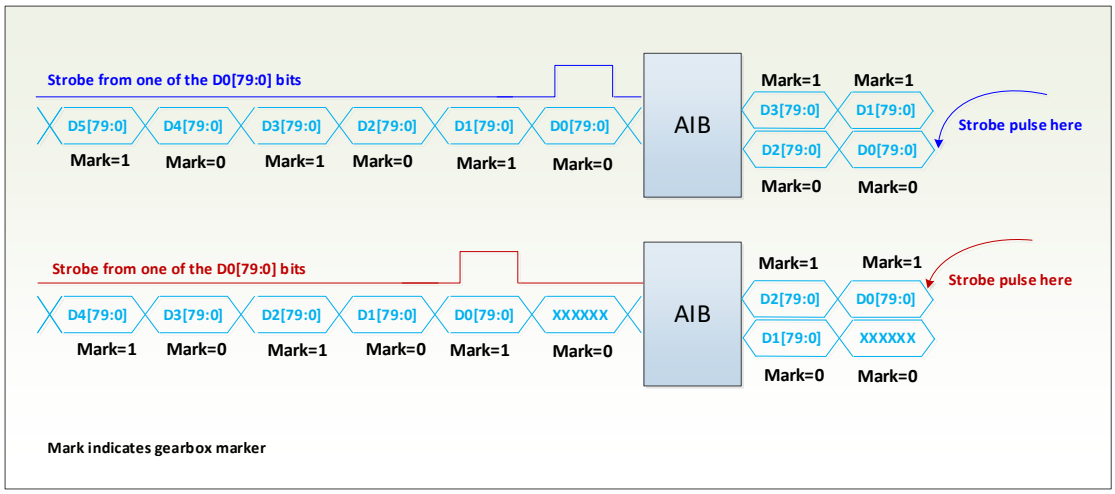

Figure 6 2:1 Data Rate conversion

In this example, the left side is an ASIC leader chiplet operating at 2 GHZ, and the right side is an FPGA follower operating at 1 GHz, half rate.

The alignment strobe bit is selected to be one of the 80 data bits, bit 0, for example. There are two positions on the RX side where the alignment strobe might be detected. It could be bit 0 or bit 80, depending on it's position in an odd or even word, since the RX side data width is 160 bits. Both sides must select the appropriate alignment strobe bit position for correct operation.

In general, the alignment strobe bit position should be defined by the widest side. In this case, it must be modulo 80 because the TX side data width is narrower, 80 bits, than the RX side 160 bits.

3.4.2 4:2 and 2:4 Data Rate Conversion

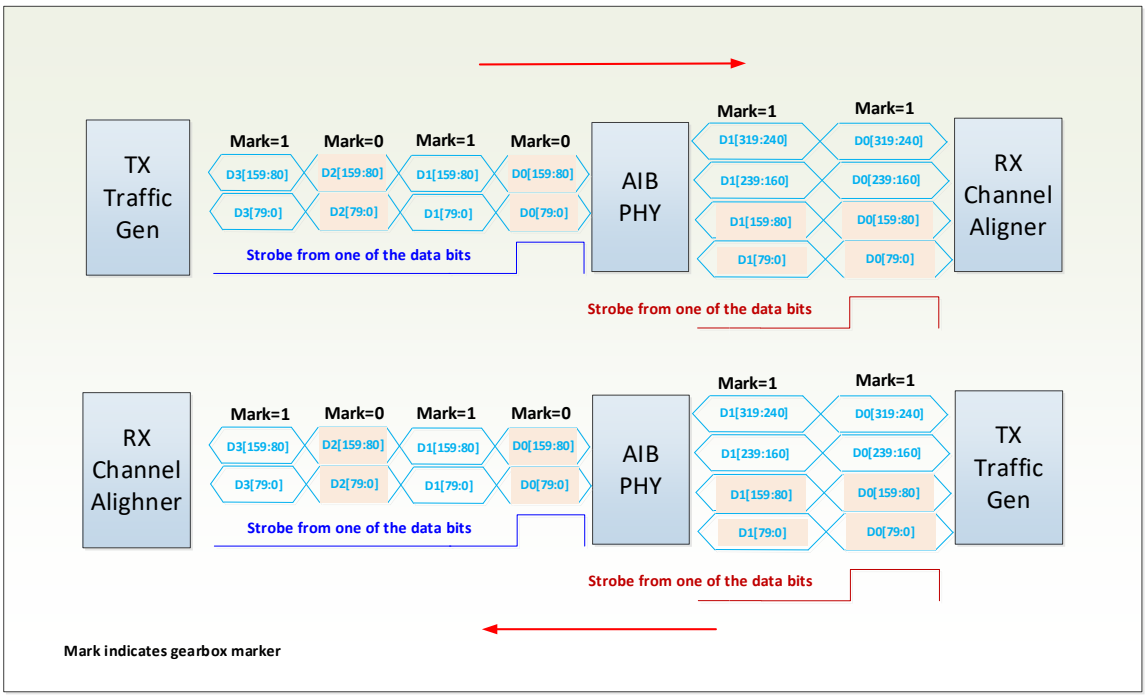

Figure 7 4:2 and 2:4 Data Rate Conversion

In this example, the left side is operating at half rate, 1 GHz, 160 bits data width. The right side is operating at quarter rate, 500 MHz, 320 bits data width.

The channel alignment strobe must be in the lower 160 bits since that is the width of the narrower, left side.

3.5 Selectable alignment strobe bit position

The alignment strobe bit position is defined by the input ports, tx_stb_wd_sel[7:0], tx_stb_bit_sel[39:0], and rx_stb_wd_sel[7:0], rx_stb_bit_sel[39:0].

The *_wd_sel inputs are one-hot encoded and control which 40 bit word of the maximum 320 data bits where the strobe will be located. The *_bit_sel inputs are one-hot encoded and control where the strobe bit is located in the selected word.

For example if tx_stb_wd_sel[7:0] = 8'h02 and tx_stb_bit_sel[39:0] = 40'h00008 select bit 43 for the strobe position.

3.6 Selectable alignment strobe interval

The strobe interval is defined by the input ports tx_stb_intv[7:0] and rx_stb_intv[7:0] and controls the number of clock cycles between alignment strobes.

The strobe interval must also be considered across the entire data path between chiplets. For the widest data width, the interval should be long enough to prevent aliasing.

3.7 Online Synchronization

The online synchronization logic usese key signals from the PHY (namely the *_rx_transfer_en) and connects them to several timers. These timers are configured to ensure remote side events have occurred, namely Word Marker Recovery by the PHY and Channel Alignment.

The counters are configured using input ports called timer_x and timer_xz that specify:

- X = Delay after *_rx_transfer_en until Word Marking is guaranteed to be synchronized.
- Z = Modest delay to ensure receive is ready before transmit occurs.

3.7.1 TX Online

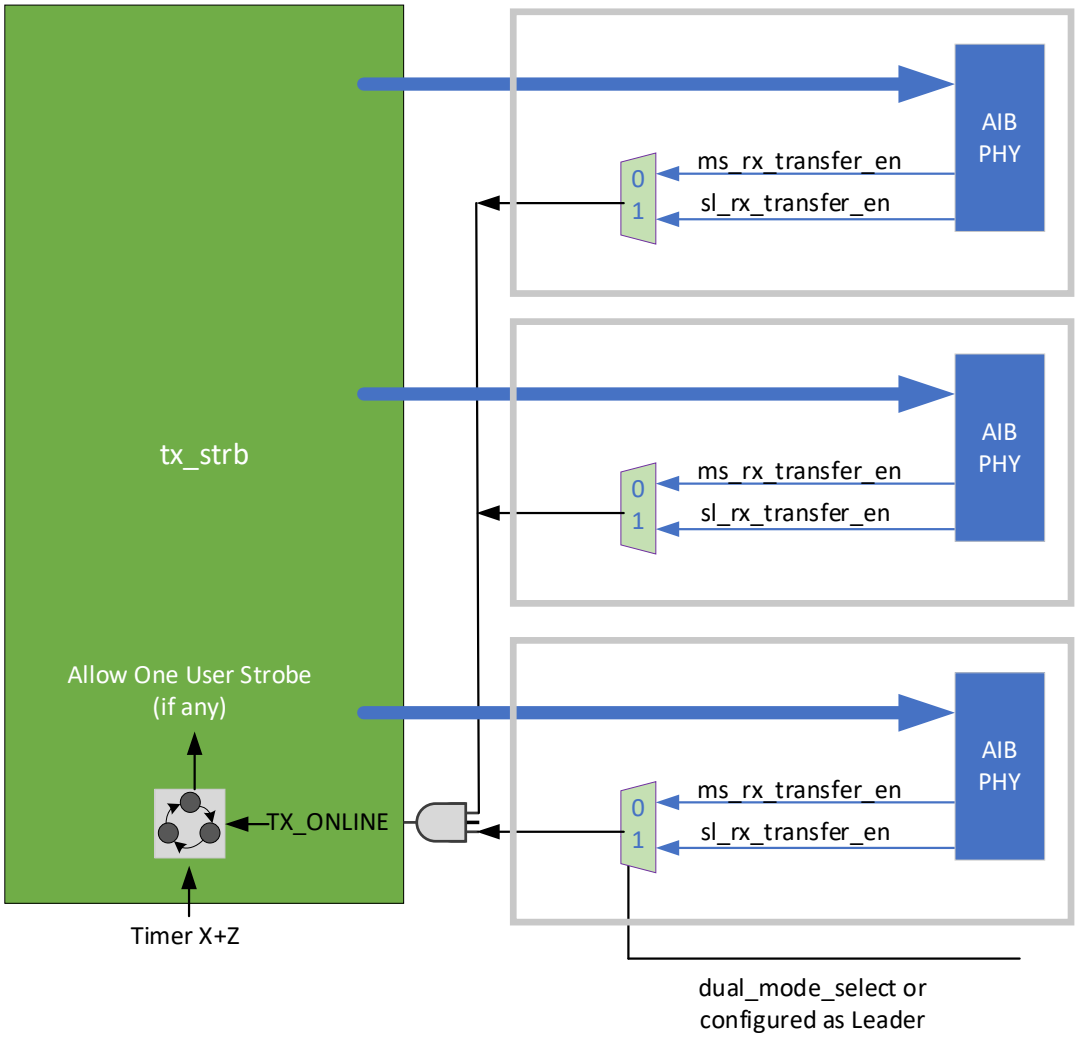

Figure 8 TX ONLINE

3.7.2 RX Online

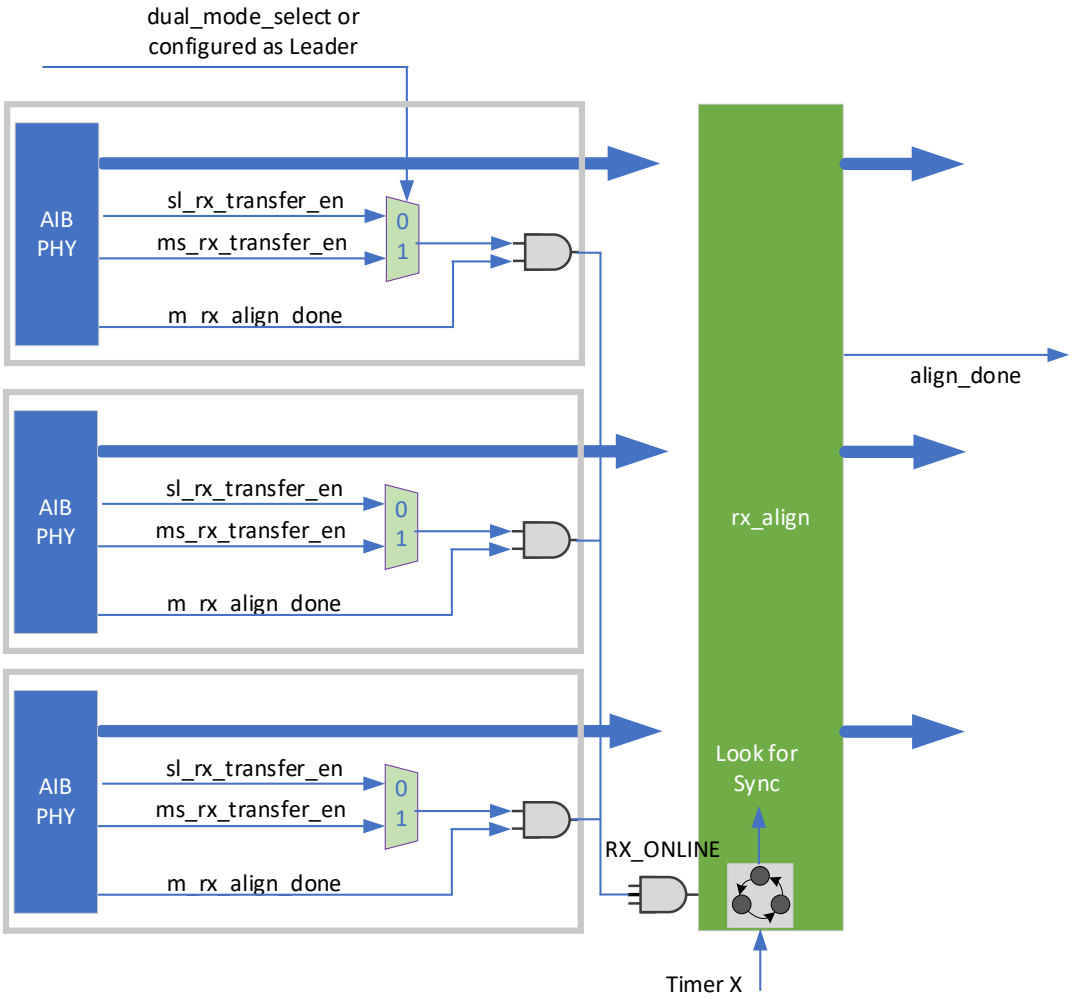

Figure 9 RX ONLINE

4. Clocks and Resets

Please refer to **Table 5 Parameters** for a definition of the parameters.

Input Port	Direction	Width	Description
Data Path			
lane_clk	in	NUM_CHANNELS	Clock per channel. The clocks have the same frequency but possibly different phases. This is the same as each PHY's m_rd_clk in an AIB PHY application. Please refer to the SYNC_FIFO parameter.

com_clk	in	1	Common clock. This is the same as the protocol adapter's m_wr_clk in an AIB PHY application. Please refer to the SYNC_FIFO parameter.
rst_n	in	1	Asynchronous reset, active low. This needs to be synchronized into each clock domain.

Table 3 Clocks and Resets

5. Interfaces

Please refer to **Table 5 Parameters** for a definition of the parameters.

I/O Port	Direction	Width	Description
Data Path			
tx_din	in	NUM_CHANNELS * BITS_PER_CHANNEL	Protocol Adapter data in
tx_dout	out	NUM_CHANNELS * BITS_PER_CHANNEL	Data out to PHY with generated strobes
rx_din	in	NUM_CHANNELS * BITS_PER_CHANNEL	Unaligned channel data in
rx_dout	out	NUM_CHANNELS * BITS_PER_CHANNEL	Aligned channel data out to Protocol Adapter
Status			
align_done	out	1	Channels are aligned when 1'b1
align_err	out	1	Alignment error detected when 1'b1
tx_stb_pos_err	out	1	The decoded TX strobe bit position is not within the data width.
rx_stb_pos_err	out	1	The decoded RX strobe bit position is not within the data width.
tx_stb_pos_coding_err	out	1	The tx_stb_wd_sel or tx_stb_bit_sel input ports are not one-hot encoded.
rx_stb_pos_coding_err	out	1	The rx_stb_wd_sel or rx_stb_bit_sel input ports are not one-hot encoded.
fifo_full	out	NUM_CHANNELS	FIFO full status per channel
fifo_pfull	out	NUM_CHANNELS	FIFO partial full status per channel

fifo_empty	out	NUM_CHANNELS	FIFO empty status per channel
fifo_pempty	out	NUM_CHANNELS	FIFO partial empty status per channel
Control Interface			
tx_online	in	1	When 1'b1, the module is online and can perform strobe generation and channel alignment. When 1'b0, the module is idle.
rx_online	in	1	When 1'b1, the module is online and can perform RX channel alignment. When 1'b0, the module is idle.
tx_stb_en	in	1	When 1'b1, the module will generate the strobes at the selected position and with the selected interval. When 1'b0, the module will not alter the strobe bits under the assumption that has already been done by the application.
tx_stb_rcvr	in	1	Recoverable strobes. When 1'b1, the module will generate a one-time strobe at the selected position. When 1'b0, the module will generate strobes at the selected position and with the selected interval.
align_fly	in	1	When 1'b1, the module will dynamically align the channels. When 1'b0, alignment only happens once at the beginning
tx_stb_wd_sel	in	8	TX path. The same value is used for all channels. Selects which 40-bit word of the maximum 320 data bits has the strobe bit. This is one-hot encoded. 1b'1 means the strobe bit is located in tx_din[39:0]. This value is used in combination with tx_stb_bit_sel to determine the actual strobe bit position.
tx_stb_bit_sel	in	40	TX path. The same value is used for all channels. Selects which bit of the word selected by tx_stb_wd_sel is the strobe bit. This is one-hot encoded.

tx_stb_intv	in	8	Tx path. The same value is used for all channels. Strobe interval cycle count.
rx_stb_wd_sel	in	8	RX path. The same value is used for all channels. Selects which 40-bit word of the maximum 320 data bits has the strobe bit. This is one-hot encoded. 1b'1 means the strobe bit is located in rx_din[39:0]. This value is used in combination with rx_stb_bit_sel to determine the actual strobe bit position.
rx_stb_bit_sel	in	40	RX path. The same value is used for all channels. Selects which bit of the word selected by rx_stb_wd_sel is the strobe bit. This is one-hot encoded.
rx_stb_intv	in	8	RX path. The same value is used for all channels. Strobe interval cycle count.
fifo_full_val	in	5	FIFO full value
fifo_pfull_val	in	5	FIFO partial full value
fifo_empty_val	in	3	FIFO empty value
fifo_pfempty_val	in	3	FIFO partial empty value
rden_dly	in	3	FIFO read enable delay cycle to write enable.
count_x	in	8	Delay after *_rx_transfer_en until Word Marking is guaranteed to be synchronized.
count_xz	in	8	Delay after *_rx_transfer_en until Word Marking is guaranteed to be synchronized plus a modest delay to ensure receive is ready before transmit occurs.

Table 4 I/O Ports

Control signals are pseudo-static and must be stable before reset deassertion. They cannot change during normal operation. They can change when reset is asserted.

6. Initialization

6.1 Initialization bring-up sequence

1. The module is held in reset by asserting rst_n

2. Drive appropriate values to control inputs like stb_wd_sel, stb_bit_sel and others. tx_online and rx_online are deasserted.
3. AIB channels go through calibration
4. AIB channels come up. The TX strobes need to stay zero
5. Bring module online by asserting tx_online and rx_online
6. The module starts generating TX strobes
7. The module checks for alignment done or reports alignment error

7. Configuration

7.1 Compile Time Parameters

Parameter	Description
NUM_CHANNELS	Number of channels to align
BITS_PER_CHANNEL	Number of bits per channel. Values range from 40 to 320.
AD_WIDTH	FIFO depth
SYNC_FIFO	When set to 1, the module operates with no synchronization between com_clk and the lane_clks. The com_clk and the lane_clks must all be driven from the same source. When set to 0, the module synchronizes the multiple lane_clks to the com_clk.

Table 5 Parameters

7.2 Configuration and Status

All of the configuration and status is handled through I/O ports. Please refer to **Interfaces** for a description.

8. References

AIB specification: https://github.com/intel/aib-phy-hardware/blob/master/docs/AIB_Intel_Specification%201_2%20.pdf

Channel Adapter HAS 0.3