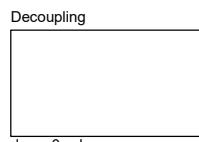
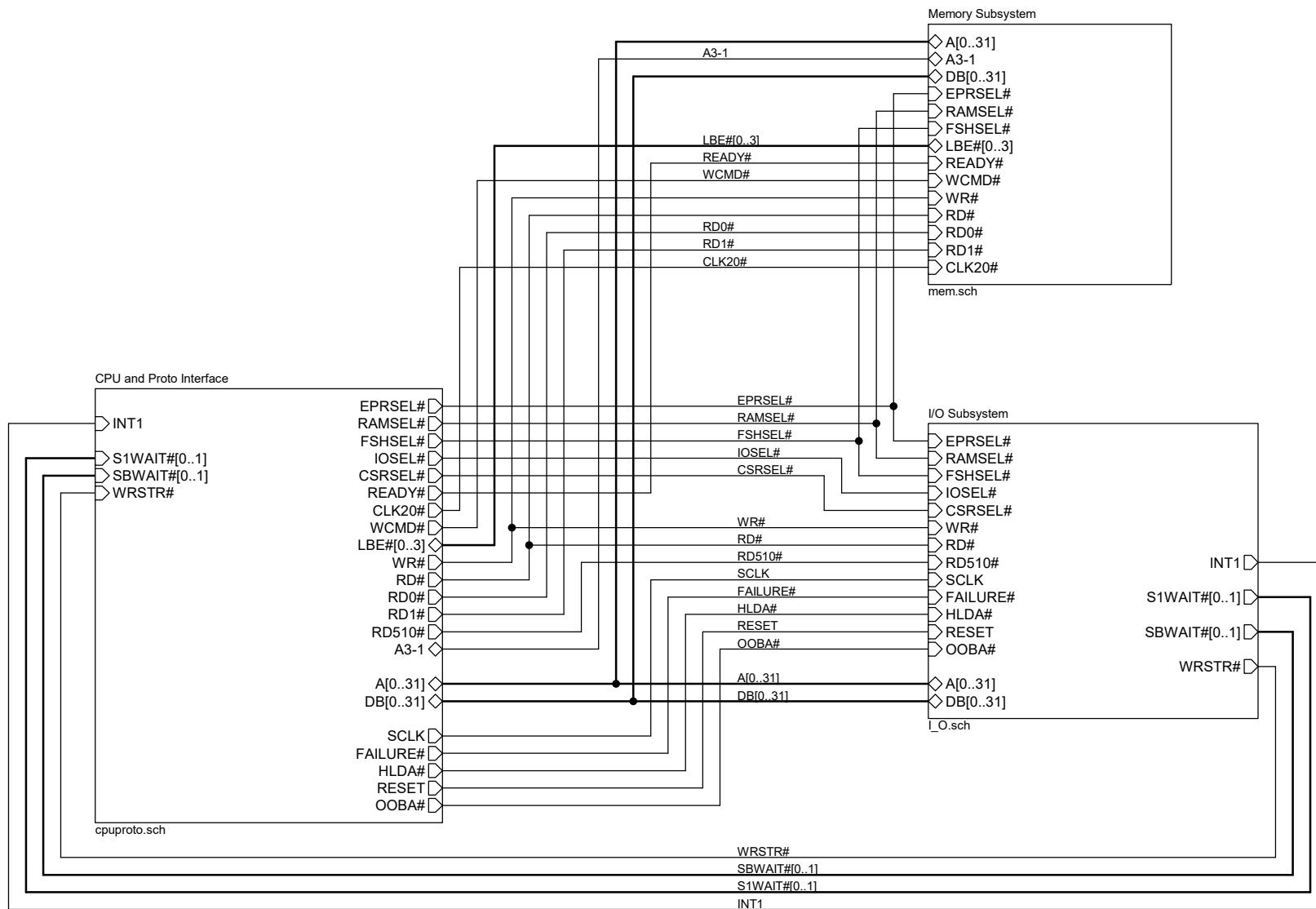
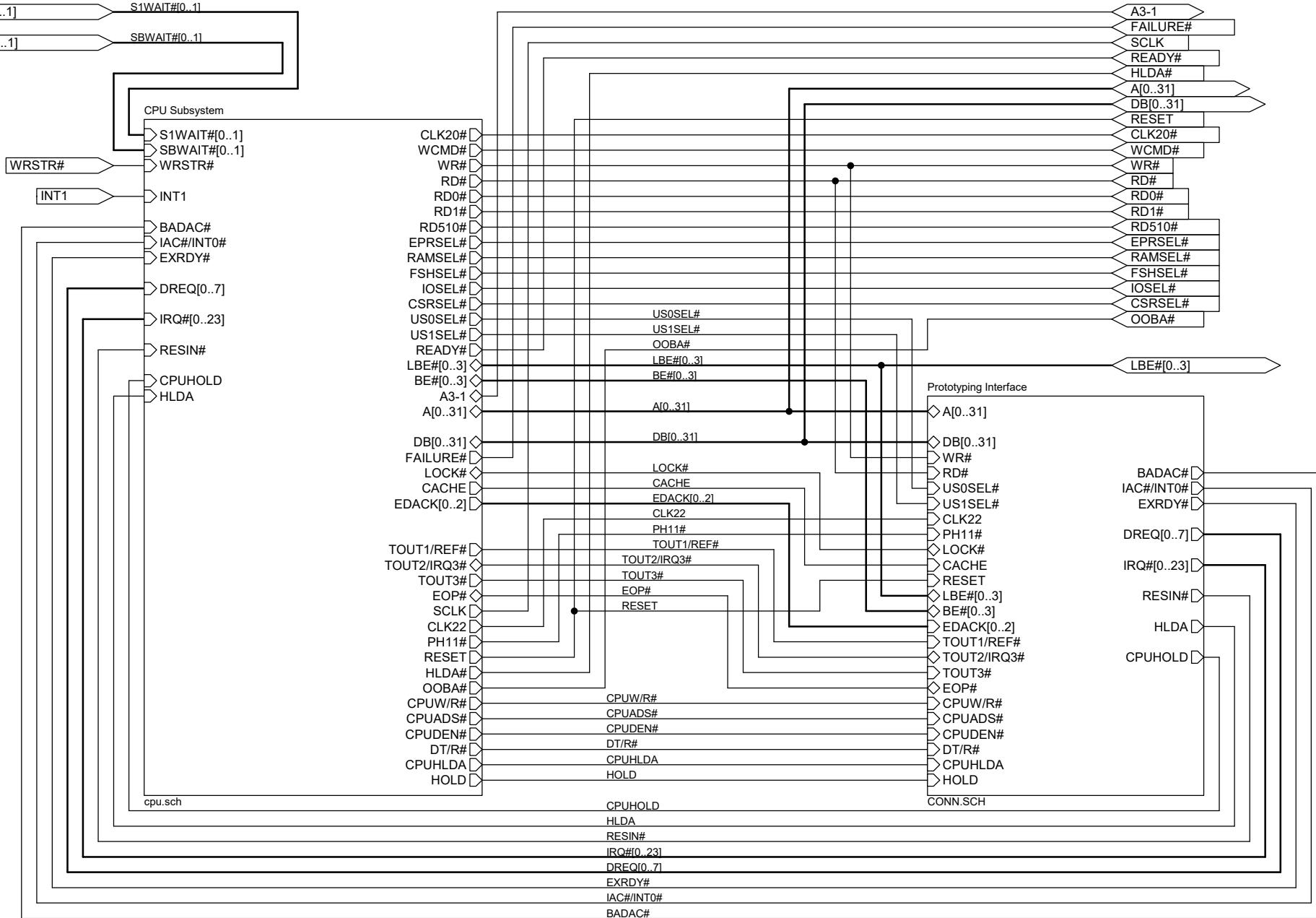


1-QT960	3
2-CPUPROTO	4
3-CPU	5
4-PROCESSR	6
5-CPUXCVRS	7
5-CPUXCVRS-bmp	8
6-CPUPULLP	9
7-DMACTINF	10
7-DMACTINF-bmp	11
8-DMACTRL	12
9-DMAPULLP	13
10-CLOCKGEN	14
10-CLOCKGEN-bmp	15
11-BUSCTRL	16
12-READYGEN	17
12-READYGEN-bmp	18
13-LOGBLK1	19
13-LOGBLK1-bmp	20
14-LOGBLK2	21
14-LOGBLK2-bmp	22
15-CONN	23
16-HEADERS	24
16-HEADERS-bmp	25
17-WWPOSTS	26
18-I_O	27
19-SERCON	28
19-SERCON-bmp	29
20-CSR	30
20-CSR-bmp	31
21-MEM	32

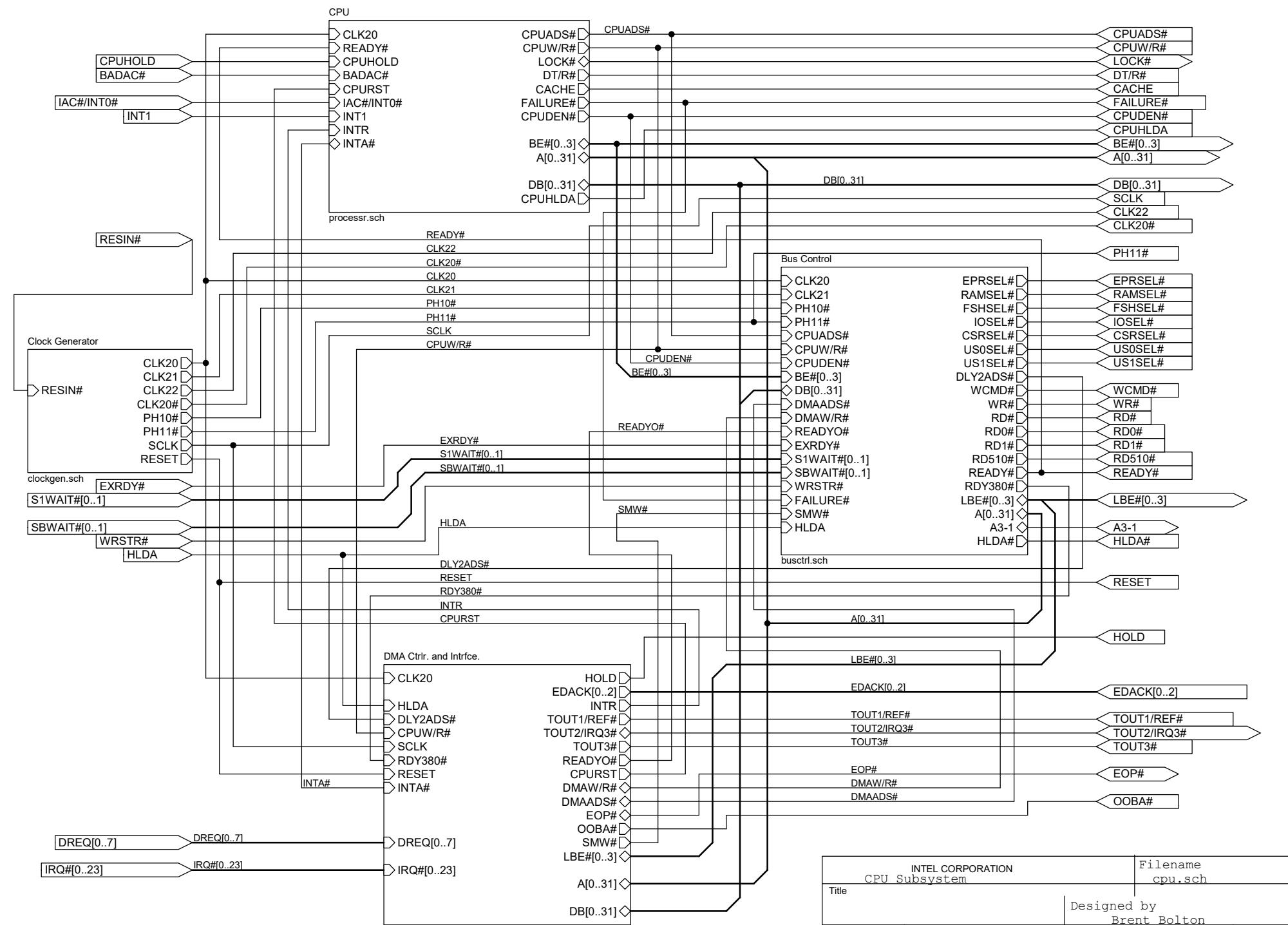
22-WRDEPRB1	33
23-WRDEPRB0	34
24-FLASHPR	35
25-RAM	36
26-MEMINT-bmp	37
27-DECAP0	38
27-DECAP0-bmp	39



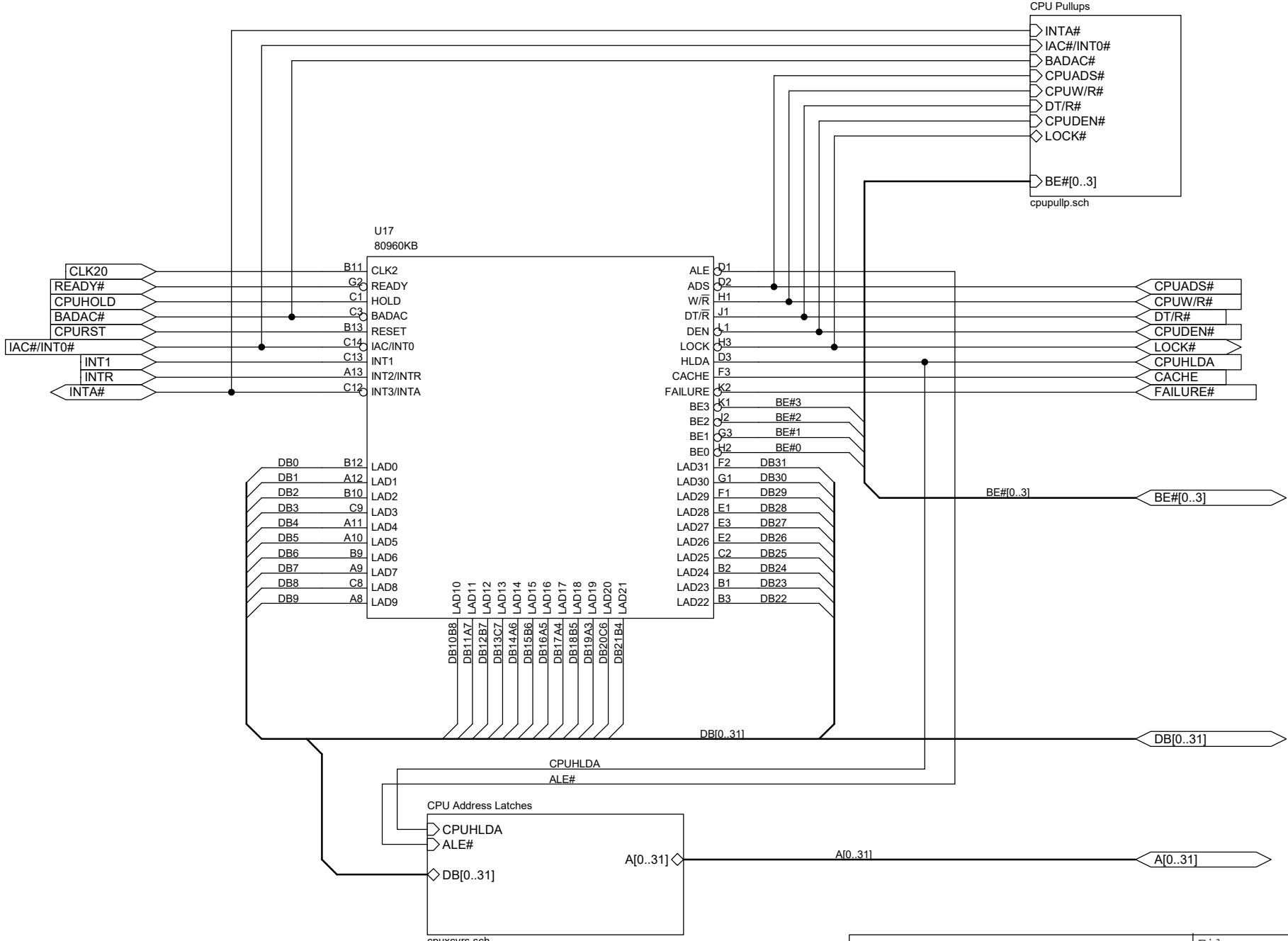
INTEL CORPORATION QT960		Filename qt960.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 1 of 27 sheets



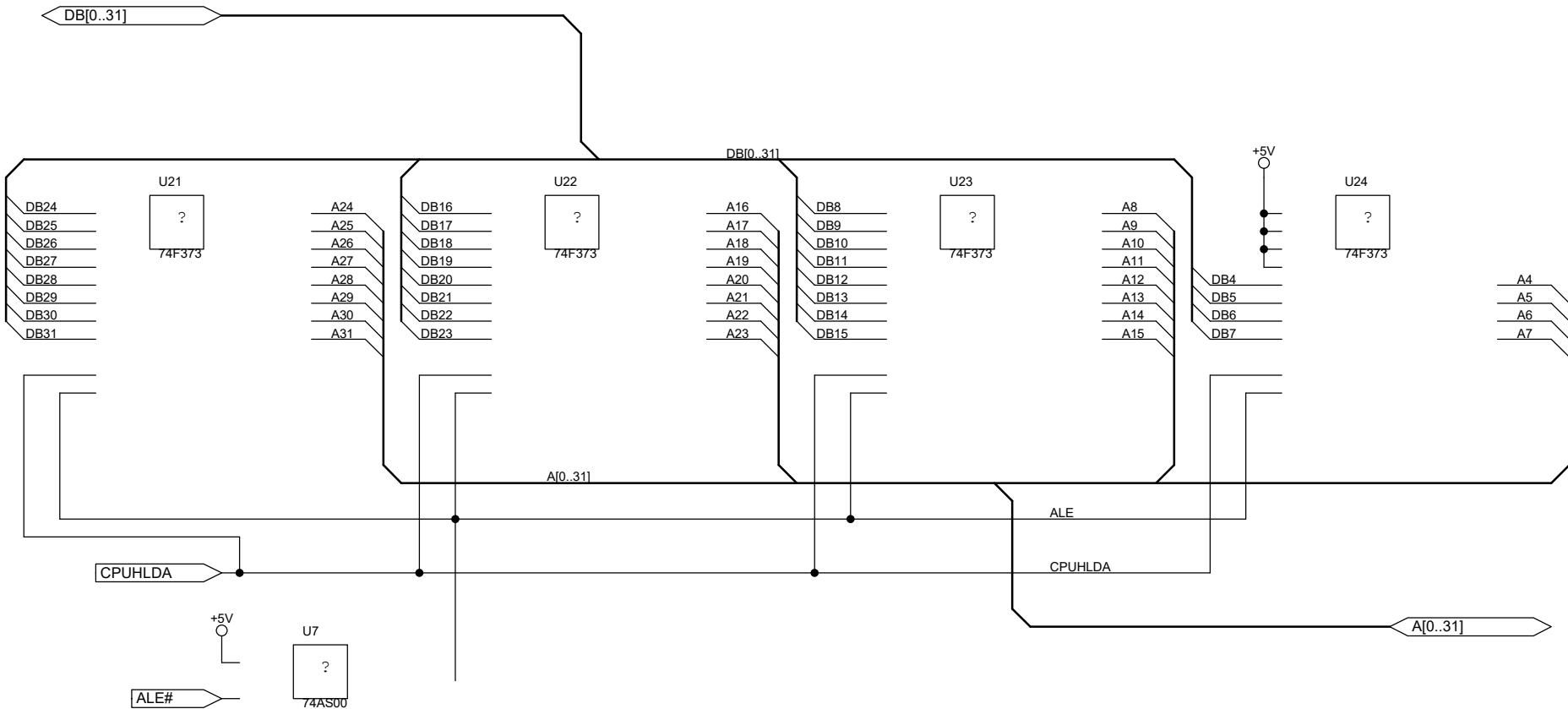
CPU Subsystem and Prototyping Interface		Filename cpupproto.sch
Title		Designed by Brent Bolton
Size	Document Number	Rev
A		2.1
Date: February 22, 1989		Sheet: 2 of 27 sheets



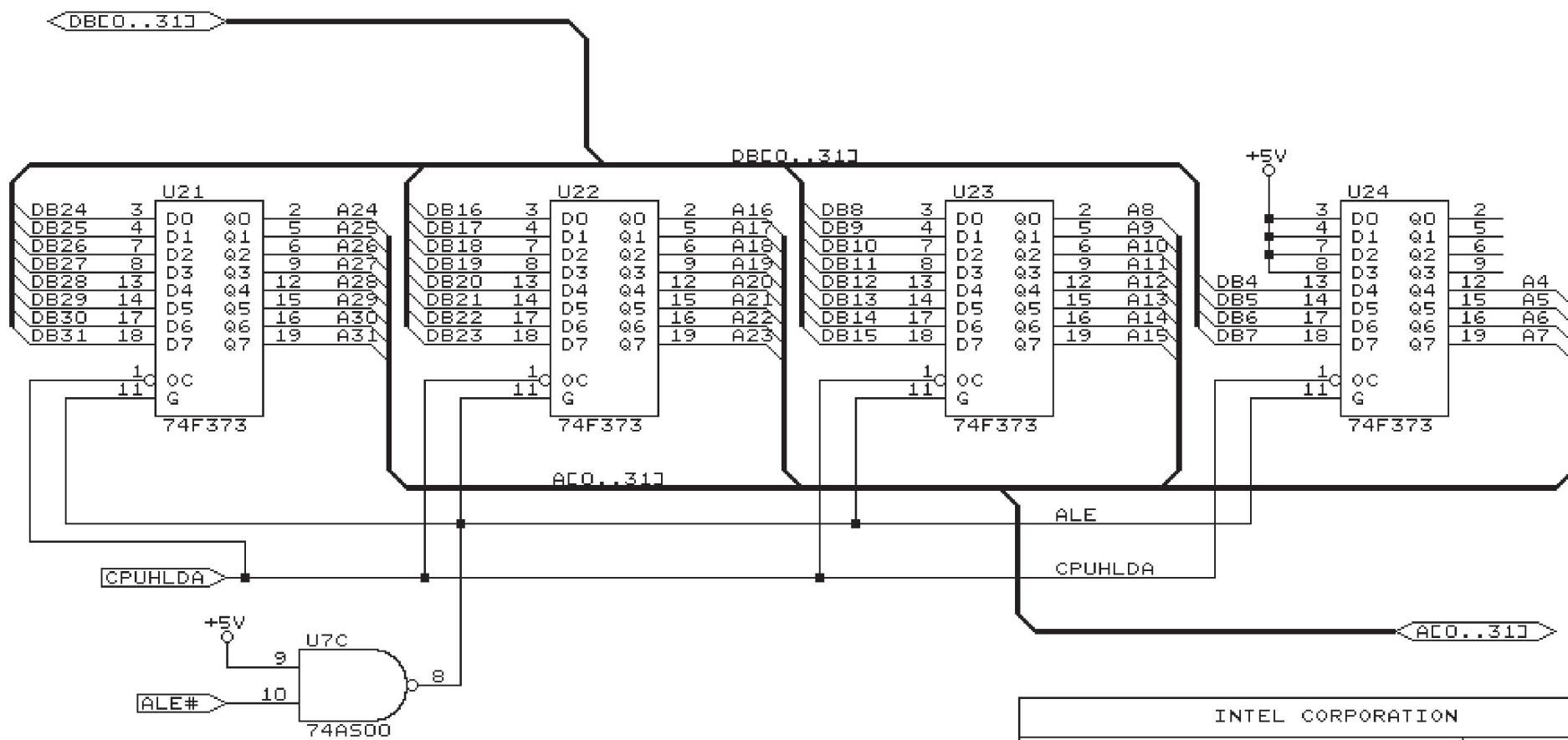
INTEL CORPORATION CPU Subsystem		Filename cpu.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 3 of 27 sheets	

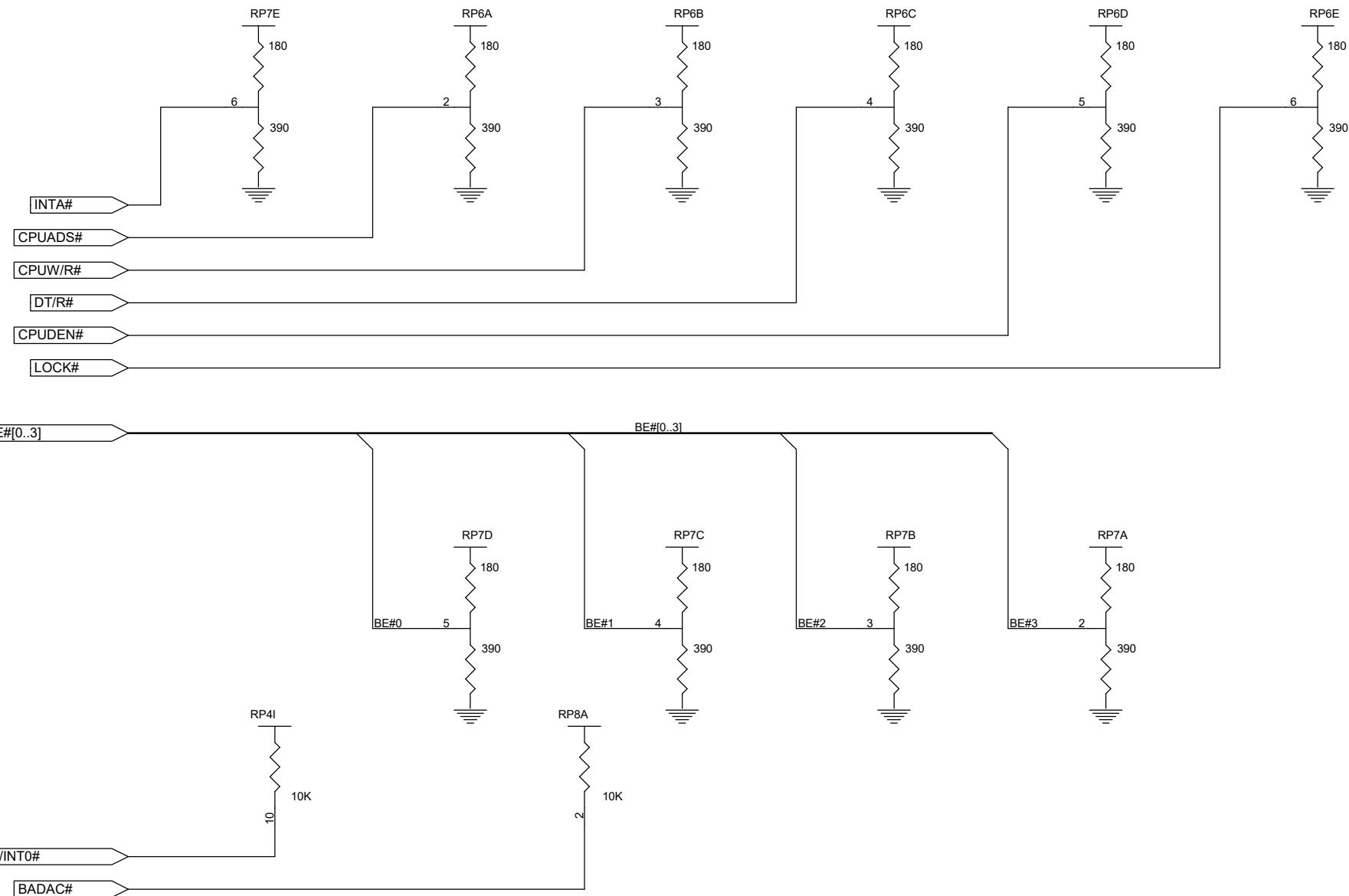


INTEL CORPORATION		Filename processr.sch
CPU		Title
		Designed by Brent Bolton
Size	Document Number	Rev
A		2.1
Date: February 22, 1989		Sheet: 4 of 27 sheets

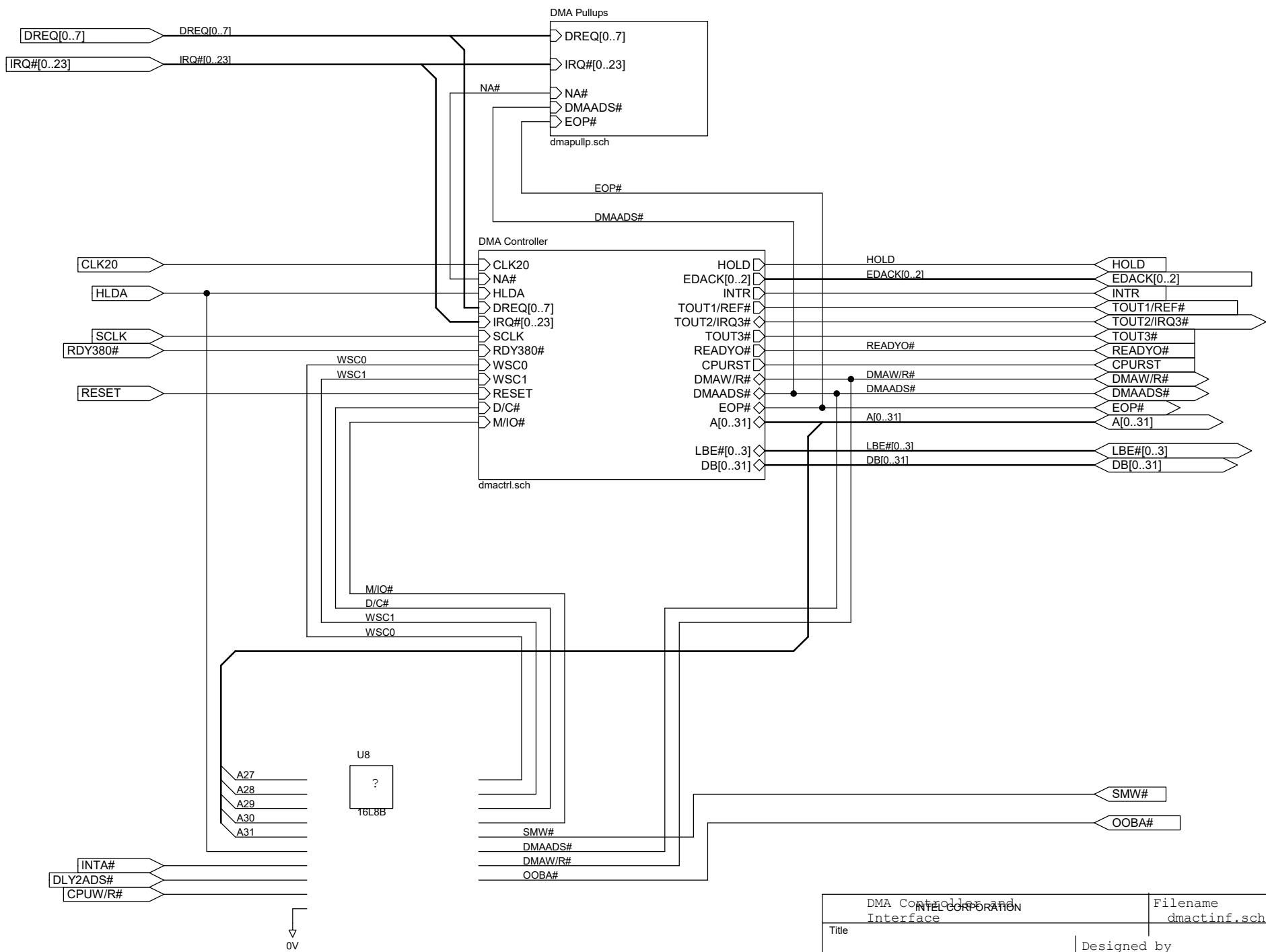


INTEL CORPORATION CPU Address Latches		Filename cpuxcvrs.sch
Title		
Designed by Brent Bolton		
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 5 of 27 sheets

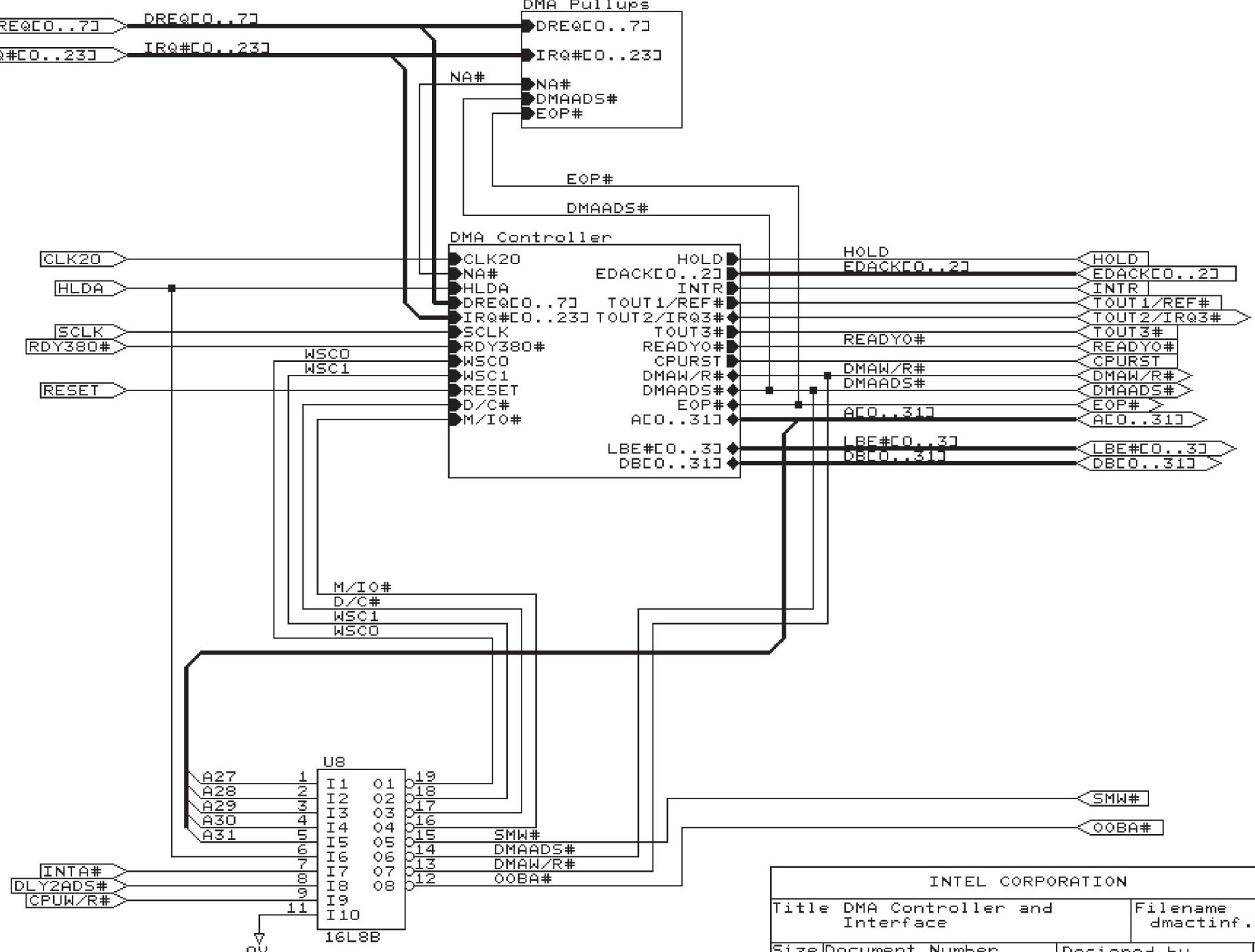




INTEL CORPORATION CPU Pullups		Filename cpupullp.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 6 of 27 sheets	

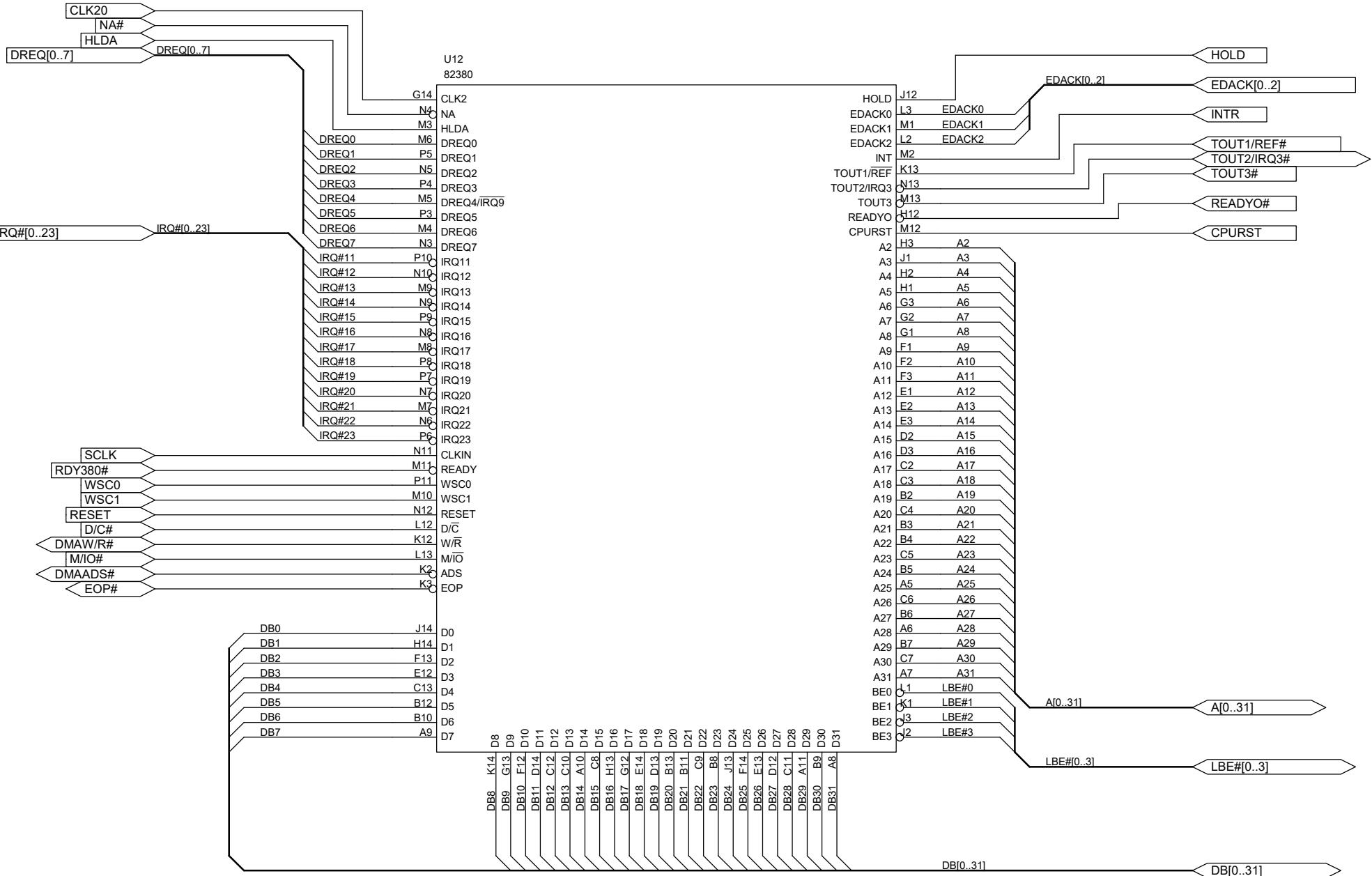


DMA Controller and Interface		INTEL CORPORATION	Filename dmactinf.sch
Title		Designed by	Brent Bolton
Size	Document Number		Rev
A			2.1
Date: February 22, 1989		Sheet: 7 of 27 sheets	

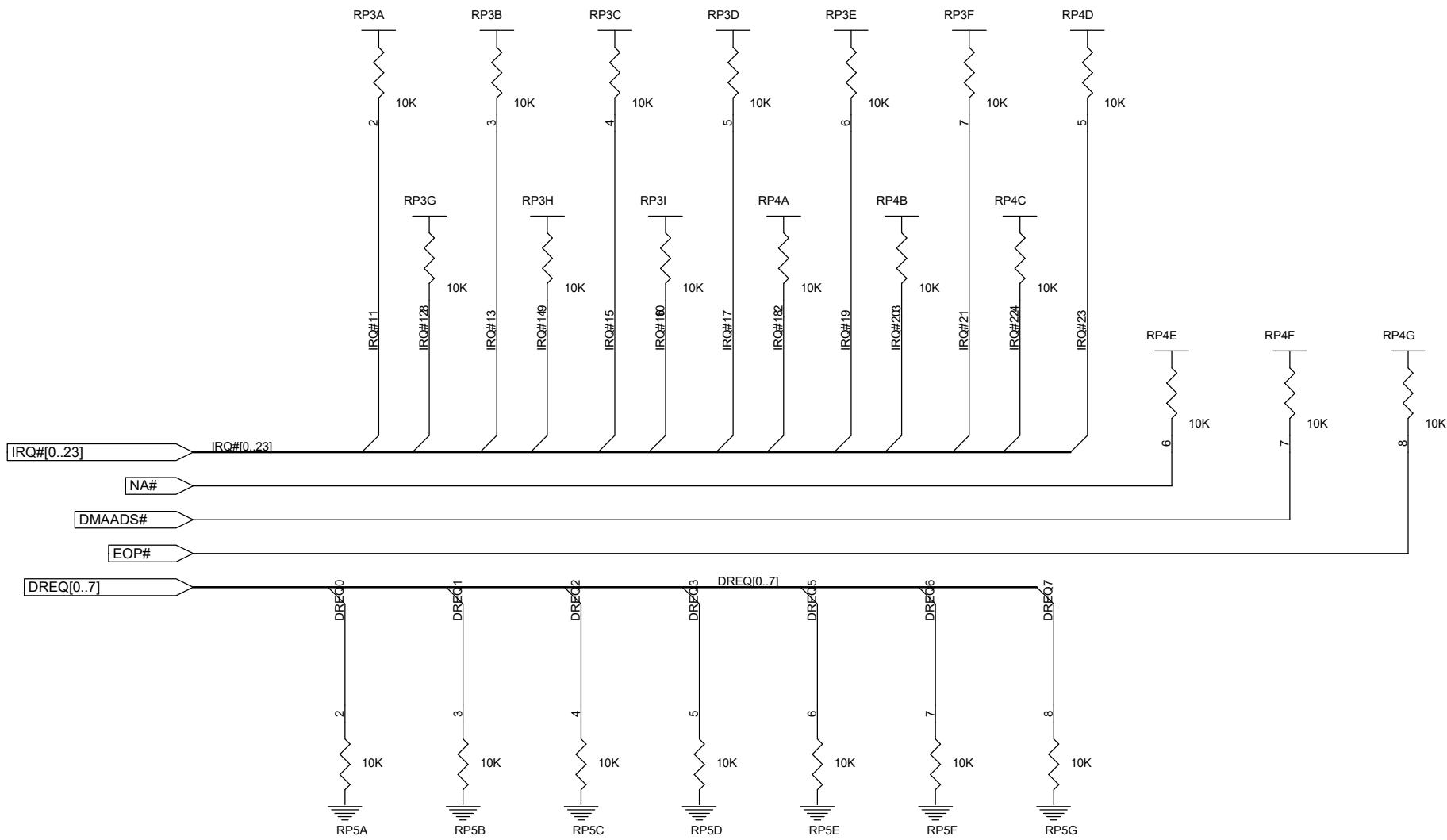


INTEL CORPORATION

Title DMA Controller and Interface		Filename dmactinf.sch
Size A	Document Number	Designed by Brent Bolton
REV 2.1		
Date: February 22, 1989 Sheet 7 of 27		

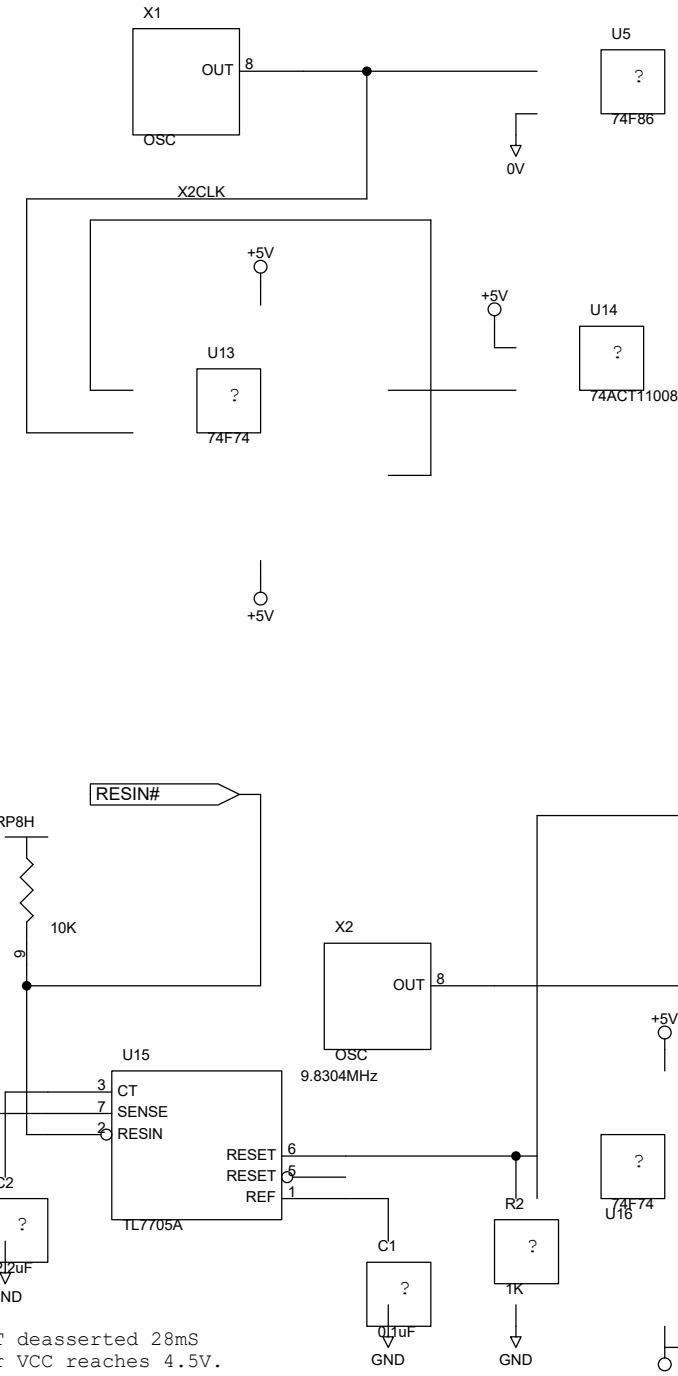


INTEL CORPORATION DMA Controller		Filename dmactrl.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 8 of 27 sheets	

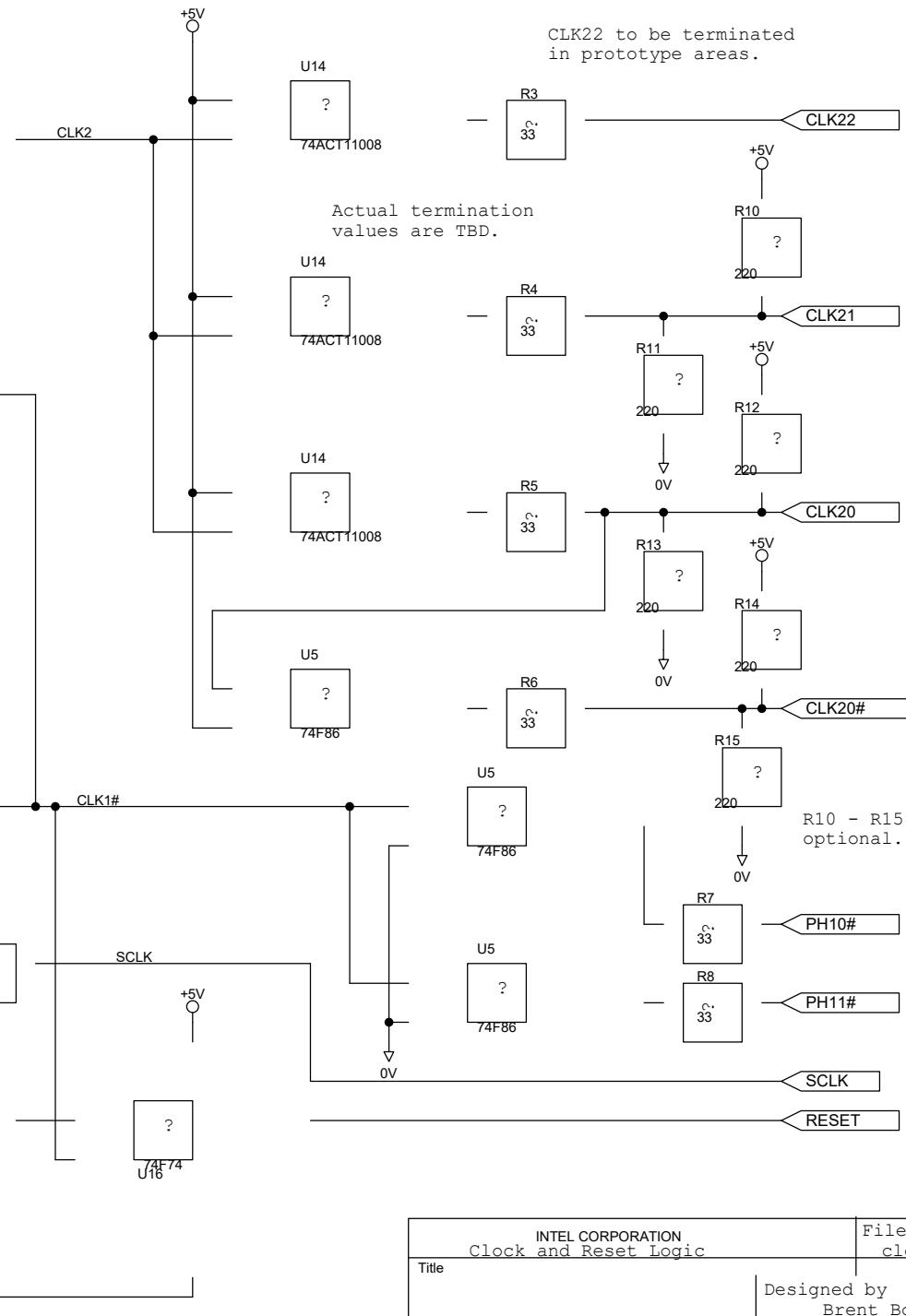


INTEL CORPORATION DMA Pullups		Filename dmapullp.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 9 of 27 sheets

2X Processor Frequency
(e. g. 40MHz for 80960KB-20)

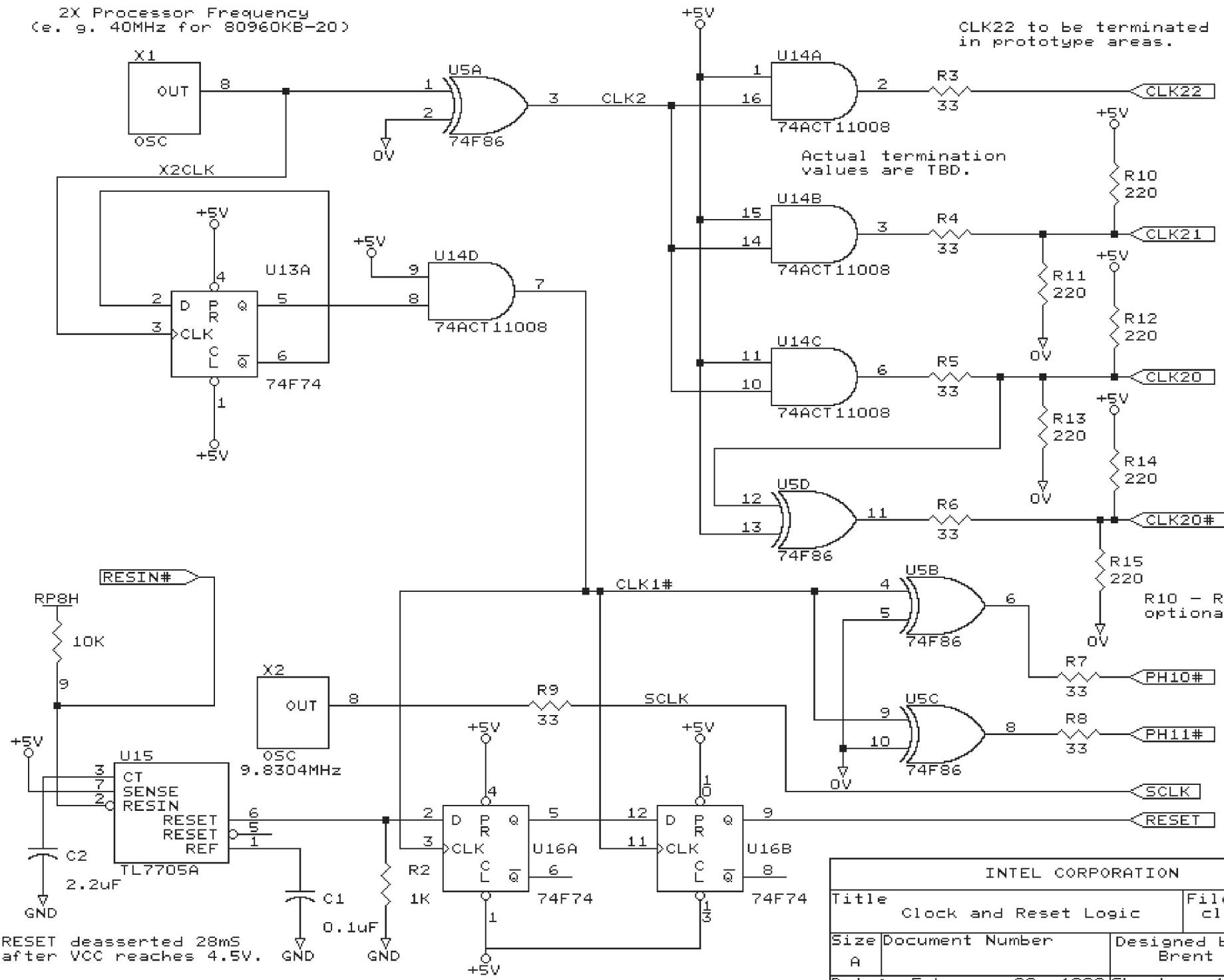


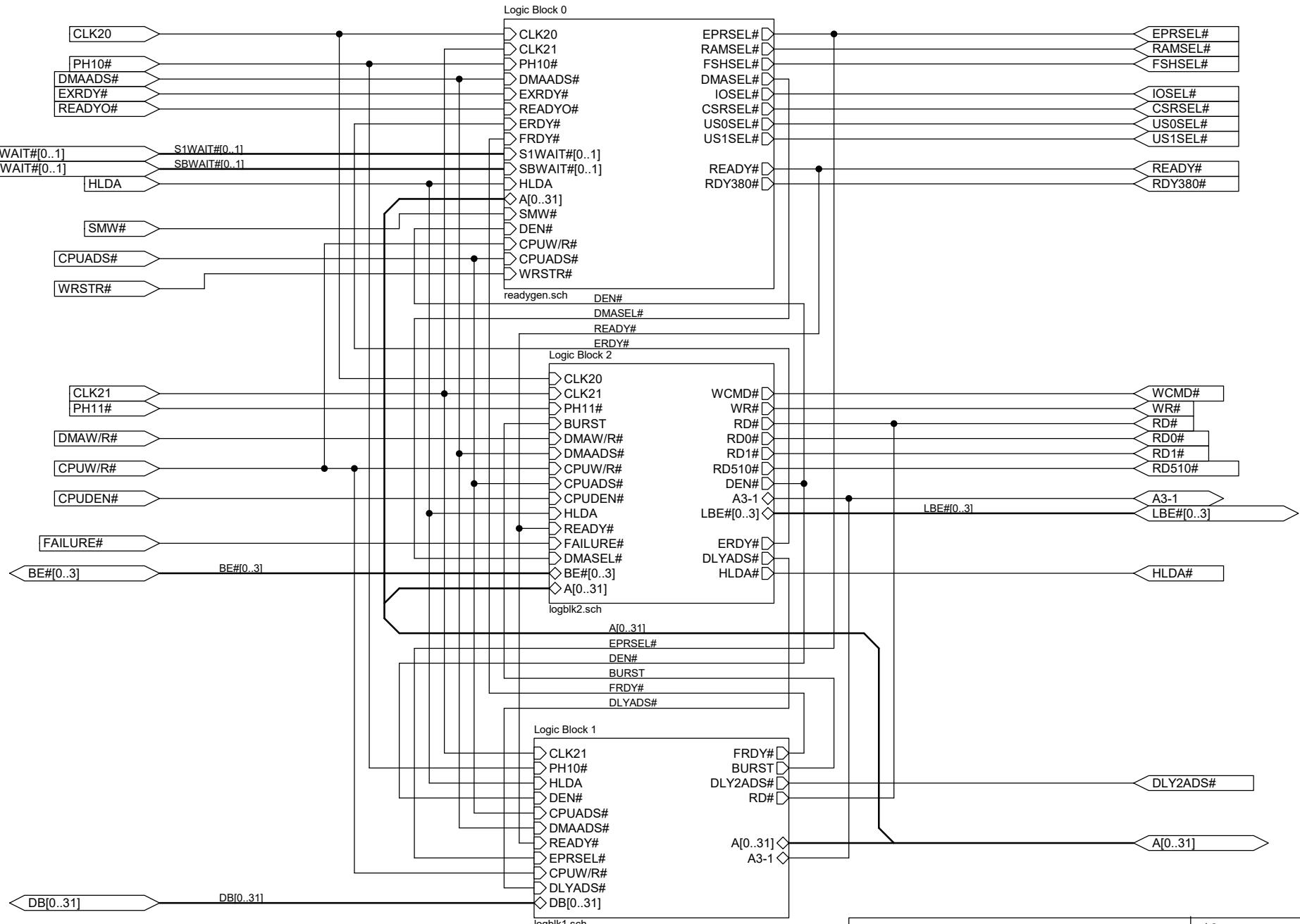
RESET deasserted 28mS
after VCC reaches 4.5V.



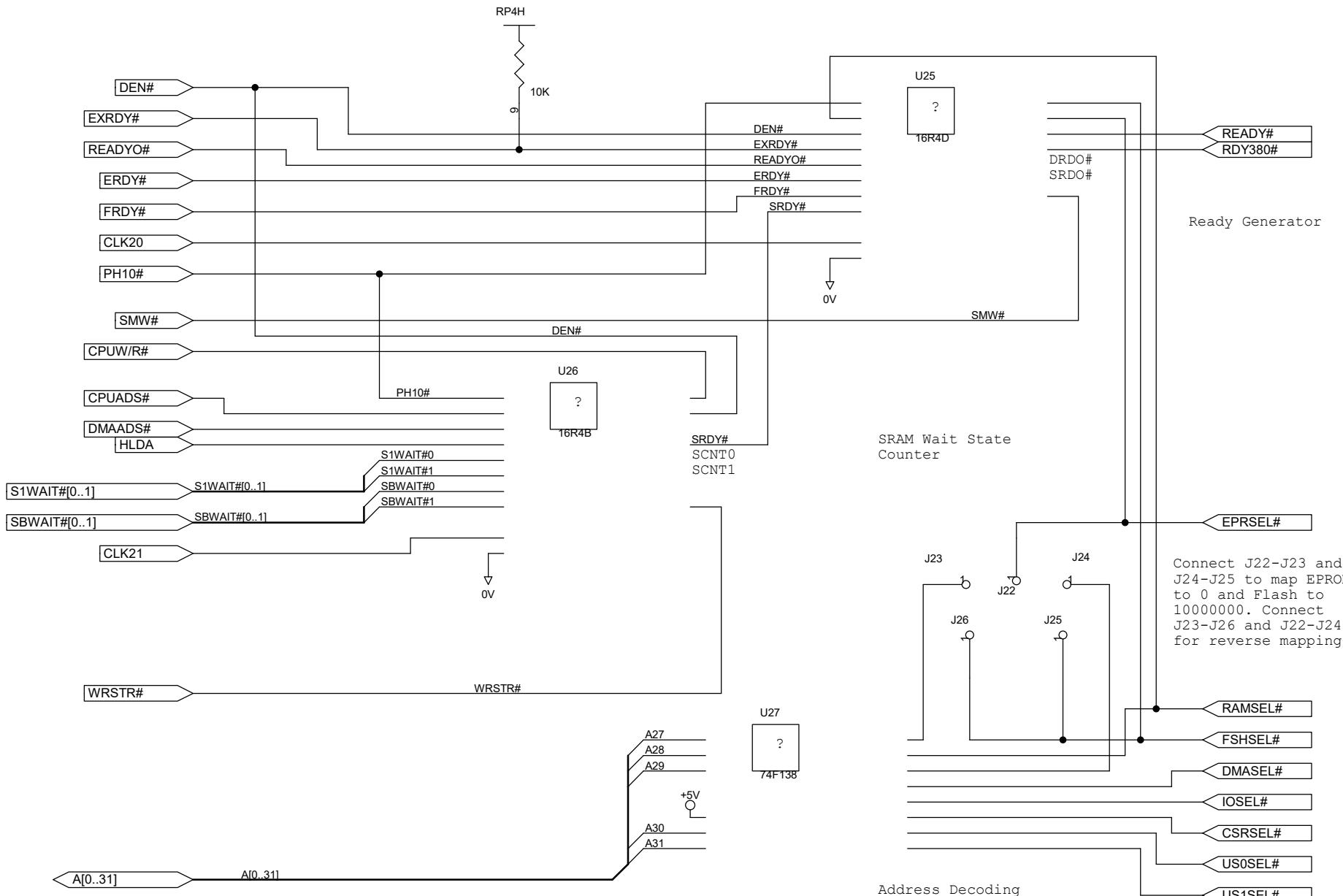
INTEL CORPORATION Clock and Reset Logic		Filename <u>clockgen.sch</u>
Title	Designed by <u>Brent Bolton</u>	
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 10 of 27 sheets

2X Processor Frequency
(e.g. 40MHz for 80960KB-20)

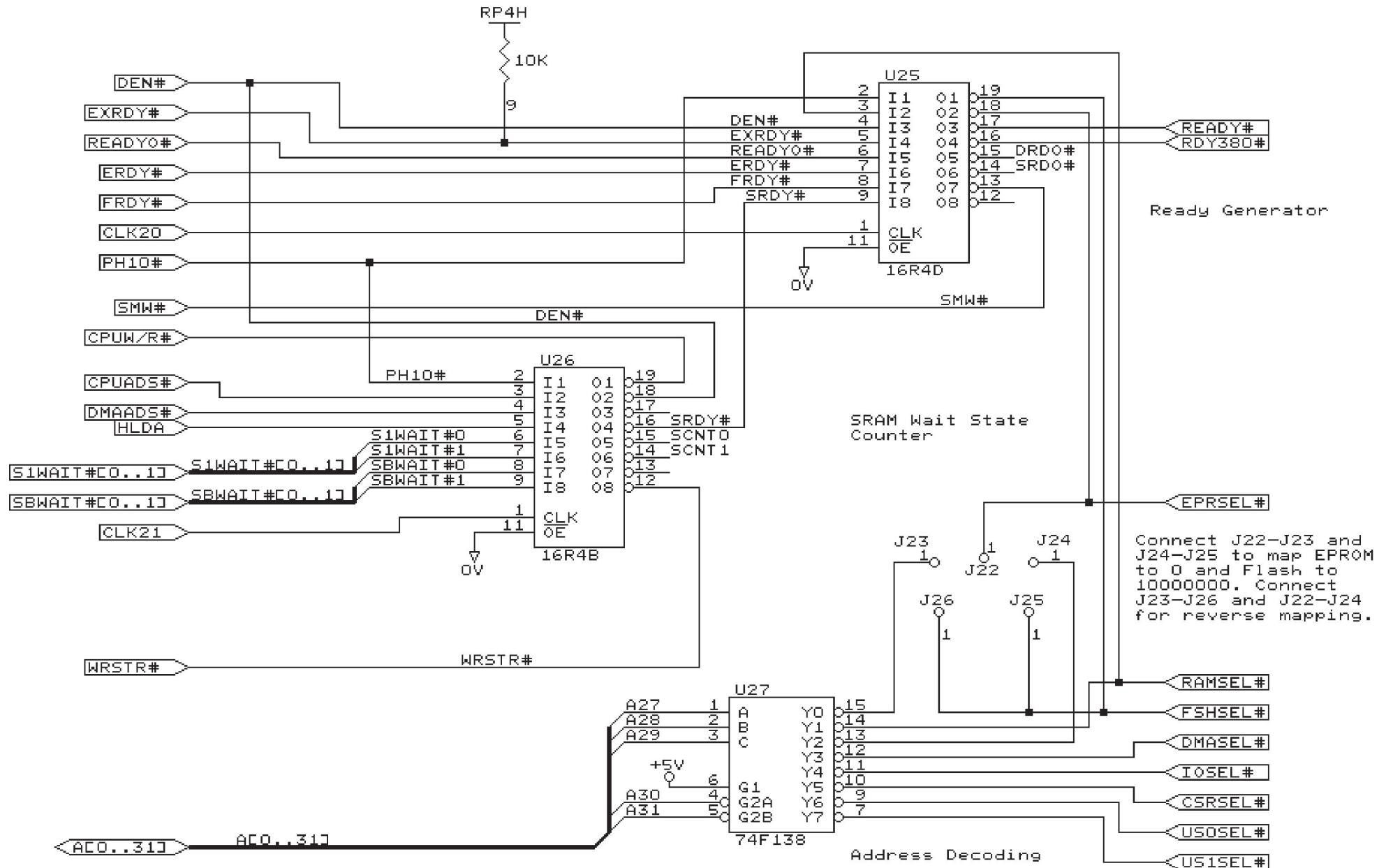


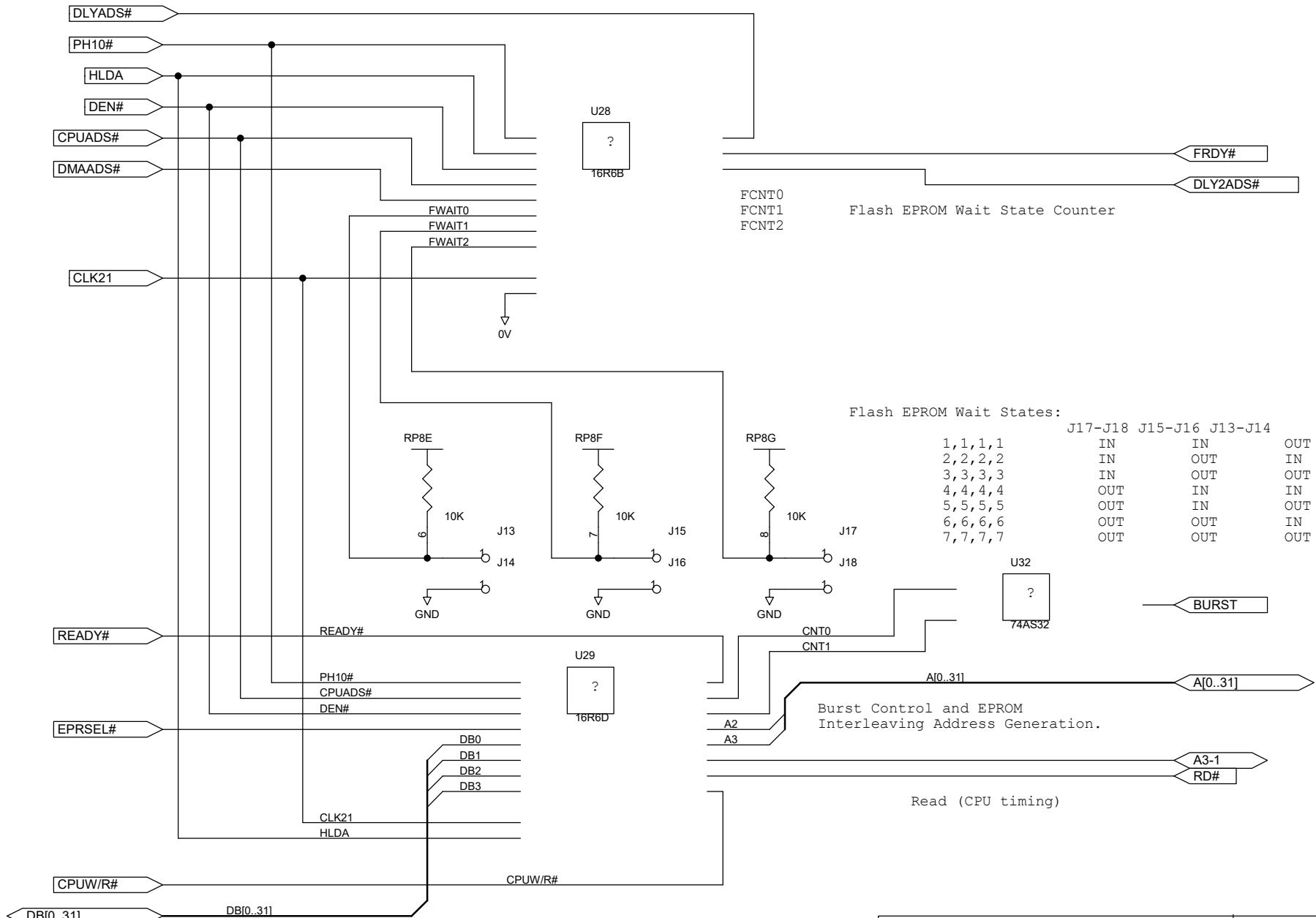


INTEL CORPORATION Bus Control		Filename busctrl.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 11 of 27 sheets	

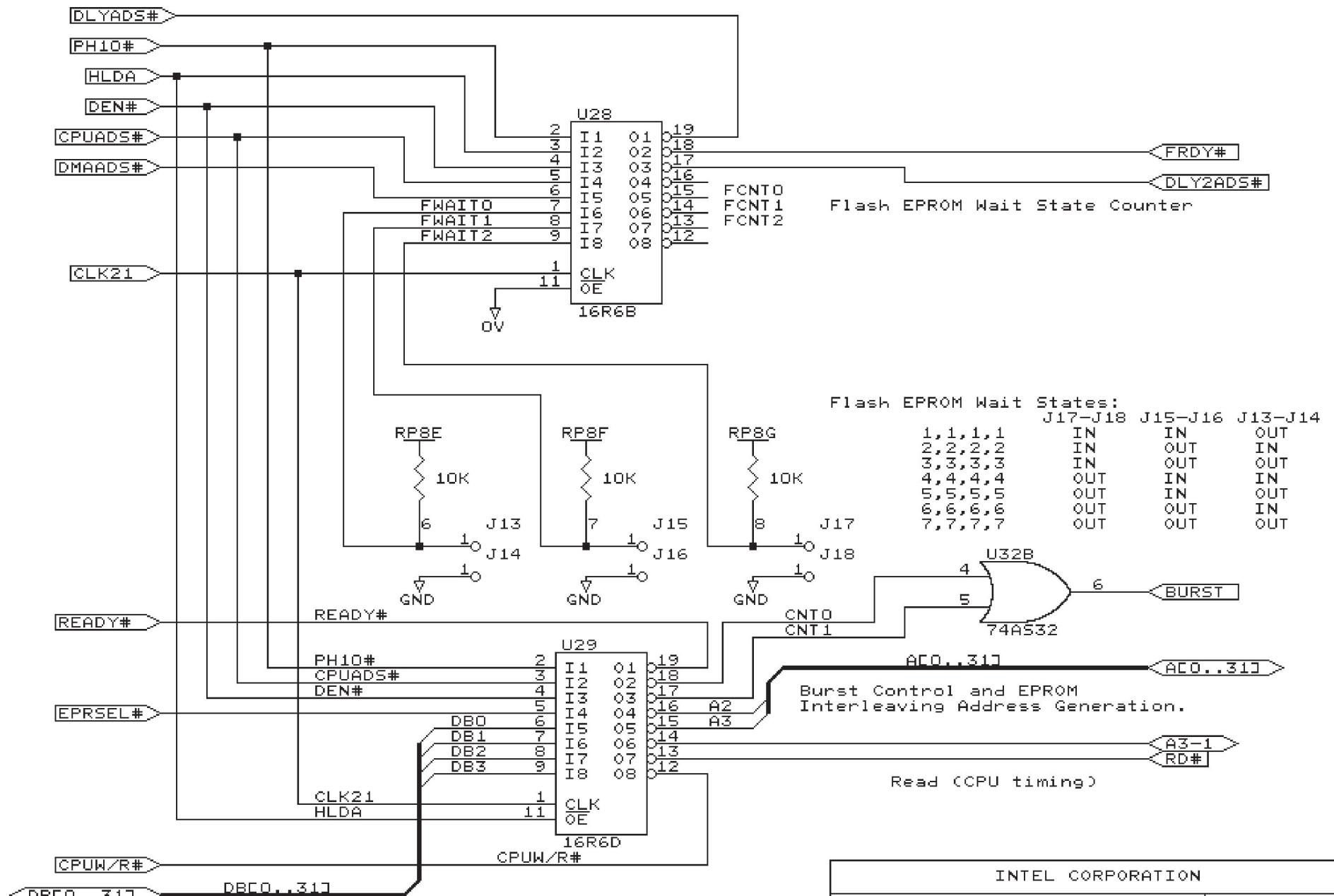


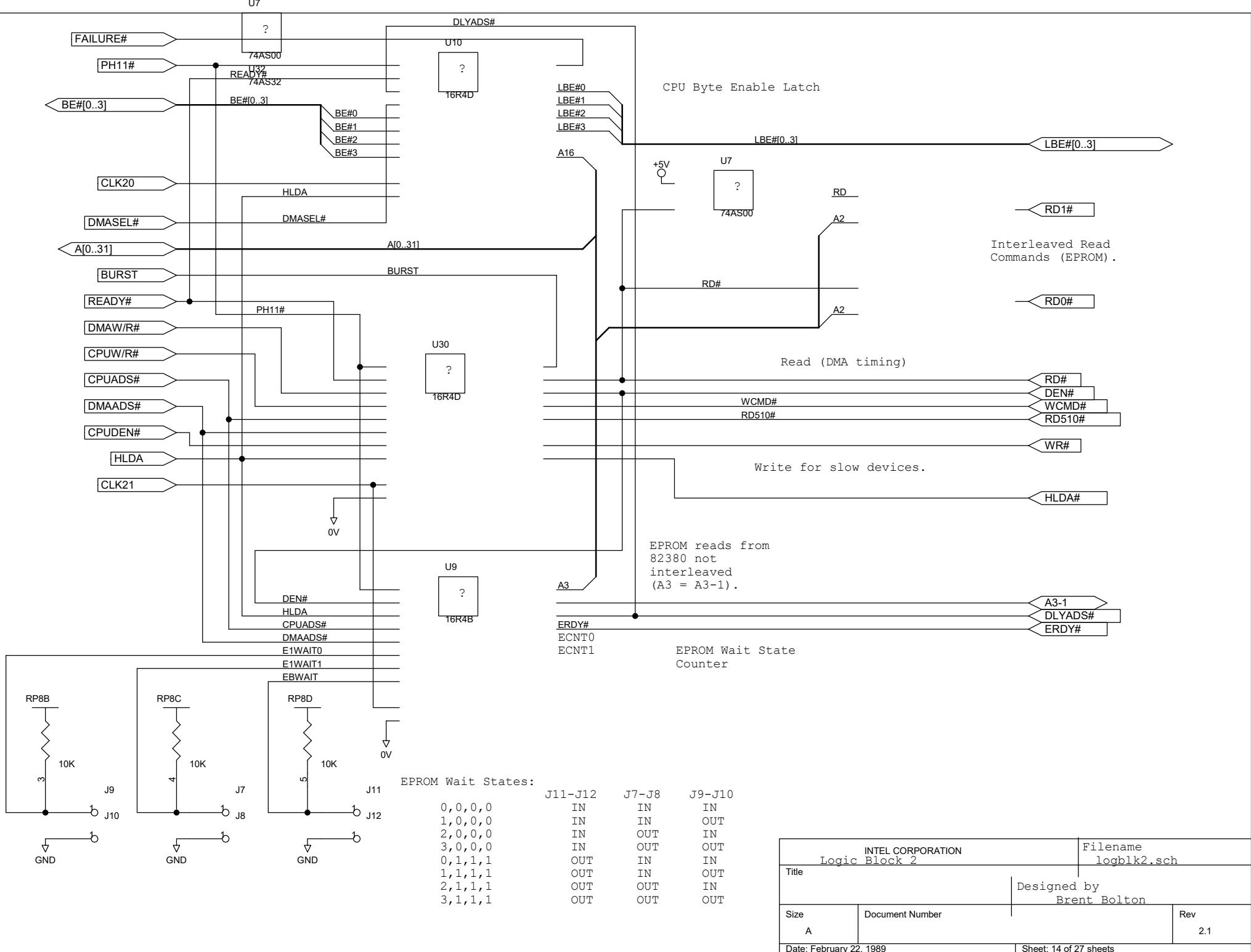
INTEL CORPORATION Logic Block 0		Filename readygen.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 12 of 27 sheets

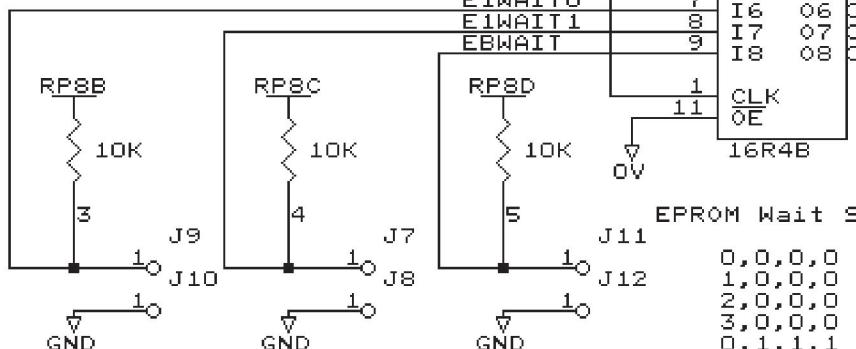
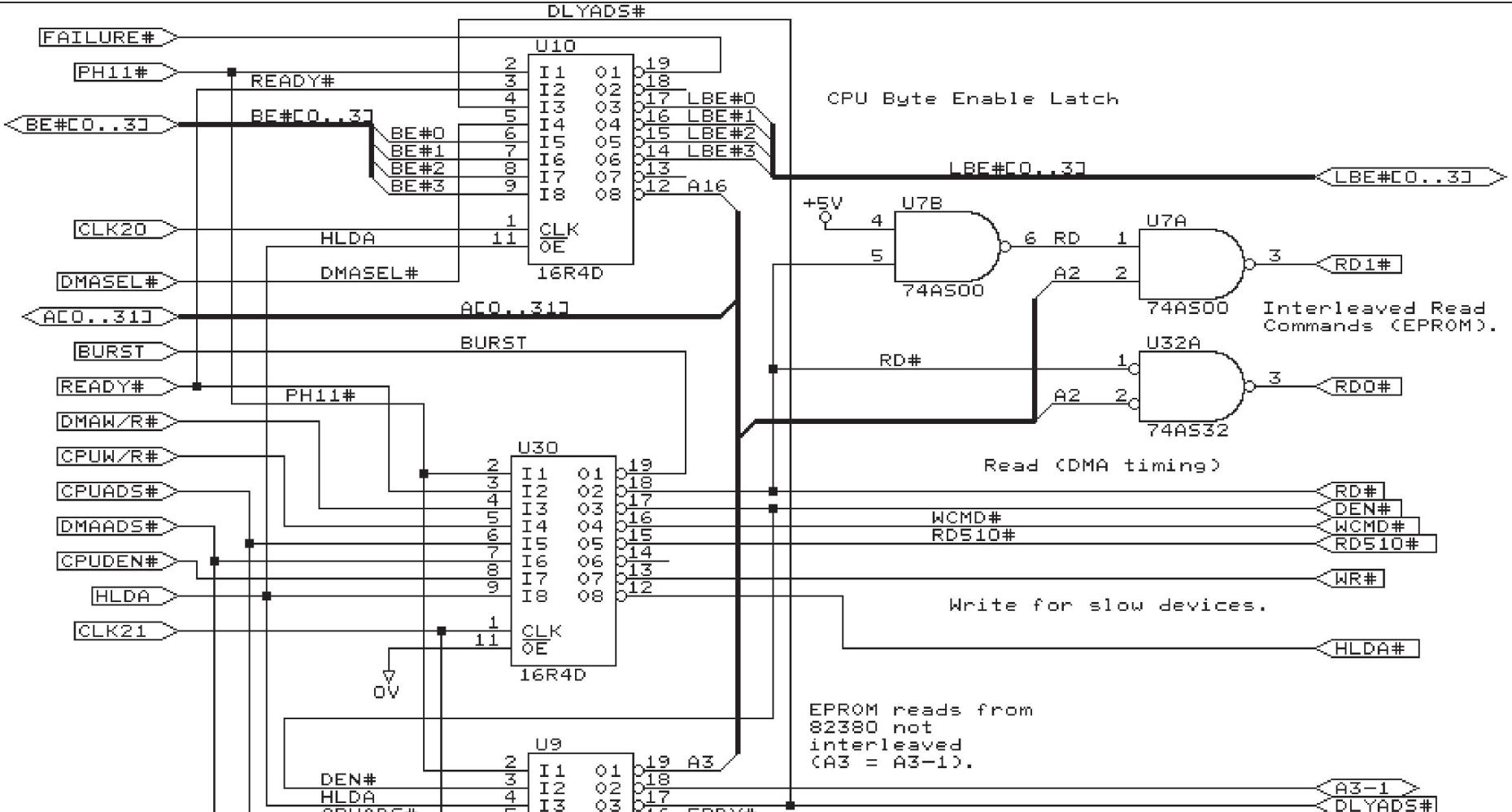




INTEL CORPORATION Logic Block 1		Filename logblk1.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 13 of 27 sheets

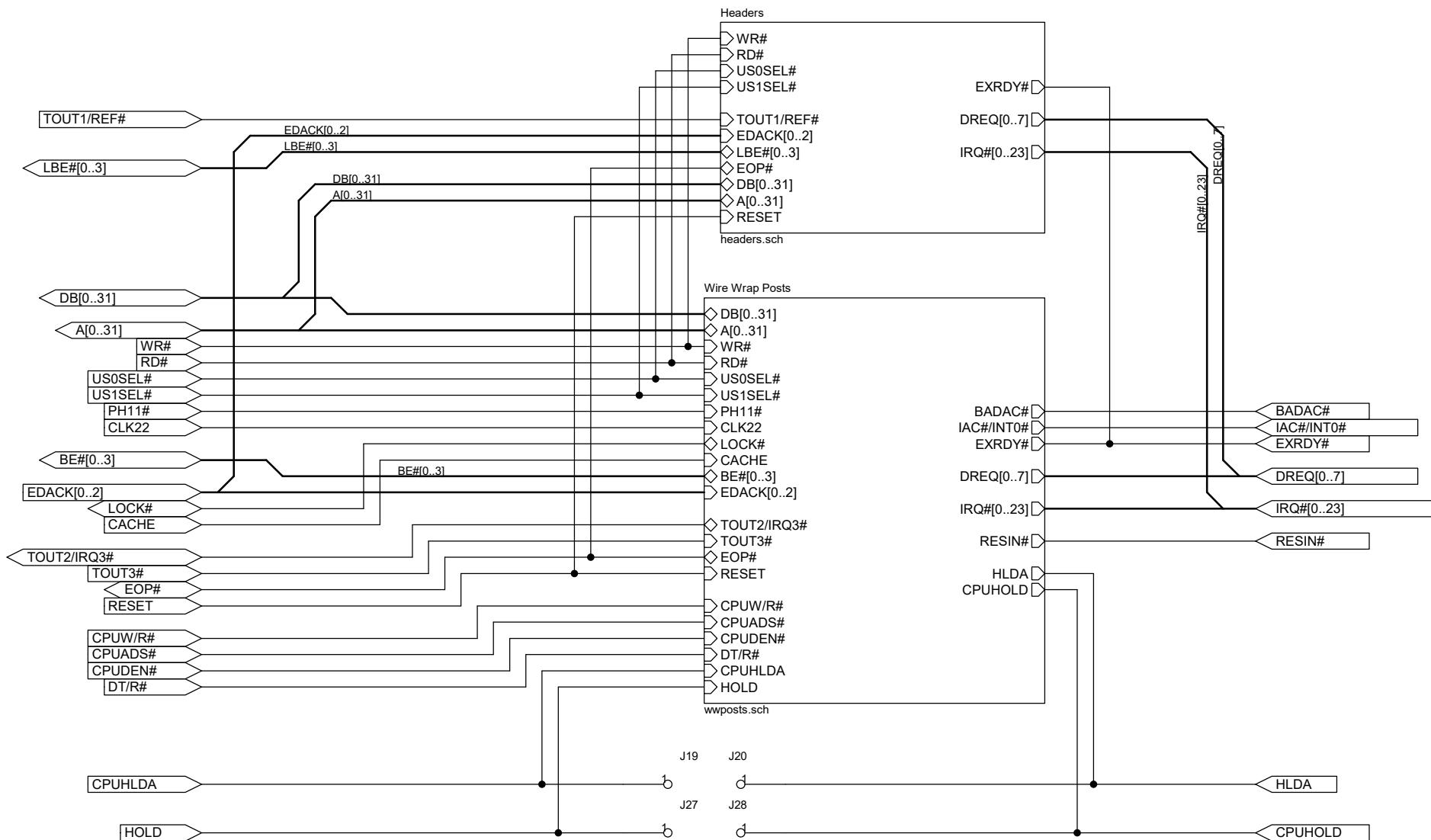






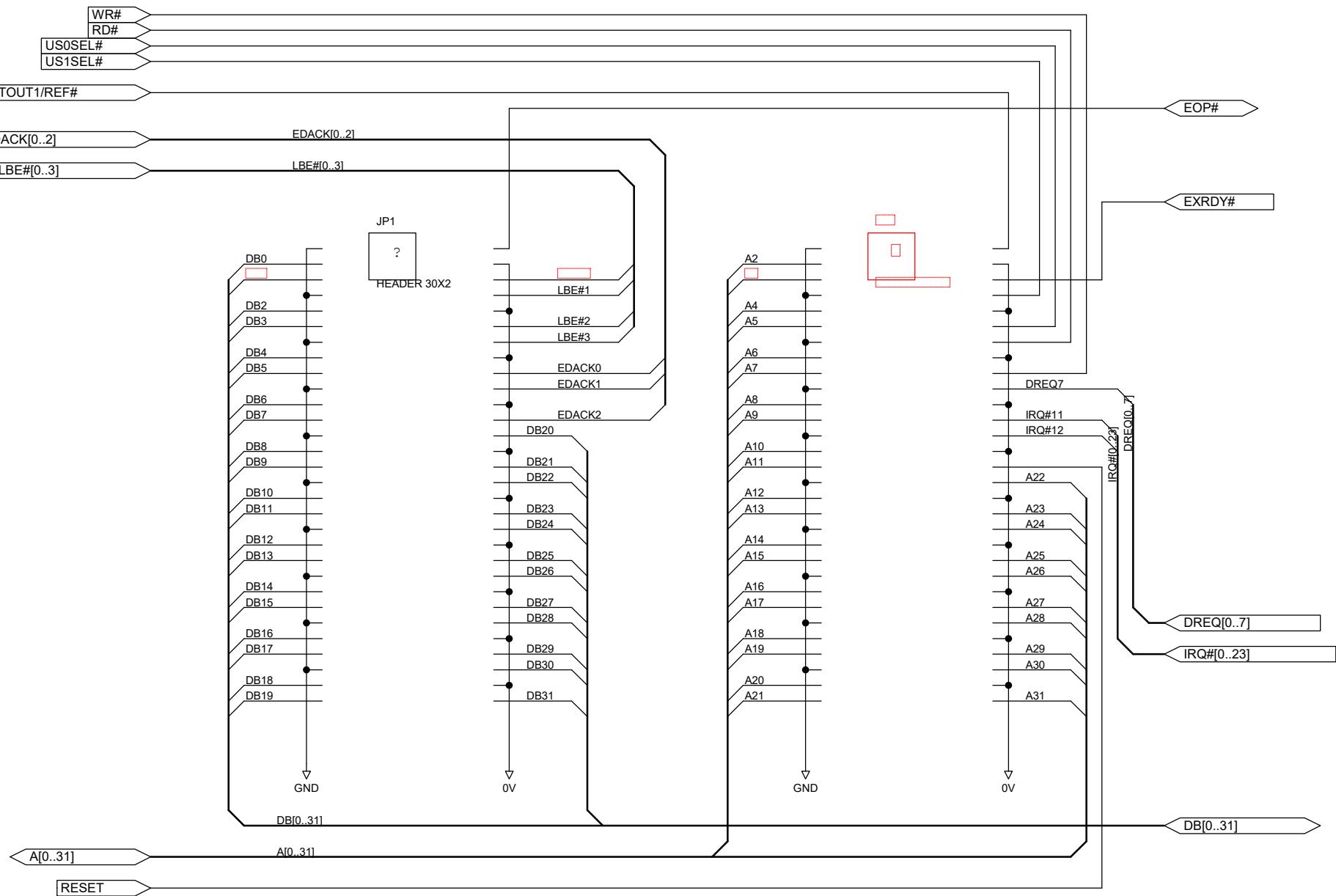
	J11-J12	J7-J8	J9-J10
0,0,0,0	IN	IN	IN
1,0,0,0	IN	IN	OUT
2,0,0,0	IN	OUT	IN
3,0,0,0	IN	OUT	OUT
0,1,1,1	OUT	IN	IN
1,1,1,1	OUT	IN	OUT
2,1,1,1	OUT	OUT	IN
3,1,1,1	OUT	OUT	OUT

INTEL CORPORATION			
Title		Filename	
Size	Document Number	Designed by	REV
A	Logic Block 2	Brent Bolton	2.1
Date: February 22, 1989	Sheet 14 of 27		

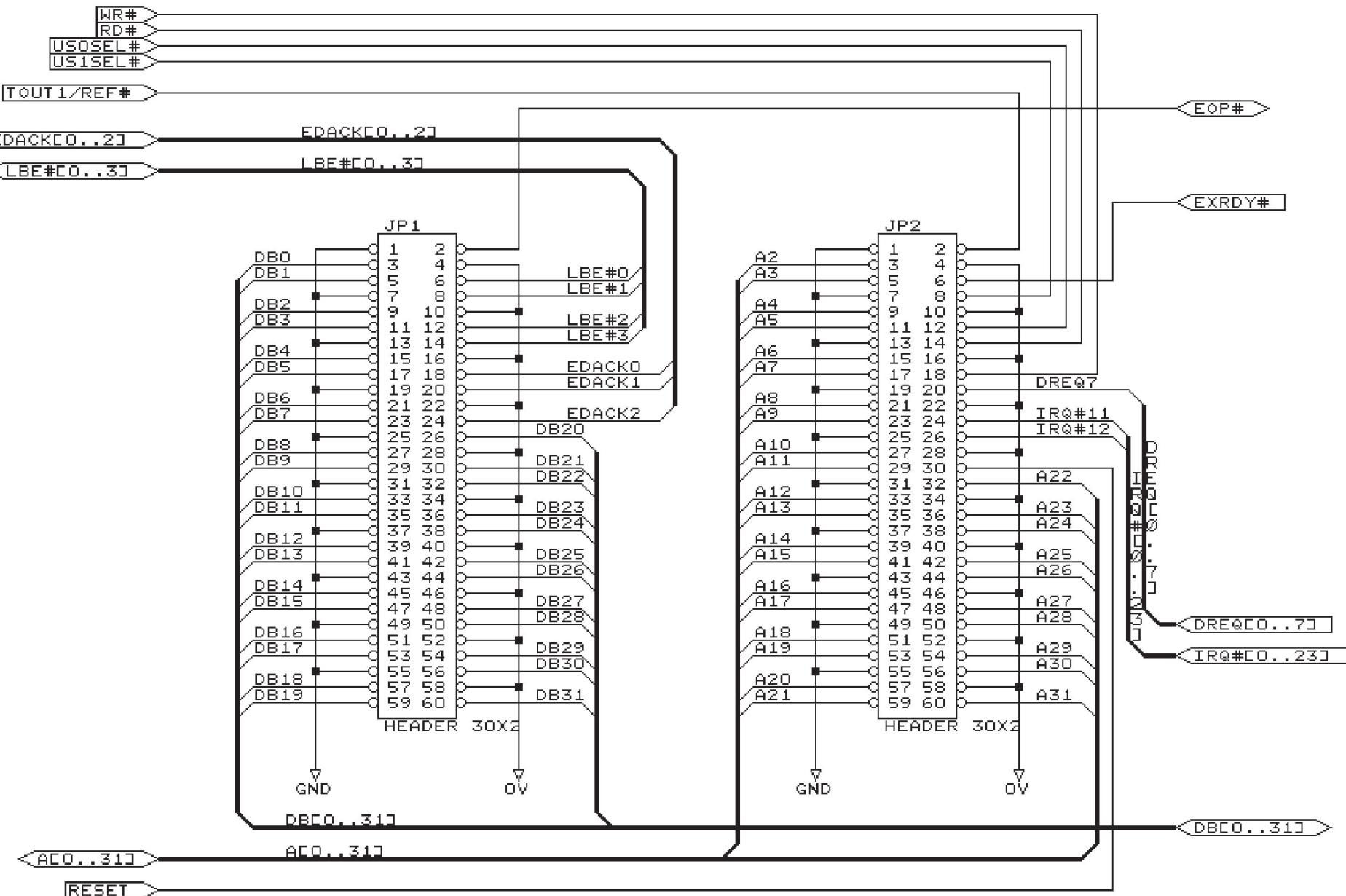


Connect J19-J20 and J27-28 for
normal operation. Disconnect
to insert external bus
arbitration logic.

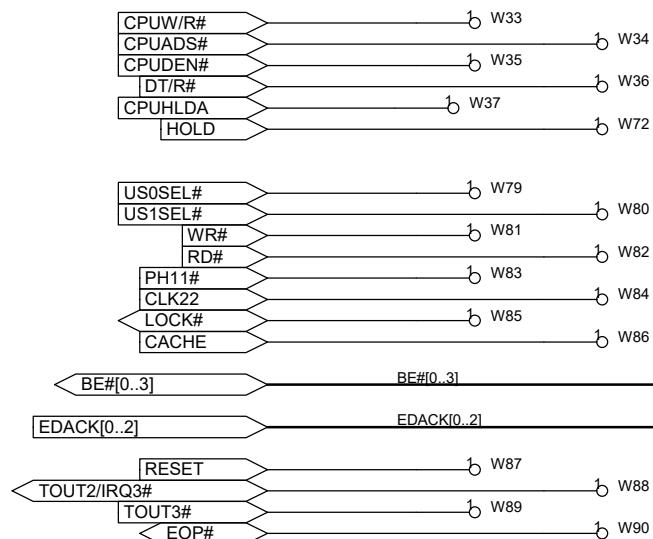
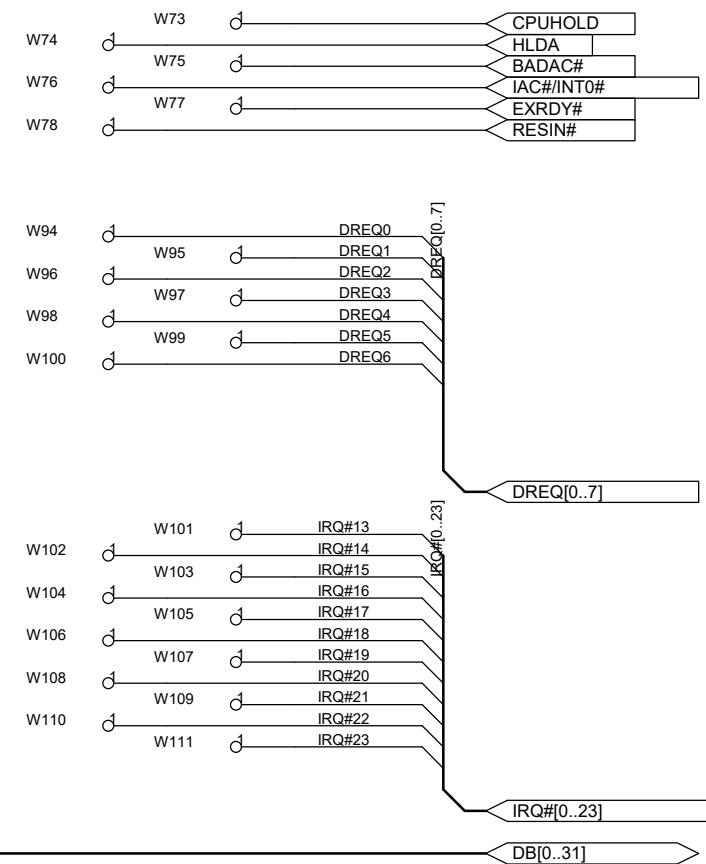
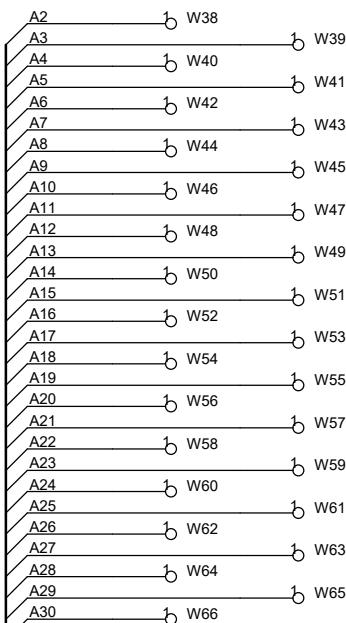
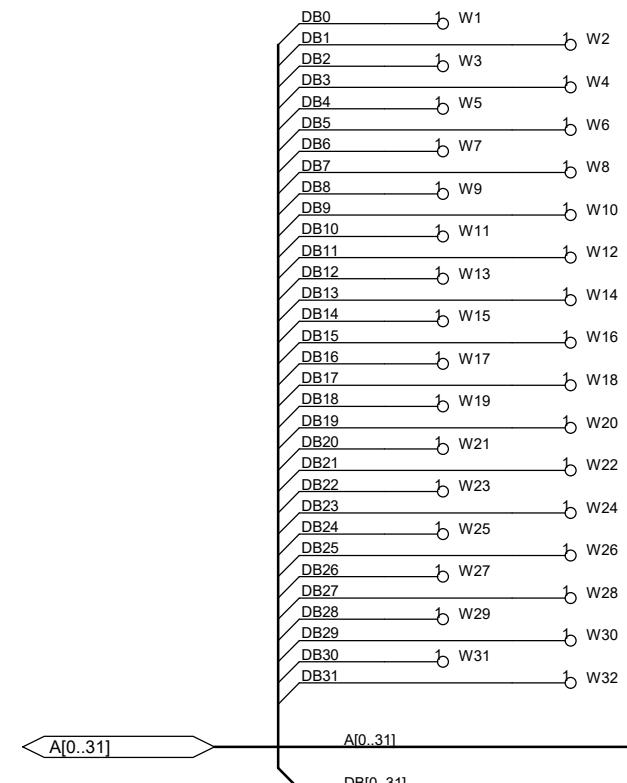
INTEL CORPORATION Prototyping Interface		Filename conn.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 15 of 27 sheets	



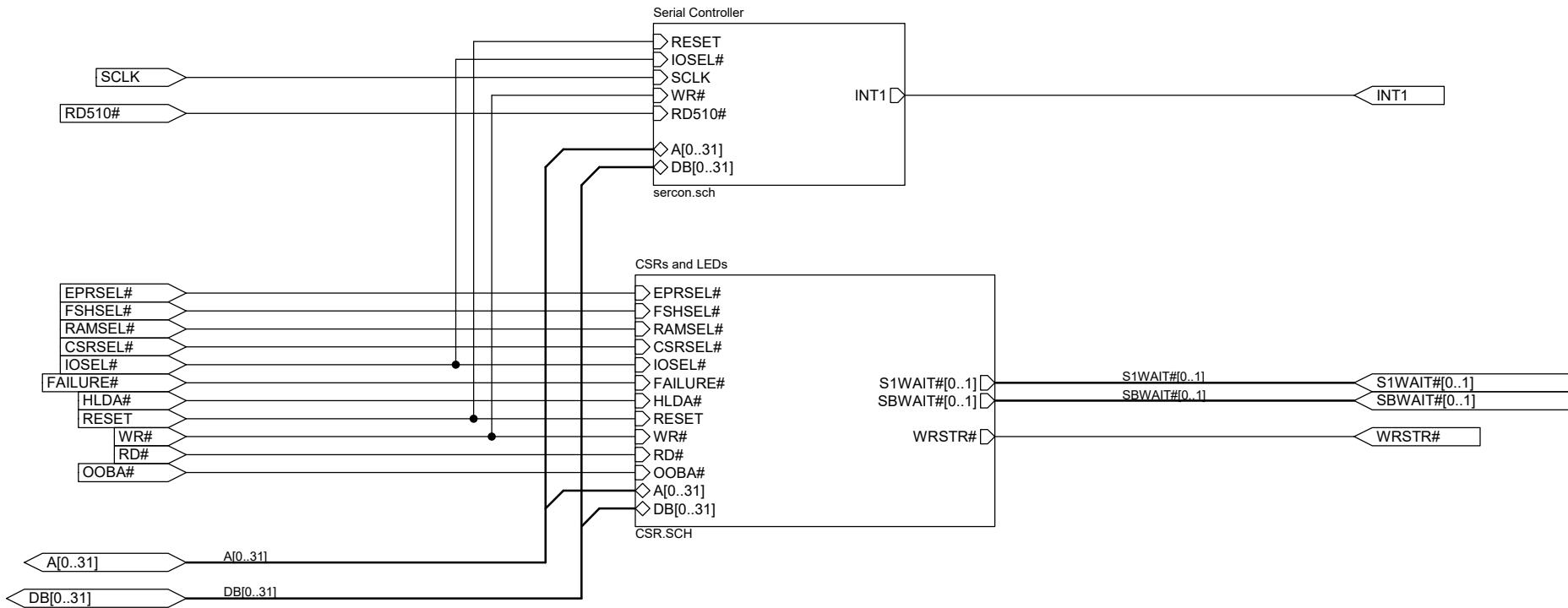
INTEL CORPORATION Headers		Filename headers.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 16 of 27 sheets



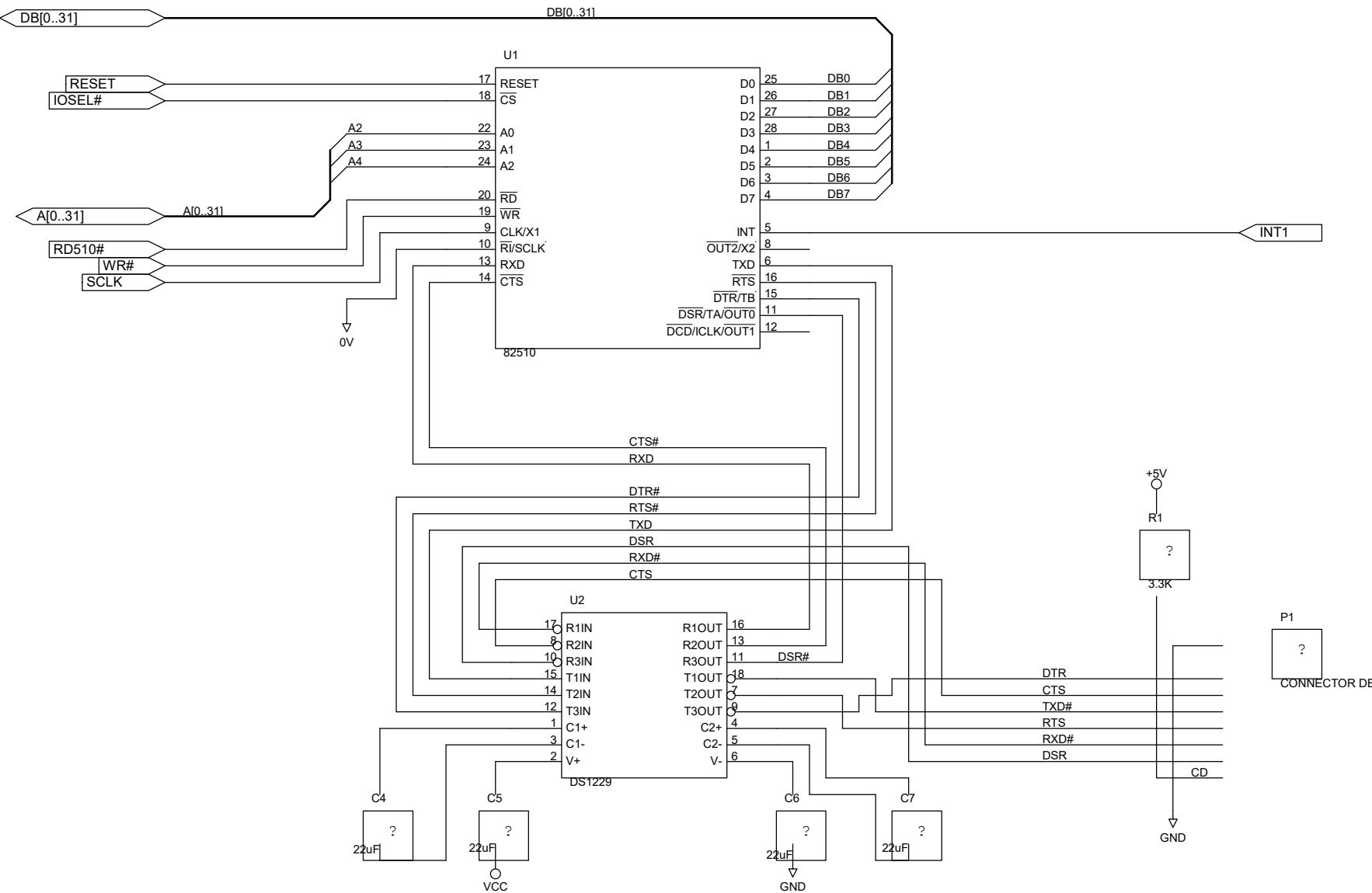
INTEL CORPORATION			
Title	Document Number	Designed by	REV
Headers		Brent Bolton	2.1
Date: February 22, 1989	Sheet 16 of 27		



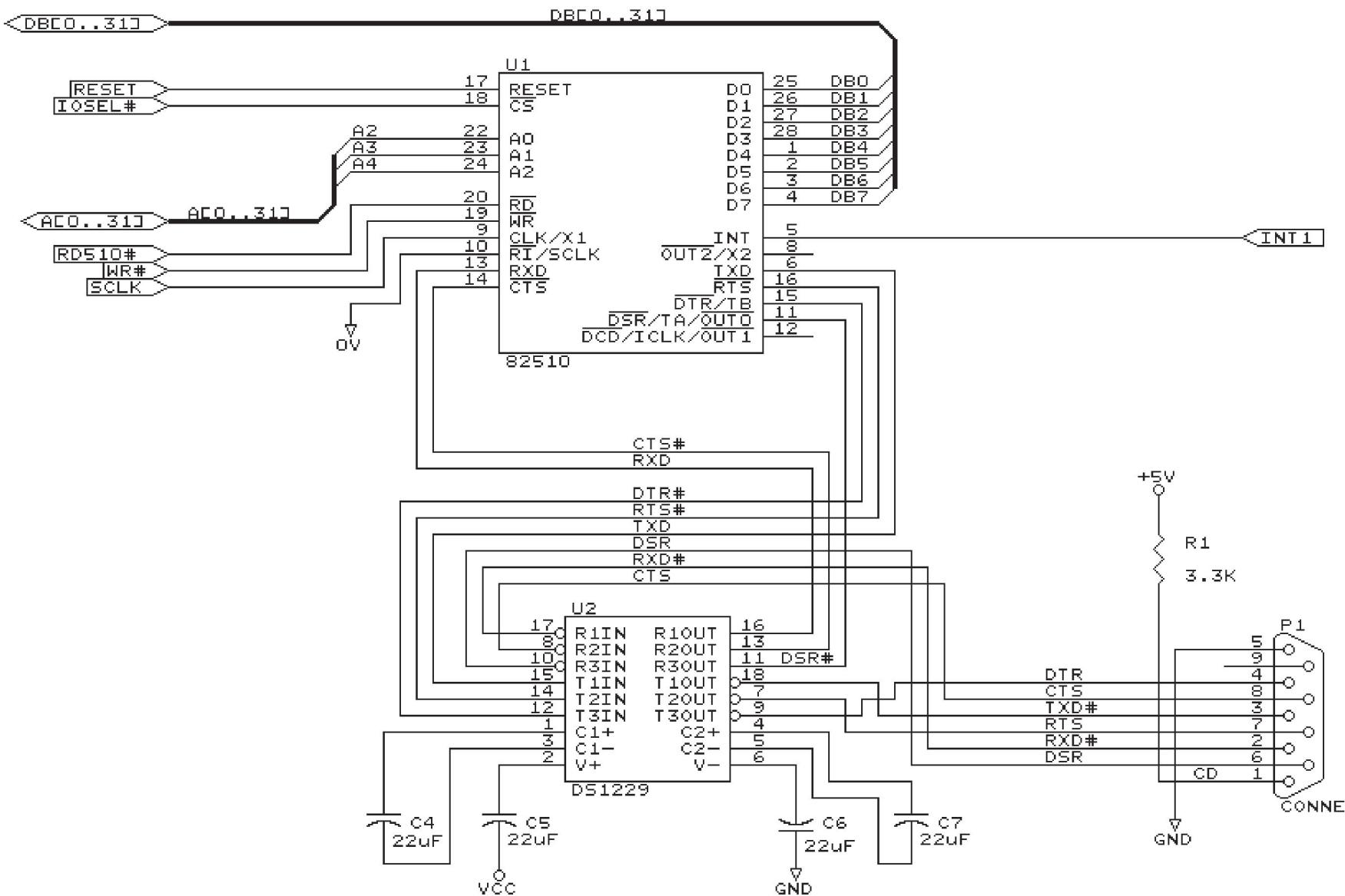
INTEL CORPORATION Wire Wrap Posts		Filename wwposts.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 17 of 27 sheets	



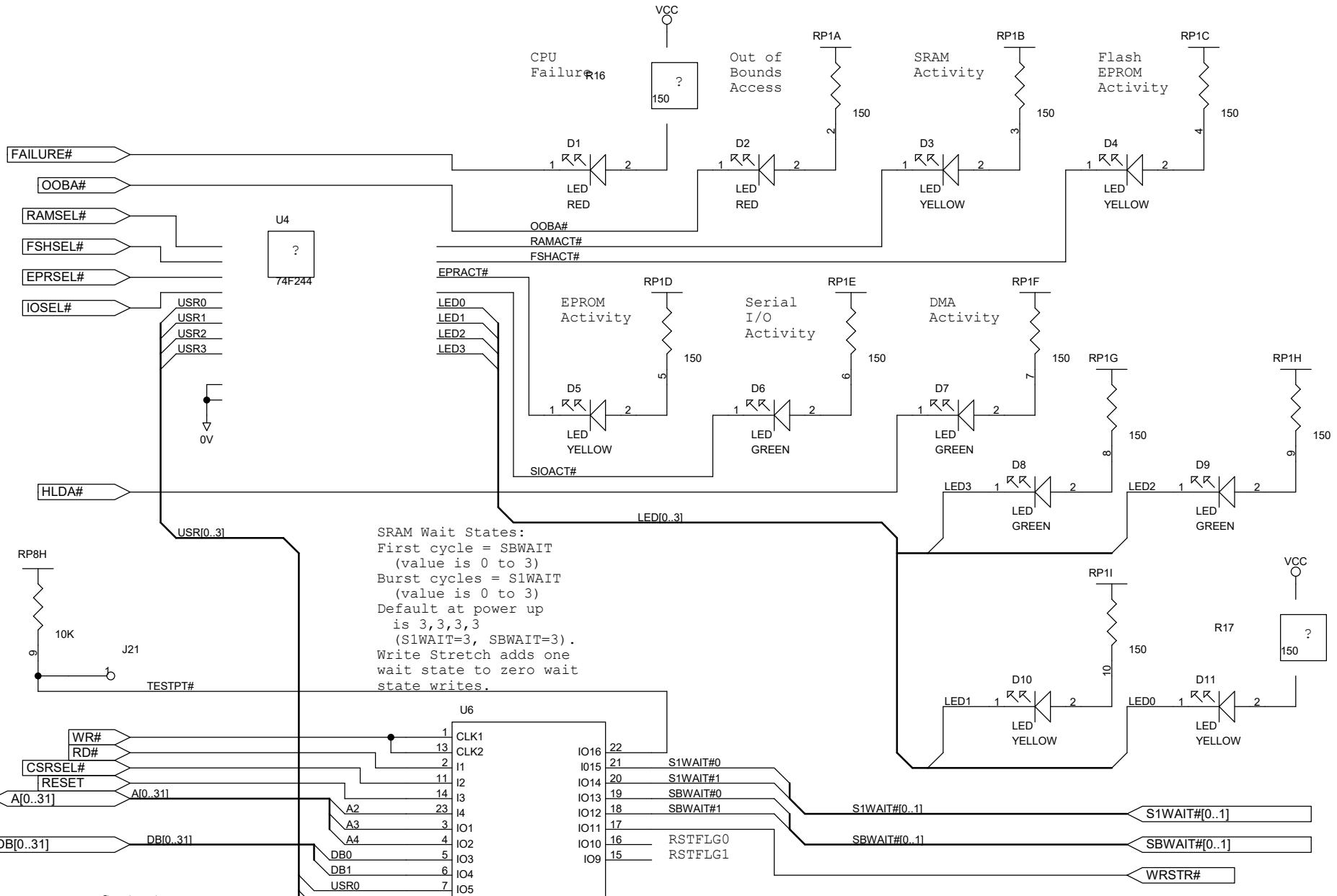
INTEL CORPORATION I/O Subsystem		Filename i_o.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 18 of 27 sheets



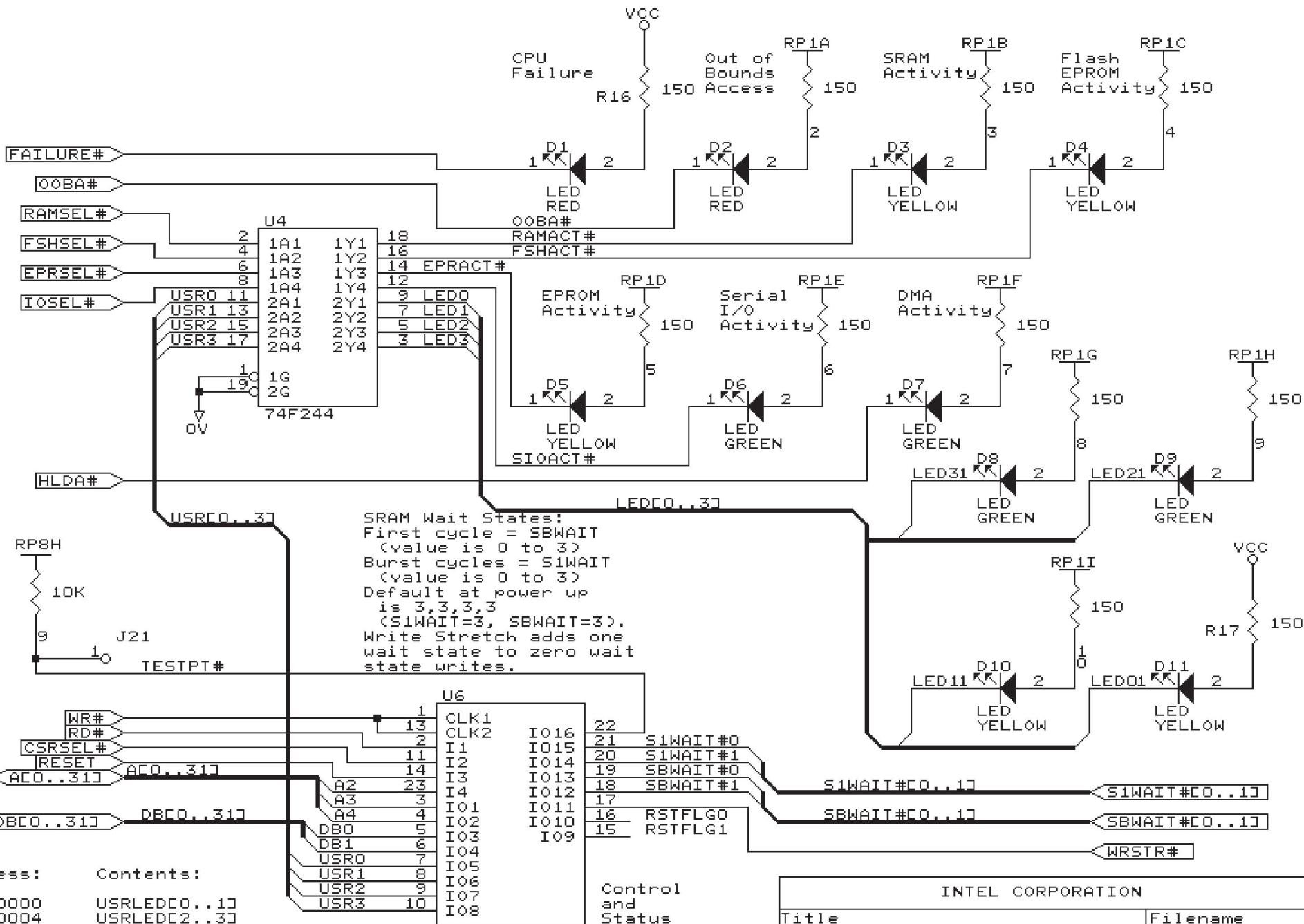
INTEL CORPORATION Serial Controller		Filename sercon.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 19 of 27 sheets	

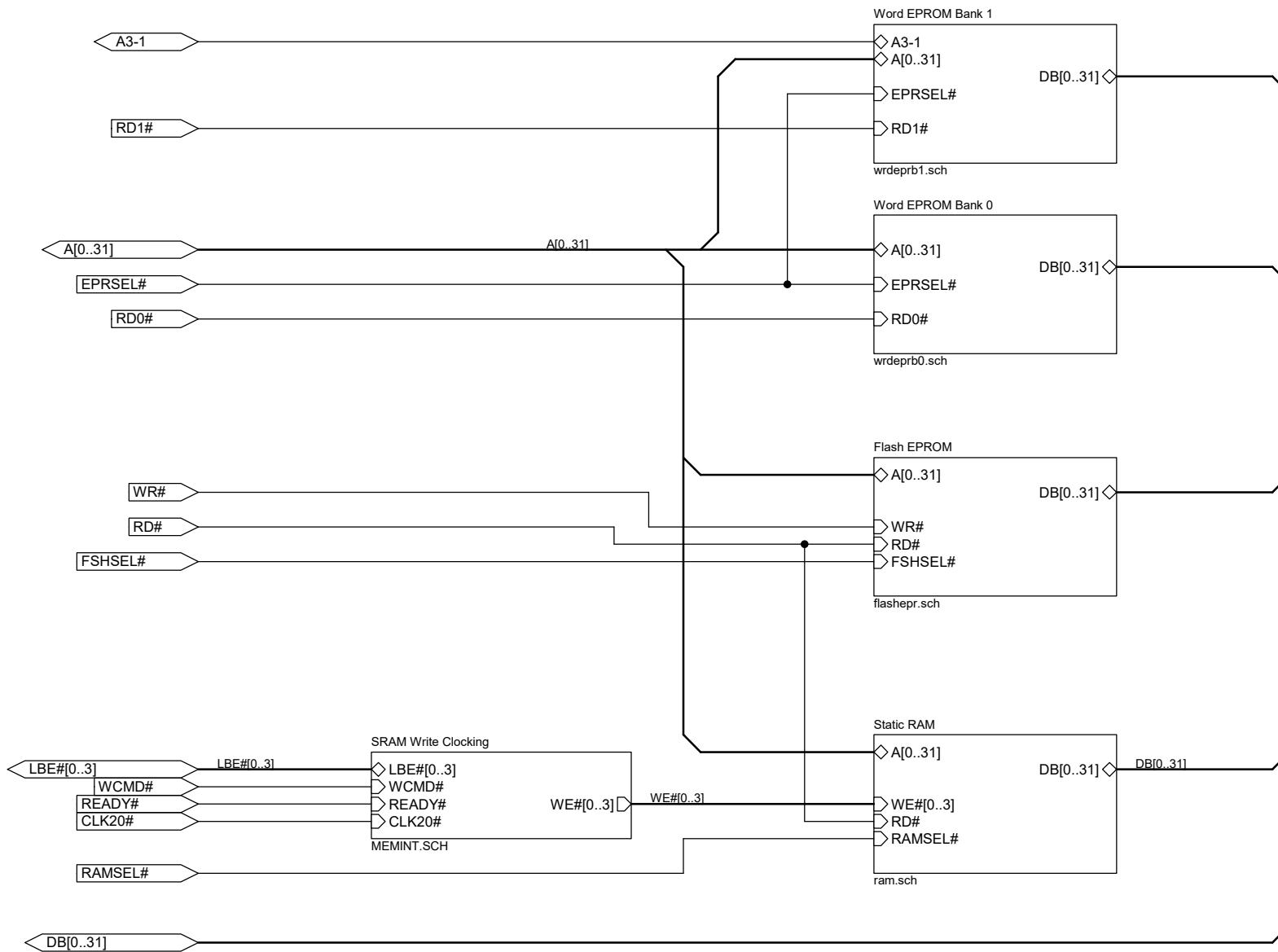


INTEL CORPORATION			
Title		Filename	
Serial Controller		sercon.sch	
Size	Document Number	Designed by	REV
A		Brent Bolton	2.1
Date: February 22, 1989	Sheet 19 of 27		

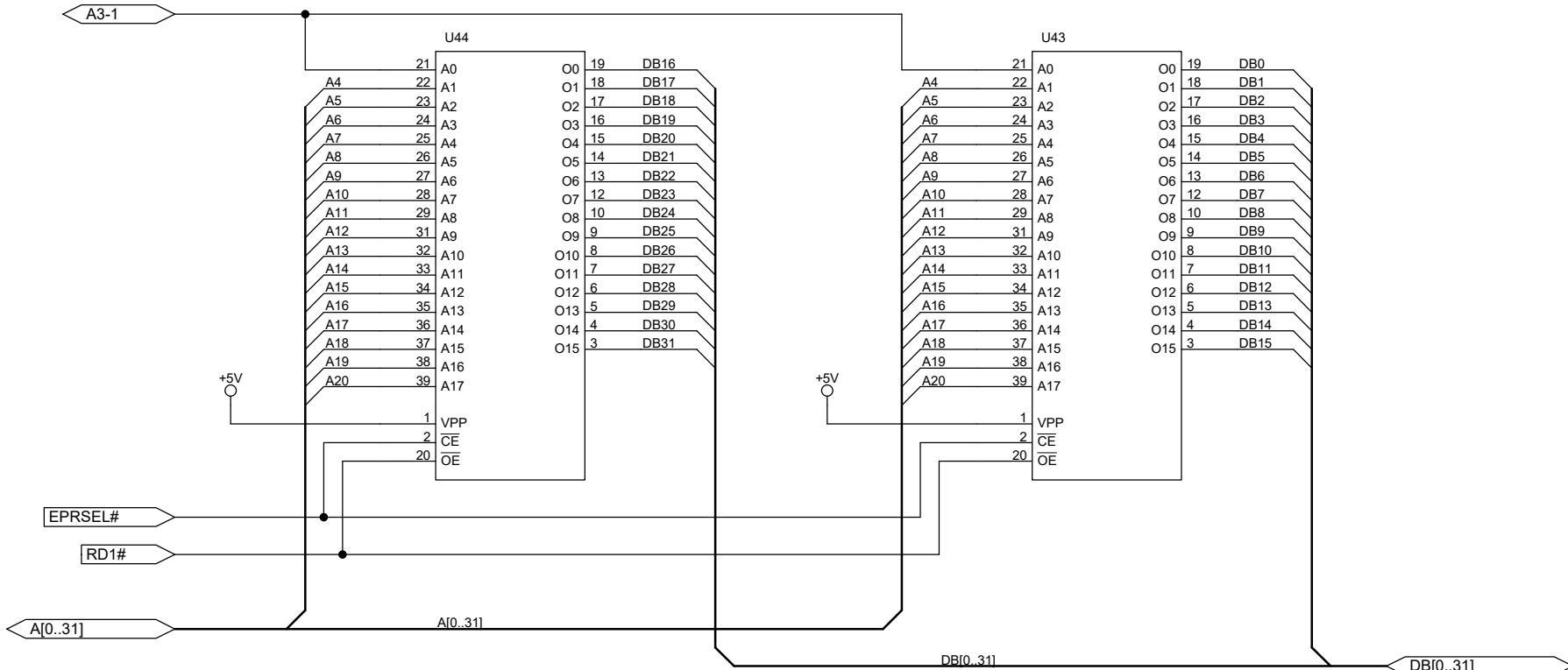


INTEL CORPORATION CSR's and LED's		Filename csr.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 20 of 27 sheets

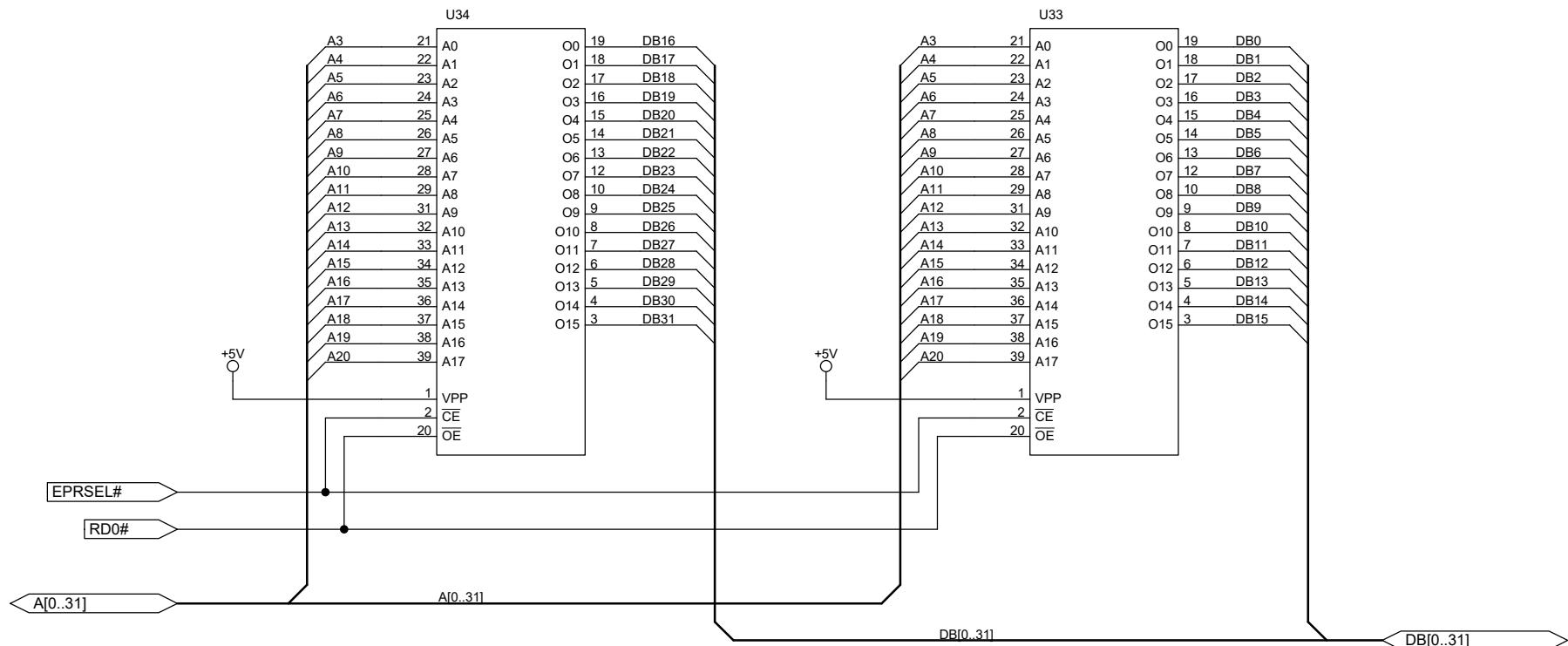




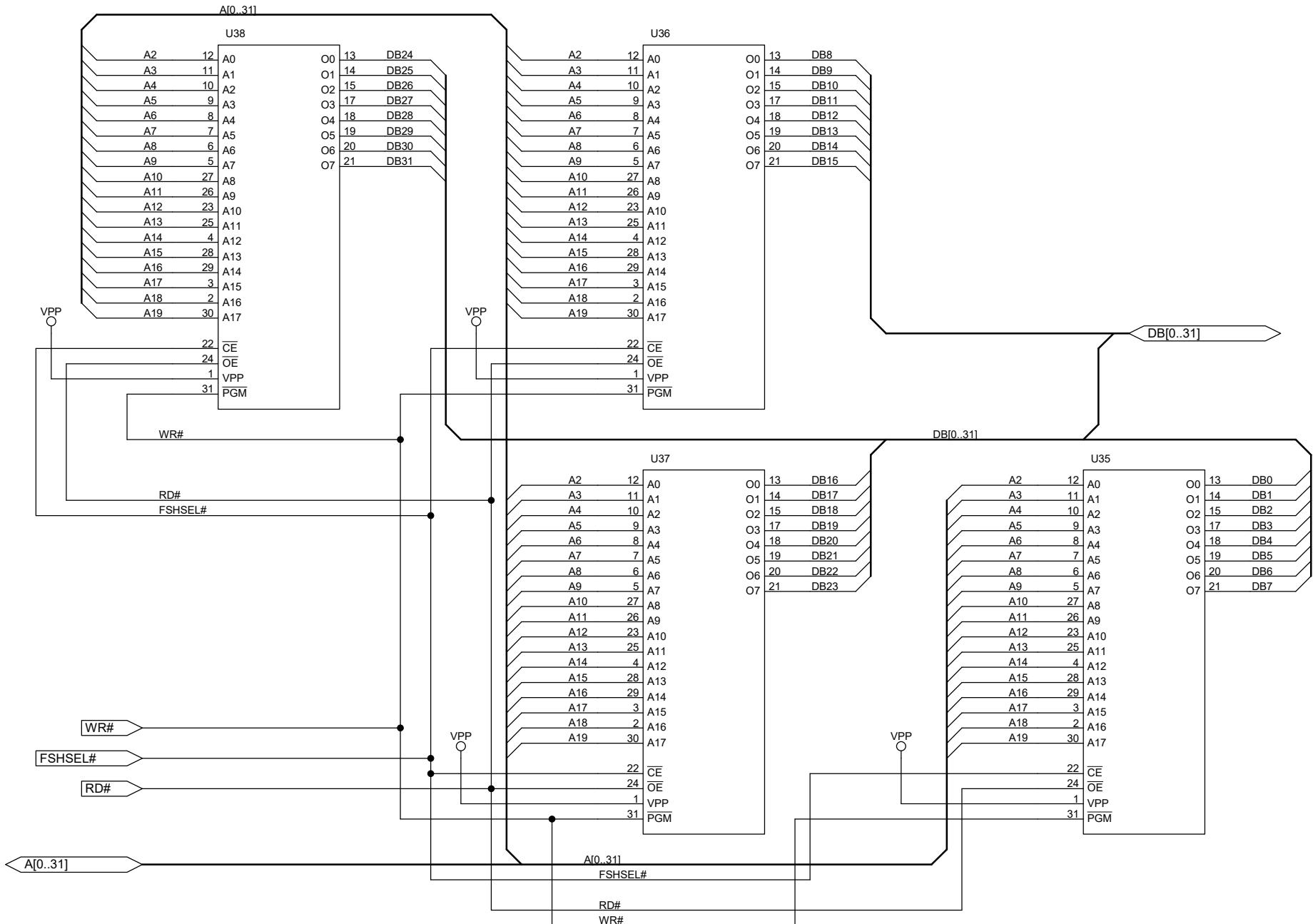
INTEL CORPORATION Memory Subsystem		Filename mem.sch
Title		
	Designed by Brent Bolton	
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 21 of 27 sheets



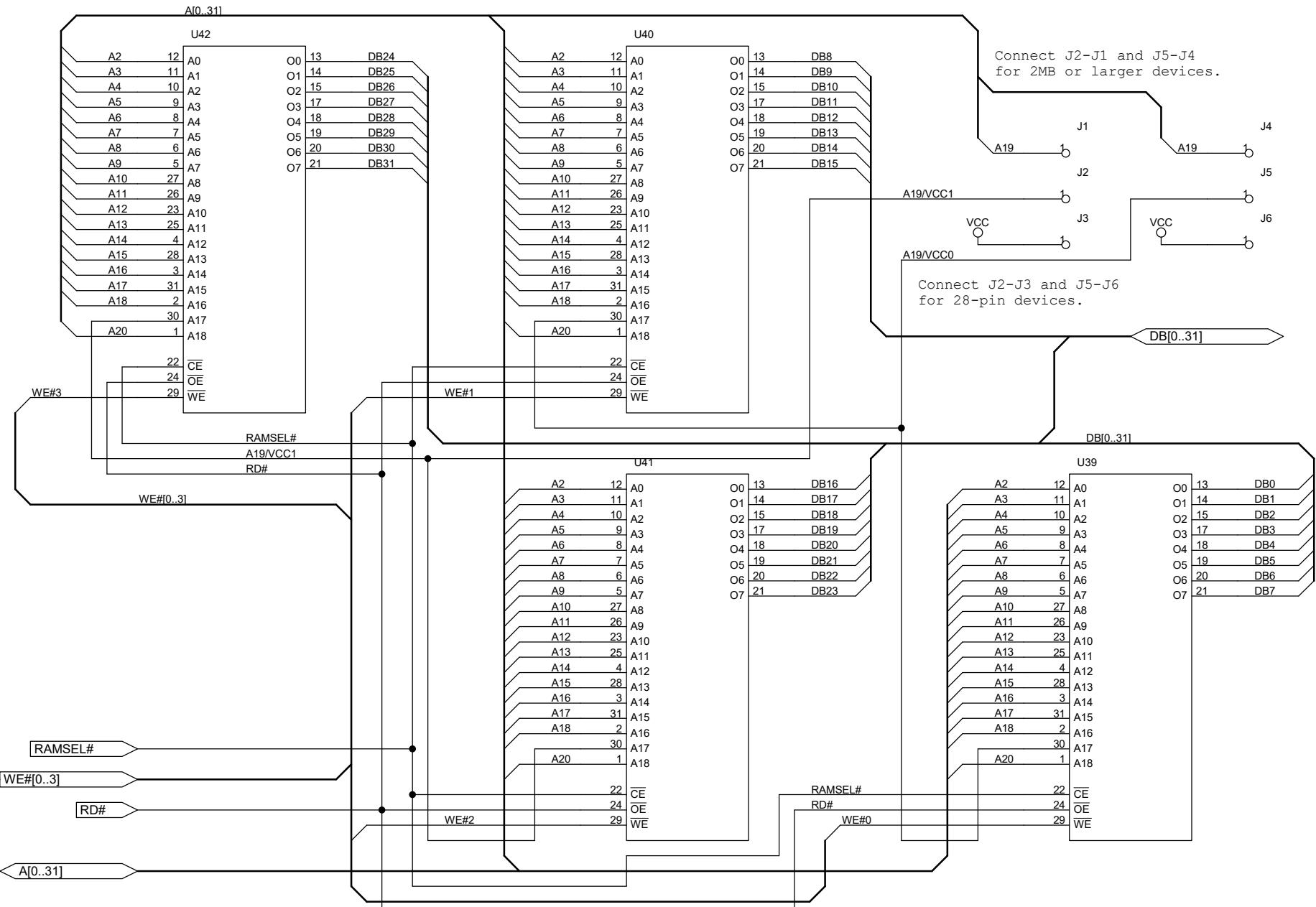
INTEL CORPORATION Word-wide EPROM Bank 1		Filename <code>wrdeprbl.sch</code>
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 22 of 27 sheets	



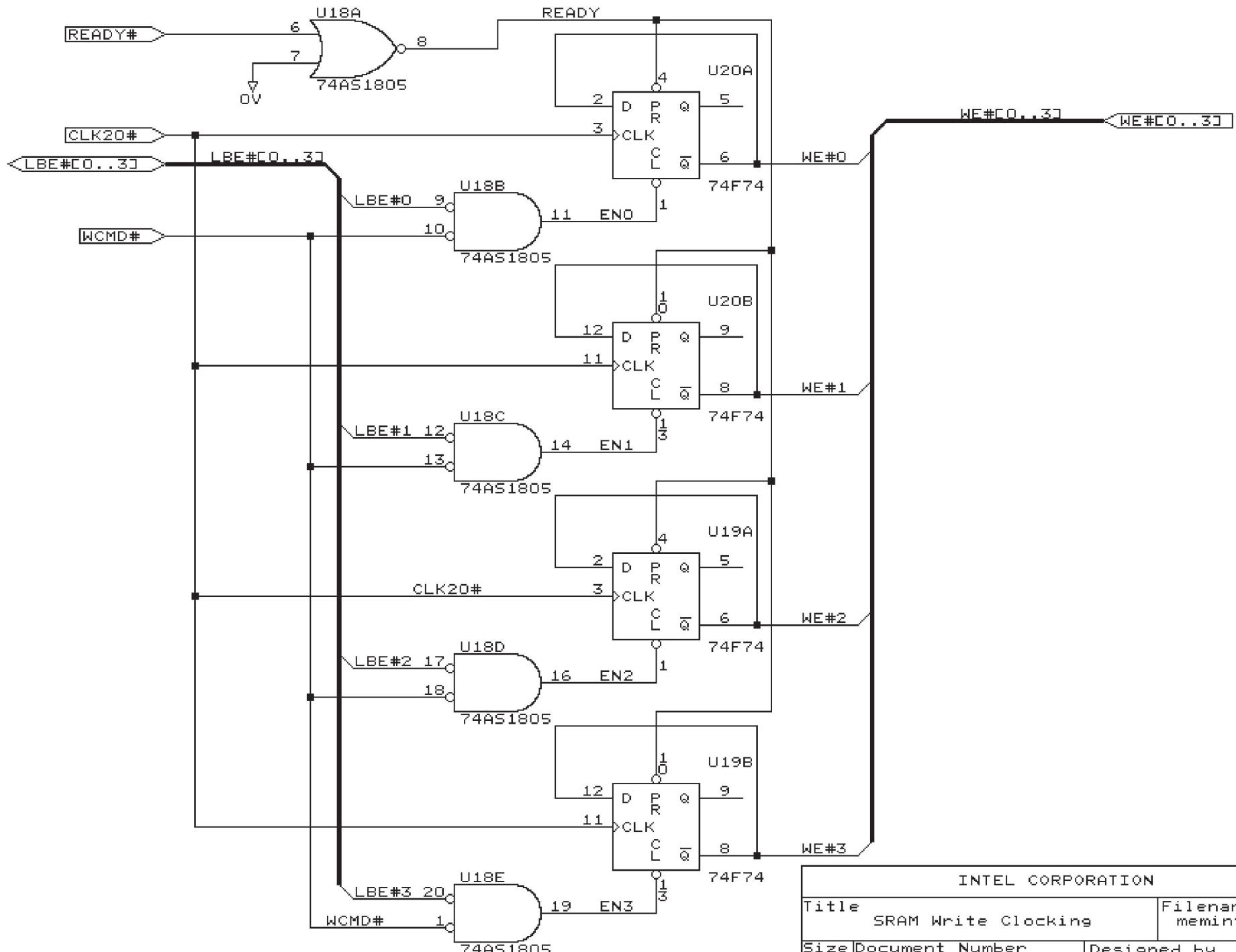
INTEL CORPORATION Word-wide EPROM Bank 0		Filename wrdeprb0.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989	Sheet: 23 of 27 sheets	



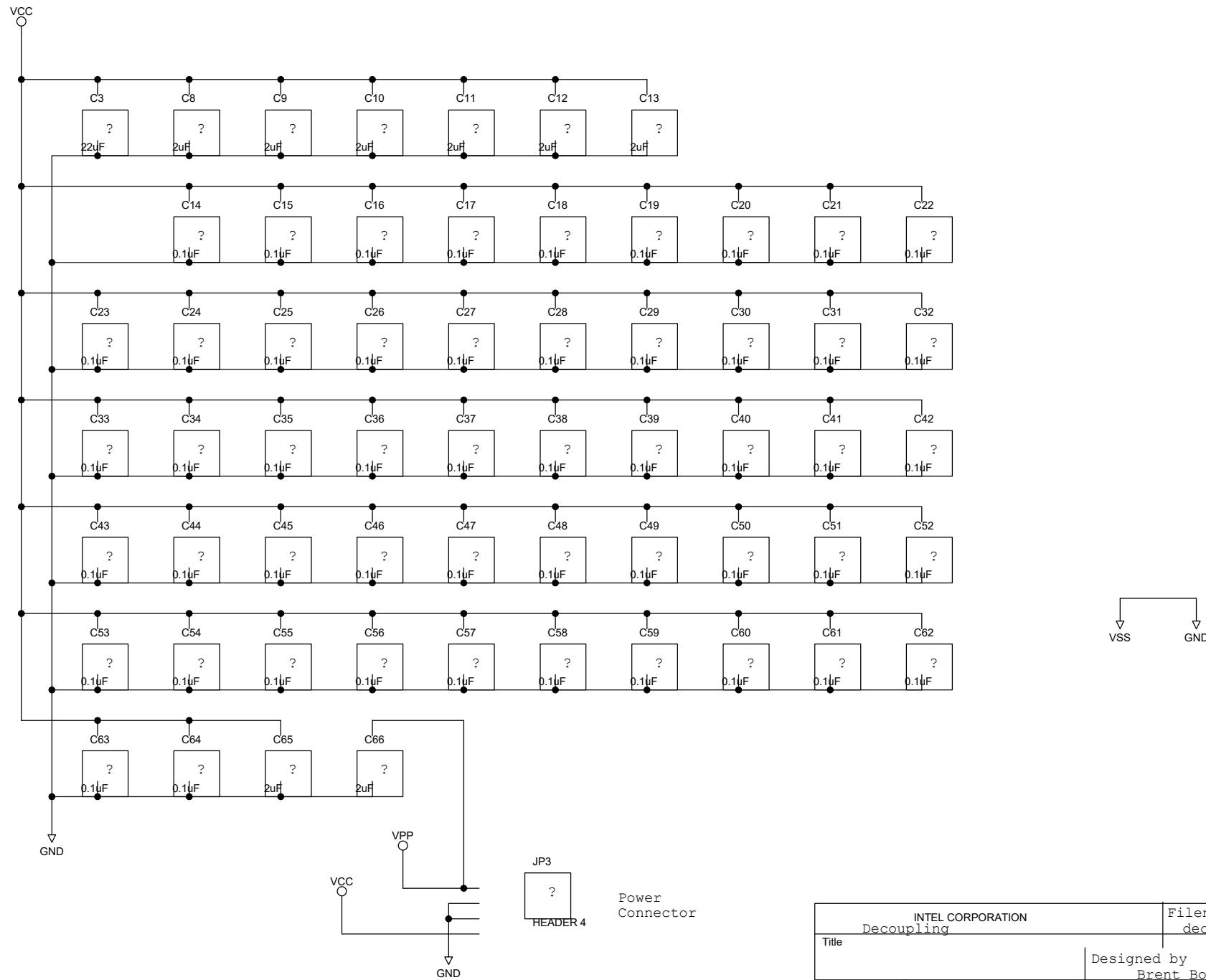
INTEL CORPORATION Flash EPROM		Filename flashepr.sch
Title		
	Designed by Brent Bolton	
Size A	Document Number	Rev 2.2
Date: January 22, 1990		Sheet: 24 of 27 sheets

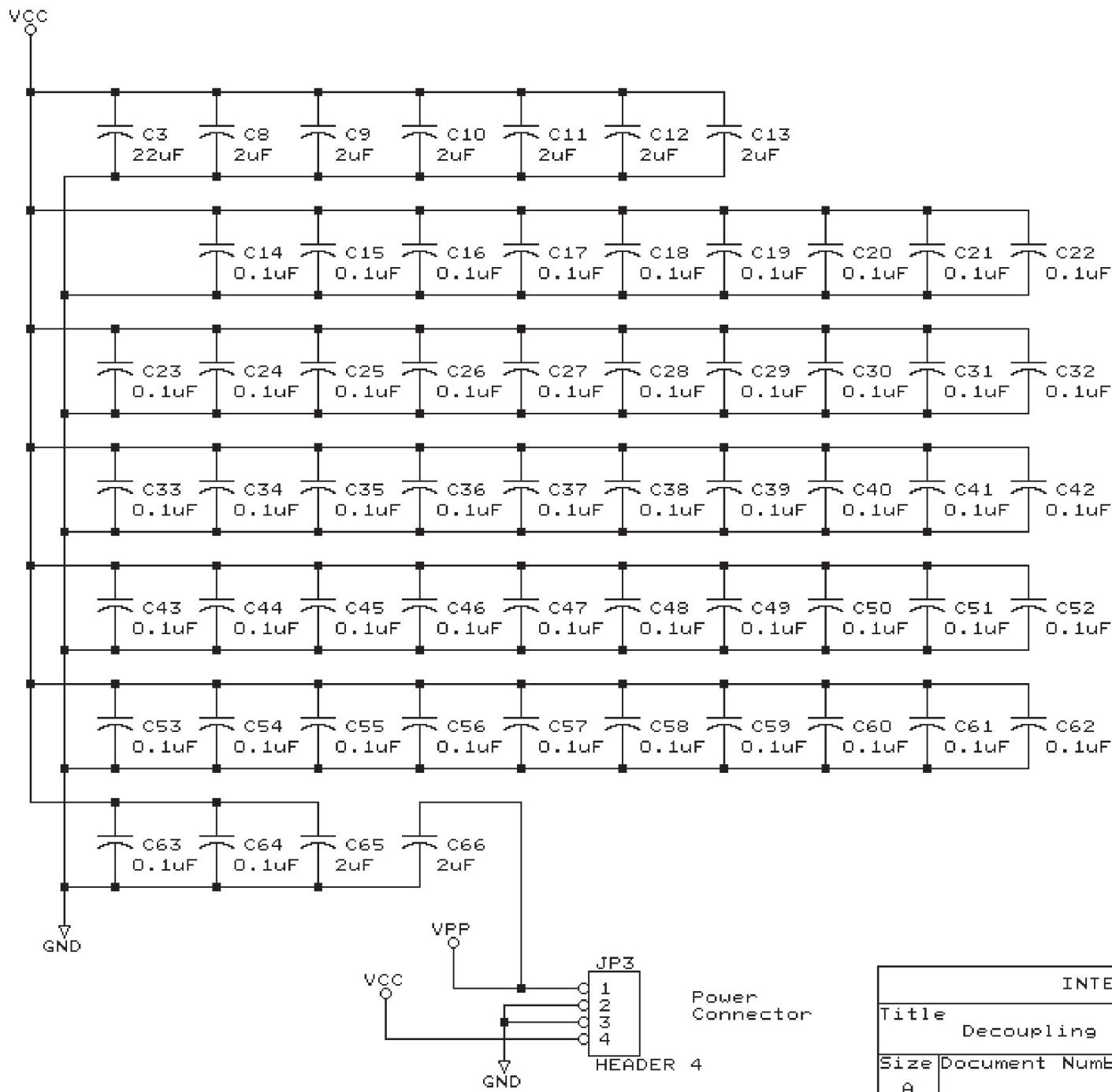


INTEL CORPORATION Static RAM		Filename ram.sch
Title		Designed by Brent Bolton
Size A	Document Number	Rev 2.1
Date: February 22, 1989		Sheet: 25 of 27 sheets



INTEL CORPORATION			
Title		Filename	
Size		Document Number	Designed by
A			Brent Bolton
			REV 2.1
Date:	February 22, 1989	Sheet	26 of 27





INTEL CORPORATION			
Title		Filename	
Decoupling		decap0.sch	
Size	Document Number	Designed by	REV
A		Brent Bolton	2.2
Date:	January 22, 1990	Sheet	27 of 27