FET Biasing

MOSFETs

- Be able to perform a dc analysis of JFET, MOSFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations

MOSFETs

- For the field-effect transistor, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation.
- A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers
- Since the graphical approach is in general the most popular, the analysis of this chapter will have graphical solutions rather than mathematical solutions.

The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

FETs Biasing

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\ \text{A}$$

$$I_D = I_S$$

For JFETs

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs

$$I_D = k(V_{GS} - V_T)^2$$

- It is particularly important to realize that all of the equations above are for the field effect transistor only !
- They do not change with each network configuration so long as the device is in the active region.
- The network simply defines the level of current and voltage associated with the operating point through its own set of equations.
- **In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network**

FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the n -channel JFET

Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach.

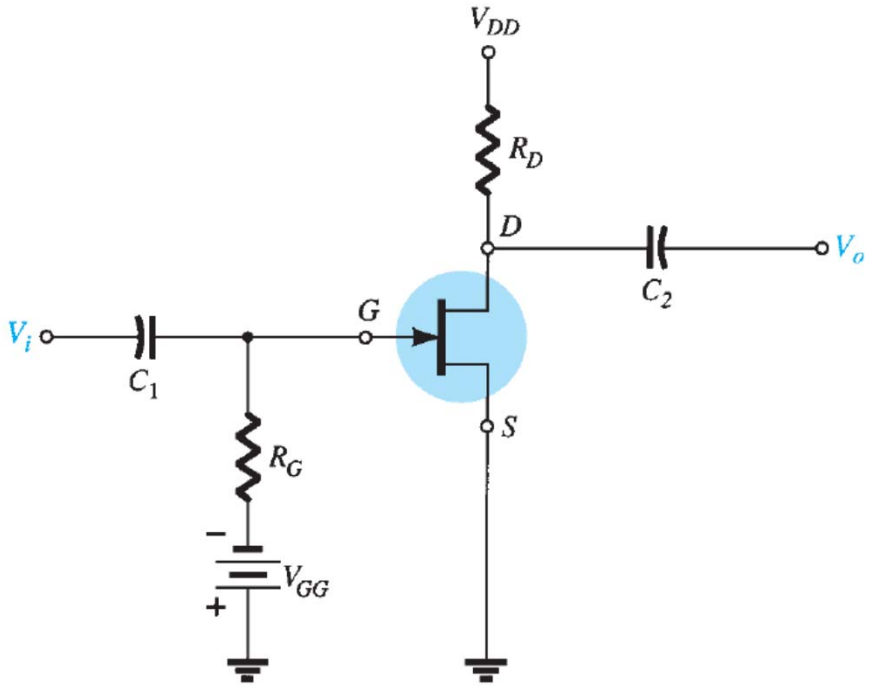


FIG. 7.1
Fixed-bias configuration.

FIXED-BIAS CONFIGURATION

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

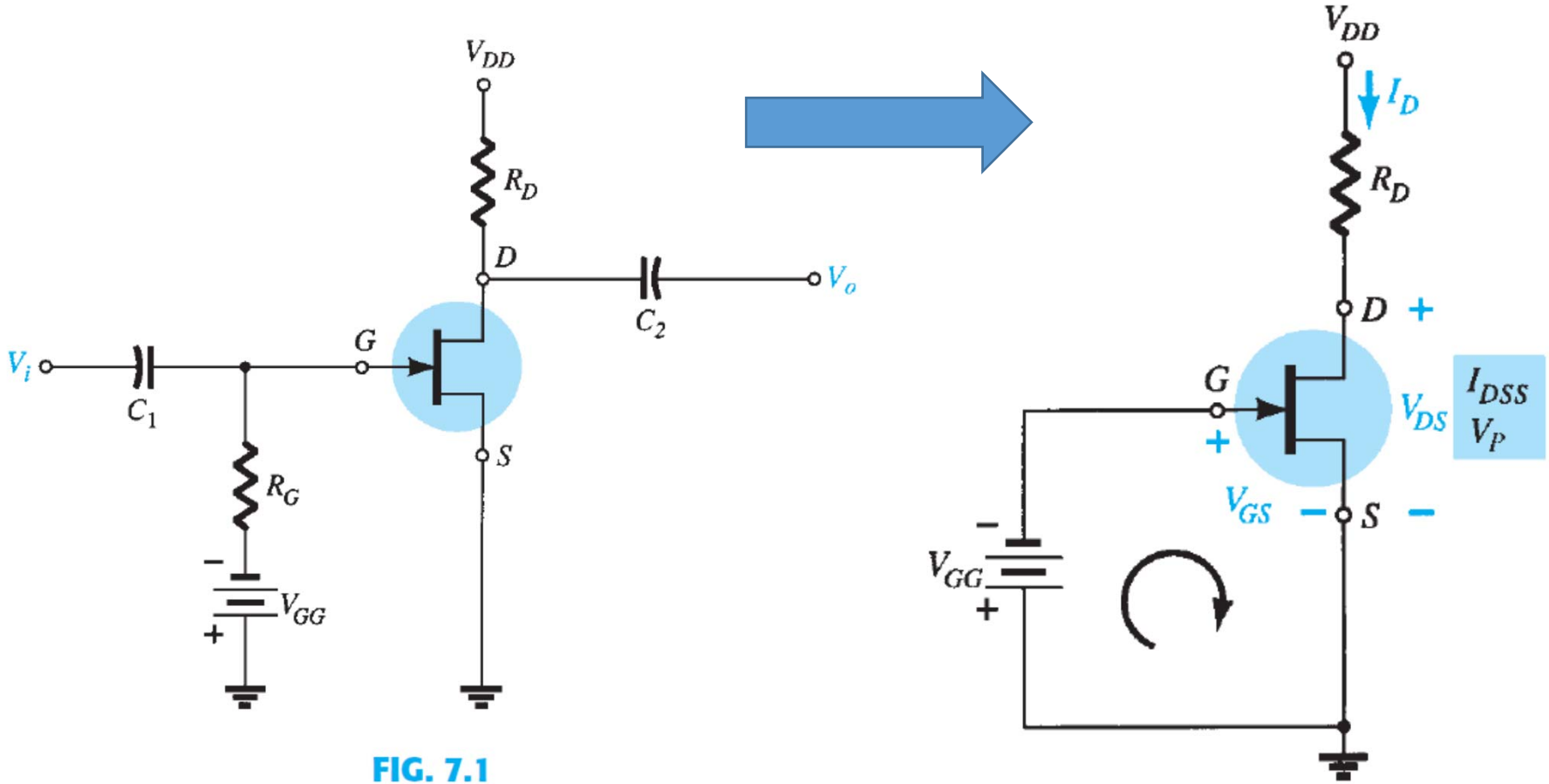
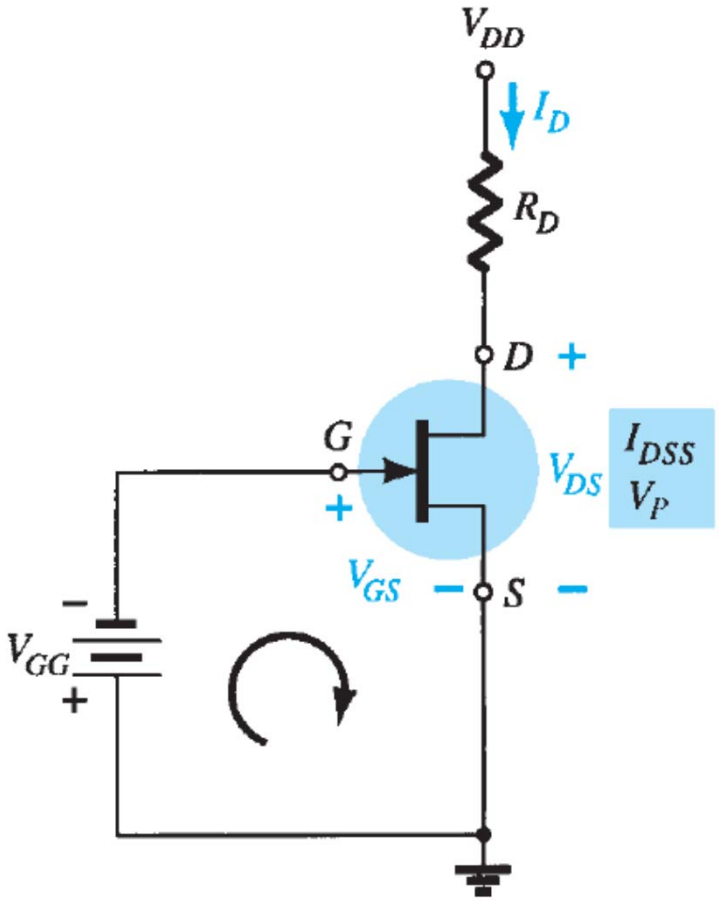


FIG. 7.1
Fixed-bias configuration.

FIXED-BIAS CONFIGURATION

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$



Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop

$$-V_{GG} - V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

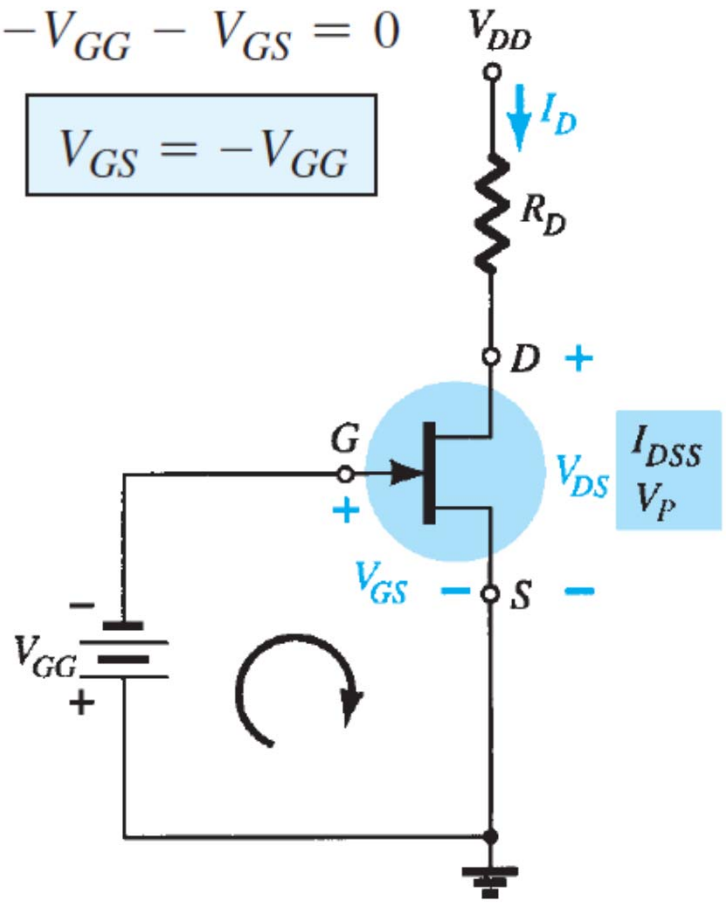
FIXED-BIAS CONFIGURATION

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$



The resulting level of drain current I_D is now controlled by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_D = ?

mathematical solution to a FET configuration

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated.

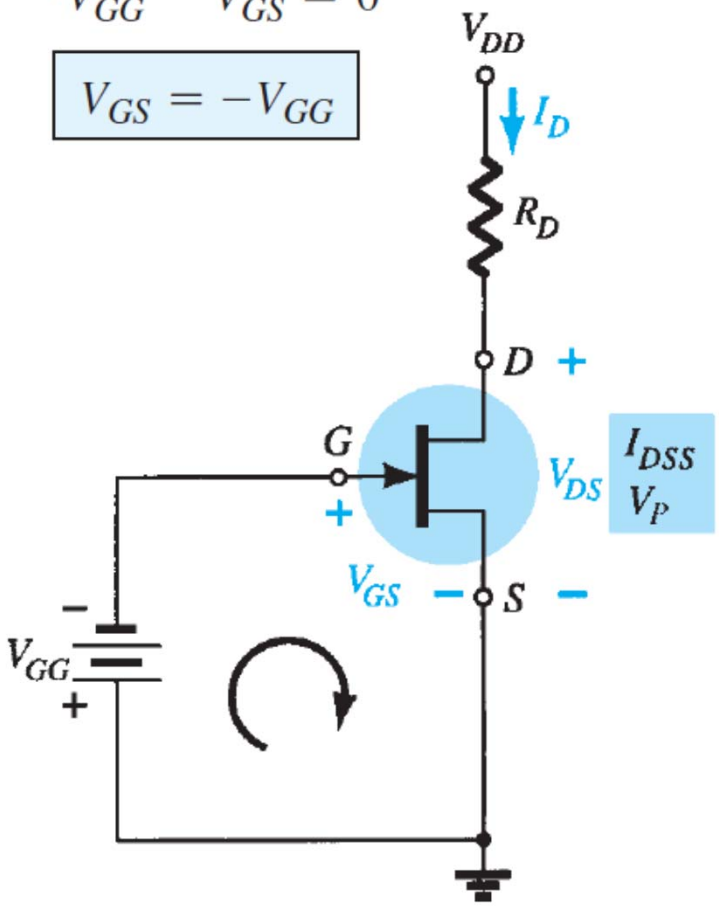
FIXED-BIAS CONFIGURATION

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

$$-V_{GG} - V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$



The resulting level of drain current I D is now controlled by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

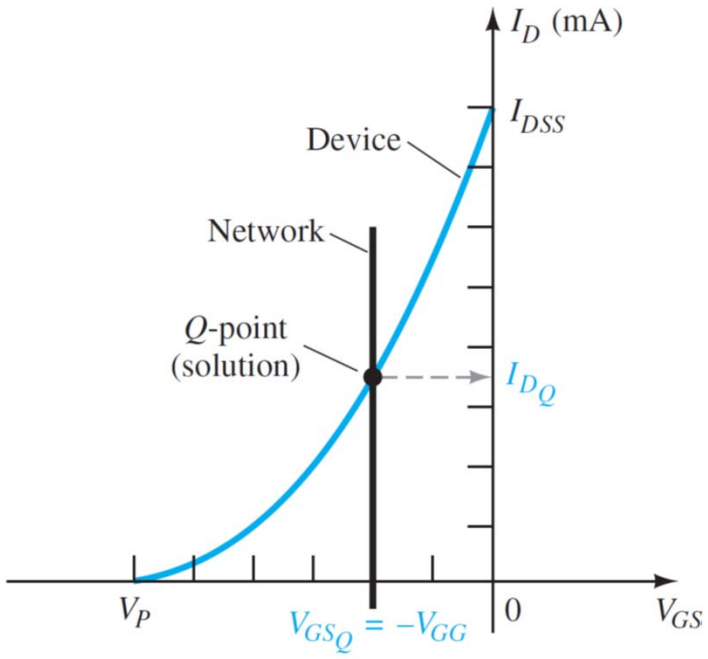


FIG. 7.4
Finding the solution for the fixed-bias configuration.

FIXED-BIAS CONFIGURATION

The dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 7.5

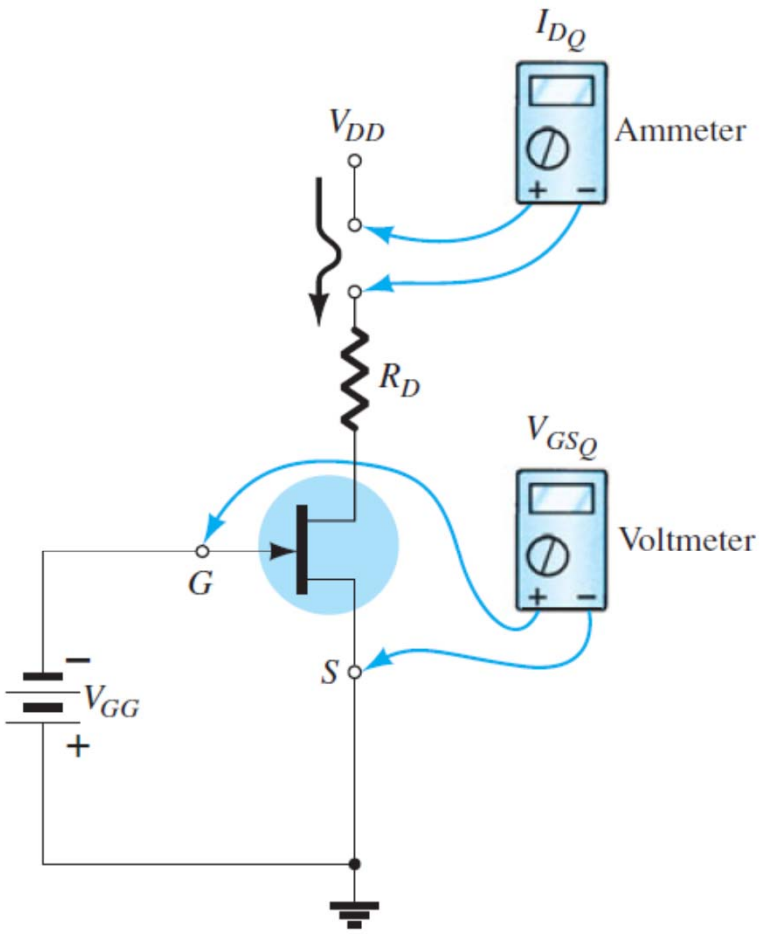


FIG. 7.5
Measuring the quiescent values of I_D and V_{GS}.

Drain-to-source voltage of the output section

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

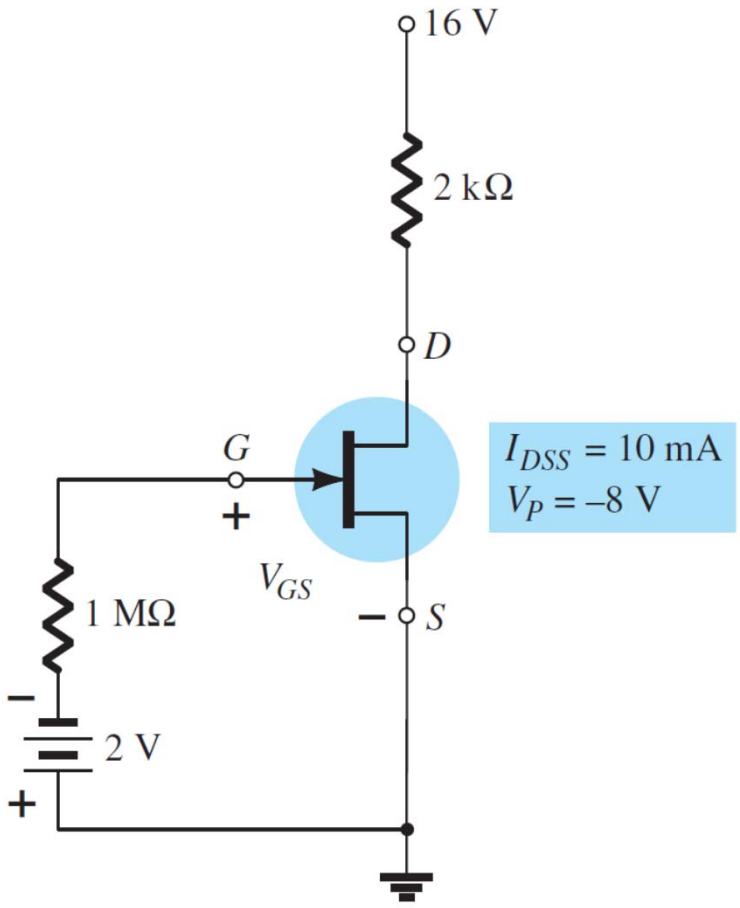
$$V_S = 0\ \text{V}$$

$$V_D = V_{DS}$$

$$V_G = V_{GS}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V

FIXED-BIAS CONFIGURATION



Determine the following for the network

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

FIXED-BIAS CONFIGURATION

Determine the following for the network

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
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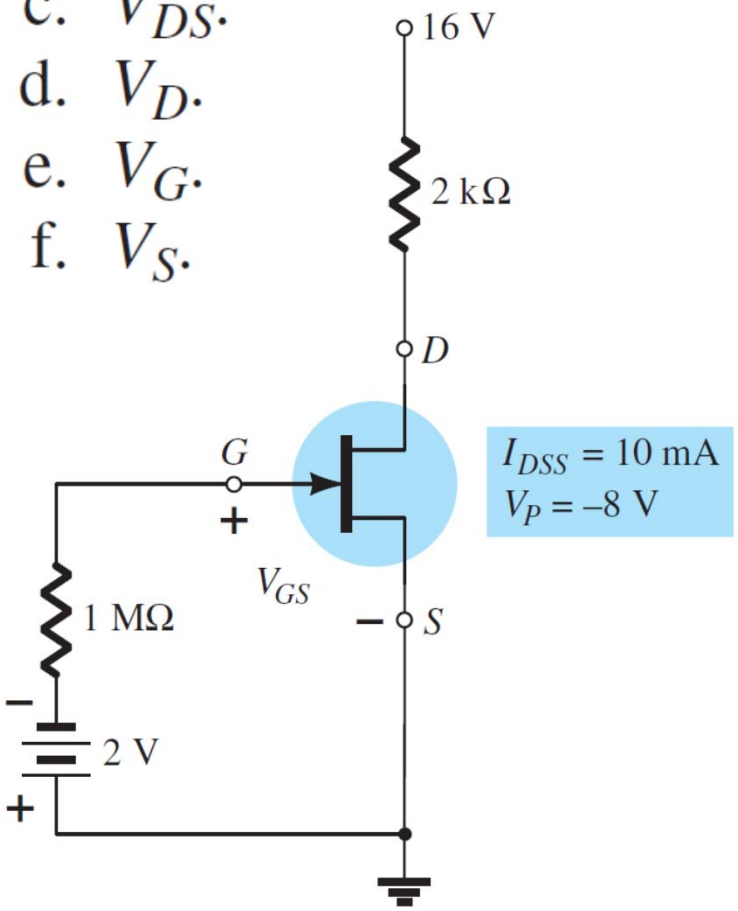
f. V_S.



Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$
$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$
$= \mathbf{5.625\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

How about Graphical Approach?

Graphical Approach

The resulting Shockley curve and the vertical line at V_{GS} = -2 V

a. Therefore,

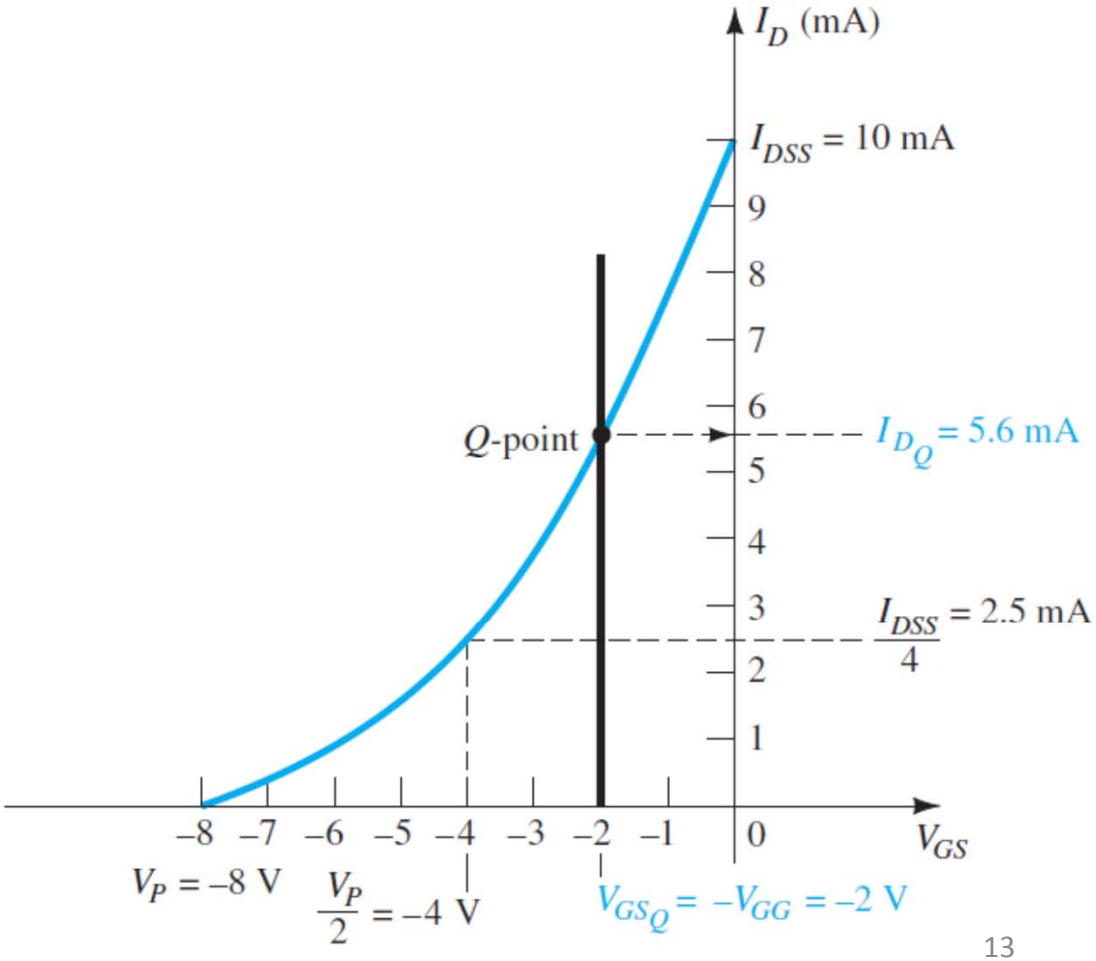
b. $I_{D_Q} = \mathbf{5.6\ mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4}$

d. $V_D = V_{DS} = \mathbf{4.8\ V}$

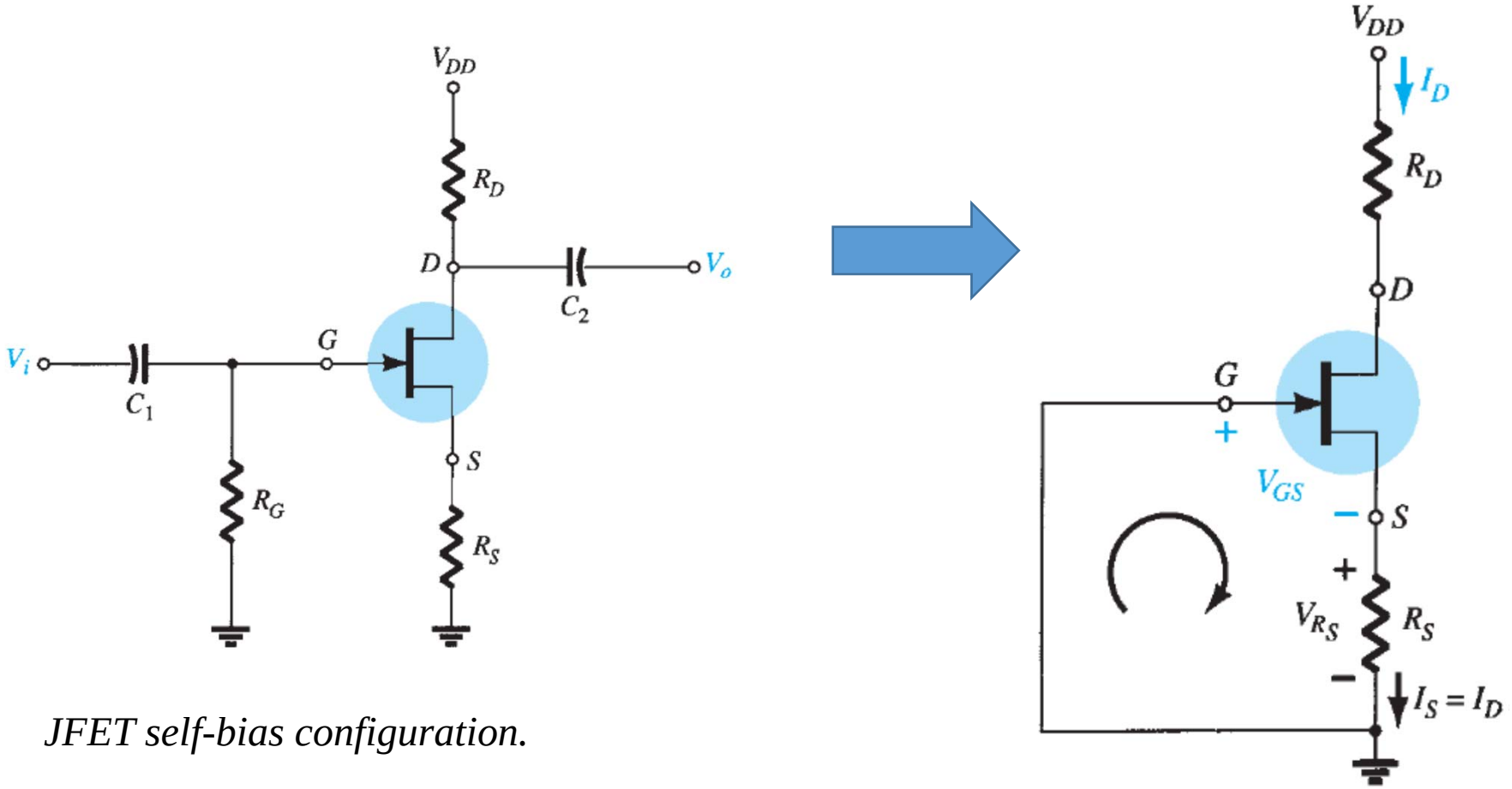
e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$



SELF-BIAS CONFIGURATION

- The self-bias configuration eliminates the need for two dc supplies. The controlling gate to- source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration



JFET self-bias configuration.

SELF-BIAS CONFIGURATION

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

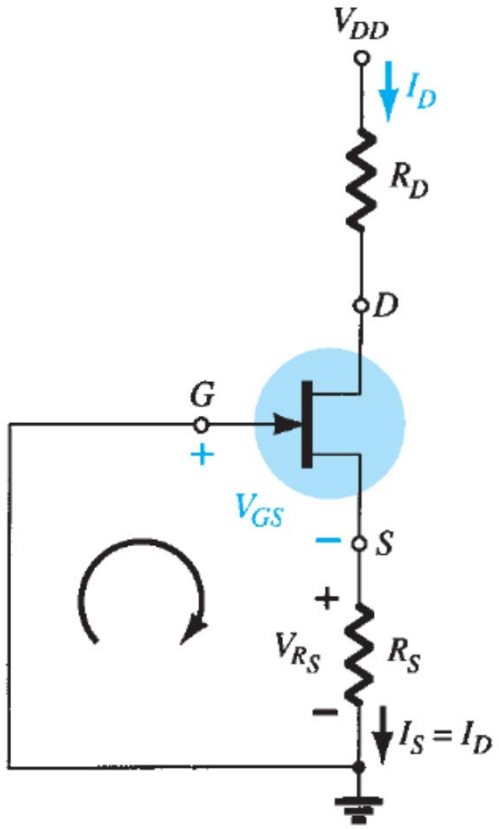
$$I_G = 0 \text{ A}$$

The current through R_S is the source current *IS*, but $I_S = I_D$ and $V_{RS} = I_D R_S$

$$-V_{GS} - V_{R_S} = 0$$

$$V_{GS} = -V_{R_S}$$

$$V_{GS} = -I_D R_S$$



JFET self-bias configuration.

- Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.
- Shockley's equation relates the input and output quantities of the device.
- Both equations relate the same two variables, I_D and V_{GS}, permitting either a mathematical or a graphical solution.

SELF-BIAS CONFIGURATION

A mathematical solution could be obtained simply by substituting into Shockley's equation as follows:

mathematical approach

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

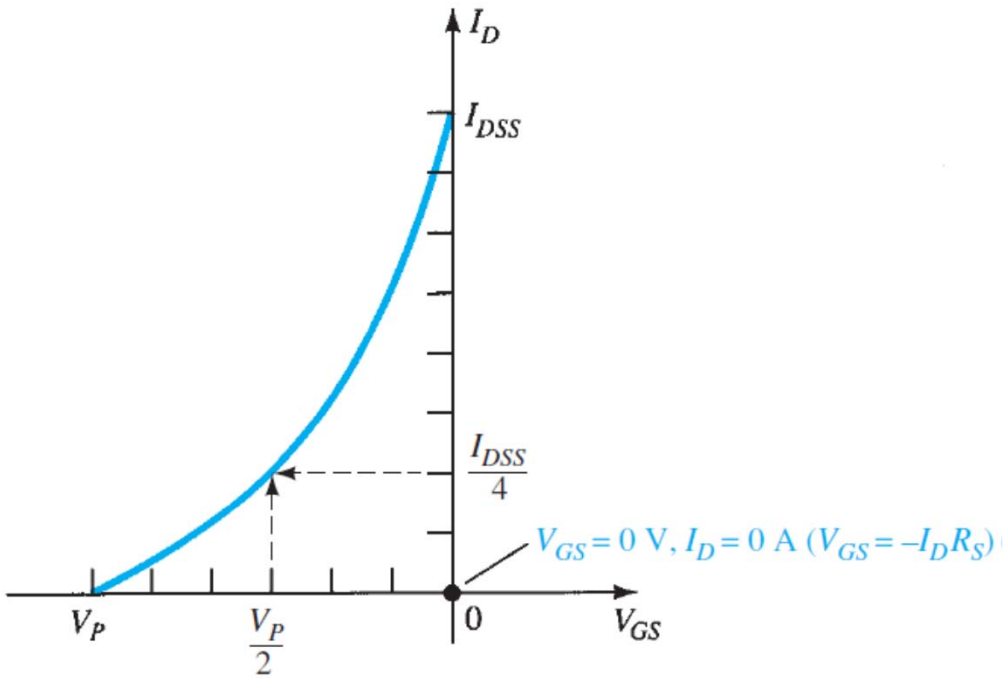
$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

$$I_D^2 + K_1 I_D + K_2 = 0$$

The graphical approach

$$V_{GS} = -I_D R_S$$



SELF-BIAS CONFIGURATION

The graphical approach

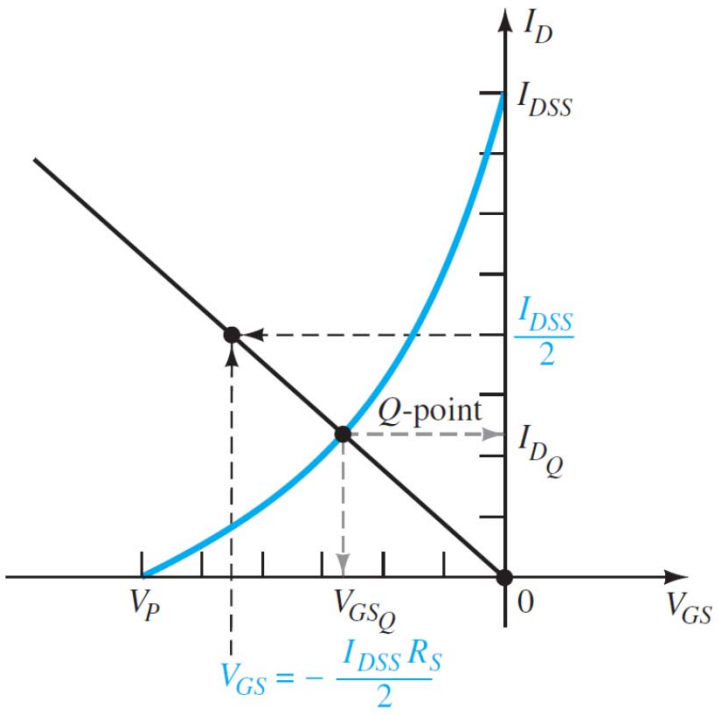
- The second point requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined.
- The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit the drawing of the straight line.

For example, that we choose a level of I_D equal to one-half the saturation level.

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

- The straight line is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve.
- The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest



SELF-BIAS CONFIGURATION

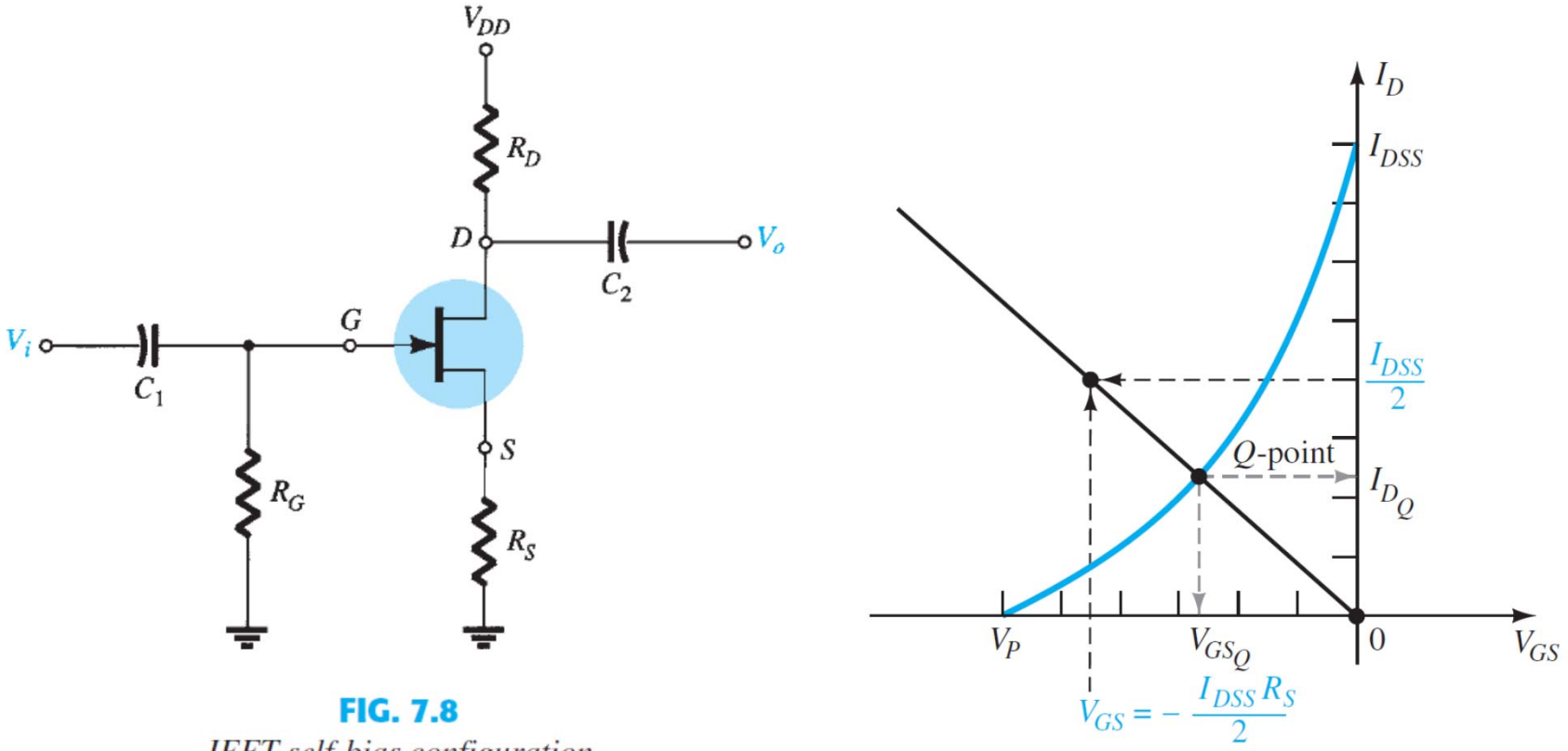


FIG. 7.8
JFET self-bias configuration.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

SELF-BIAS CONFIGURATION

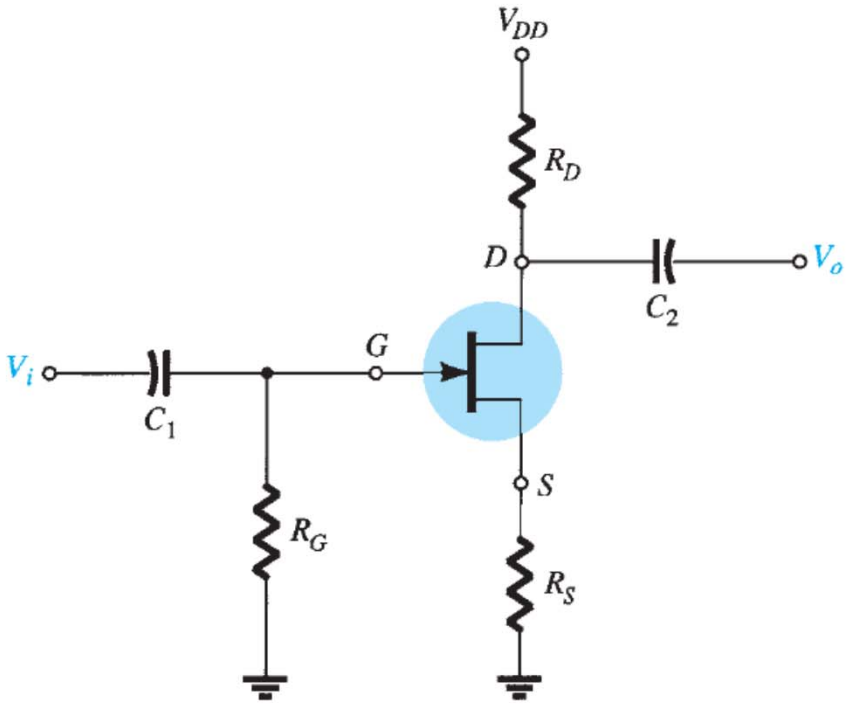


FIG. 7.8
JFET self-bias configuration.

$$I_D = I_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

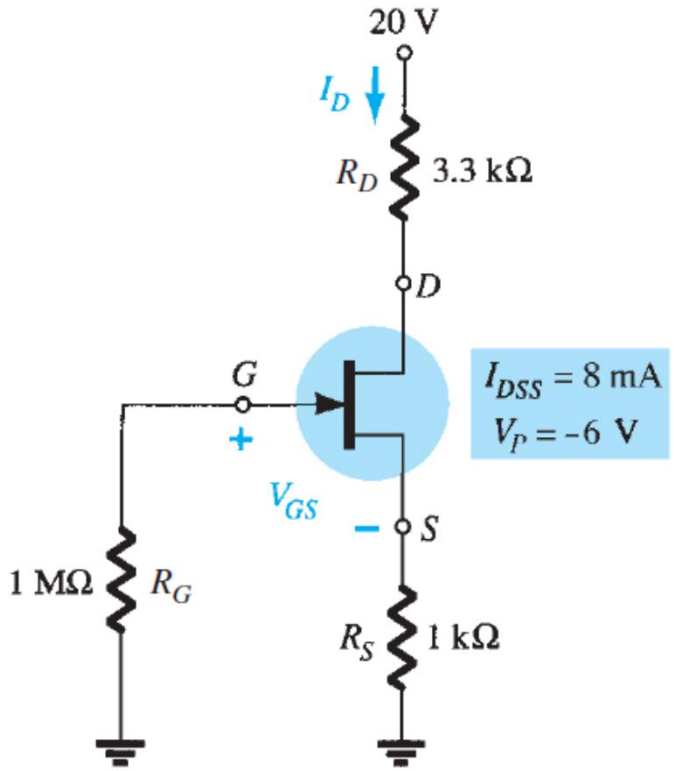
$$V_S = I_D R_S$$

$$V_G = 0\ \text{V}$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

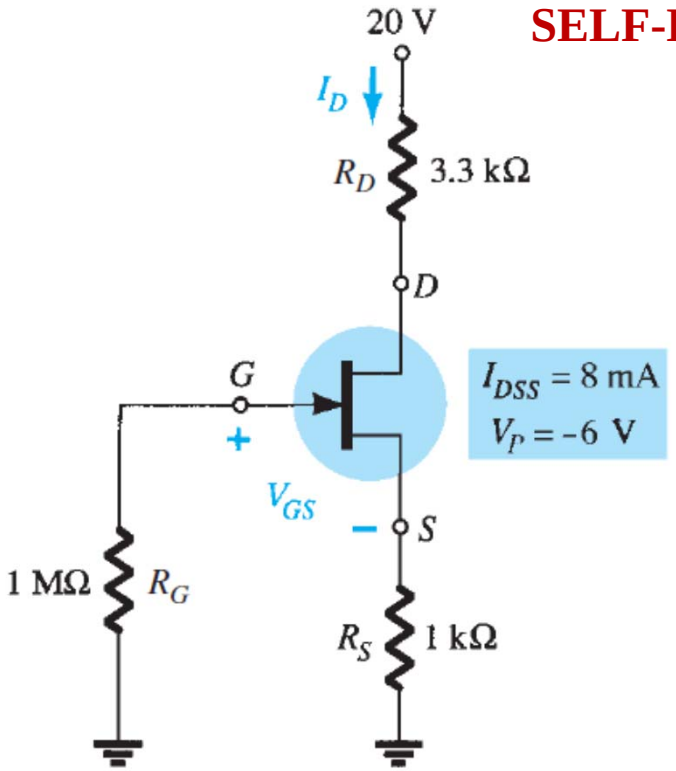
SELF-BIAS CONFIGURATION

Determine the following for the network



a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

SELF-BIAS CONFIGURATION



Determine the following for the network

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

Solution:

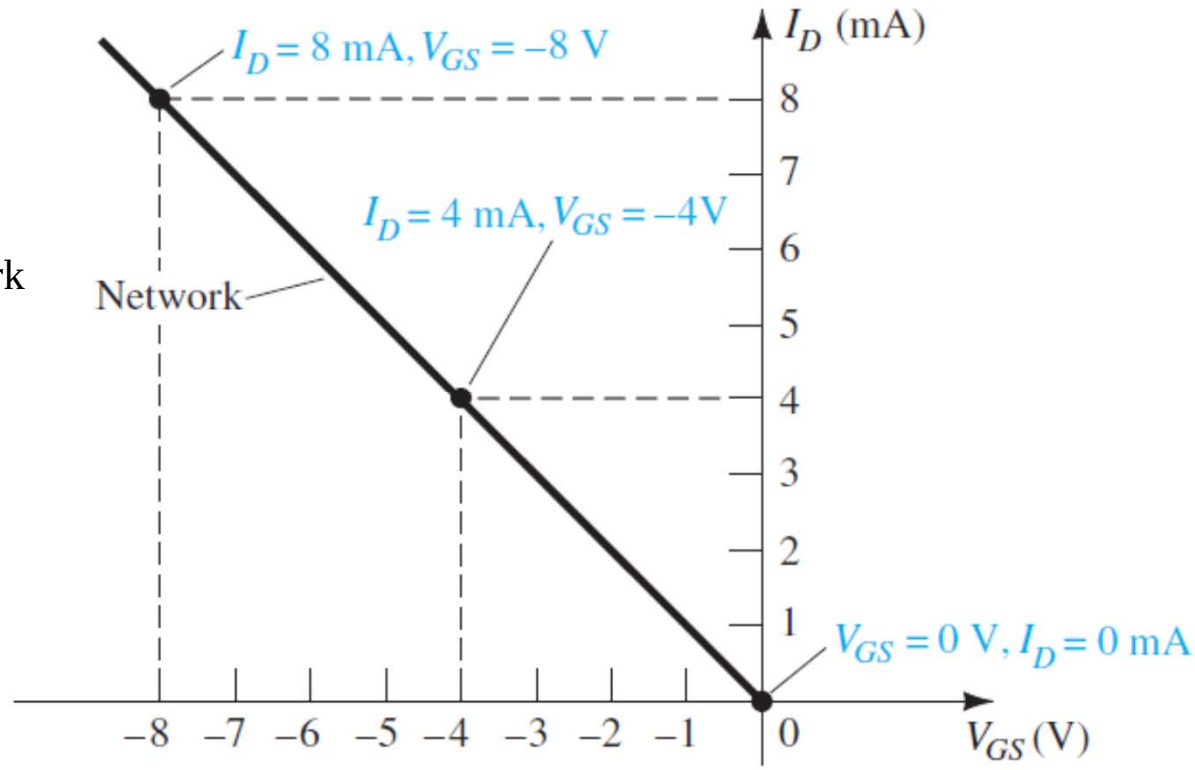
a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

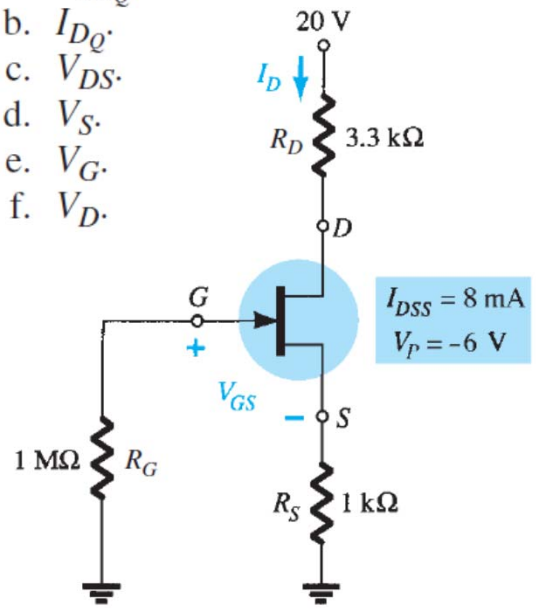
$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

The result is the plot of Fig. 7.13 as defined by the network.



SELF-BIAS CONFIGURATION

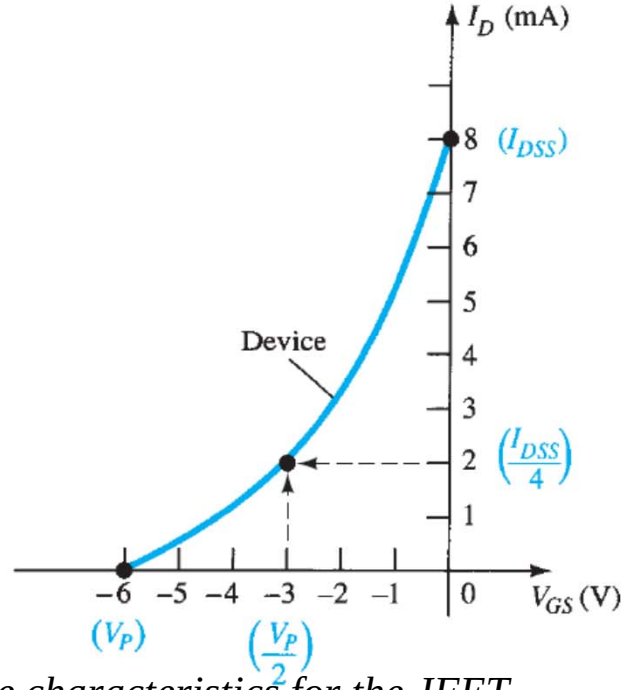
a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.



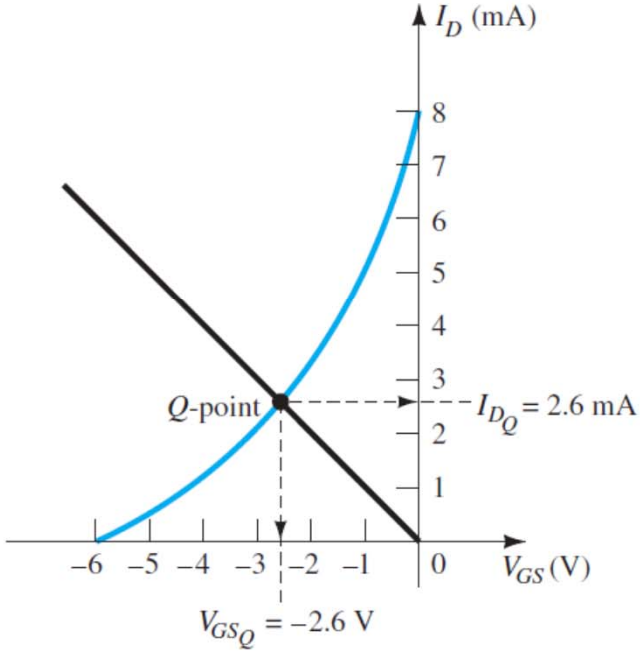
b. At the quiescent point

$$I_{D_Q} = 2.6\ \text{mA}$$

$$V_{GS_Q} = -2.6\ \text{V}$$



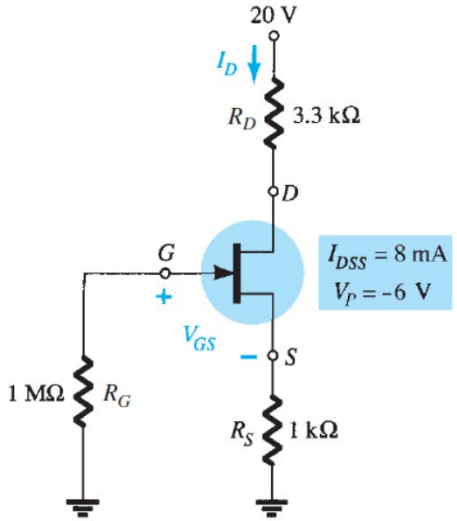
Sketching the device characteristics for the JFET



Determining the Q-point for the network

SELF-BIAS CONFIGURATION

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.



c. Eq. (7.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$
$= 20\text{ V} - 11.18\text{ V}$
$= \mathbf{8.82\text{ V}}$

d. Eq. (7.12): $V_S = I_D R_S$
$= (2.6\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.6\text{ V}}$

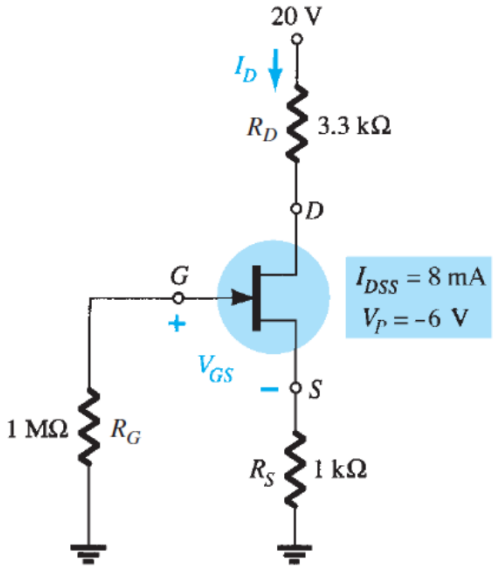
e. Eq. (7.13): $V_G = \mathbf{0\text{ V}}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\text{ V}}$

or $V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\text{ V}}$

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\ \Omega$.
b. $R_S = 10\ \text{k}\Omega$.



Solution: Both $R_S = 100\ \Omega$ and $R_S = 10\ \text{k}\Omega$ are plotted on Fig. 7.16.

a. For $R_S = 100\ \Omega$:

$$I_{D_Q} \cong \mathbf{6.4\ mA}$$

and from Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

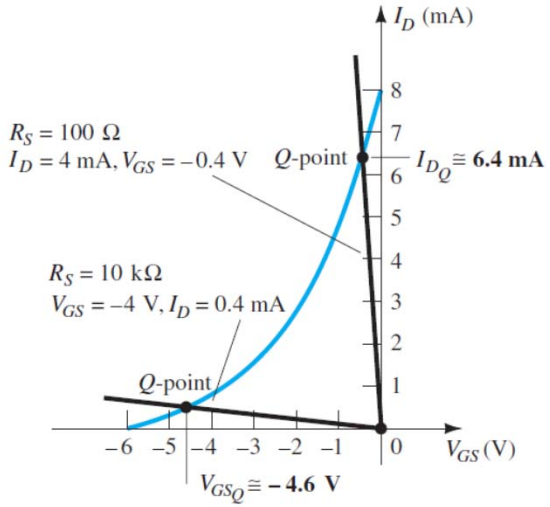
b. For $R_S = 10\ \text{k}\Omega$

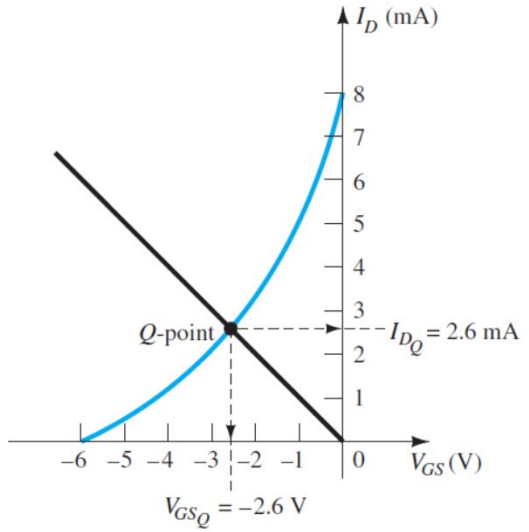
$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

and from Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

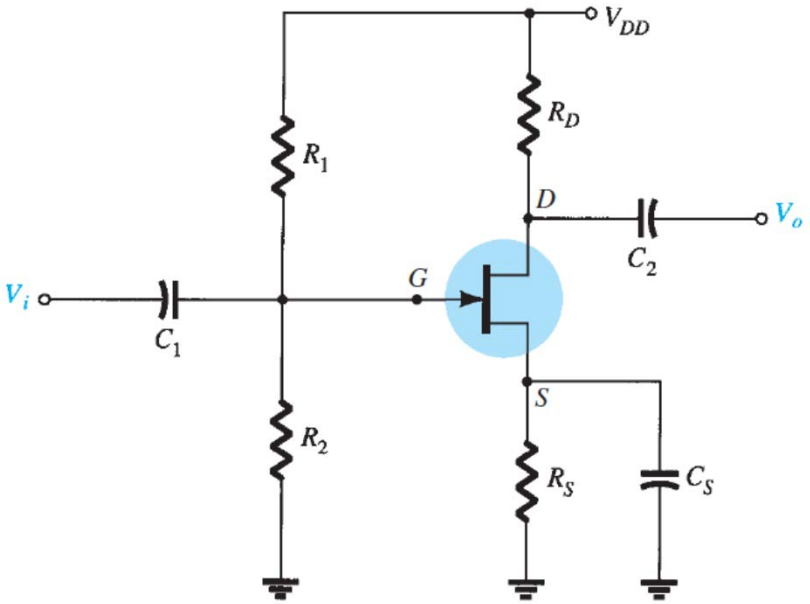


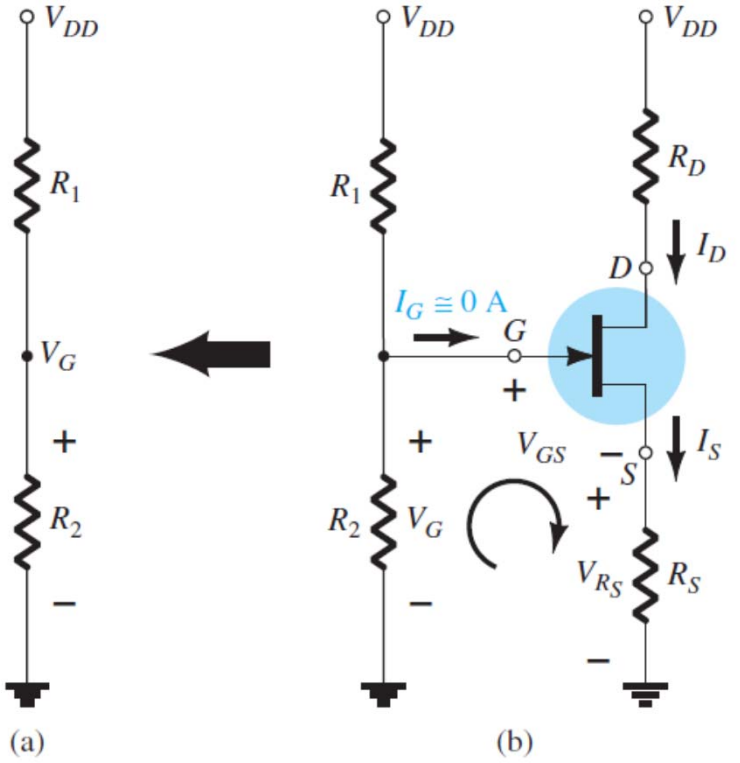


VOLTAGE-DIVIDER BIASING

The basic construction is exactly the same as BJT, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers

Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R1} = I_{R2}$



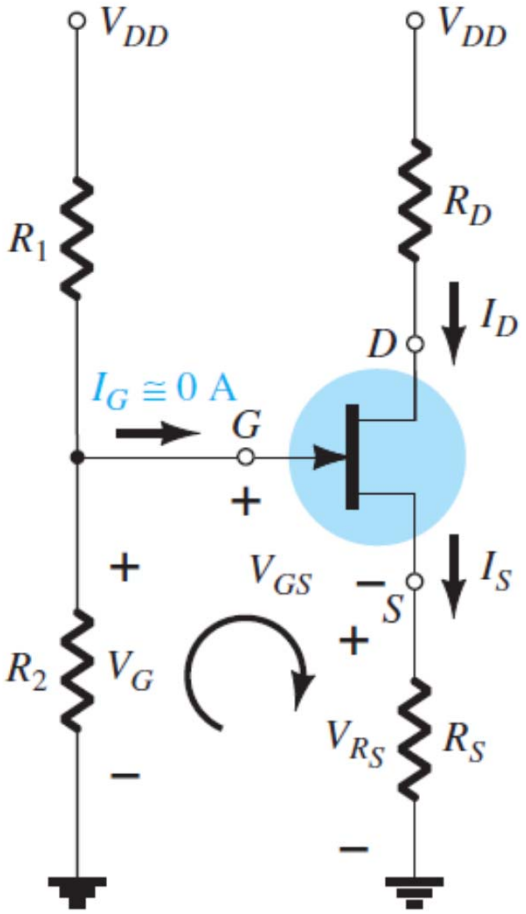


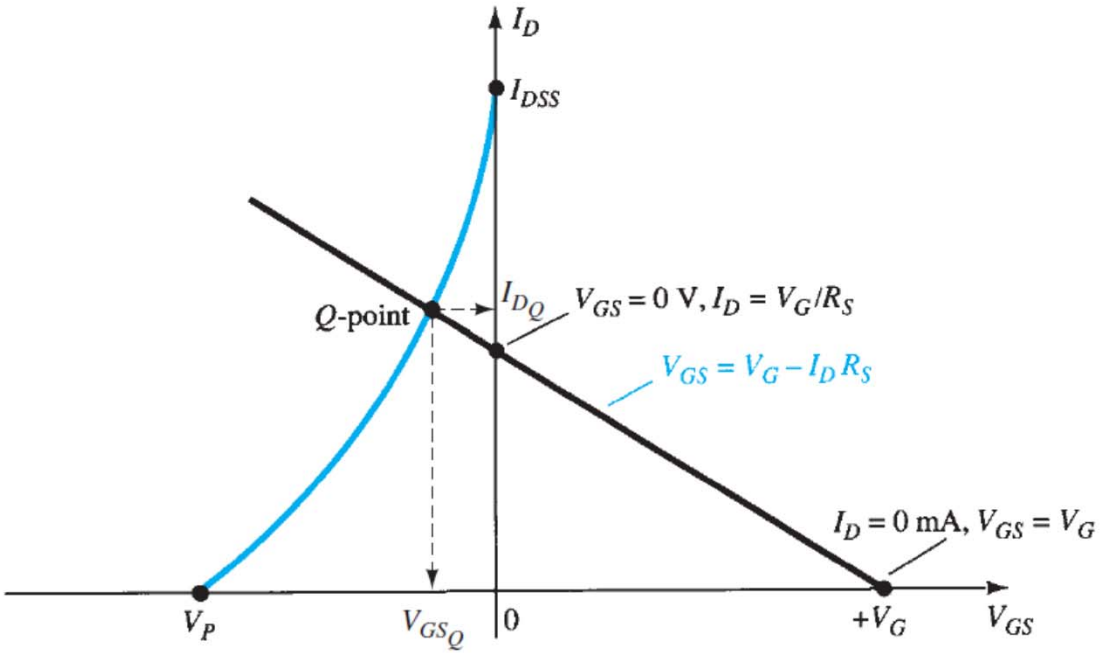
$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S$$

VOLTAGE-DIVIDER BIASING





$$V_{GS} = V_G - I_D R_S$$

$$= V_G - (0\text{ mA})R_S$$

$$V_{GS} = V_G|_{I_D = 0\text{ mA}}$$

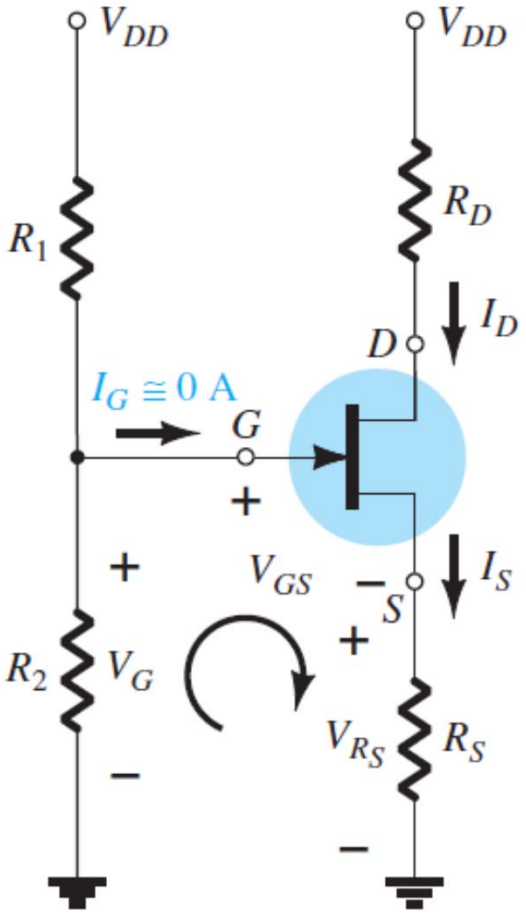
$$V_{GS} = V_G - I_D R_S$$

$$0\text{ V} = V_G - I_D R_S$$

$$I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS} = 0\text{ V}}$$

$$V_{GS} = V_G - I_D R_S$$

VOLTAGE-DIVIDER BIASING



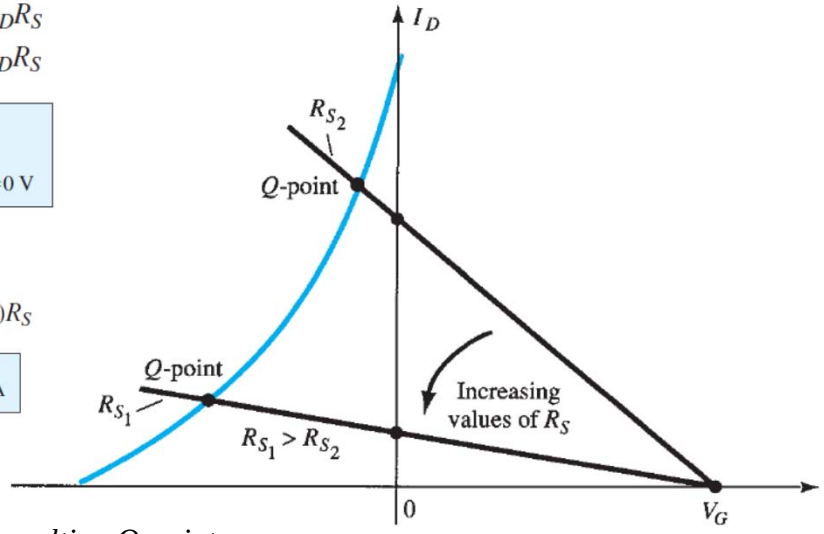
$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = V_G - I_D R_S$$
$$0\,\text{V} = V_G - I_D R_S$$

$$I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS}=0\,\text{V}}$$

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\,\text{mA})R_S$$

$$V_{GS} = V_G|_{I_D=0\,\text{mA}}$$



Effect of RS on the resulting Q-point.

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

ENHANCEMENT-TYPE MOSFETs

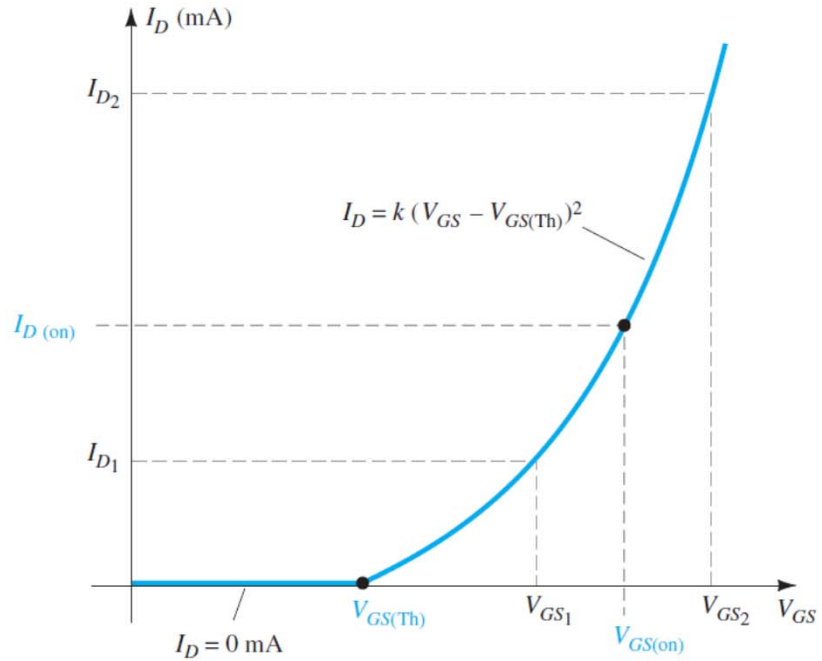
- Recall that for the *n* -channel enhancement-type MOSFET, the drain current is zero for levels of gate to- source voltage less than the threshold level $V_{GS(Th)}$, as shown in Figure.
- For levels of *V GS* greater than *VGS*(Th), the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

- Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(on)}$) and its corresponding level of $V_{GS(on)}$,

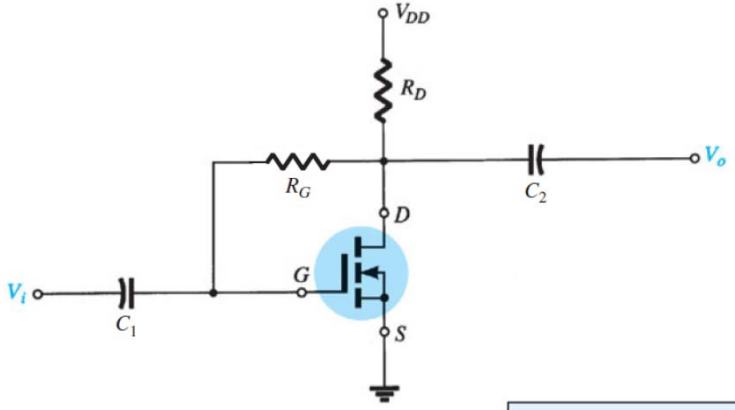
$$I_D = k(V_{GS} - V_{GS(Th)})^2$$
$$I_{D(on)} = k(V_{GS(on)} - V_{GS(Th)})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$



Feedback Biasing Arrangement

Since $I_G = 0$ mA, $V_{RG} = 0$ V and the dc equivalent network



A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

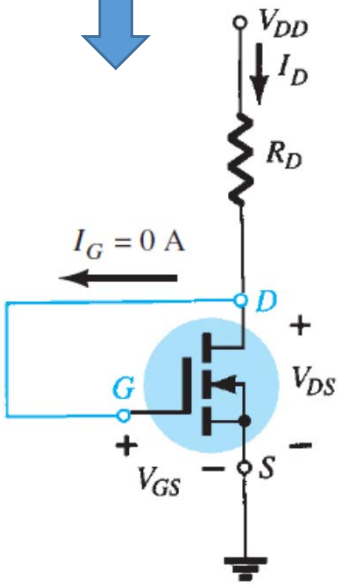
and

$$\boxed{V_{DS} = V_{GS}}$$

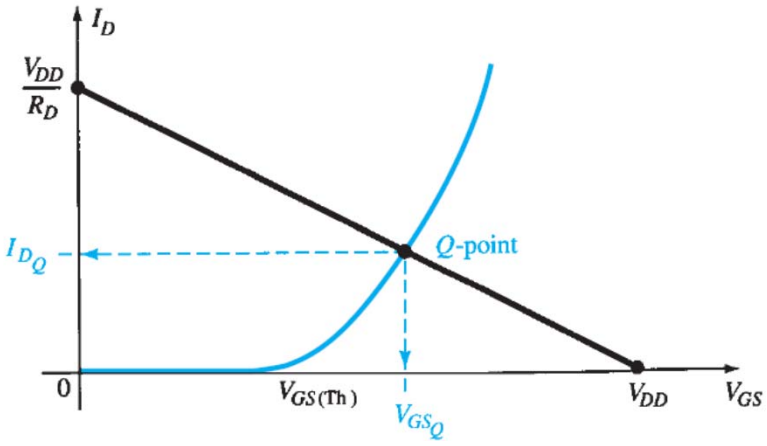
For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \qquad \boxed{V_{GS} = V_{DD}\big|_{I_D = 0\text{ mA}}} \qquad \boxed{I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\text{ V}}}$$

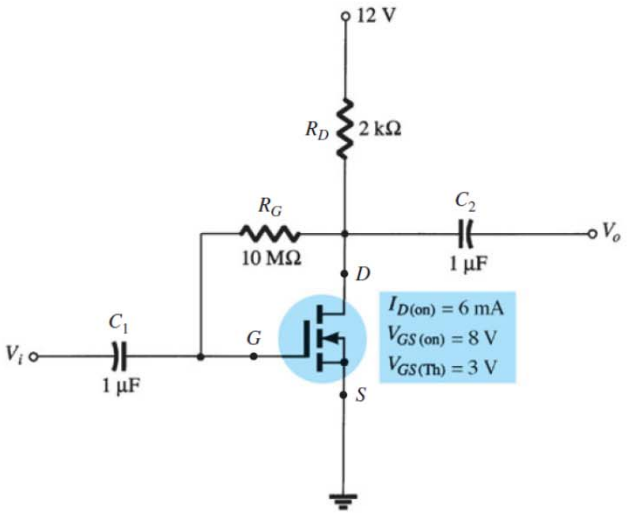


DC equivalent of the network



Determining the Q-point for the network

Determine IDQ and VDSQ for the enhancement-type MOSFET



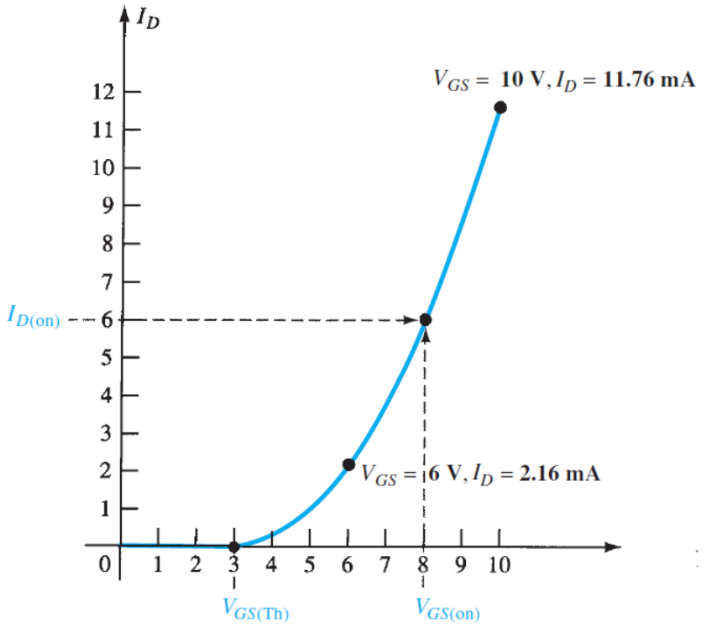
Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. 7.41. Solving for k, we obtain

$$\text{Eq. (7.34):} \quad k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$



For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

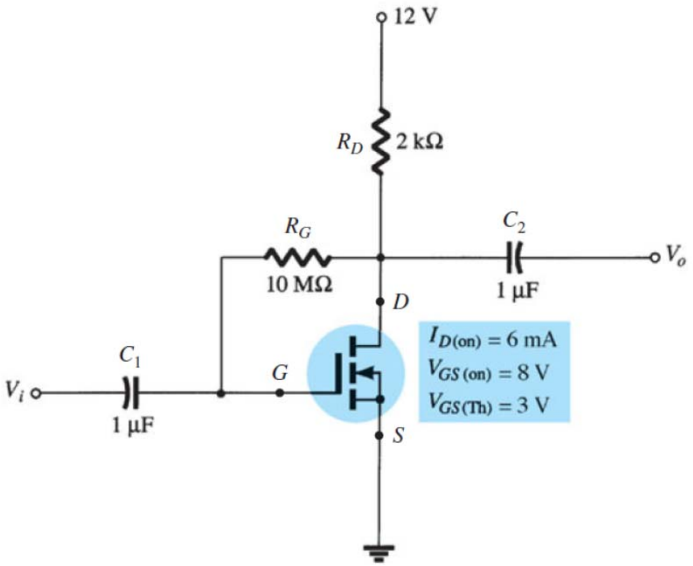
$$= 2.16\text{ mA}$$

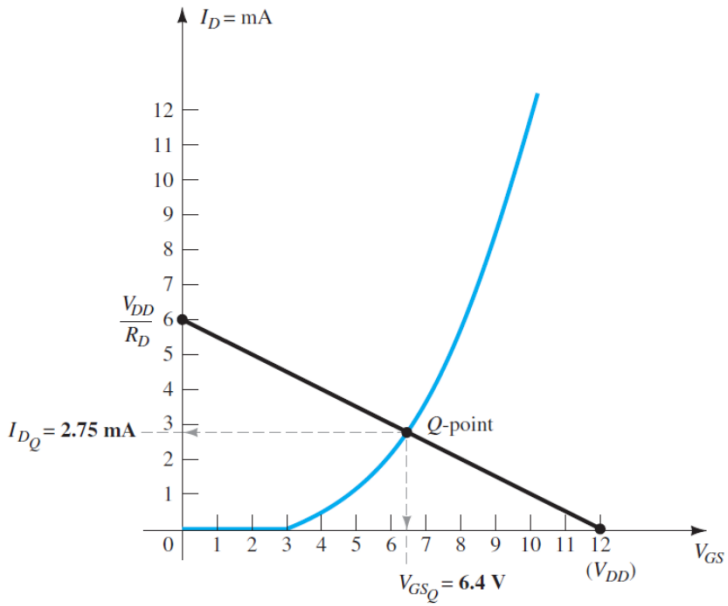
as shown on Fig. 7.41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76\text{ mA}$$

Determine IDQ and VDSQ for the enhancement-type MOS





Determining the Q-point for the network

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

Eq. (7.37): $$V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$

Eq. (7.38): $$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 7.42.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

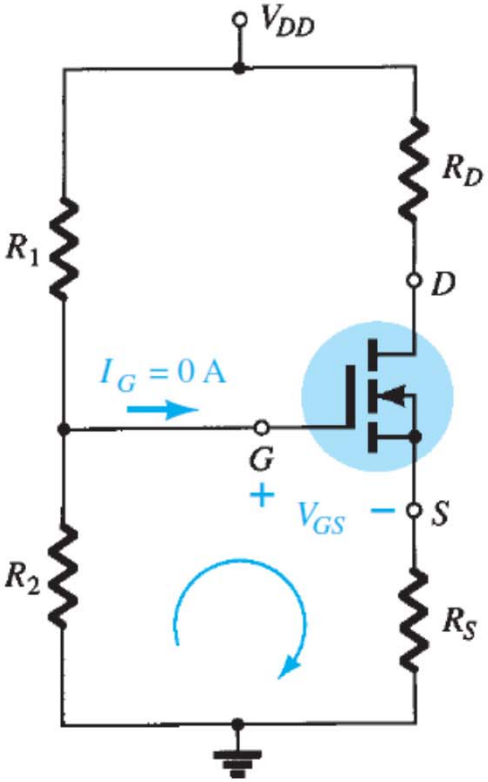
and $$V_{GS_Q} = 6.4\text{ V}$$

with $$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

Voltage-Divider Biasing Arrangement

The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$



Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

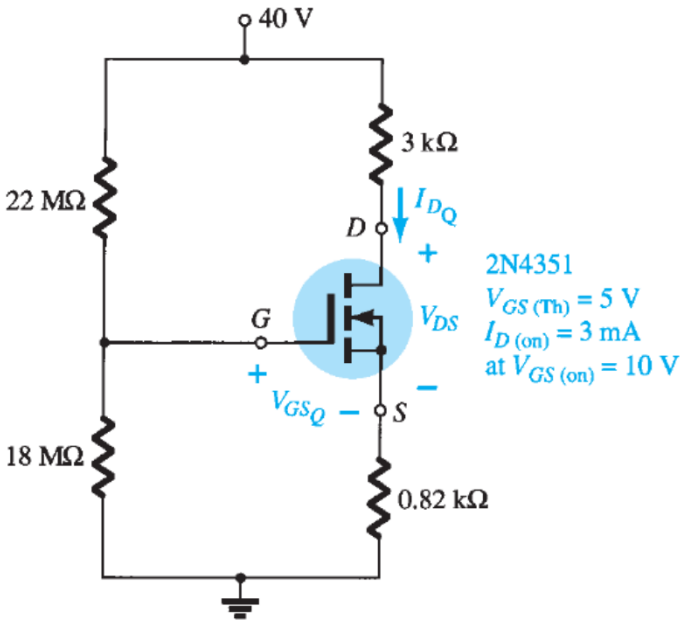
- Since the characteristics are a plot of I_D versus V_{GS} and relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection.
- Once I_{DQ} and V_{GSQ} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

Voltage-Divider Biasing Arrangement

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$



Device

$$V_{GS(\text{Th})} = 5\ \text{V}, \quad I_{D(\text{on})} = 3\ \text{mA with } V_{GS(\text{on})} = 10\ \text{V}$$

Eq. (7.34): $$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\ \text{mA}}{(10\ \text{V} - 5\ \text{V})^2} = 0.12 \times 10^{-3}\ \text{A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

Voltage-Divider Biasing Arrangement

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When $I_D = 0$ mA,

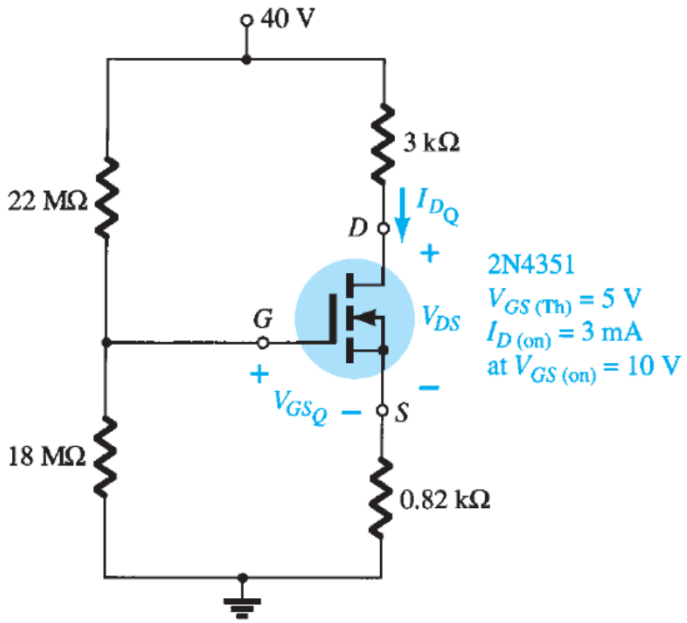
$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

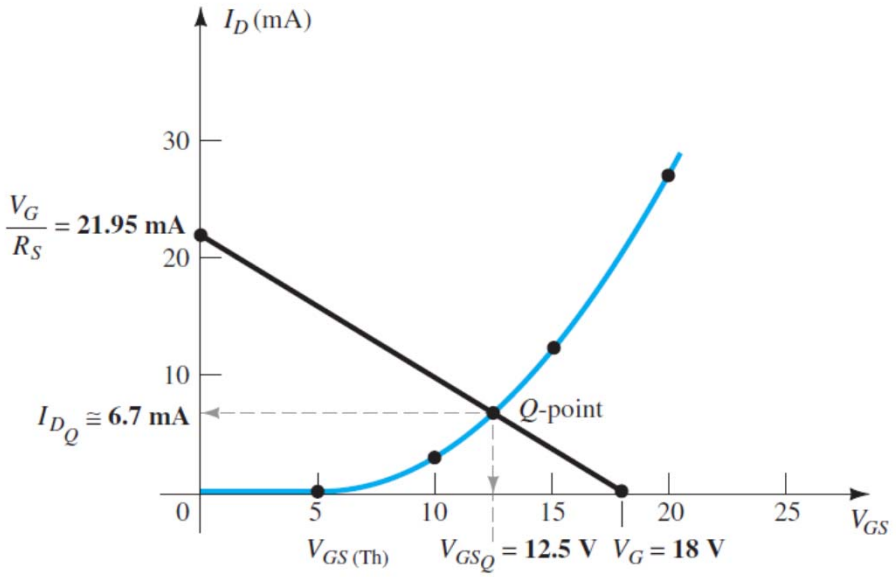
as appearing on Fig. 7.45. When $V_{GS} = 0$ V,

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

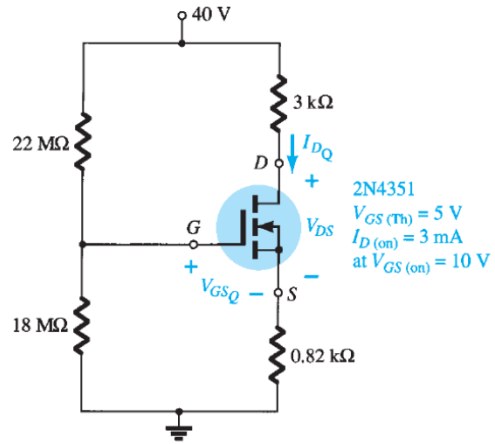
$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$





Voltage-Divider Biasing Arrangement

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network



$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

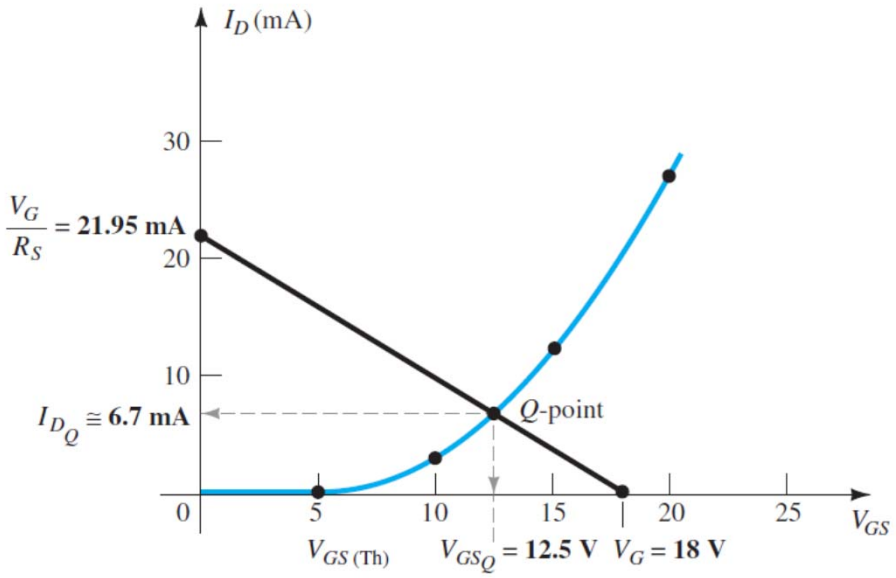
$$V_{GS_Q} = \mathbf{12.5\ V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$

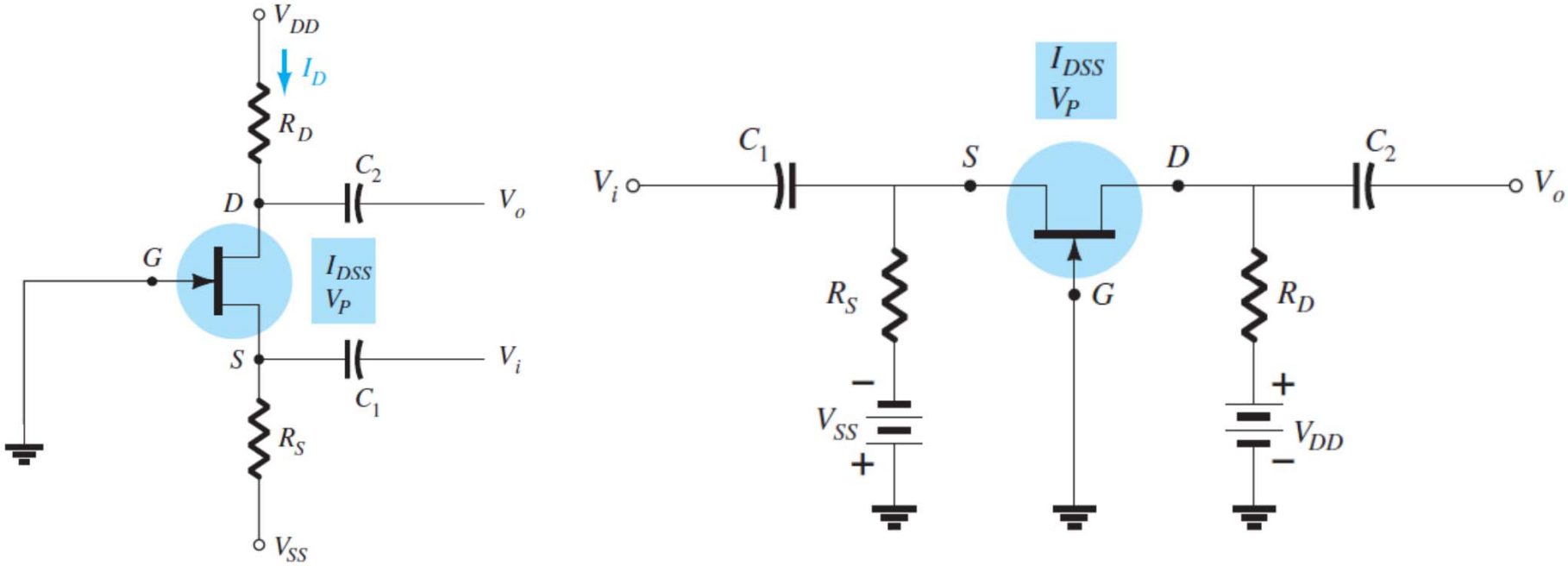
$$= 40\ \text{V} - 25.6\ \text{V}$$

$$= \mathbf{14.4\ V}$$



COMMON-GATE CONFIGURATION

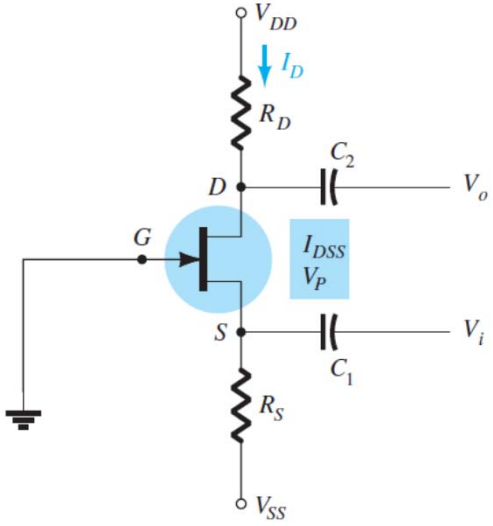
- The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown

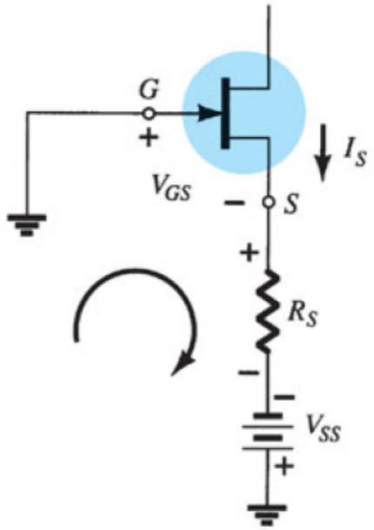


Two versions of the common-gate configuration.

COMMON-GATE CONFIGURATION

- The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown





$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S$$

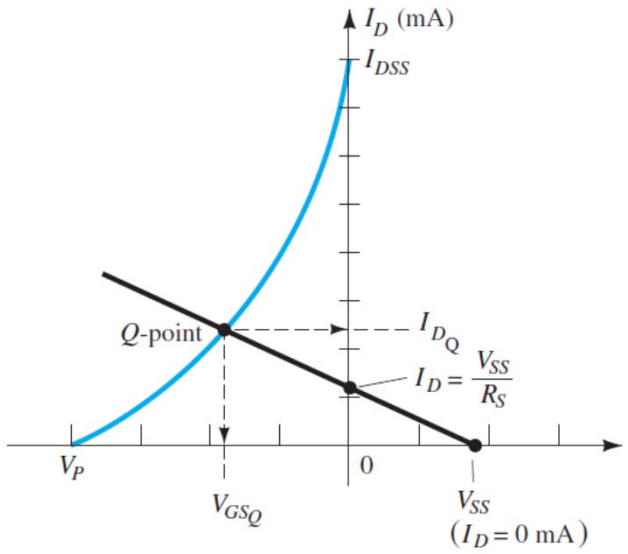
$$I_S = I_D$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

$$V_{GS} = V_{SS} - (0)R_S$$

$$\boxed{V_{GS} = V_{SS}|_{I_D=0\text{mA}}}$$

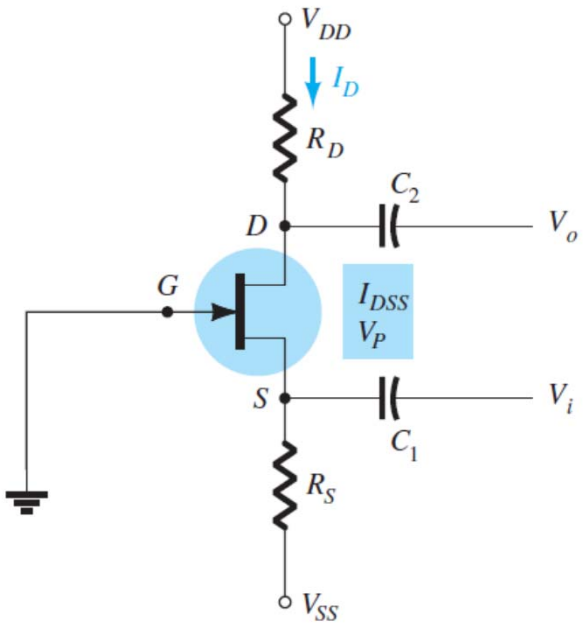
$$\boxed{I_D = \left.\frac{V_{SS}}{R_S}\right|_{V_{GS}=0\text{ V}}}$$



Determining the Q-point for the network

COMMON-GATE CONFIGURATION

- The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown



$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

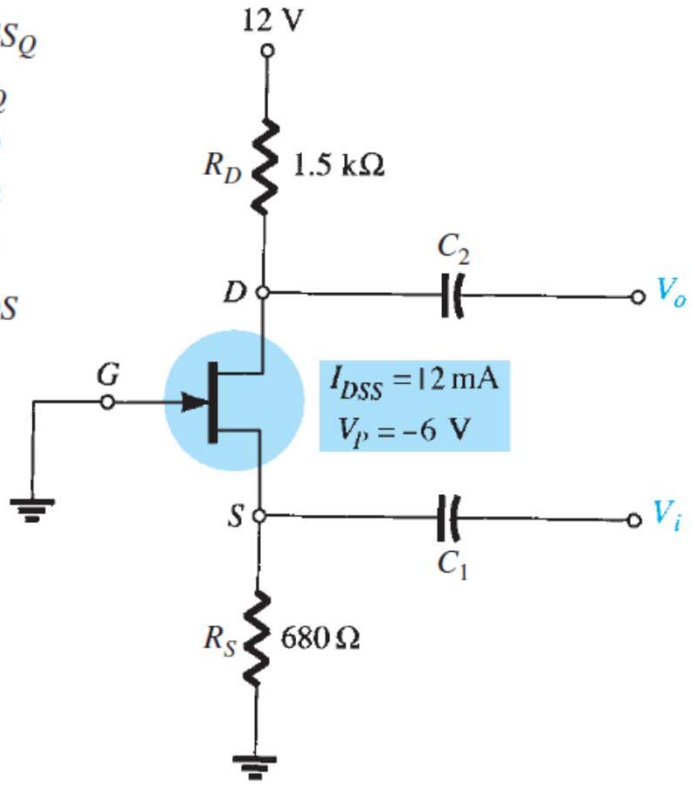
$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = -V_{SS} + I_D R_S$$

Determine the following for the common-gate configuration

a. V_{GS_Q}
b. I_{D_Q}
c. V_D
d. V_G
e. V_S
f. V_{DS}



$$V_{GS} = V_{SS} - I_D R_S$$

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = -V_{SS} + I_D R_S$$

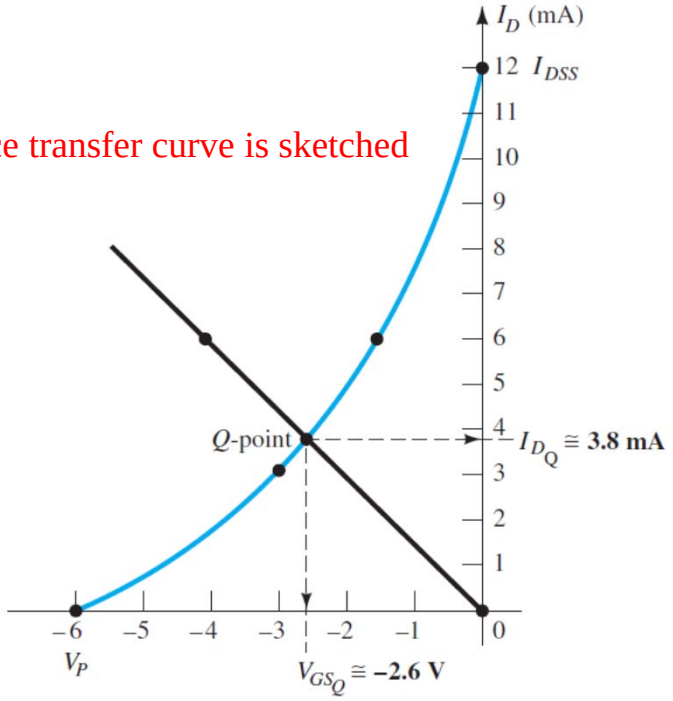
$$V_{GS} = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S$$

Choosing I_D = 6 mA

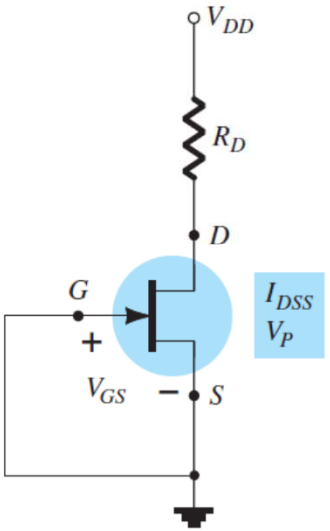
V_{GS} = -$I_D$$R_S$ = -(6 mA)(680) = -4.08 V

The device transfer curve is sketched

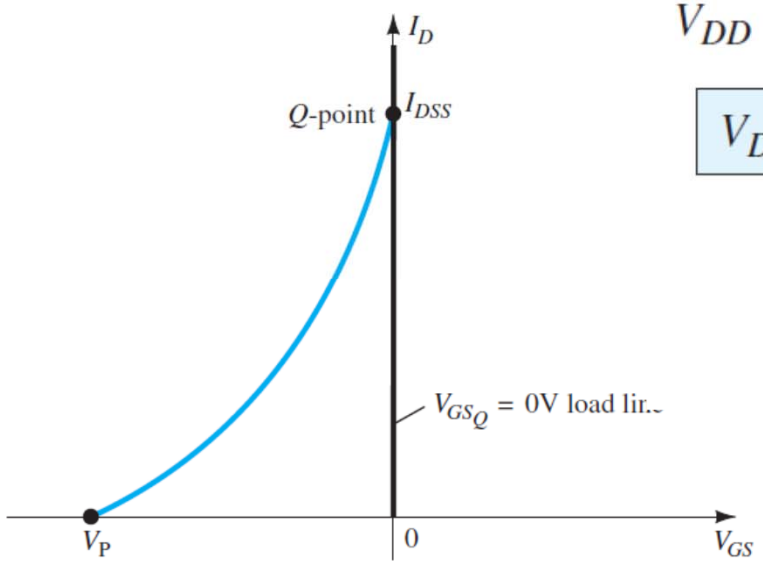


7.6 SPECIAL CASE: $V_{GS_Q} = 0$ V

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 7.28. Note that direct connection of the gate and source terminals to ground resulting in $V_{GS} = 0$ V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at $V_{GS_Q} = 0$ V as shown in Fig. 7.29.



Special case $V_{GS_Q} = 0$ V configuration.



Finding the Q-point for the network

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_D = V_{DS}$$

$$V_S = 0\ \text{V}$$

$$I_{D_Q} = I_{DSS}$$