Field-Effect Transistors

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET),
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET,

- ***The BJT transistor is a current-controlled device as depicted in Fig. 6.1a ,***
- ***whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b .***

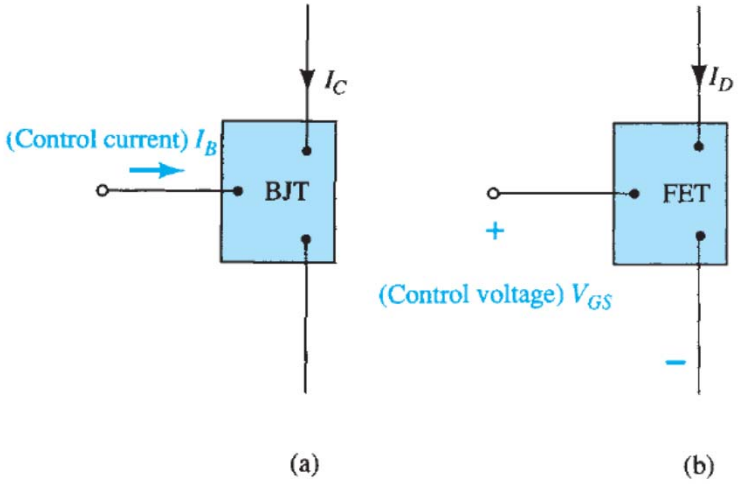


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

Types of FET's

- JFET – Junction Field Effect Transistor
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
  - D-MOSFET - Depletion Mode MOSFET
  - E- MOSFET - Enhancement Mode MOSFET

Construction of the n -channel JFET

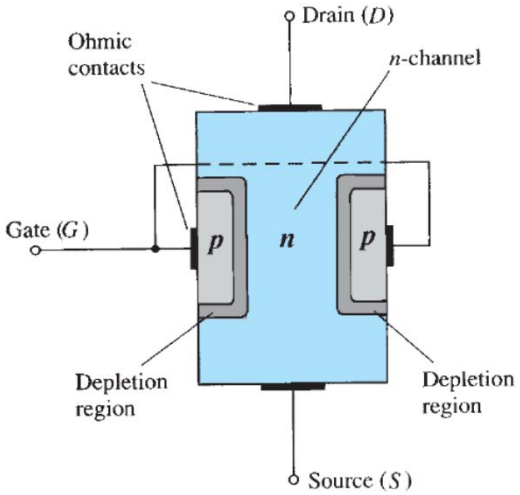


FIG. 6.3
Junction field-effect transistor (JFET).

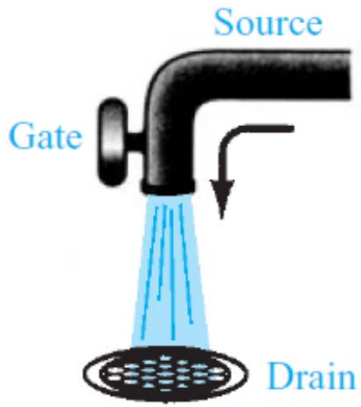


FIG. 6.4
Water analogy for the JFET control mechanism.

- There are two types of JFET's: n-channel and p-channel. The n-channel is more widely used.
- There are three terminals: Drain (D) and Source (S) are connected to n-channel Gate (G) is connected to the p-type material

JFET Operating Characteristics

VGS = 0 V, *VDS* -Some Positive Value

- The instant the voltage *VDD* (= *VDS*) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5 .
- The path of charge flow clearly reveals that the drain and source currents are equivalent (I_D = I_S). Under the condition
- In Fig. 6.5 , the flow of charge is relatively uninhibited and is limited solely by the resistance of the *n* -channel between drain and source.

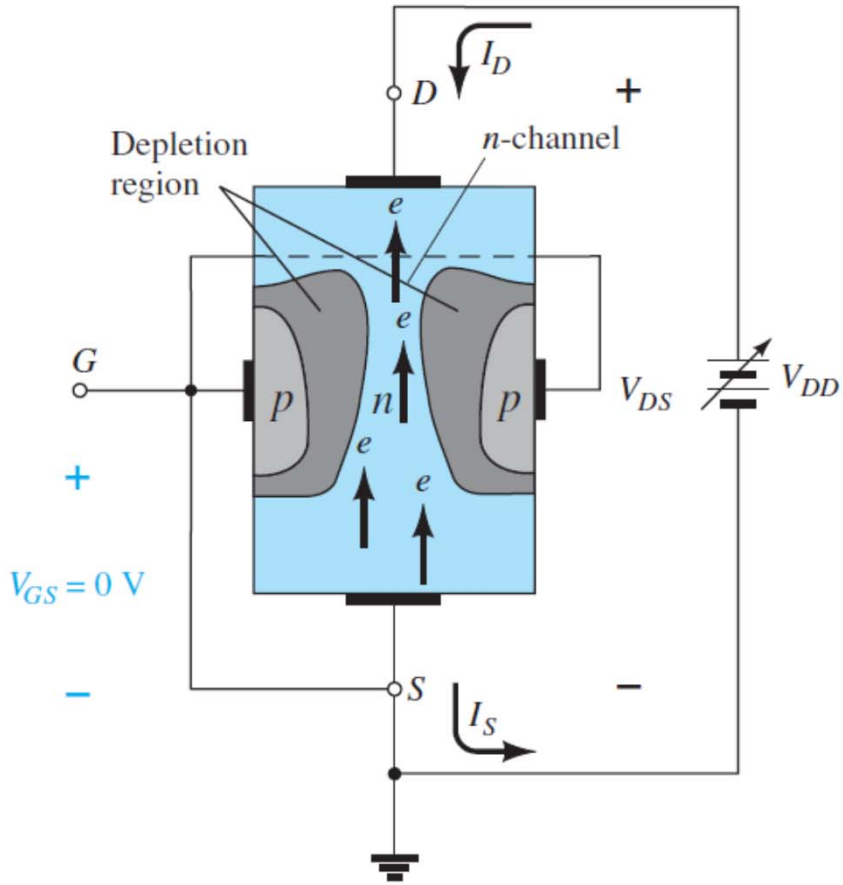


FIG. 6.5
JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.

JFET Operating Characteristics

VGS = 0 V, *VDS* -Some Positive Value

- It is important to note that the depletion region is wider near the top of both p –type materials.
- Assuming a uniform resistance in the n -channel, we can break down the resistance of the channel into the divisions appearing in Fig. 6.6
- The result is that the upper region of the p -type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V.
- Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider is the depletion region

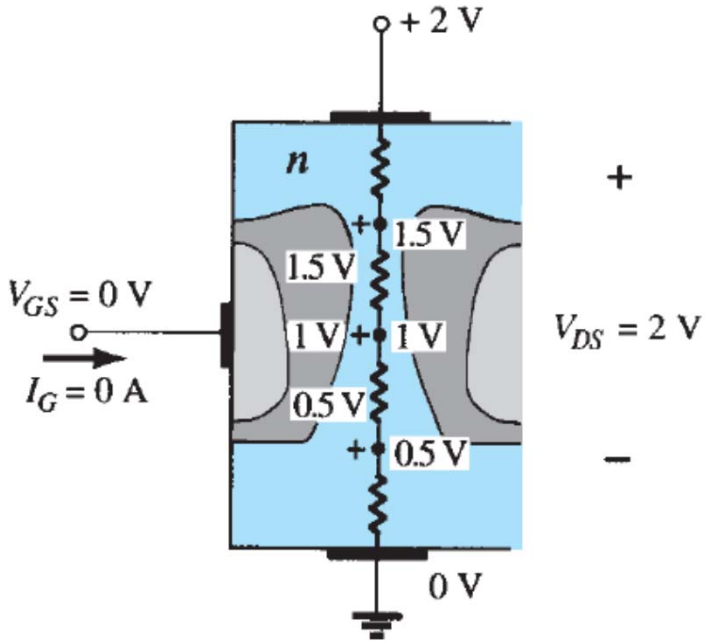


FIG. 6.6

Varying reverse-bias potentials across the p–n junction of an n-channel JFET.

The fact that $I_G = 0$ A is an important characteristic of the JFET.

JFET Operating Characteristics

V_{GS} = 0 V, V_{DS} Some Positive Value

- As the voltage V DS is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I D versus V DS will appear as shown in Fig. 6.7.
- The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region.
- If V_{DS} is increased to a level where it appears that the two depletion regions would"touch" as shown in Fig. 6.8 , a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P , as shown in Fig. 6.7 .

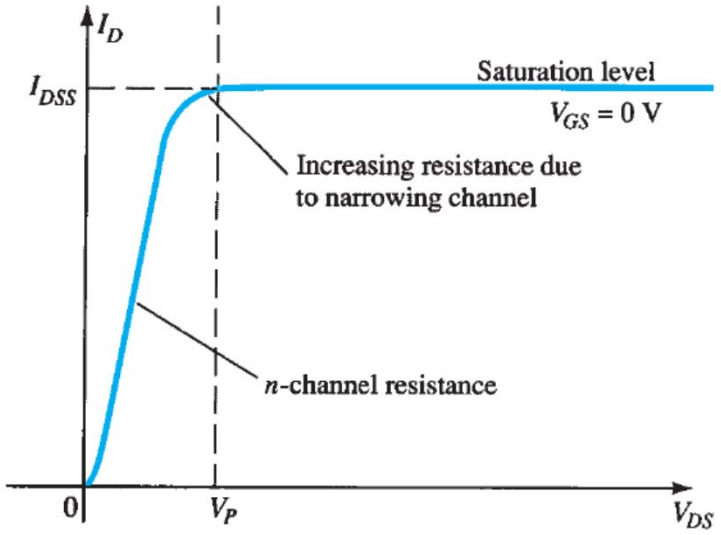


FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

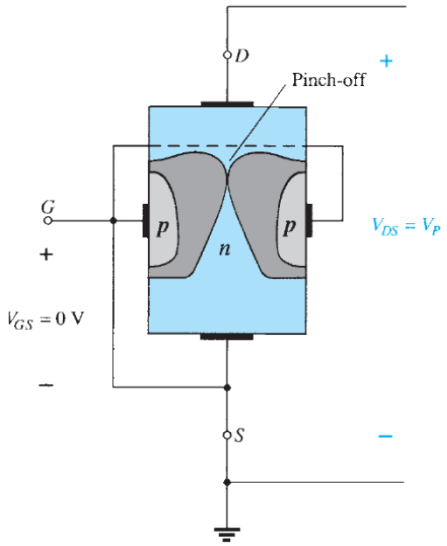


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

JFET Operating Characteristics

V_{GS} = 0 V, V_{DS} Some Positive Value

- As V_{DS} is increased beyond V_P , the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same.
- In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source.
- As shown in Fig. 6.9 , the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels > V_P) is determined by the applied load.
- The choice of notation I_{DSS} is derived from the fact that it is the drain-to- source current with a short-circuit connection from gate to source.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS} = 0 V and $V_{DS} > |V_P|$.

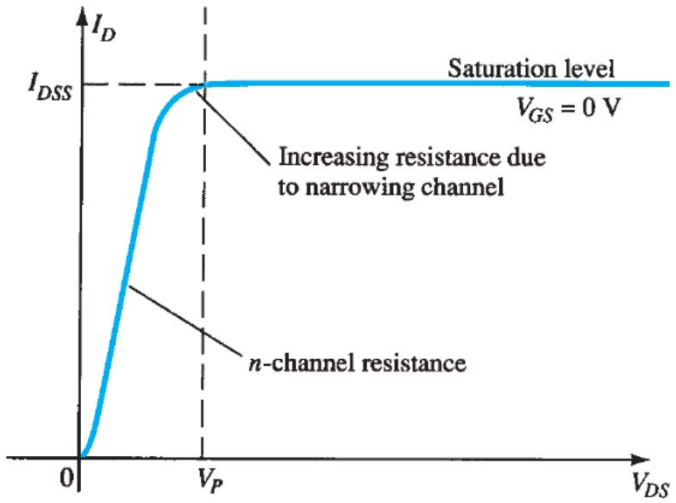


FIG. 6.7
I_D versus V_{DS} for $V_{GS} = 0$ V.

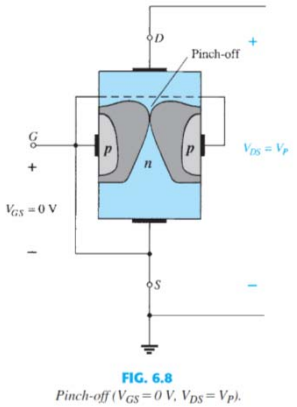


FIG. 6.8
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

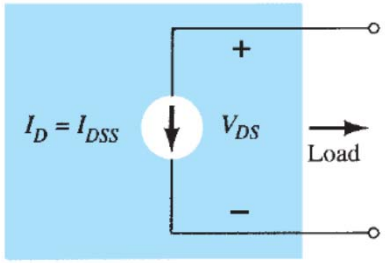


FIG. 6.9
Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

JFET Operating Characteristics

V GS < 0 V

- The voltage from gate to source, denoted V_{GS} , is the controlling voltage of the JFET.
- Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET

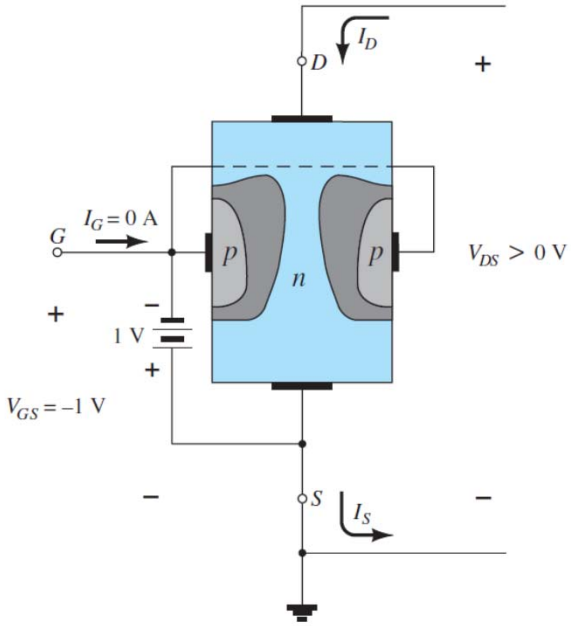


FIG. 6.10

Application of a negative voltage to the gate of a JFET.

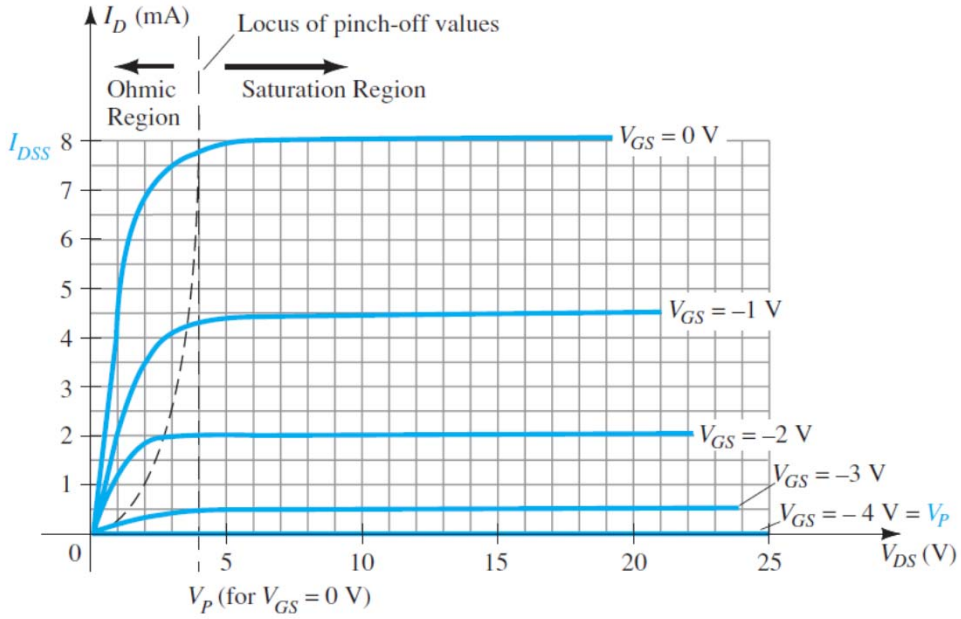


FIG. 6.11

n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

JFET Operating Characteristics: *p* -Channel Devices

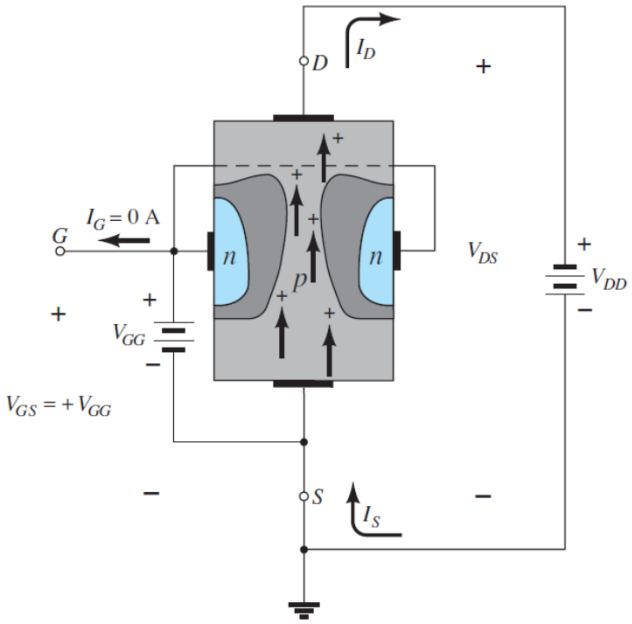


FIG. 6.12
p-Channel JFET.

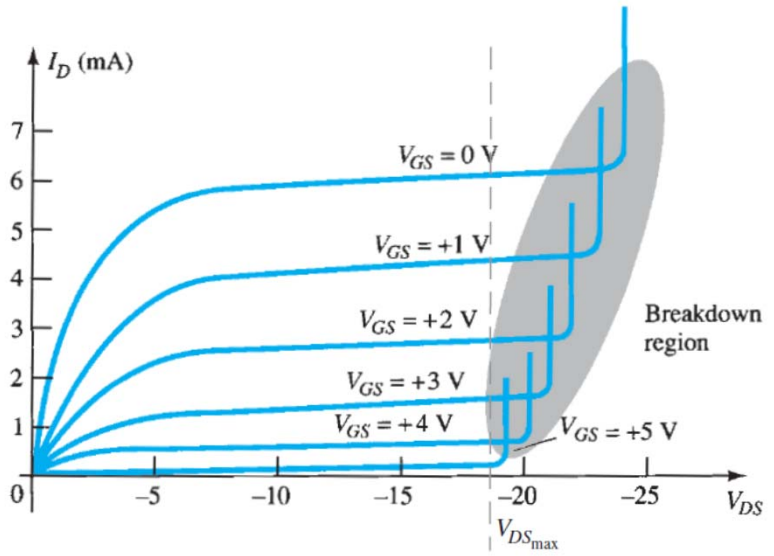


FIG. 6.13
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

- For the p -channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.13 , which has an I_{DSS} of 6 mA and a pinch off voltage of V_{GS} = +6 V.
- The region to the right of the pinch-off locus of Fig. 6.11 is the region typically employed in linear amplifiers

JFET – Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 6.14. Note that the arrow is pointing in for the *n*-channel device of Fig. 6.14a to represent the direction in which I_G would flow if the *p*–*n* junction were forward-biased. For the *p*-channel device (Fig. 6.14b) the only difference in the symbol is the direction of the arrow in the symbol.

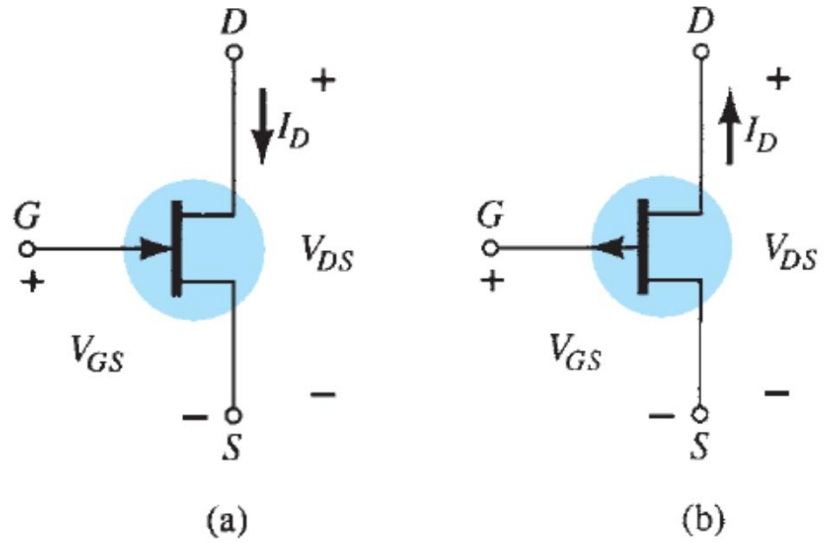


FIG. 6.14

JFET symbols: (a) n-channel; (b) p-channel.

JFET Operating Characteristics

There are three basic operating conditions for a JFET:

JFET's operate in the depletion mode only

- $V_{GS} = 0$, V_{DS} is a minimum value depending on I_{DSS} and the drain and source resistance
- $V_{GS} < 0$, V_{DS} at some positive value and
- Device is operating as a Voltage-Controlled Resistor

For an n channel JFET, V_{GS} may never be positive*

For an p channel JFET, V_{GS} may never be negative*

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$, as shown in Fig. 6.15a.

For gate-to-source voltages V_{GS} is less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A), as in Fig. 6.15b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as in Fig. 6.15c.

A similar list can be developed for p-channel JFETs.

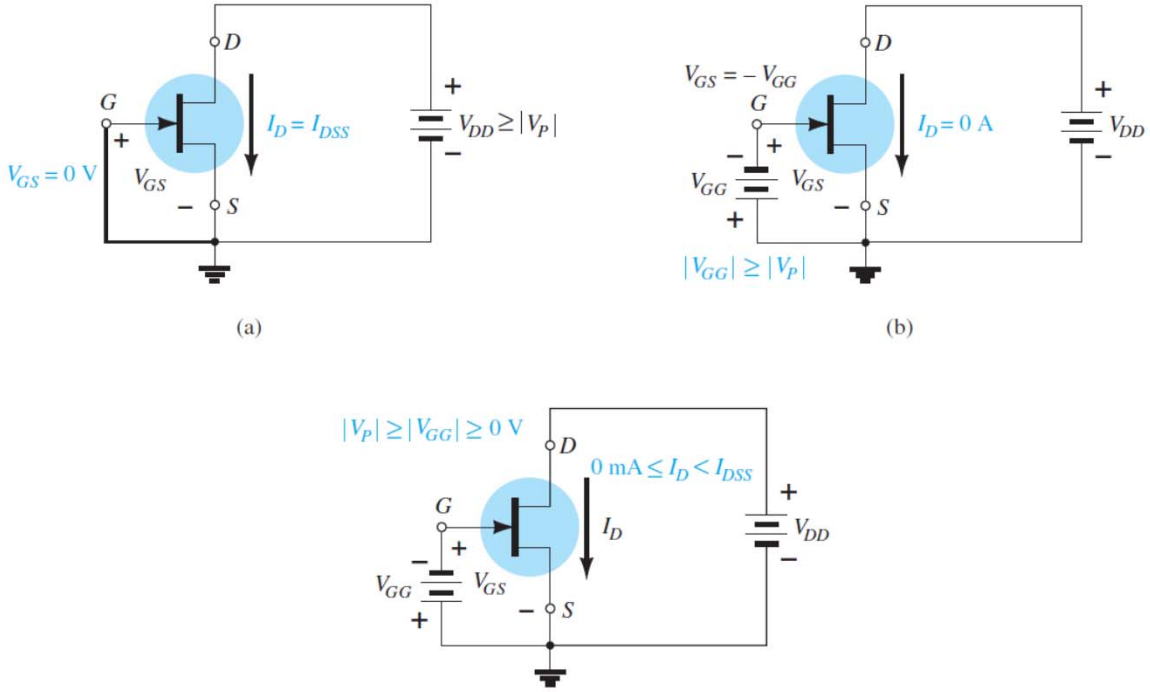
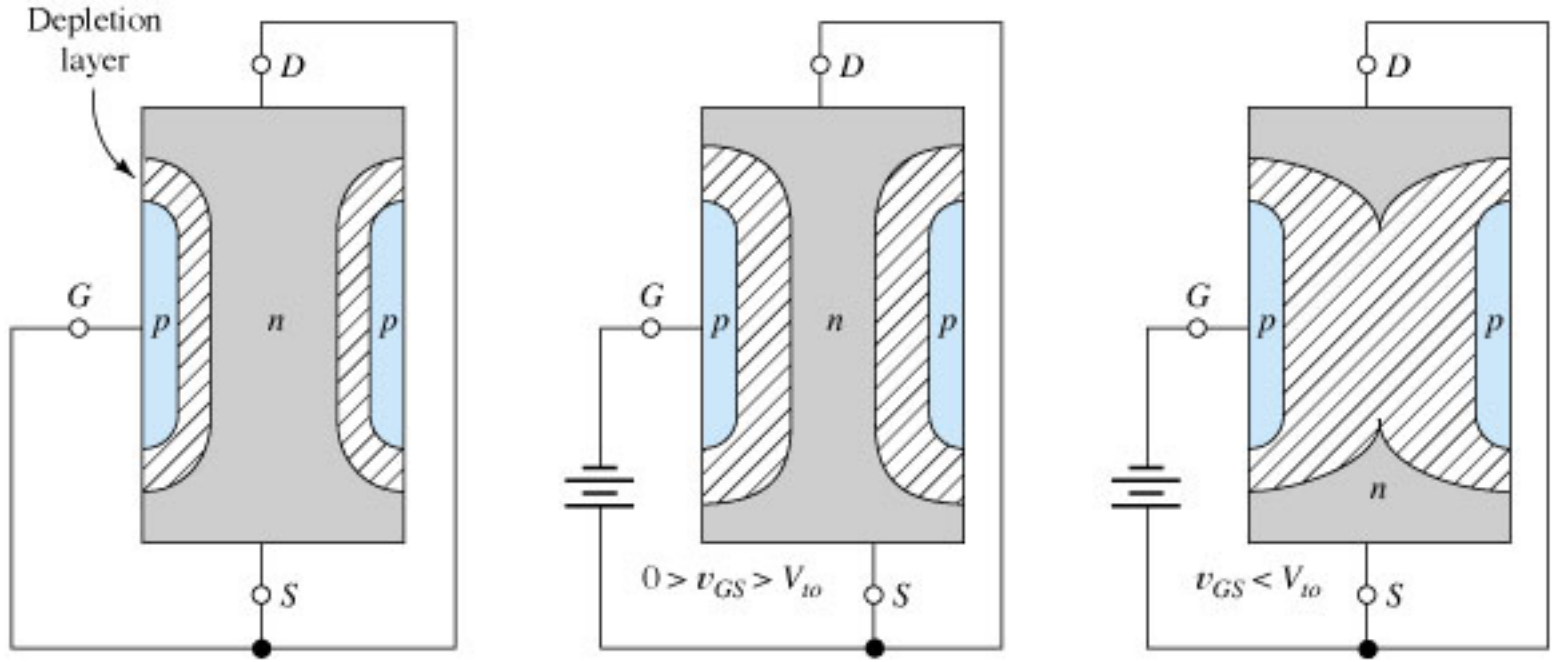


FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

N-Channel JFET Operation



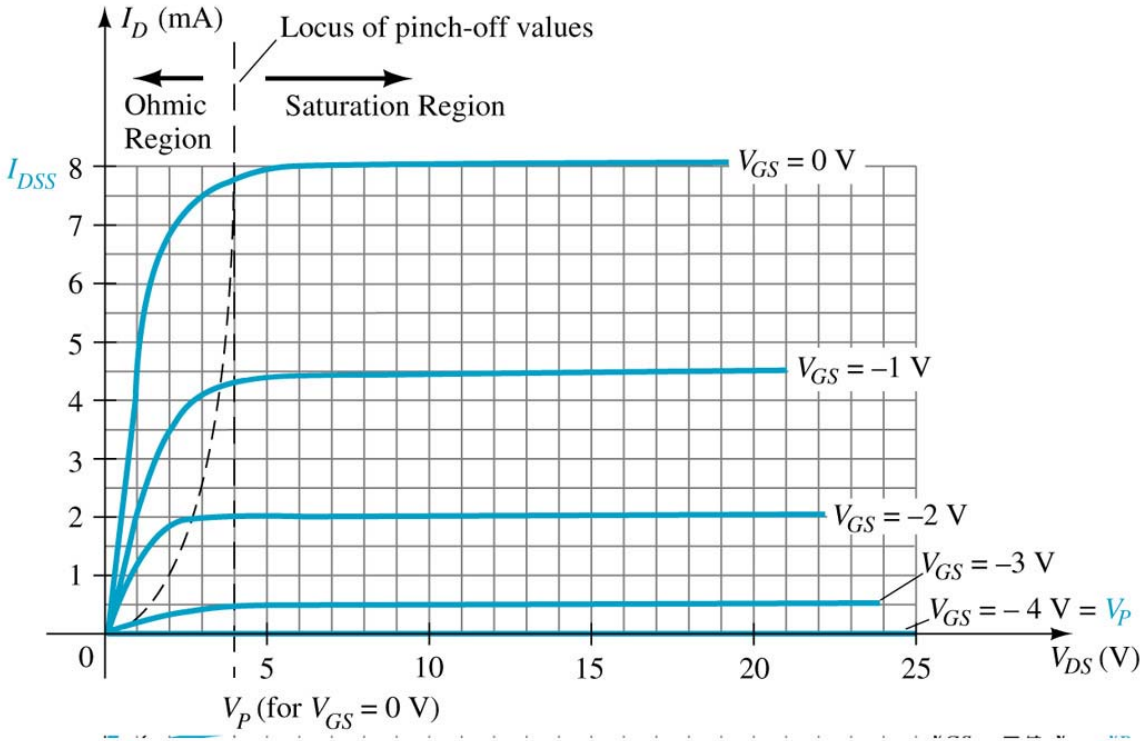
(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

The nonconductive depletion region becomes thicker with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

$I_D \leq I_{DSS}$



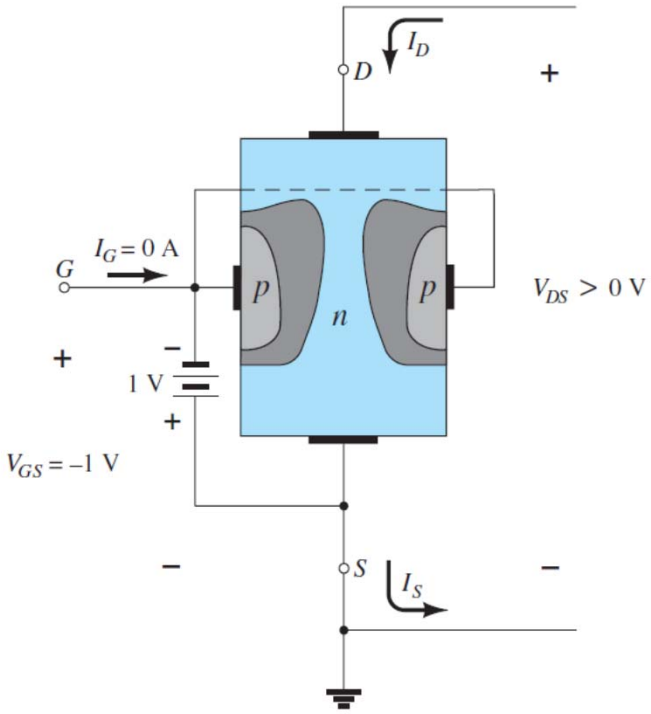


FIG. 6.10
Application of a negative voltage to the gate of a JFET.

As V_{GS} becomes more negative:

- the JFET will pinch-off at a lower voltage (Vp).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D will reach 0A. V_{GS} at this point is called Vp or $V_{GS(off)}$.
- Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. ID will increases uncontrollably if $V_{DS} > V_{DSmax}$.

Symbols

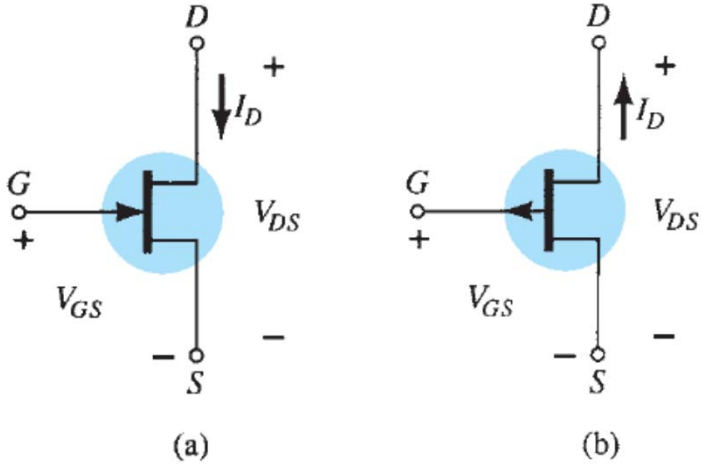
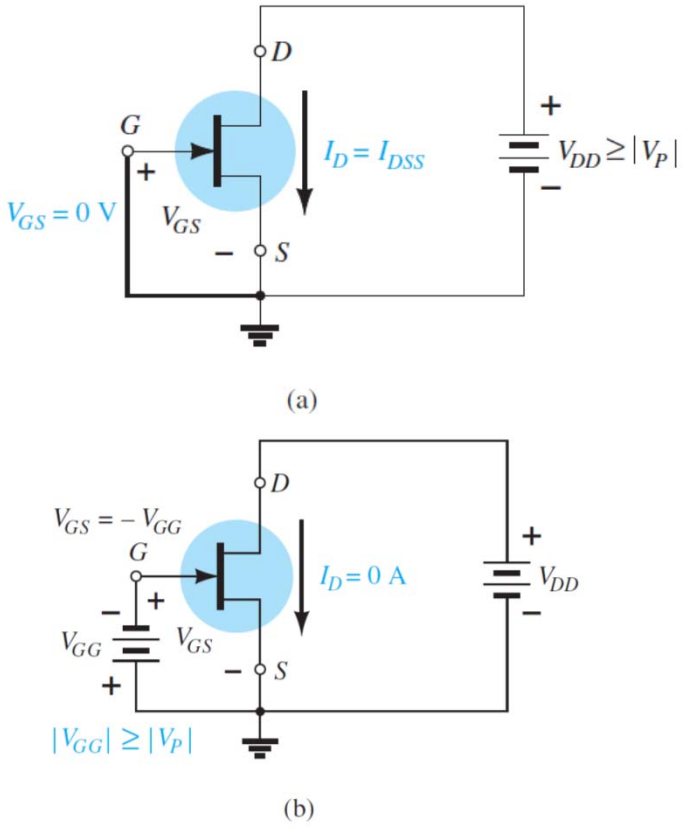


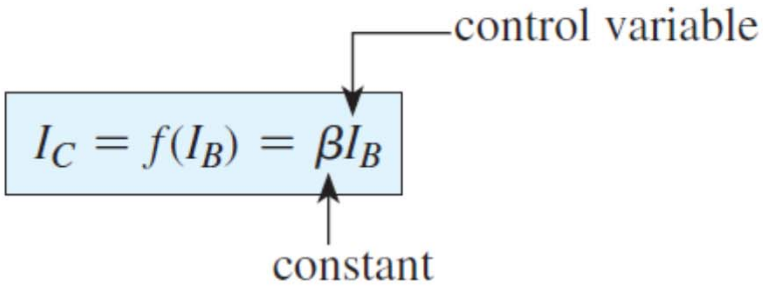
FIG. 6.14
JFET symbols: (a) n-channel; (b) p-channel.



(a) $V_{GS} = 0$ *V,* $I_D = I_{DSS}$*;*
(b) cutoff ($I_D = 0$ *A)* V_{GS} *less than the pinch-off level;*
(c) I_D *is between 0 A and* I_{DSS} *for* V_{GS} *0 V and greater than the pinch-off level.*

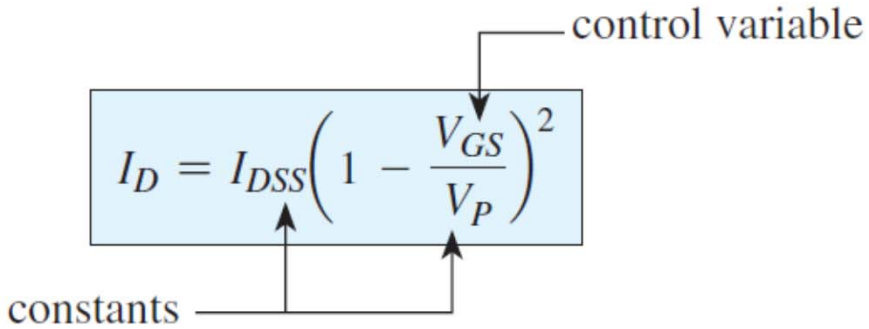
TRANSFER CHARACTERISTICS

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,



(6.2)

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):



(6.3)

TRANSFER CHARACTERISTICS

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

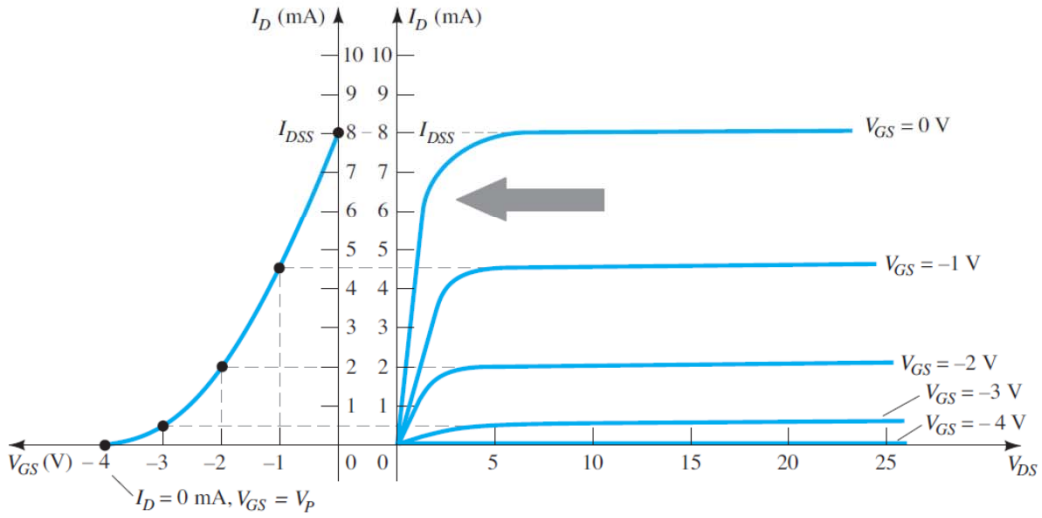


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} = V_P$, $I_D = 0$ mA

Applying Shockley's Equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\,|_{V_{GS}=0\text{ V}}$$

$$I_D = 0\text{ A}\,|_{V_{GS}=V_P}$$

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}\,(0.75)^2$$

$$= 8\text{ mA}\,(0.5625)$$

$$= \mathbf{4.5\text{ mA}}$$

TRANSFER CHARACTERISTICS

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

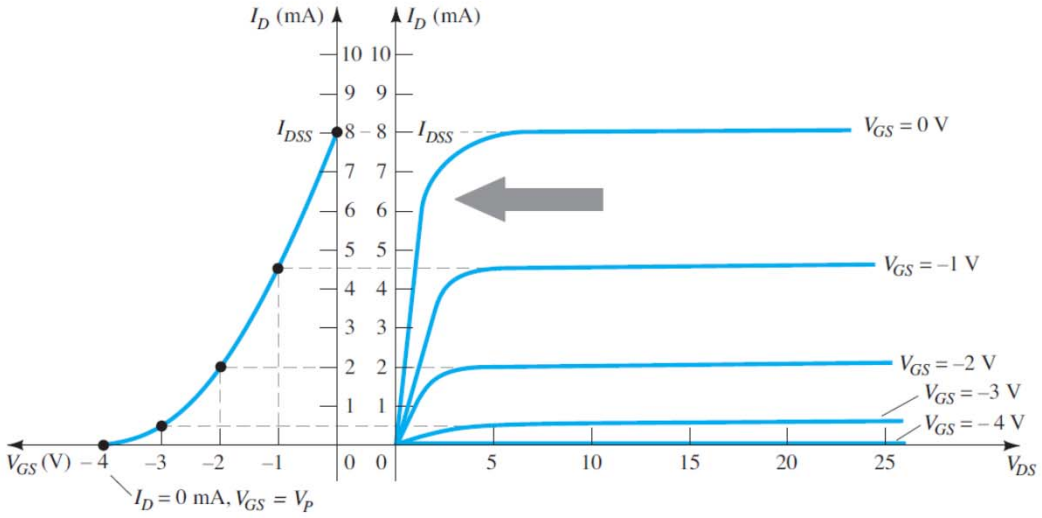


FIG. 6.17
Obtaining the transfer curve from the drain characteristics.

- It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets), the level of I_D can be found for any level of V_{GS} .
- Conversely, by using basic algebra we can obtain [from Eq. (6.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straightforward and results in

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$\begin{aligned} V_{GS} &= -4\,\text{V}\left(1 - \sqrt{\frac{4.5\,\text{mA}}{8\,\text{mA}}}\right) \\ &= -4\,\text{V}(1 - \sqrt{0.5625}) = -4\,\text{V}(1 - 0.75) \\ &= -4\,\text{V}(0.25) \\ &= \mathbf{-1\,V} \end{aligned}$$

TRANSFER CHARACTERISTICS

Shorthand Method

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

$$\boxed{I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS} = V_P/2}}$$

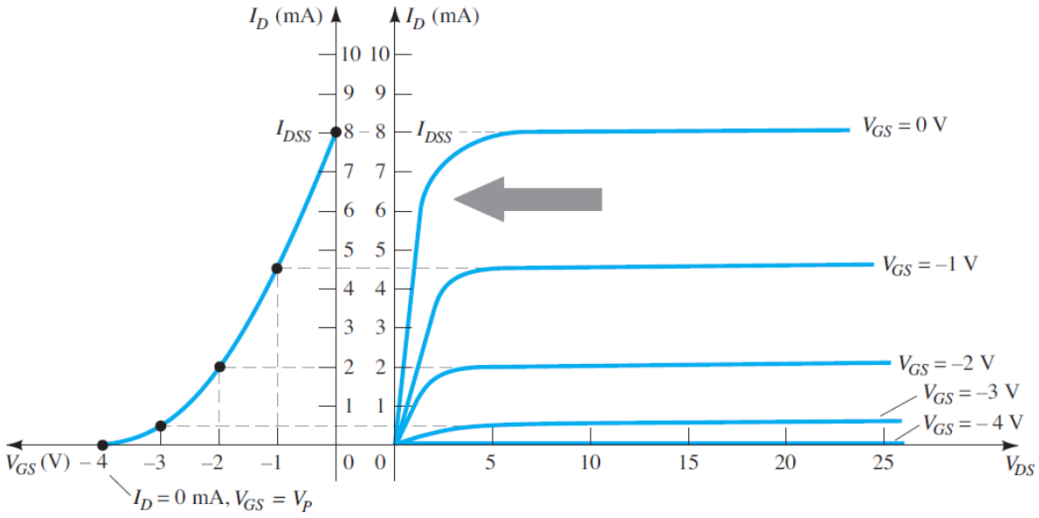


FIG. 6.17
Obtaining the transfer curve from the drain characteristics.

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}}$$

TABLE 6.1
V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12\text{ mA}$ and $V_P = -6\text{ V}$.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\text{ mA}} \quad \text{and} \quad V_{GS} = \mathbf{0\text{ V}}$$

and

$$I_D = \mathbf{0\text{ mA}} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\text{ V}}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\text{ mA}}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\text{ mA}}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\text{ V}}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

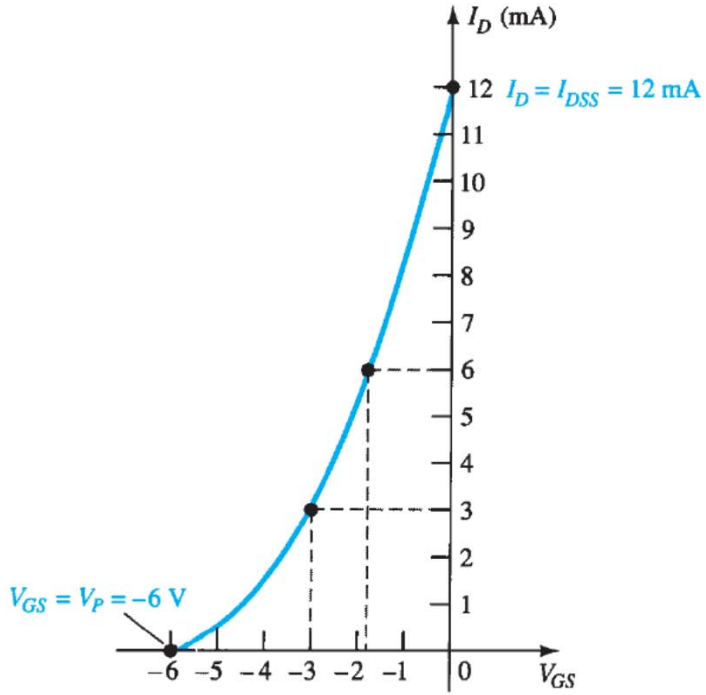


FIG. 6.18
Transfer curve for Example 6.1.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4\text{ mA}$ and $V_P = 3\text{ V}$.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\text{ V}}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\text{ mA}}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\text{ mA}}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\text{ V}}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

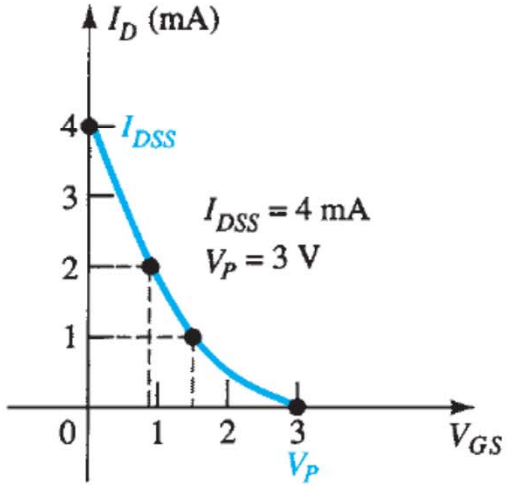


FIG. 6.19
Transfer curve for the p-channel device of Example 6.2.

IMPORTANT RELATIONSHIPS

TABLE 6.2

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$