General Electronics II

3rd April 2018 (Tue.)

Room: E202 10:30-12:00

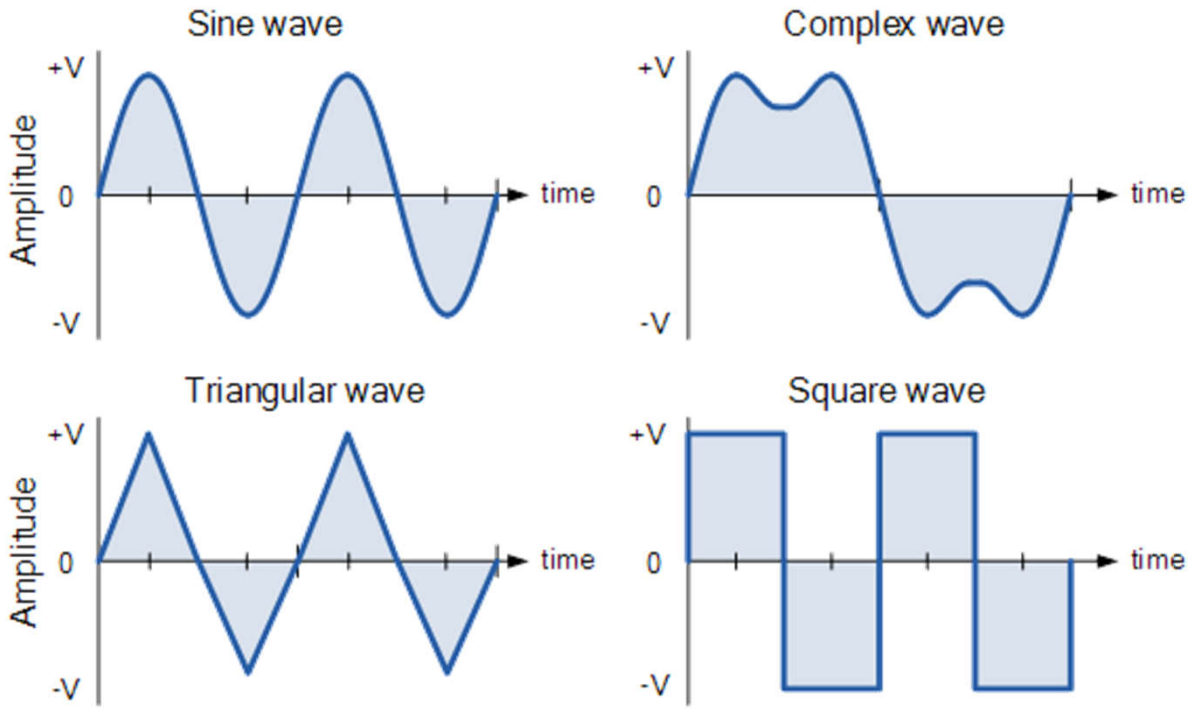
ผู้สอน : ดร. อัจฉรา พิเชฐจำเริญ

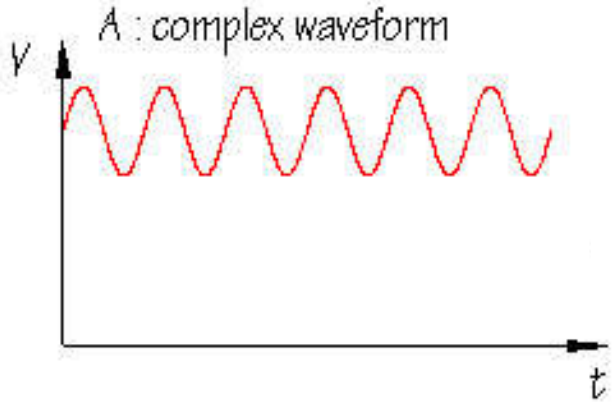
BJT AC Analysis

Outline:

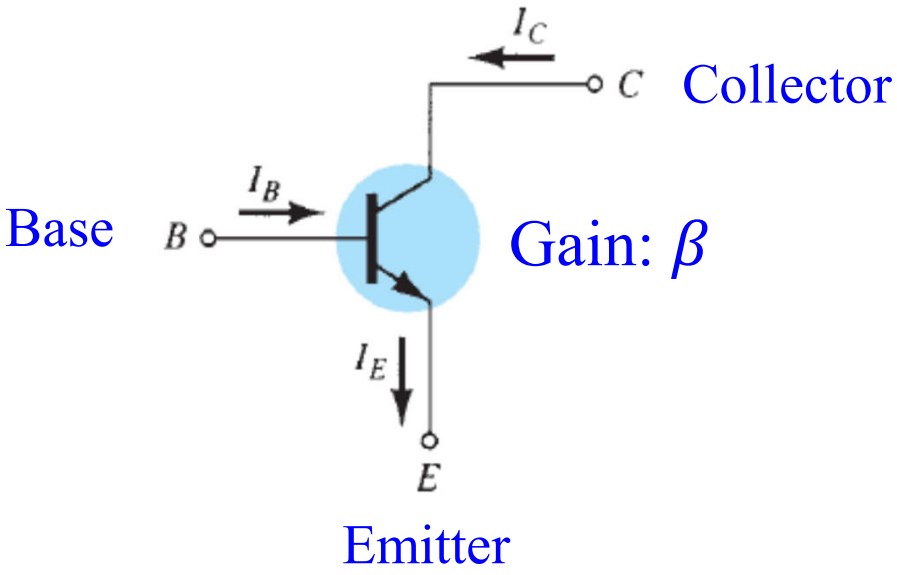
- Review of ac
- r_e model
- Common-Emitter Fixed-Bias Configuration
- Voltage-Divider Bias
- CE Emitter-Bias Configuration

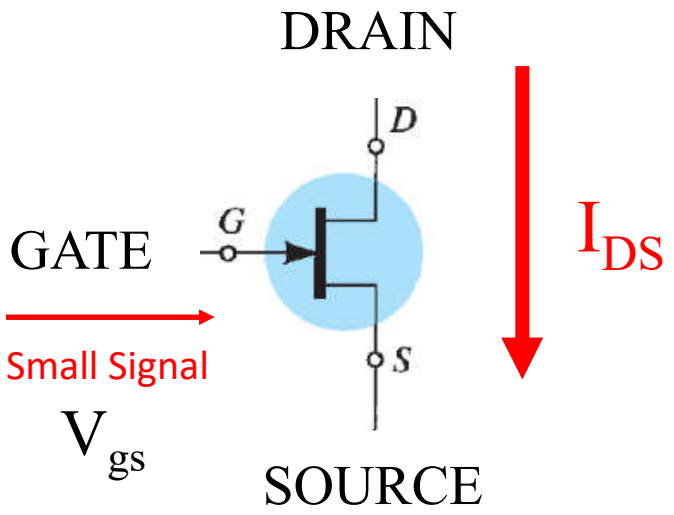
AC waveform


Sine wave
+V
0
-V
Amplitude
time
Complex wave
+V
0
-V
time
Triangular wave
+V
0
-V
Amplitude
time
Square wave
+V
0
-V
time


A : complex waveform
V
t

Review:





How large of I_C, I_B, I_E ?

BJT = Current control device
FET = Voltage control device

BJT has β (beta)
FET has g_m transconductance factor

Amplifier Modeling:

- Approximation of device behavior to Equivalent circuit.

- Apply with circuit analysis theory to solve the parameters.

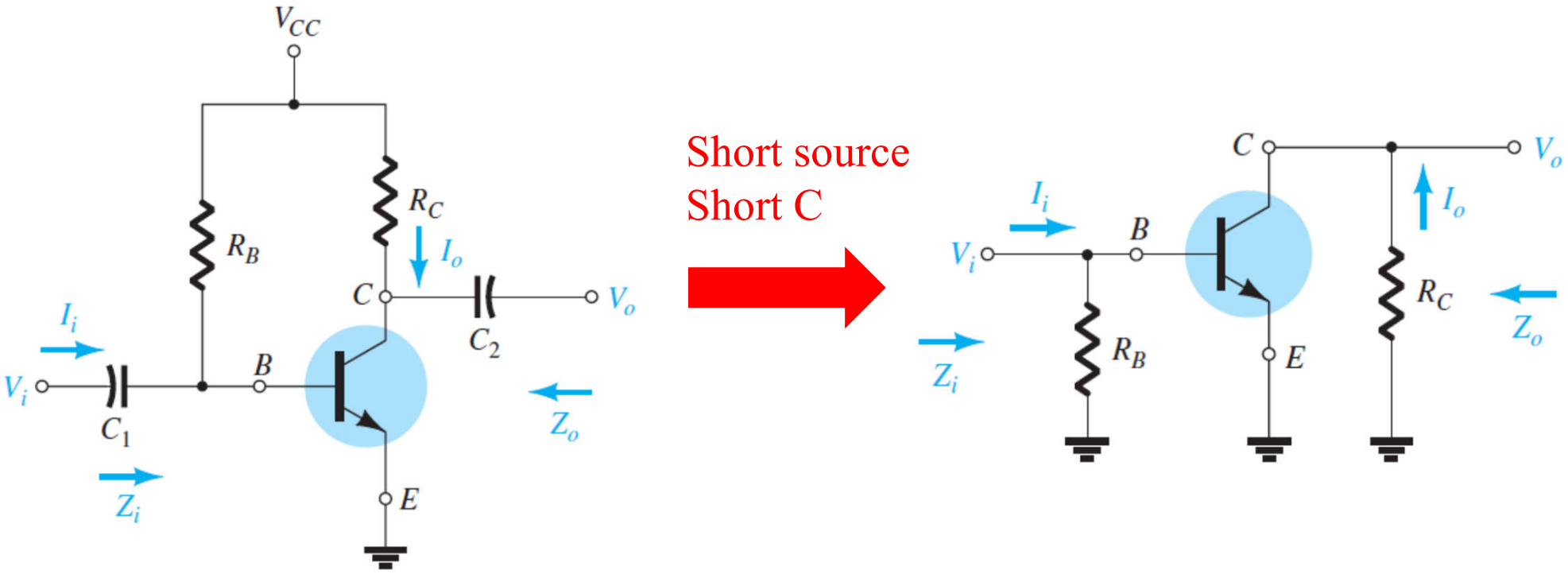
1. Hybrid Equivalent Network → data sheet data

2. r_e model → actual operation data but no feedback terms

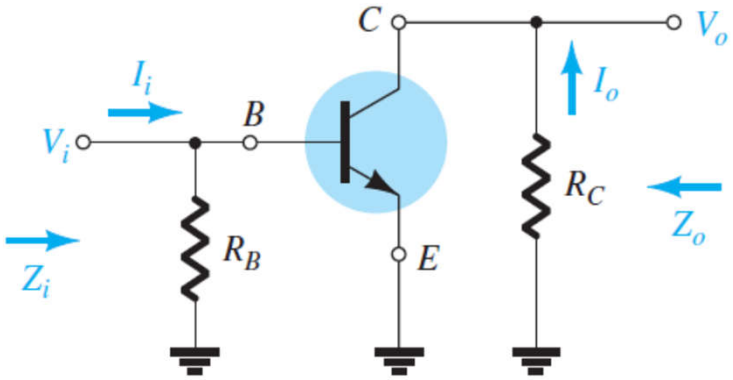
3. Two-port system

r_e Transister Model

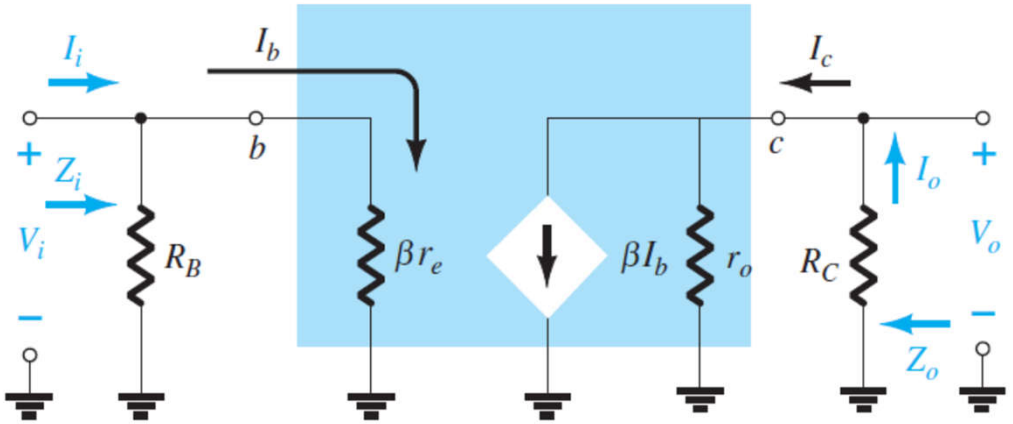
Common-Emitter Fixed-Bias Configuration



Transform to r_e model



Parameters



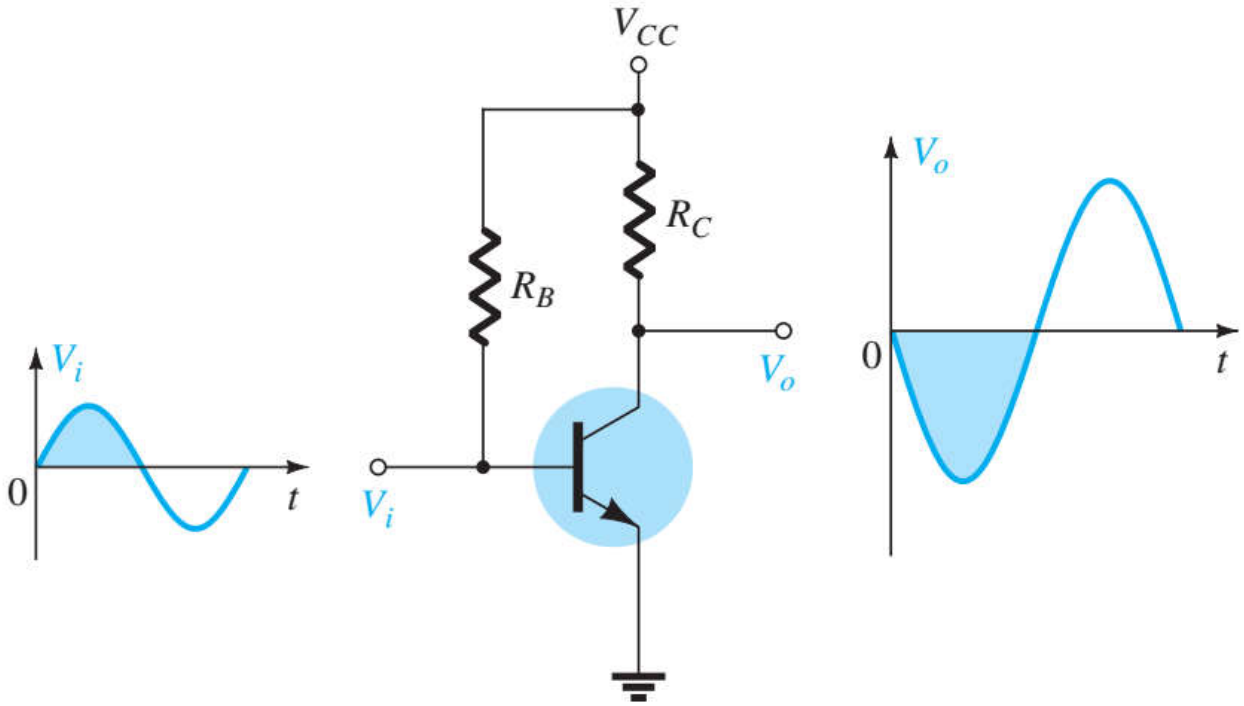
Z_i =

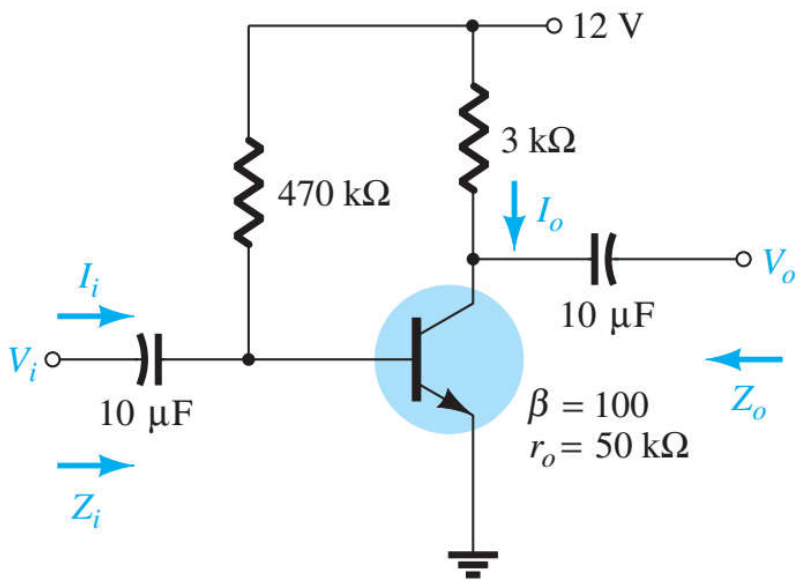
$$r_e = \frac{26\ mV}{I_E}$$

$V_i = 0$; Z_o =

A_v =

180° phase shift





a. Determine r_e.
b. Find Z_i (with $r_o = \infty\,\Omega$).
c. Calculate Z_o (with $r_o = \infty\,\Omega$).
d. Determine A_v (with $r_o = \infty\,\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all calculations and compare results.

VOLTAGE-DIVIDER BIAS