

Field-Effect Transistors

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET),
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET,

The BJT transistor is a current-controlled device as depicted in Fig. 6.1a , whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b .

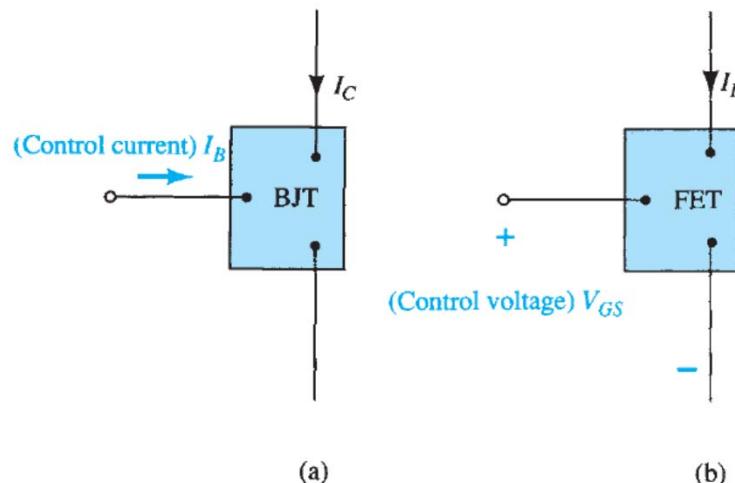


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

Types of FET's

- JFET – Junction Field Effect Transistor
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
 - D-MOSFET - Depletion Mode MOSFET
 - E- MOSFET - Enhancement Mode MOSFET

Construction of the n -channel JFET

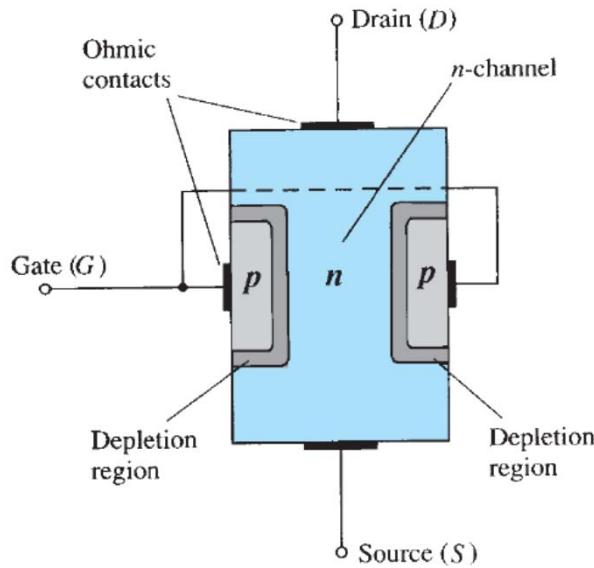


FIG. 6.3
Junction field-effect transistor (JFET).

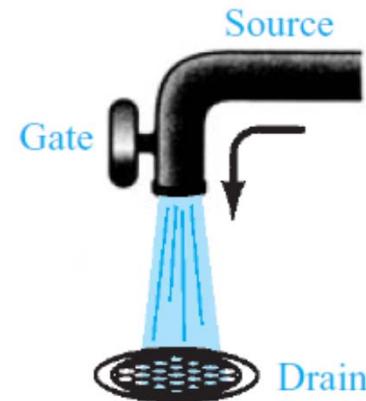


FIG. 6.4
Water analogy for the JFET control mechanism.

- There are two types of JFET's: n-channel and p-channel. The n-channel is more widely used.
- There are three terminals: Drain (D) and Source (S) are connected to n-channel Gate (G) is connected to the p-type material

JFET Operating Characteristics

$V_{GS} = 0 \text{ V}$, V_{DS} Some Positive Value

- The instant the voltage $VDD (=VDS)$ is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5 .
- The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the condition
- In Fig. 6.5 , the flow of charge is relatively uninhibited and is limited solely by the resistance of the n -channel between drain and source.

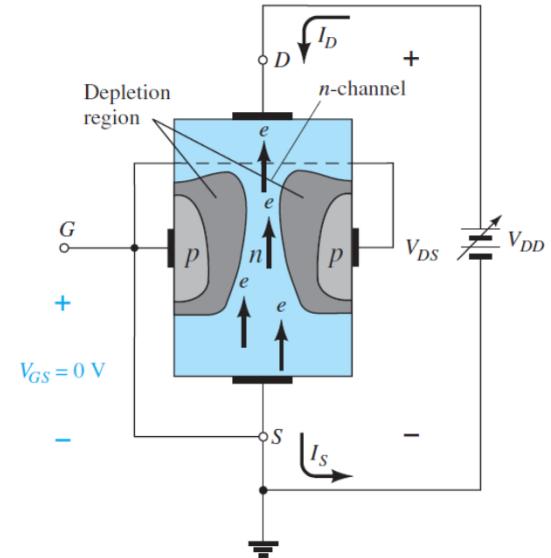


FIG. 6.5
JFET at $V_{GS} = 0 \text{ V}$ and $V_{DS} > 0 \text{ V}$.

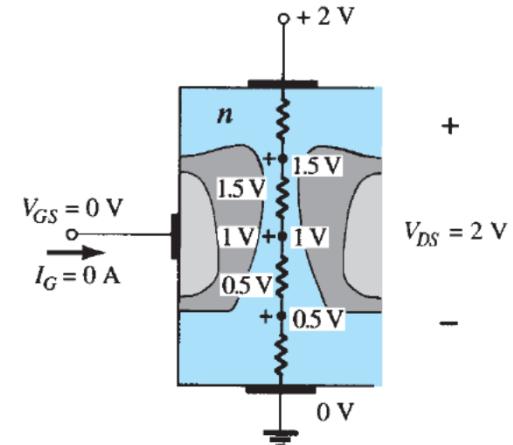


FIG. 6.6
Varying reverse-bias potentials across the p-n junction of an n-channel JFET.

JFET Operating Characteristics

$V_{GS} = 0 \text{ V}$, V_{DS} Some Positive Value

- The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching “infinite” ohms in the horizontal region.
- If V_{DS} is increased to a level where it appears that the two depletion regions would “touch” as shown in Fig. 6.8 , a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P , as shown in Fig. 6.7 .

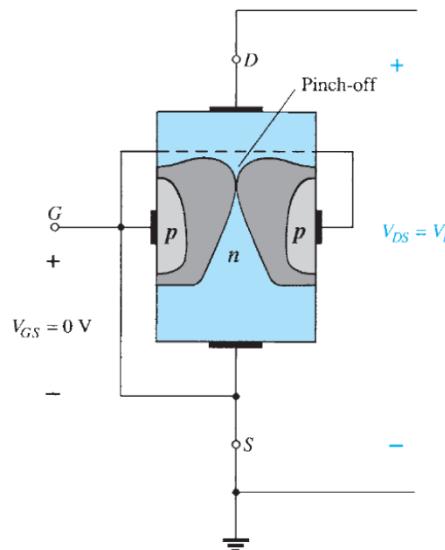


FIG. 6.8
Pinch-off ($V_{GS} = 0 \text{ V}$, $V_{DS} = V_P$).

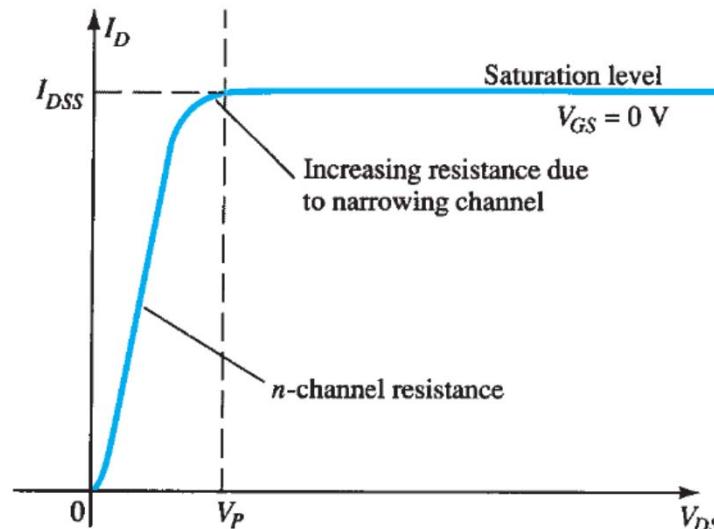


FIG. 6.7
 I_D versus V_{DS} for $V_{GS} = 0 \text{ V}$.

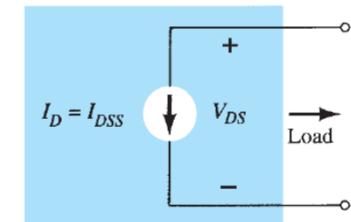


FIG. 6.9
Current source equivalent for
 $V_{GS} = 0 \text{ V}$, $V_{DS} > V_P$.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0 \text{ V}$ and $V_{DS} > |V_P|$.

JFET Operating Characteristics

$V_{GS} < 0 \text{ V}$

- The voltage from gate to source, denoted V_{GS} , is the controlling voltage of the JFET.
- Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET

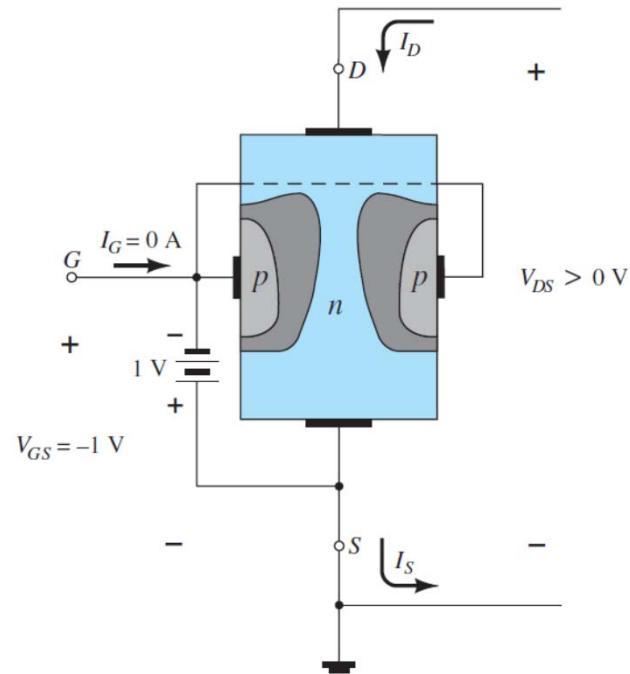


FIG. 6.10

Application of a negative voltage to the gate of a JFET.

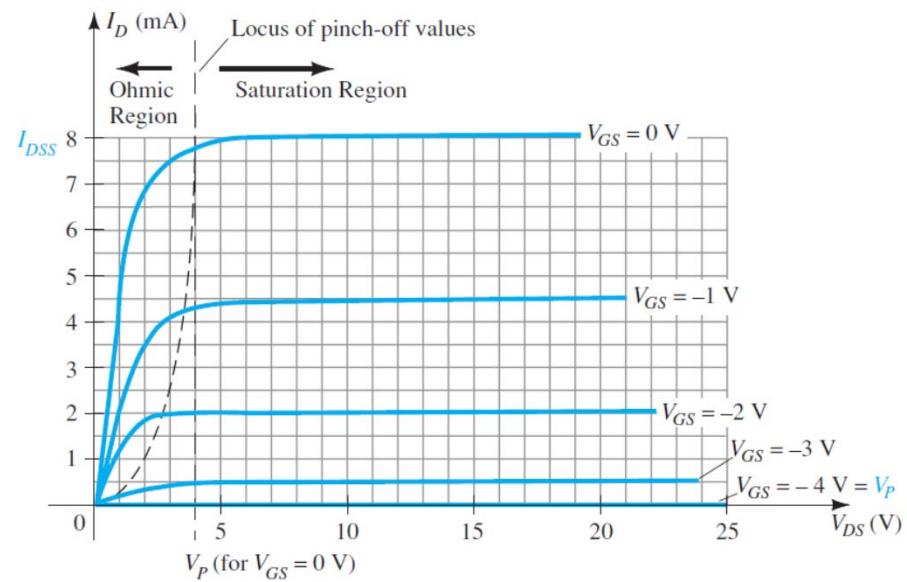


FIG. 6.11

n-Channel JFET characteristics with $I_{DSS} = 8 \text{ mA}$ and $V_p = -4 \text{ V}$.

The level of V_{GS} that results in $I_D = 0 \text{ mA}$ is defined by $V_{GS} = V_p$, with V_p being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

JFET Operating Characteristics: *p*-Channel Devices

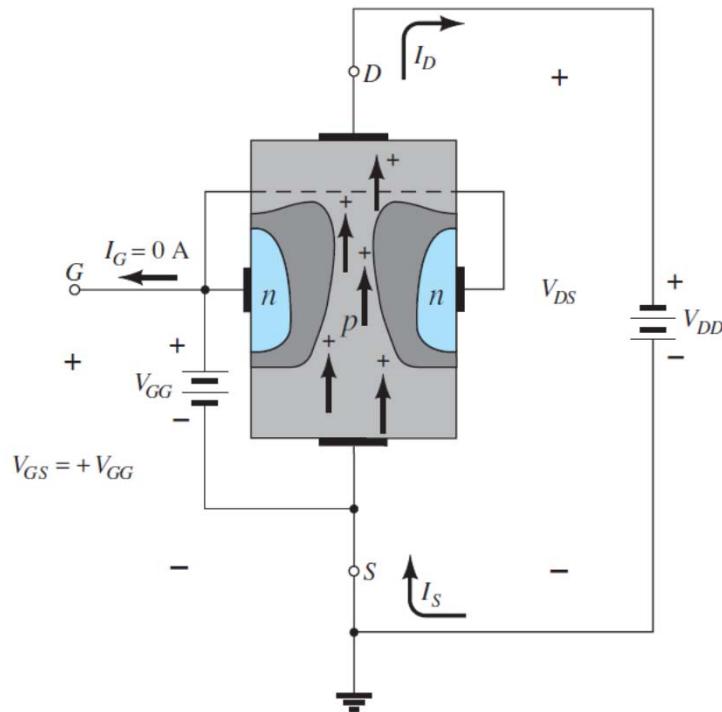


FIG. 6.12
p-Channel JFET.

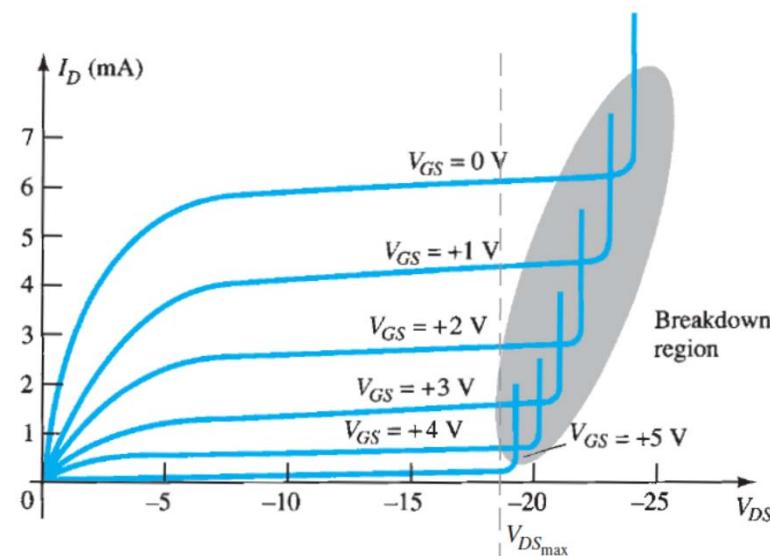


FIG. 6.13
p-Channel JFET characteristics with $I_{DSS} = 6 \text{ mA}$ and $V_P = +6 \text{ V}$.

- For the p -channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.13 , which has an I_{DSS} of 6 mA and a pinch off voltage of $V_{GS} = +6 \text{ V}$.

JFET Operating Characteristics

There are three basic operating conditions for a JFET:

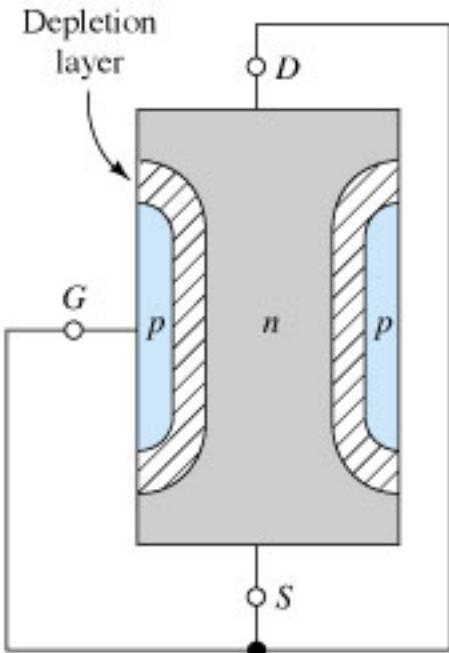
JFET's operate in the depletion mode only

- $V_{GS} = 0$, V_{DS} is a minimum value depending on ID_{SS} and the drain and source resistance
- $V_{GS} < 0$, V_{DS} at some positive value and
- Device is operating as a Voltage-Controlled Resistor

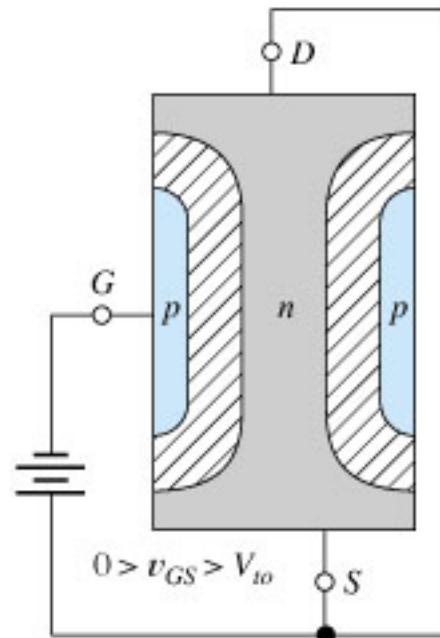
For an n channel JFET, V_{GS} may never be positive*

For an p channel JFET, V_{GS} may never be negative*

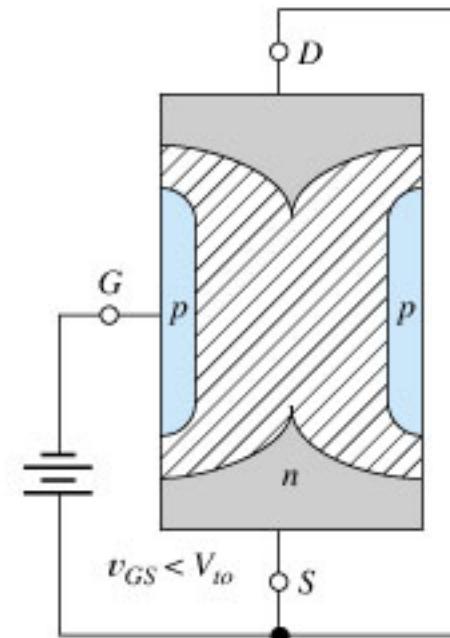
N-Channel JFET Operation



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source



(b) Moderate gate-to-channel reverse bias results in narrower channel



(c) Bias greater than pinch-off voltage; no conductive path from drain to source

The nonconductive depletion region becomes thicker with increased reverse bias.
(Note: The two gate regions of each FET are connected to each other.)

$$|I_D| \leq |I_{DSS}|$$

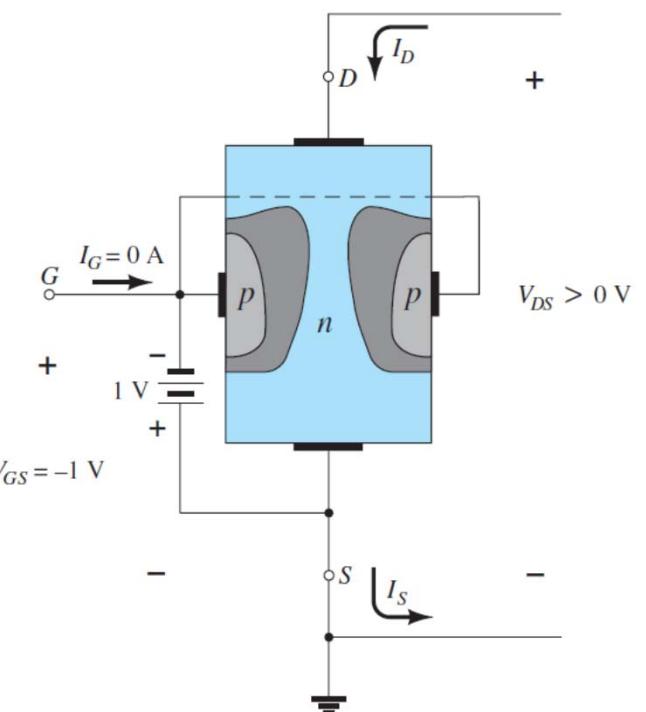
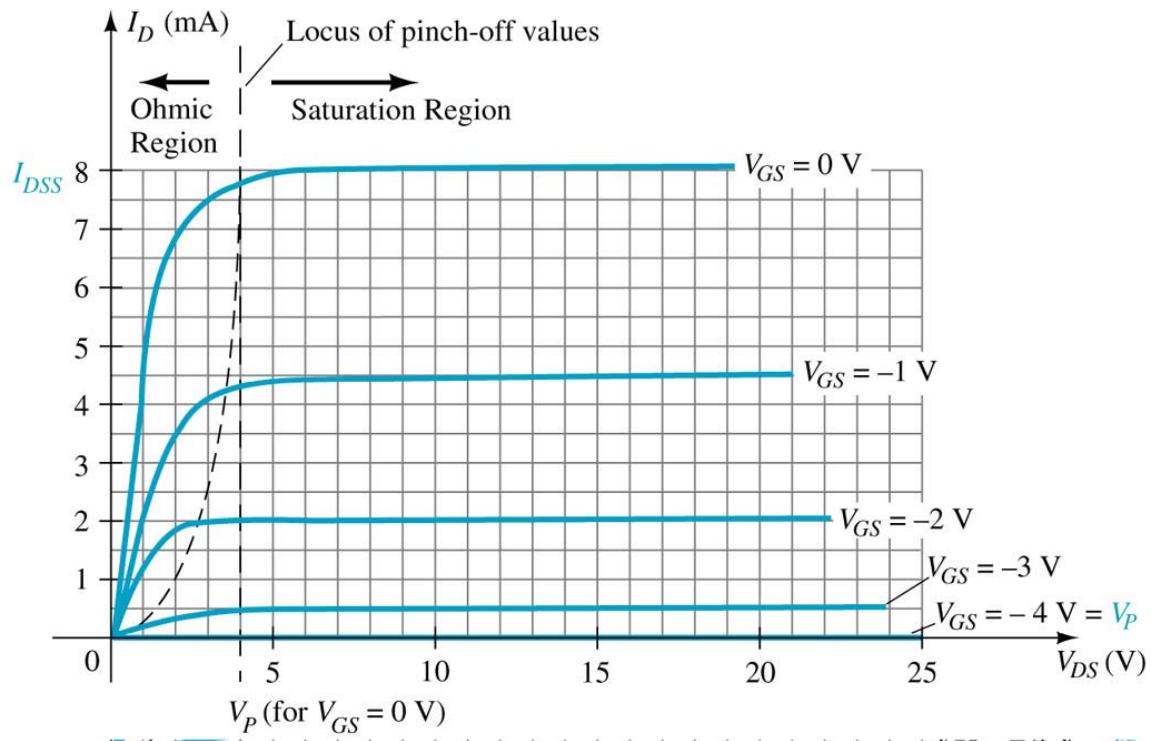


FIG. 6.10

Application of a negative voltage to the gate of a JFET.

As V_{GS} becomes more negative:

- the JFET will pinch-off at a lower voltage (V_p).
- $|I_D|$ decreases ($|I_D| < |I_{DSS}|$) even though V_{DS} is increased.
- Eventually $|I_D|$ will reach 0A. V_{GS} at this point is called V_p or $V_{GS(off)}$.
- Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. $|I_D|$ will increase uncontrollably if $V_{DS} > V_{DSmax}$.

Symbols

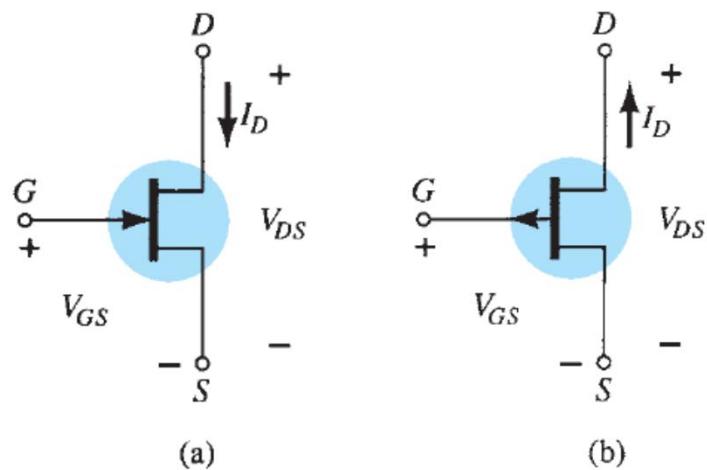
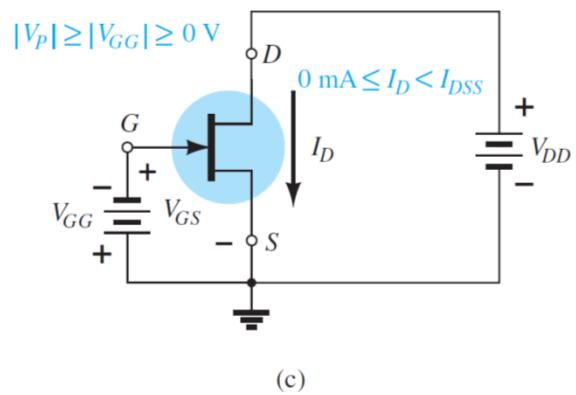
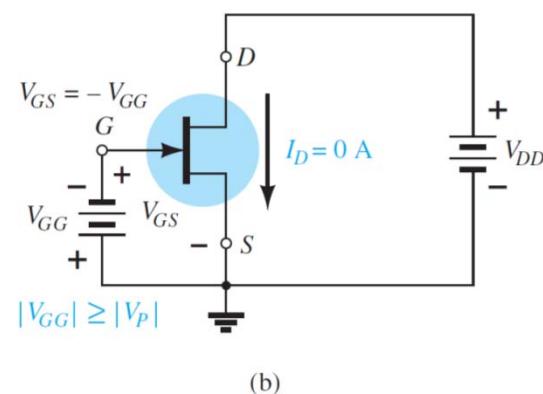
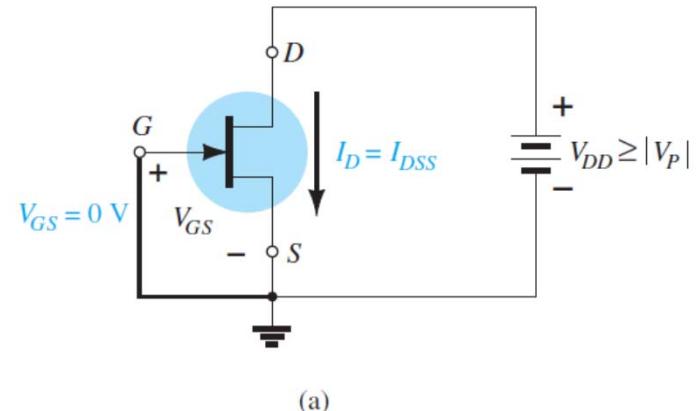


FIG. 6.14

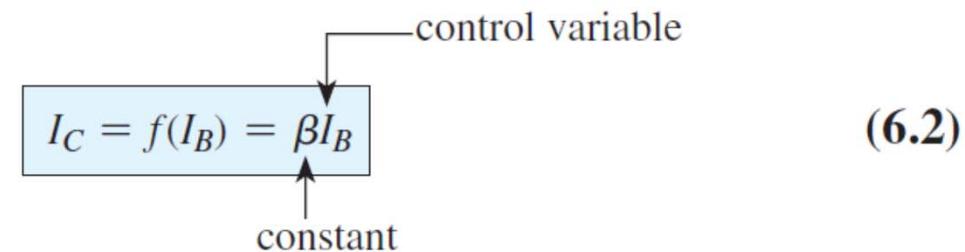
JFET symbols: (a) n-channel; (b) p-channel.

- (a) $V_{GS} = 0$ V, $I_D = I_{DSS}$;
 - (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level;
 - (c) I_D is between 0 A and I_{DSS} for $V_{GS} > 0$ V and greater than the pinch-off level.

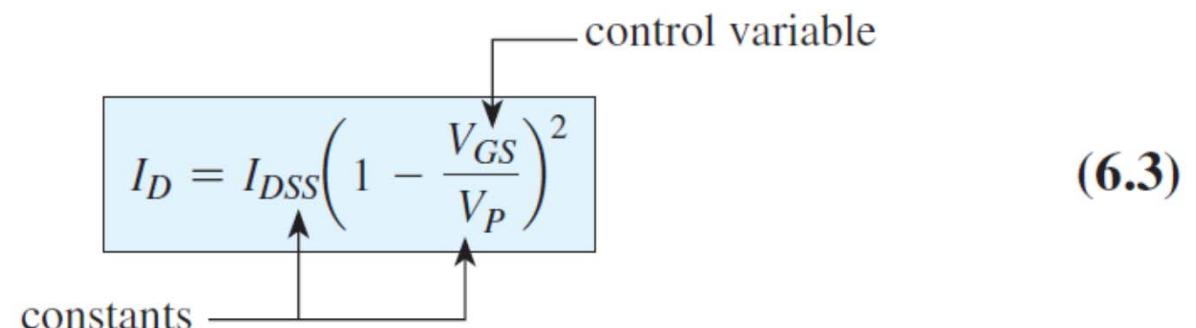


TRANSFER CHARACTERISTICS

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \quad (6.2)$$


Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad (6.3)$$


TRANSFER CHARACTERISTICS

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

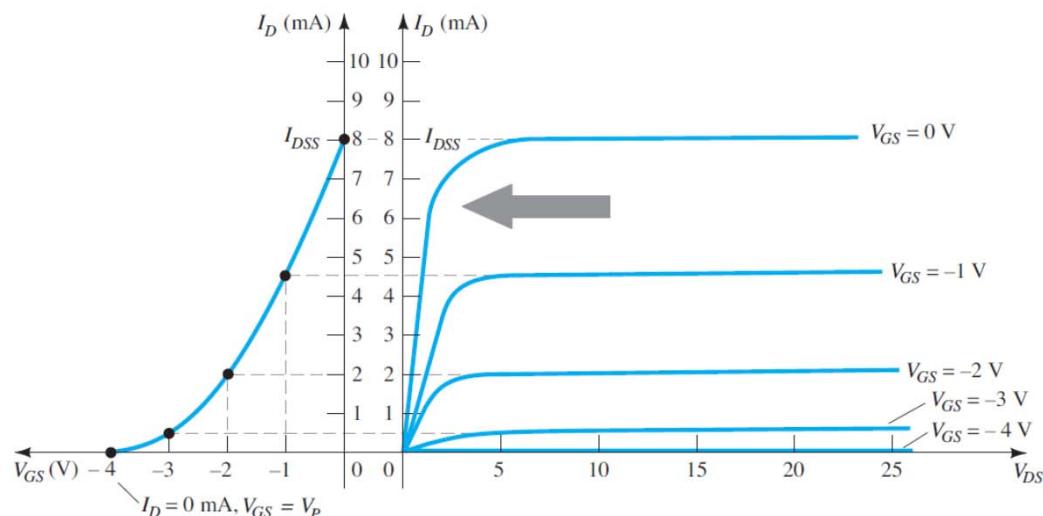


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

For the drain characteristics of Fig. 6.17, if we substitute $V_{GS} = -1 \text{ V}$,

$$\begin{aligned}
 I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \\
 &= 8 \text{ mA} \left(1 - \frac{-1 \text{ V}}{-4 \text{ V}} \right)^2 = 8 \text{ mA} \left(1 - \frac{1}{4} \right)^2 = 8 \text{ mA} (0.75)^2 \\
 &= 8 \text{ mA} (0.5625) \\
 &= \mathbf{4.5 \text{ mA}}
 \end{aligned}$$

$$\boxed{\text{When } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS}}$$

$$\boxed{\text{When } V_{GS} = V_P, \quad I_D = 0 \text{ mA}}$$

Applying Shockley's Equation

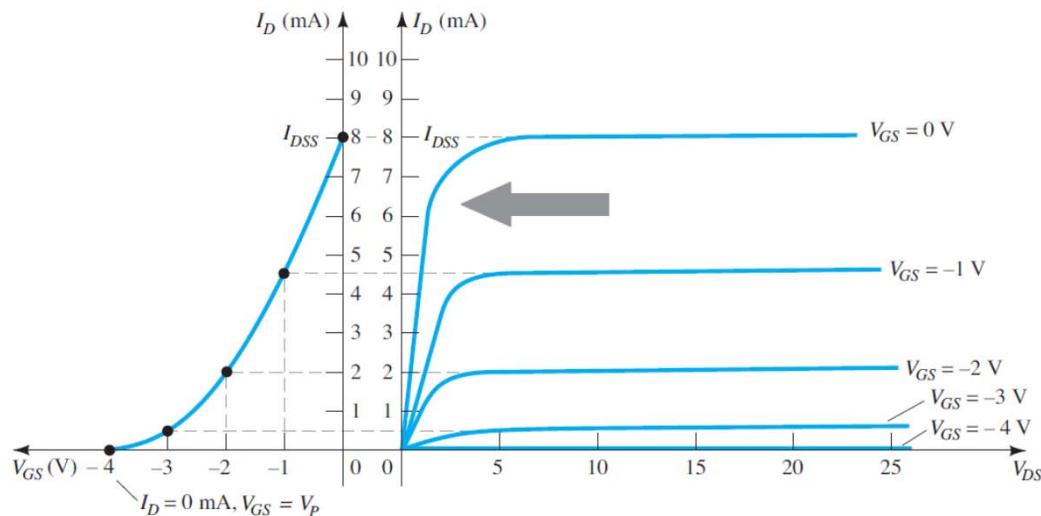
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$\boxed{I_D = I_{DSS} \mid V_{GS}=0 \text{ V}}$$

$$\boxed{I_D = 0 \text{ A} \mid V_{GS}=V_P}$$

TRANSFER CHARACTERISTICS

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.



$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

$$\begin{aligned}
 V_{GS} &= -4 \text{ V} \left(1 - \sqrt{\frac{4.5 \text{ mA}}{8 \text{ mA}}} \right) \\
 &= -4 \text{ V} (1 - \sqrt{0.5625}) = -4 \text{ V} (1 - 0.75) \\
 &= -4 \text{ V} (0.25) \\
 &= \mathbf{-1 \text{ V}}
 \end{aligned}$$

TRANSFER CHARACTERISTICS

Shorthand Method

$$\begin{aligned}
 I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \\
 &= I_{DSS} \left(\frac{1 - V_P/2}{V_P} \right)^2 = I_{DSS} \left(1 - \frac{1}{2} \right)^2 = I_{DSS}(0.5)^2 \\
 &= I_{DSS}(0.25)
 \end{aligned}$$

$$I_D = \frac{I_{DSS}}{4} \Big|_{V_{GS} = V_P/2}$$

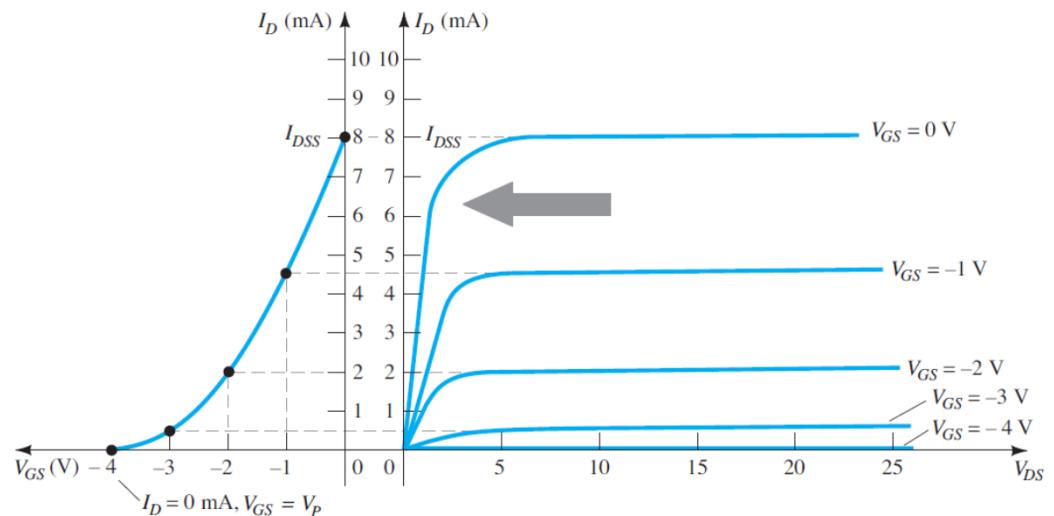


FIG. 6.17

Obtaining the transfer curve from the drain characteristics.

$$\begin{aligned}
 V_{GS} &= V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right) \\
 &= V_P \left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}} \right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)
 \end{aligned}$$

$$V_{GS} \cong 0.3V_P \Big|_{I_D = I_{DSS}/2}$$

TABLE 6.1
 V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12 \text{ mA}$ and $V_P = -6 \text{ V}$.

Solution: Two plot points are defined by

$$I_{DSS} = 12 \text{ mA} \quad \text{and} \quad V_{GS} = 0 \text{ V}$$

and

$$I_D = 0 \text{ mA} \quad \text{and} \quad V_{GS} = V_P$$

At $V_{GS} = V_P/2 = -6 \text{ V}/2 = -3 \text{ V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12 \text{ mA}/4 = 3 \text{ mA}$. At $I_D = I_{DSS}/2 = 12 \text{ mA}/2 = 6 \text{ mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

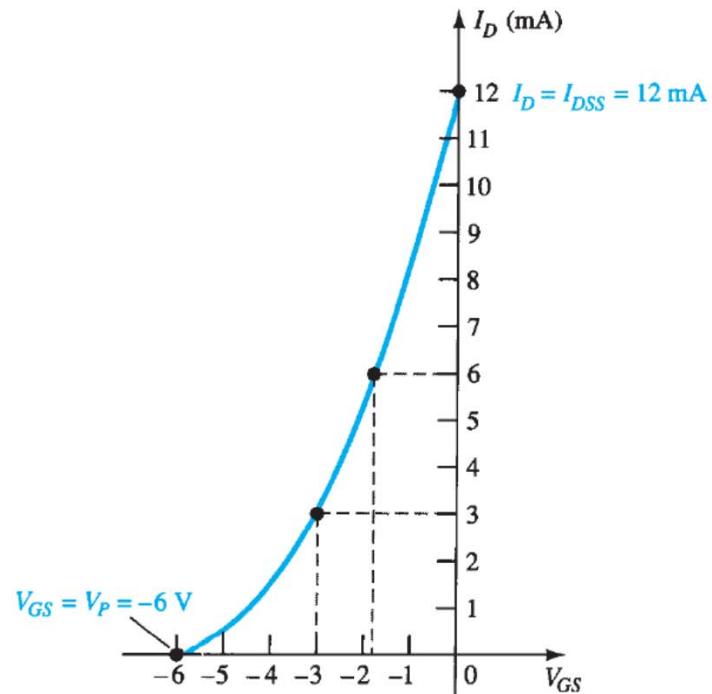


FIG. 6.18
Transfer curve for Example 6.1.

EXAMPLE 6.2 Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4 \text{ mA}$ and $V_P = 3 \text{ V}$.

Solution: At $V_{GS} = V_P/2 = 3 \text{ V}/2 = 1.5 \text{ V}$, $I_D = I_{DSS}/4 = 4 \text{ mA}/4 = 1 \text{ mA}$. At $I_D = I_{DSS}/2 = 4 \text{ mA}/2 = 2 \text{ mA}$, $V_{GS} = 0.3V_P = 0.3(3 \text{ V}) = 0.9 \text{ V}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P .

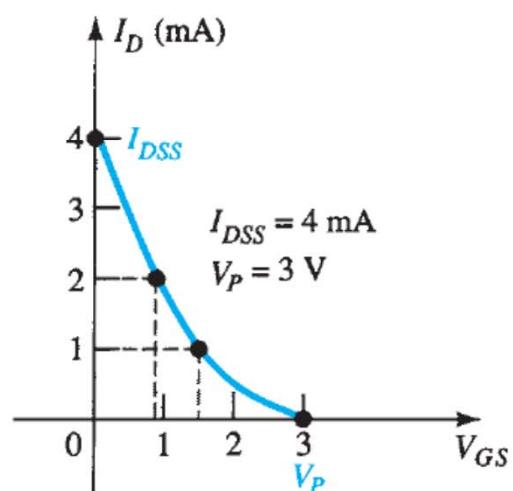


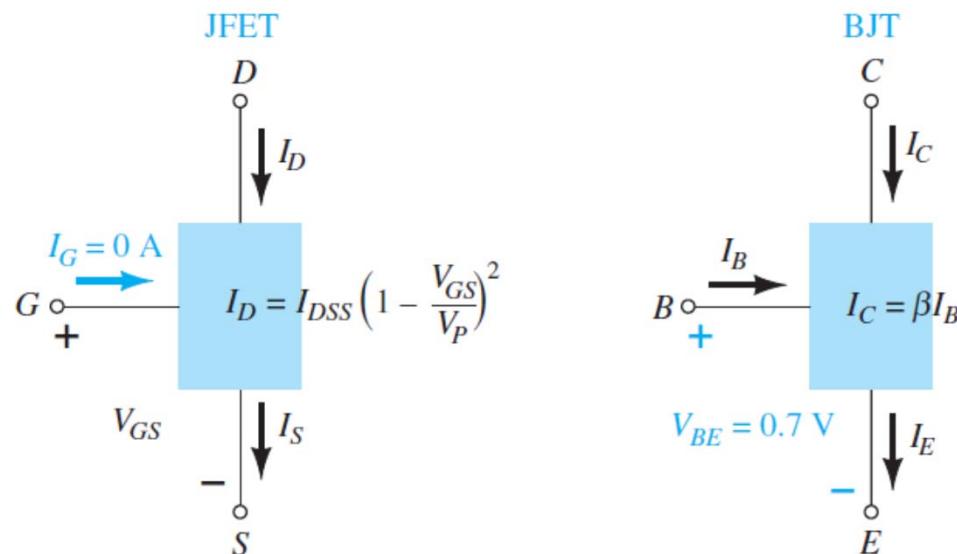
FIG. 6.19

Transfer curve for the p-channel device of Example 6.2.

IMPORTANT RELATIONSHIPS

TABLE 6.2

<i>JFET</i>	<i>BJT</i>
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$	$\Leftrightarrow I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow I_C \cong I_E$
$I_G \cong 0 \text{ A}$	$\Leftrightarrow V_{BE} \cong 0.7 \text{ V}$



MOSFET's

MOSFETs

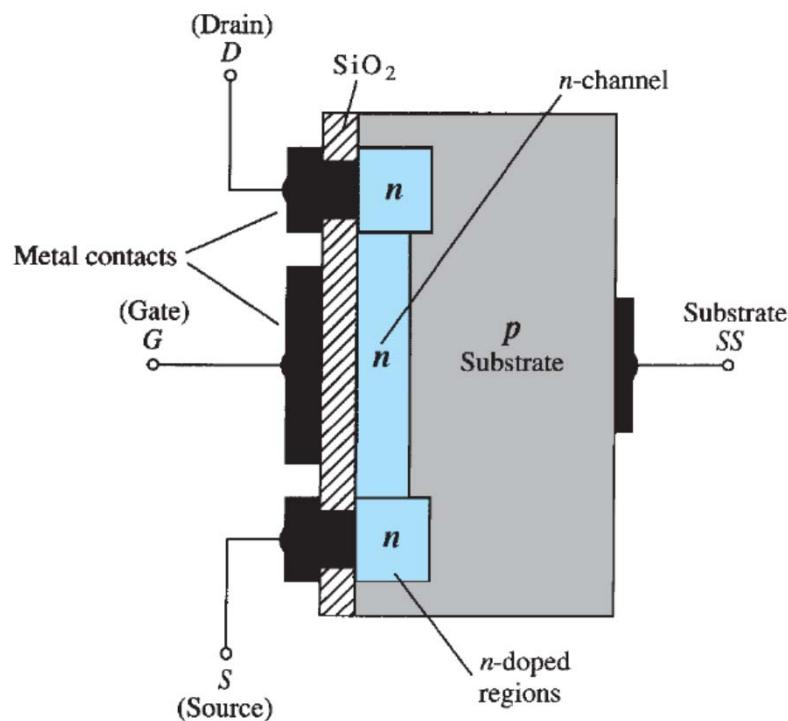
MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful

There are 2 types of MOSFET's:

- Depletion mode MOSFET (D-MOSFET)
 - Operates in Depletion mode the same way as a JFET when $V_{GS} \leq 0$
 - Operates in Enhancement mode like E-MOSFET when $V_{GS} > 0$
- **Enhancement Mode MOSFET (E-MOSFET)**
 - Operates in Enhancement mode
 - $I_{DSs} = 0$ until $V_{GS} > V_T$ (threshold voltage)

Basic construction of the n -channel depletion-type MOSFET

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.



- It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.
- Because of the very high input impedance, the gate current I_G is essentially ~ 0 A for dc biased configurations.

FIG. 6.24

n-Channel depletion-type MOSFET.

Basic Operation and Characteristics

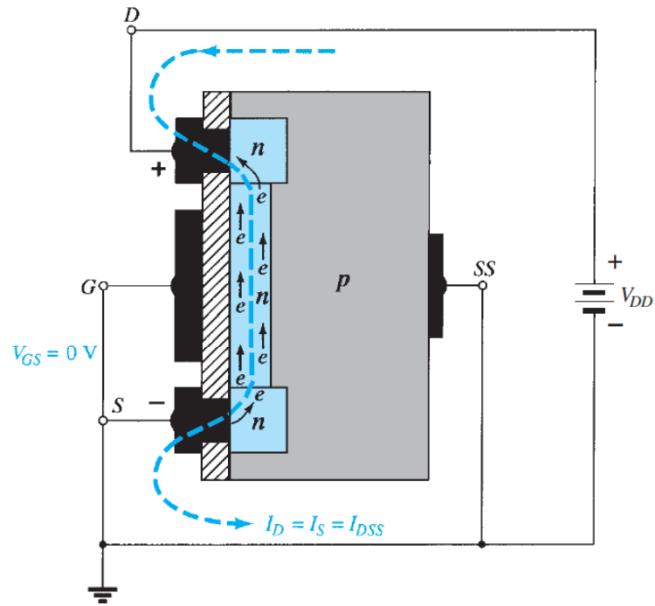


FIG. 6.25

n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD} .

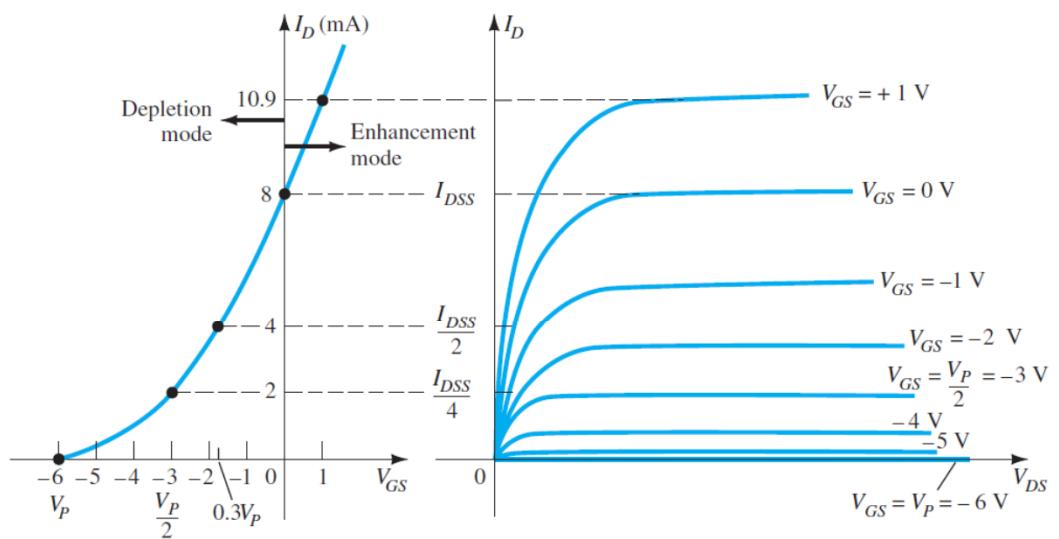


FIG. 6.26

Drain and transfer characteristics for an n-channel depletion-type MOSFET.

- the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals.
- The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS} ,

Basic Operation and Characteristics

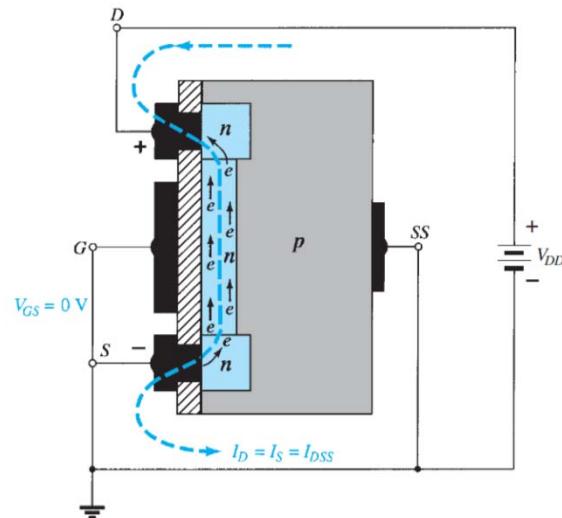


FIG. 6.25
n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD} .

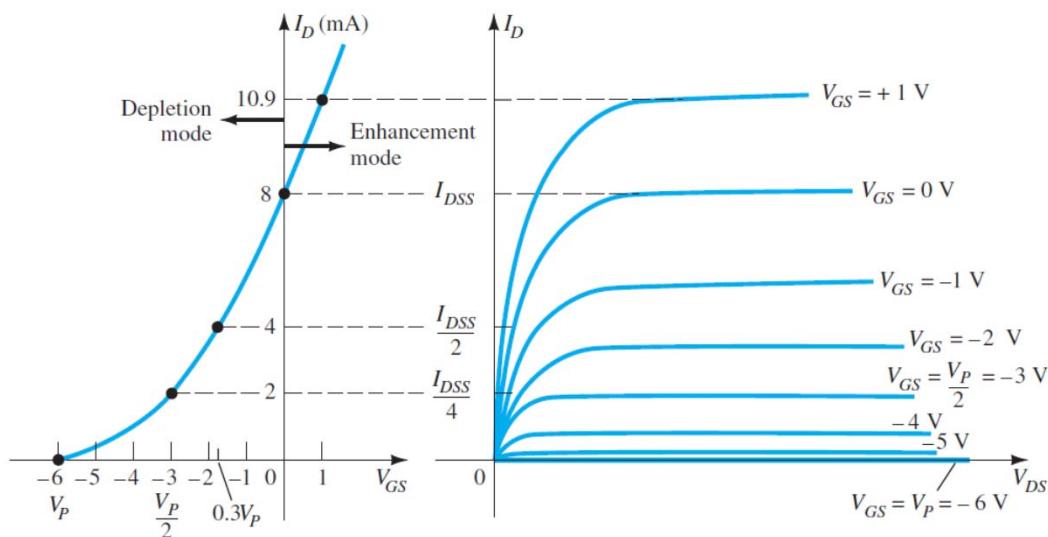


FIG. 6.26
Drain and transfer characteristics for an n-channel depletion-type MOSFET.

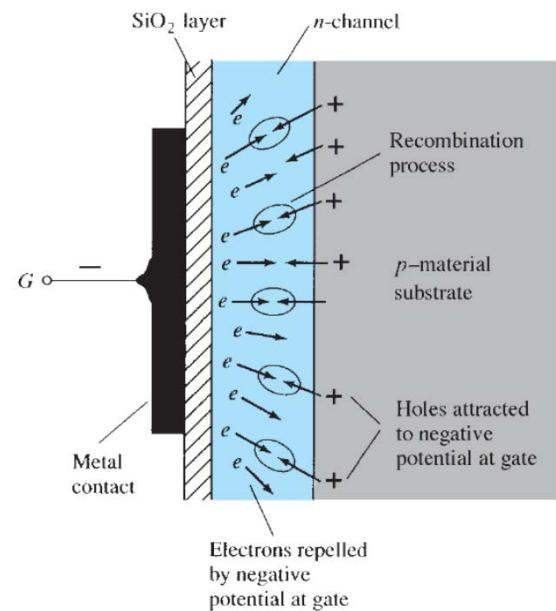


FIG. 6.27
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

Depletion region

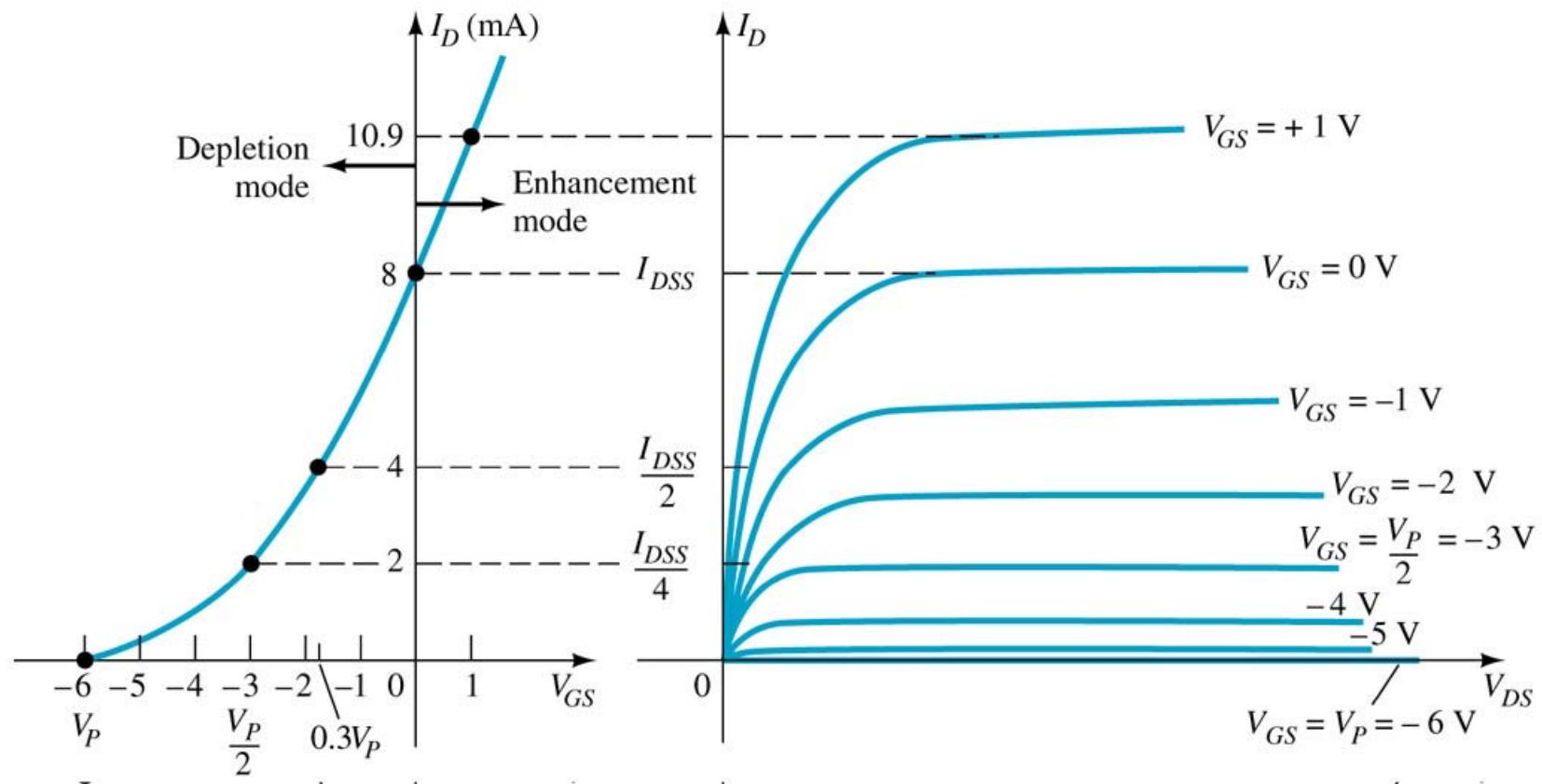
- The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} ,

Enhancement region

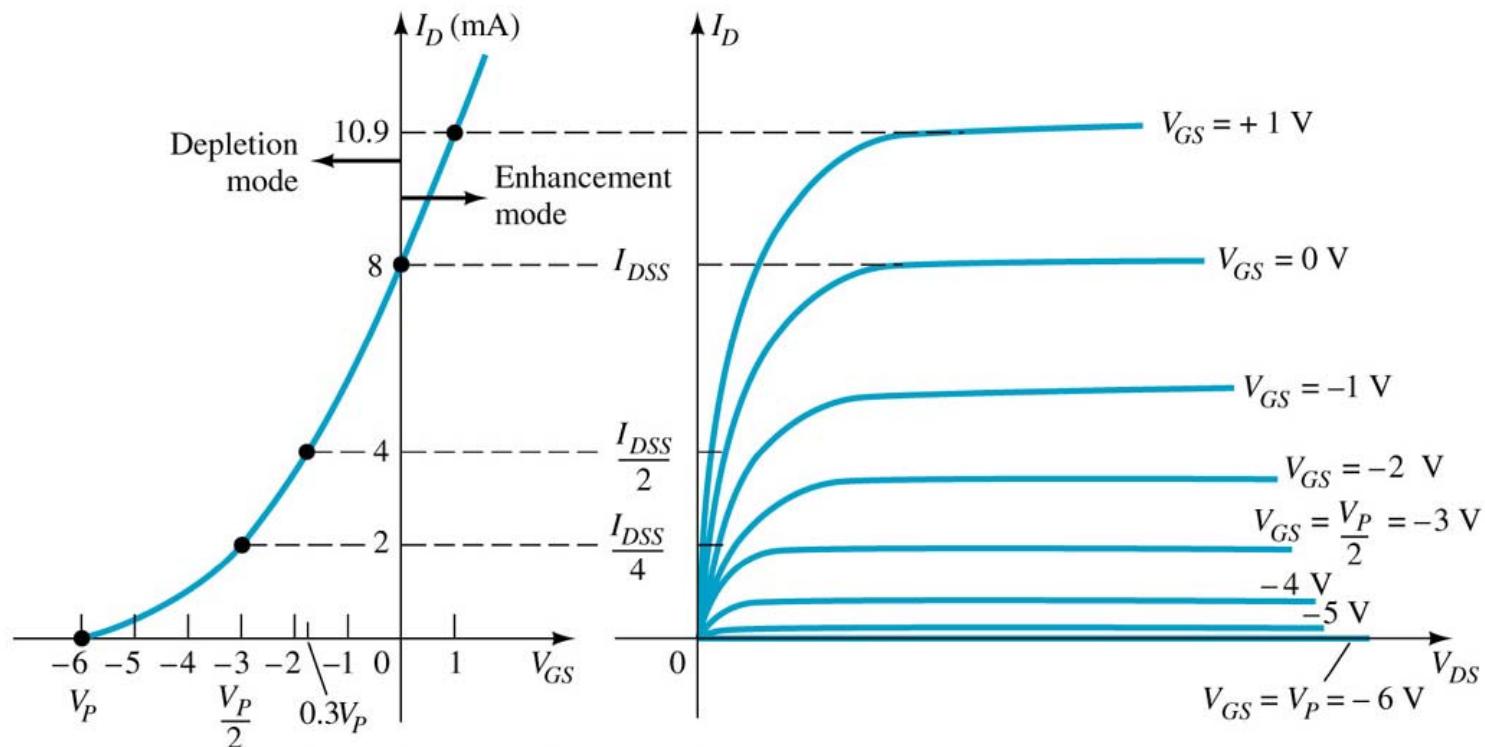
- For positive values of V_{GS} , the positive gate will draw additional electrons (free carriers) from the p-type substrate

Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



D-MOSFET Depletion Mode Operation



The transfer characteristics are similar to the JFET

In Depletion Mode operation:

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} < 0$ V, $I_D < I_{DSS}$

When $V_{GS} > 0$ V, $I_D > I_{DSS}$

The formula used to plot the Transfer Curve, is:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

EXAMPLE 6.3 Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10 \text{ mA}$ and $V_P = -4 \text{ V}$.

Solution:

$$\text{At } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{GS} = V_P = -4 \text{ V}, \quad I_D = 0 \text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

$$\text{and at } I_D = \frac{I_{DSS}}{2},$$

$$V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$$

all of which appear in Fig. 6.28.

Before plotting the positive region of V_{GS} , keep in mind that I_D increases very rapidly with increasing positive values of V_{GS} . In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$\begin{aligned} I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= (10 \text{ mA}) \left(1 - \frac{+1 \text{ V}}{-4 \text{ V}}\right)^2 = (10 \text{ mA}) (1 + 0.25)^2 = (10 \text{ mA}) (1.5625) \\ &\approx 15.63 \text{ mA} \end{aligned}$$

which is sufficiently high to finish the plot.

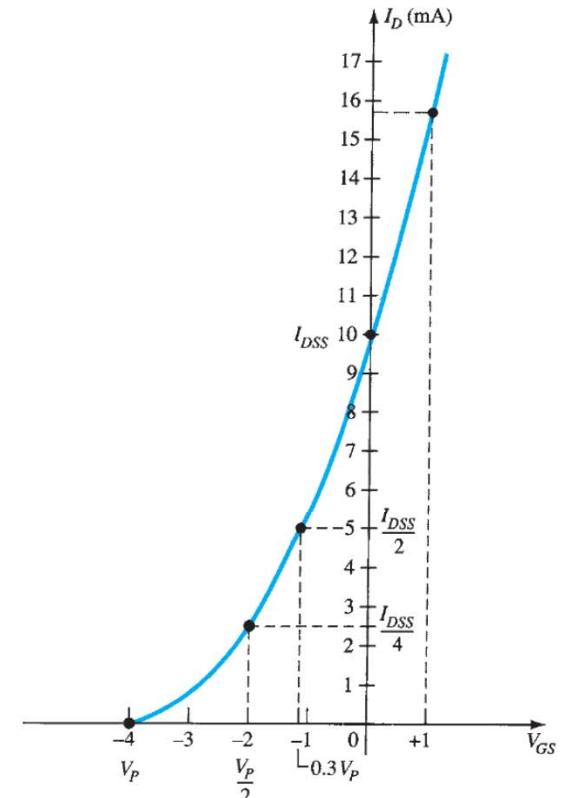


FIG. 6.28
Transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10 \text{ mA}$ and $V_P = -4 \text{ V}$.

p -Channel Depletion-Type MOSFET

The drain characteristics would appear exactly as in Fig. 6.26 , but with V_{DS} having negative values, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 6.29c . The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 6.29b .

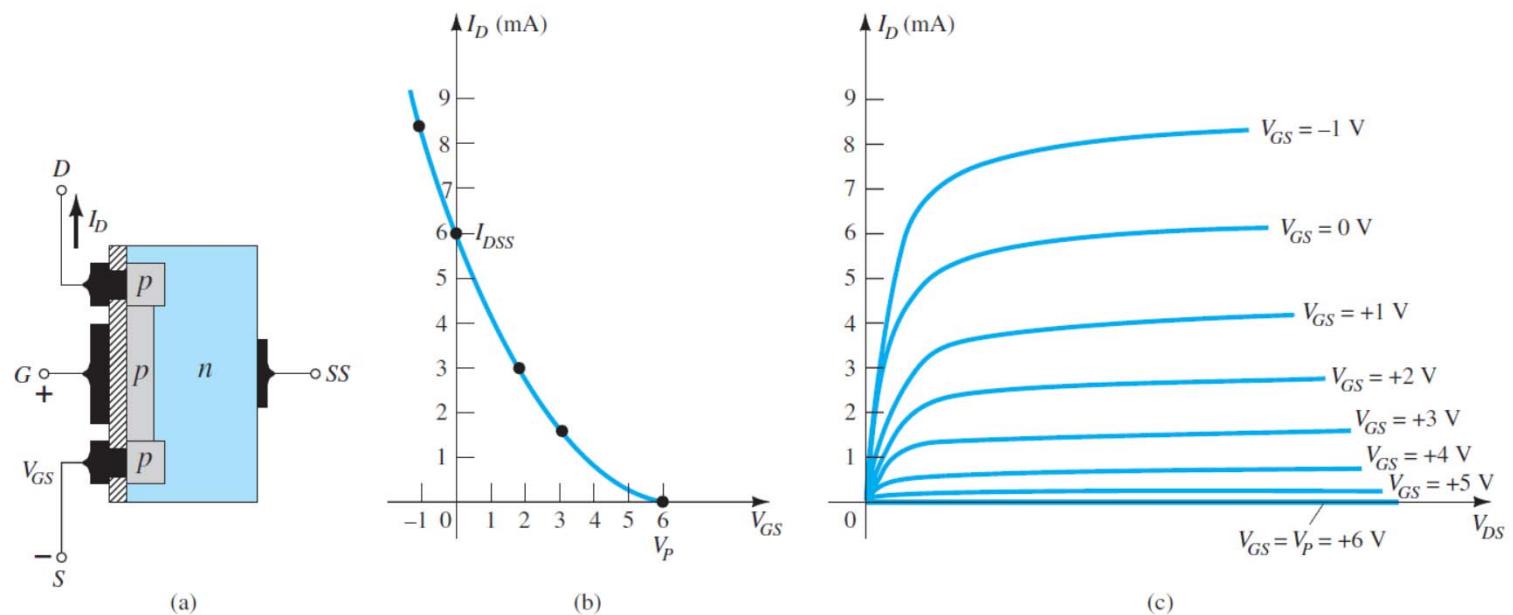
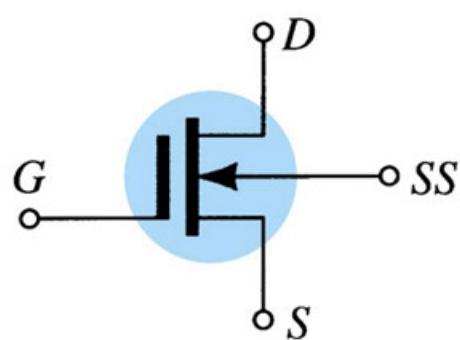


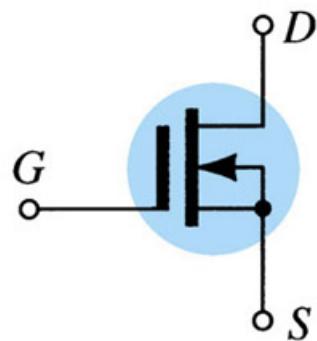
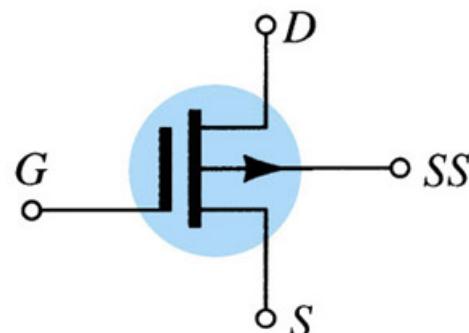
FIG. 6.29
p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

D-MOSFET Symbols

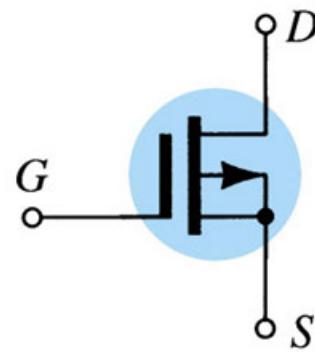
n-channel



p-channel



(a)



(b)

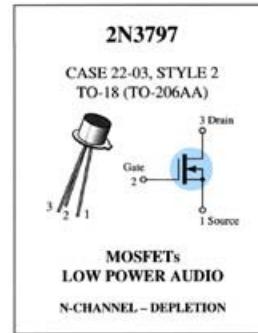
Specification Sheet

MAXIMUM RATINGS			
Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3797	V_{DS}	20	Vdc
Gate-Source Voltage	V_{GS}	± 10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	mW mW/ $^\circ\text{C}$
Junction Temperature Range	T_J	+175	$^\circ\text{C}$
Storage Channel Temperature Range	T_{UG}	-65 to +200	$^\circ\text{C}$

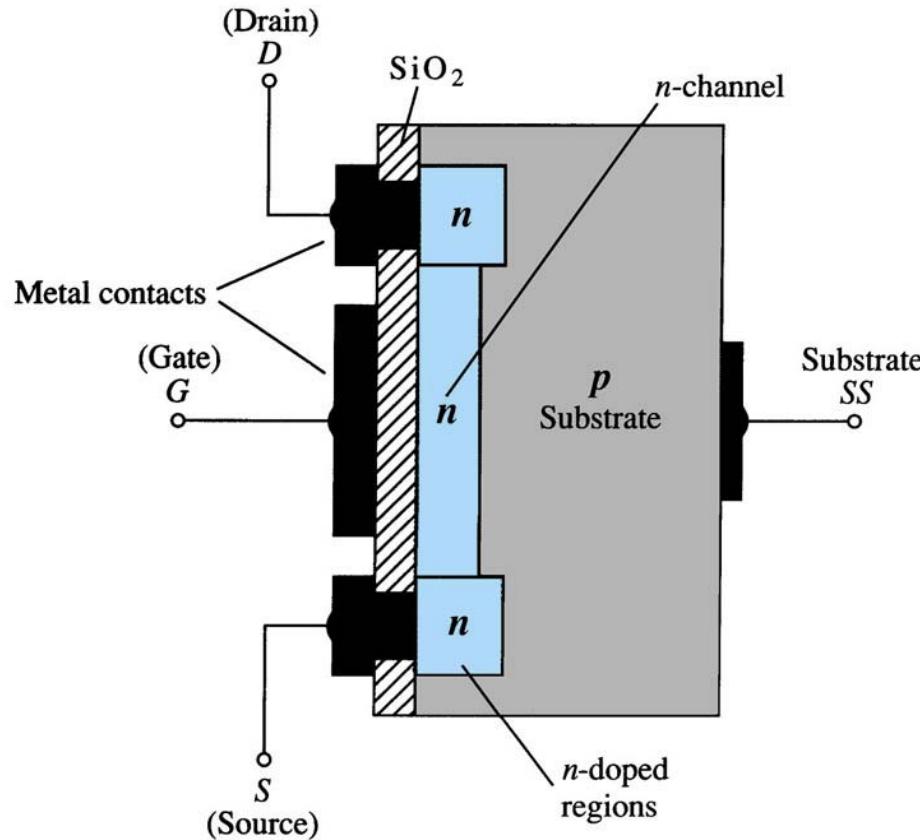
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain Source Breakdown Voltage ($V_{GS} = -7.0 \text{ V}$, $I_D = 5.0 \mu\text{A}$)	$V_{BR(DS)}$	20	25	—	Vdc
Gate Reverse Current (I) ($V_{GS} = -10 \text{ V}$, $V_{DS} = 0$) ($V_{GS} = -10 \text{ V}$, $V_{DS} = 0$, $T_A = 150^\circ\text{C}$)	I_{GDS}	— —	— —	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0 \mu\text{A}$, $V_{DS} = 10 \text{ V}$)	$V_{GS(off)}$	—	-5.0	-7.0	Vdc
Drain-Gate Reverse Current (I) ($V_{DG} = 10 \text{ V}$, $I_g = 0$)	I_{DGO}	—	—	1.0	pAdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$)	$I_{DS(0)}$	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10 \text{ V}$, $V_{GS} = +3.5 \text{ V}$)	$I_{DS(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)	$ Y_{fs} $	1500	2300	3000	μmhos
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)		1500	—	—	
Output Admittance ($I_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)	$ Y_{os} $	—	27	60	μmhos
Input Capacitance ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{in}	—	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)	C_{res}	—	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$, $R_g = 3 \text{ megohms}$)	NF	—	3.8	—	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

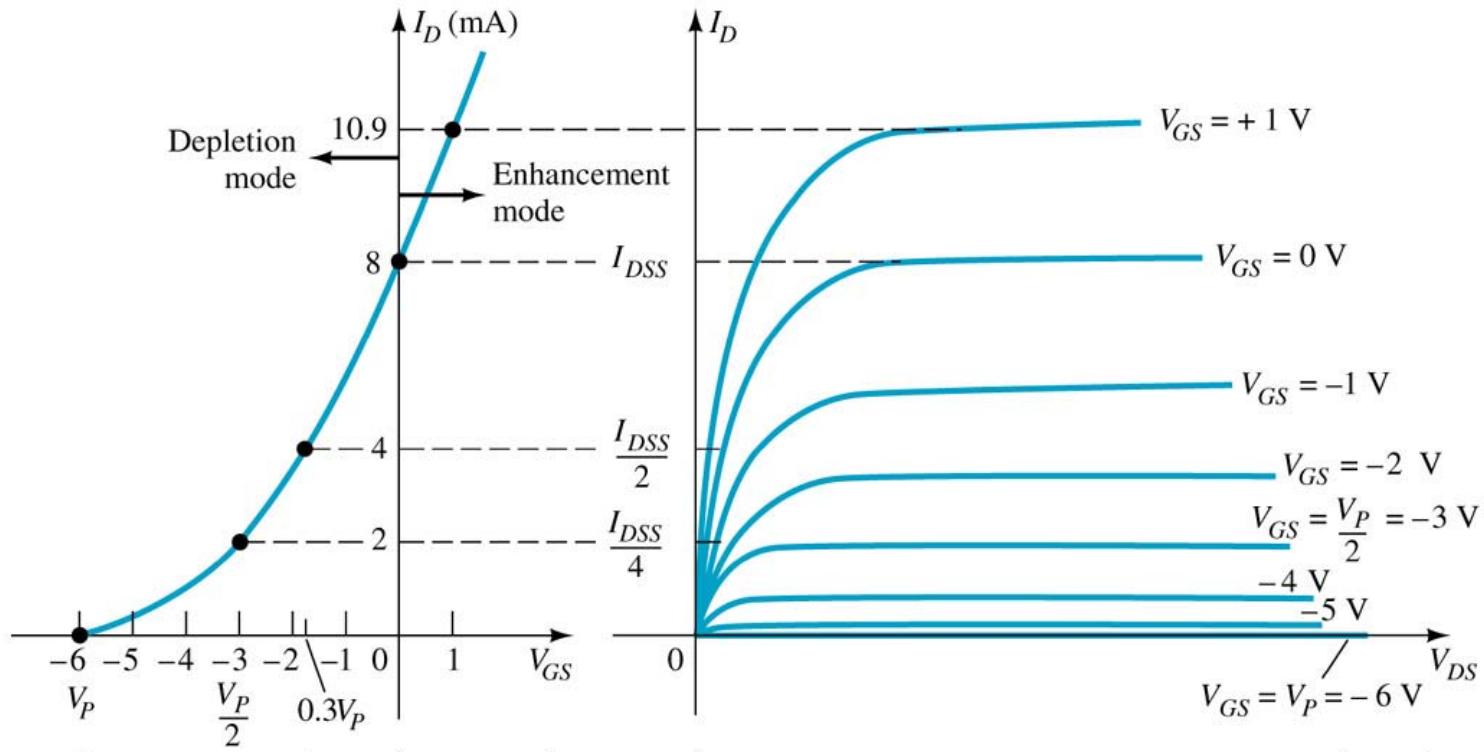


Depletion Mode MOSFET Construction



The Drain (D) and Source (S) leads connect to the n-doped regions. These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2 . The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

D-MOSFET Enhancement Mode Operation

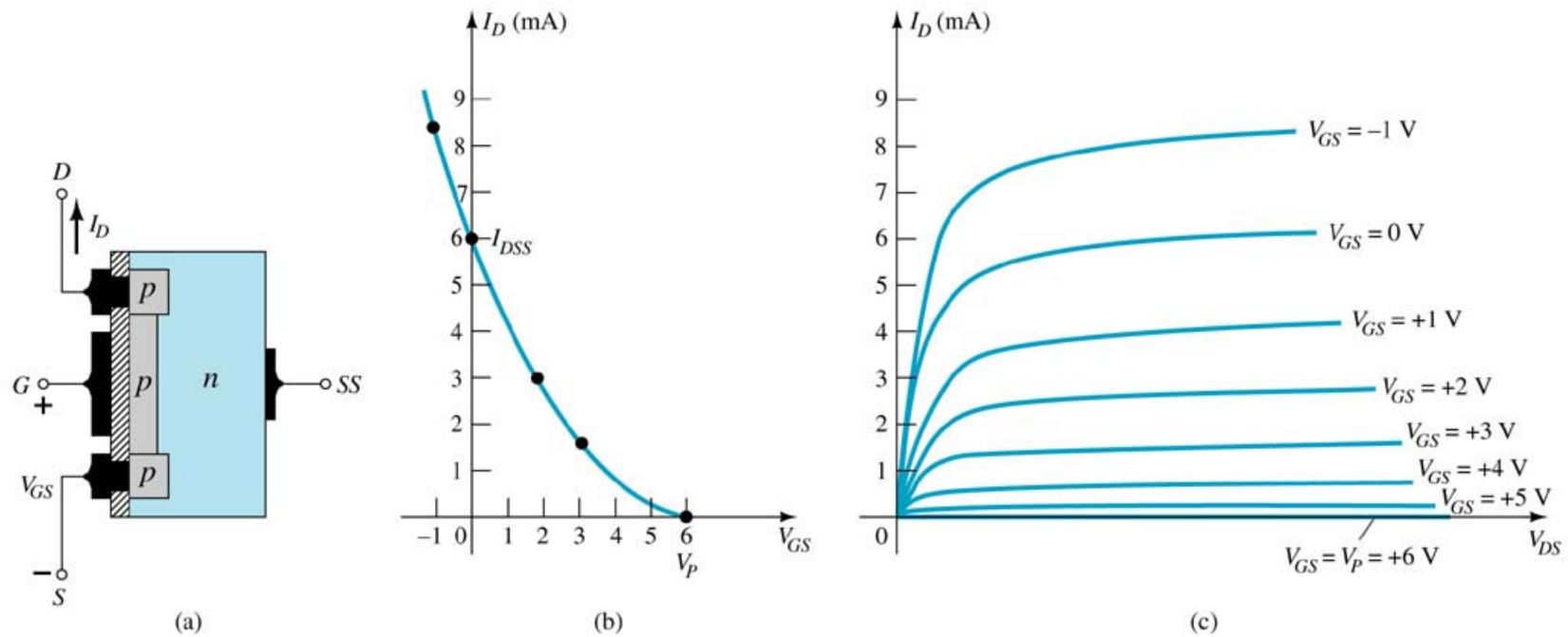


Enhancement Mode operation

In this mode, the transistor operates with $V_{GS} > 0\text{ V}$, and I_D increases above I_{DSS} . Shockley's equation, the formula used to plot the Transfer Curve, still applies but V_{GS} is positive:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

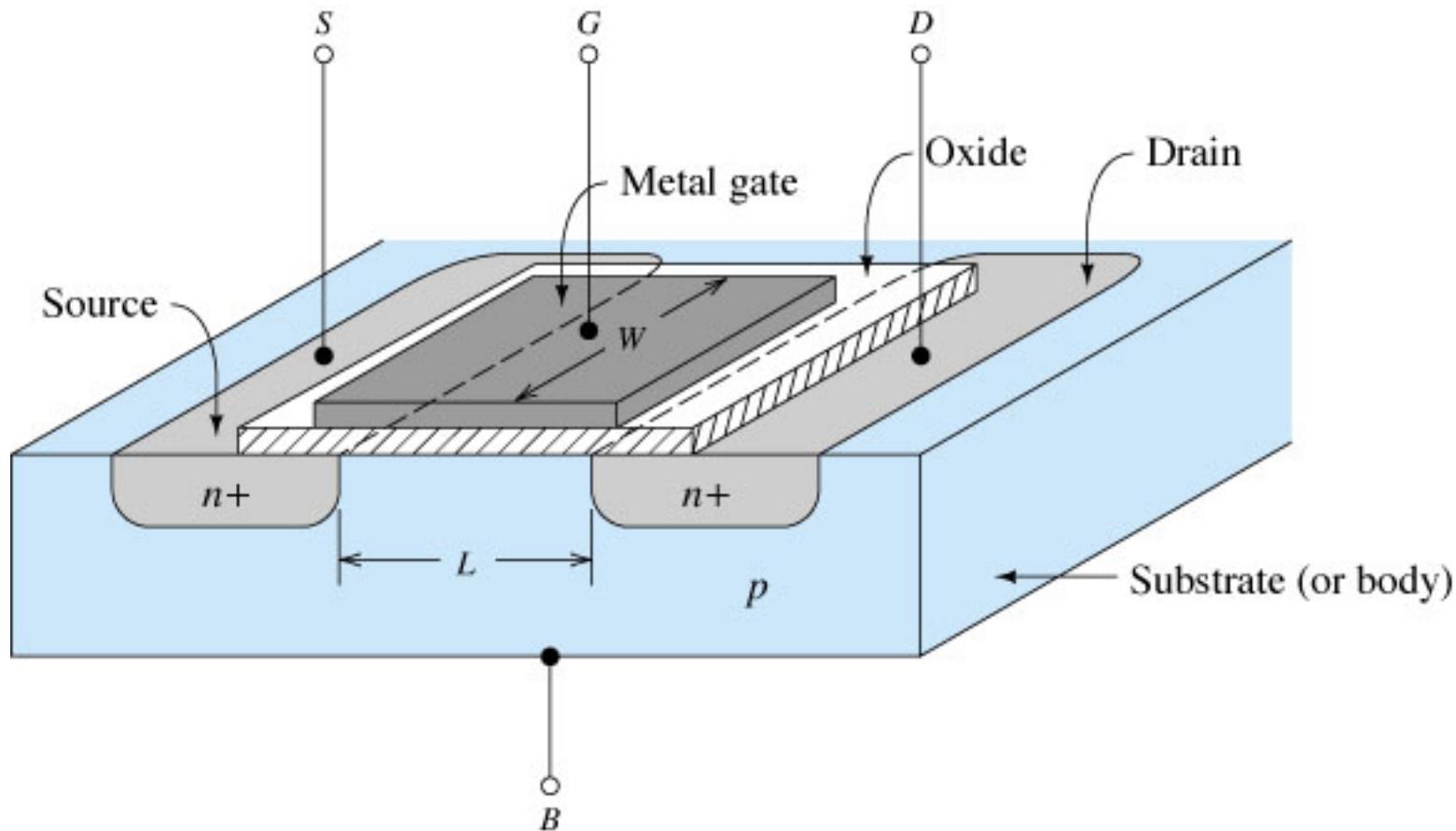
p-Channel Depletion Mode MOSFET



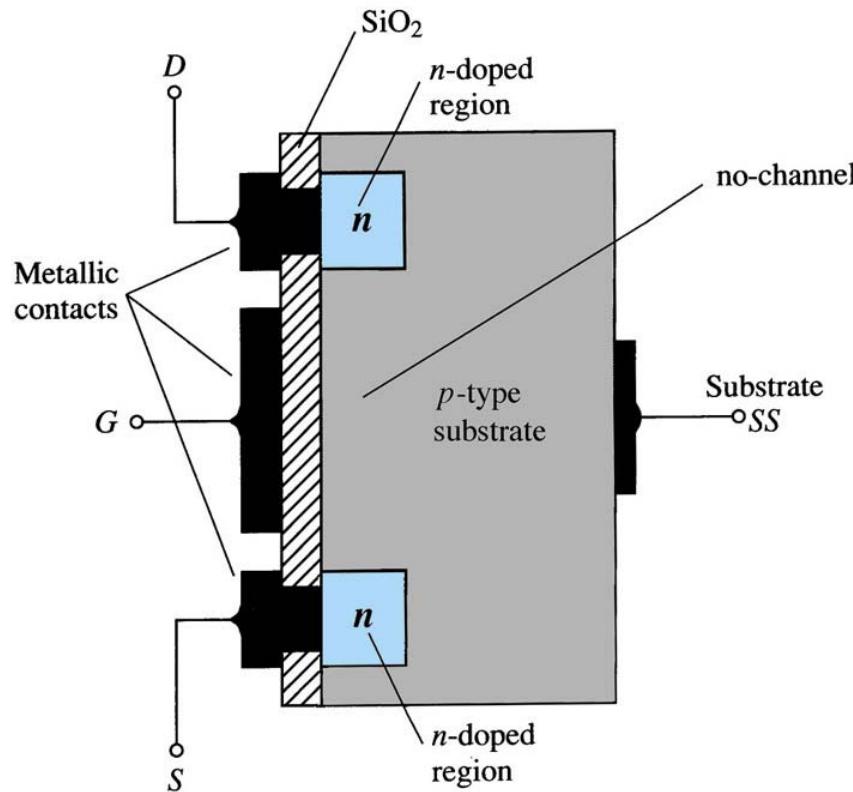
The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

Enhancement Mode MOSFET's

n-Channel E-MOSFET showing channel length L and channel width W



Enhancement Mode MOSFET Construction



- The Drain (D) and Source (S) connect to the n-doped regions
- These n-doped regions are not connected via an n-channel without an external voltage
- The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device

- the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$.
- there are in fact two reverse-biased p–n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source

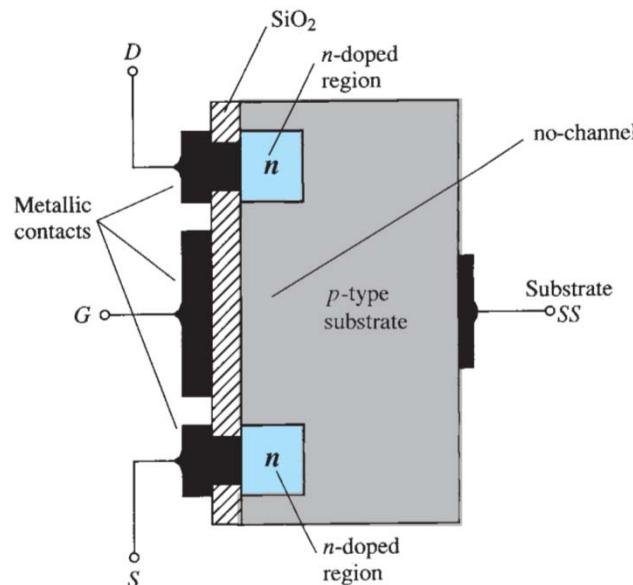


FIG. 6.32

n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

Both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source

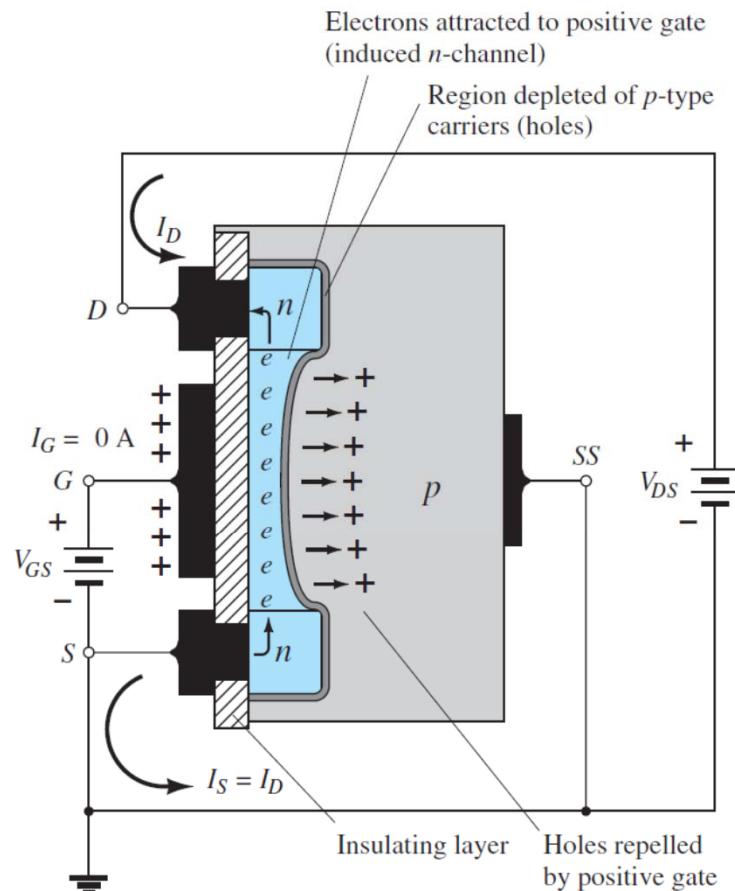
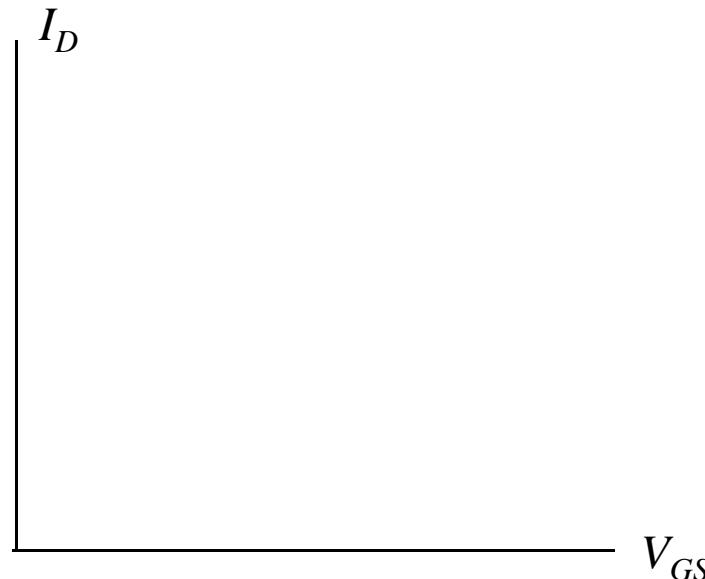


FIG. 6.33

Channel formation in the *n*-channel enhancement-type MOSFET.

- As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n* -type region can support a measurable flow between drain and source.
- The level of V_{GS} that results in the significant increase in drain current is called the **threshold voltage** and is given the symbol V_T .



- By the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*

Basic Operation and Characteristics

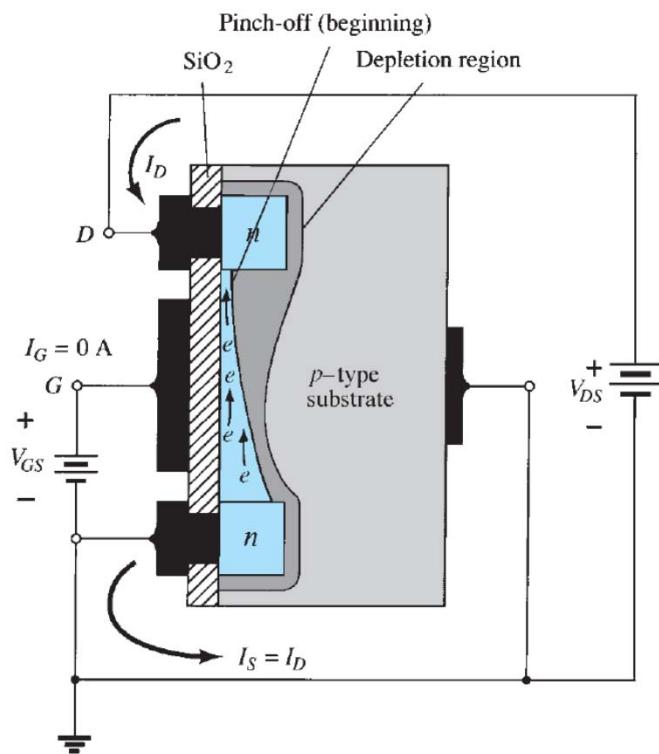


FIG. 6.34

Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS} .

- Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established
- any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

- As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.
- However, if we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET.
- The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 6.34 .

$$V_{DG} = V_{DS} - V_{GS}$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 V to 5 V, the voltage V_{DG} [by Eq. (6.13)] will increase from -6 V to -3 V and the gate will become less and less positive with respect to the drain.

I_D

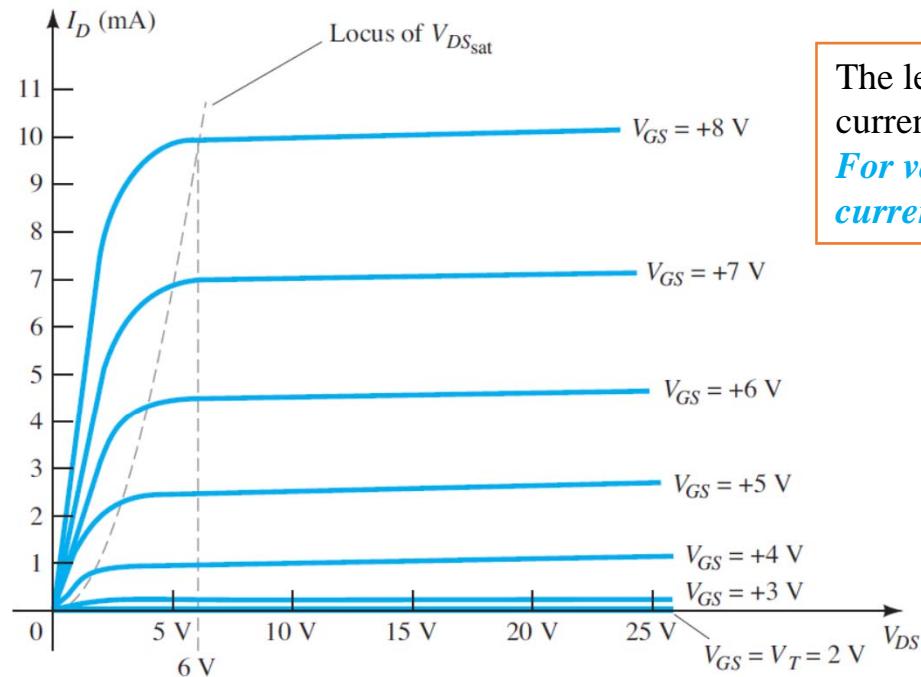
V_{DS}

Basic Operation and Characteristics

The drain characteristics of Fig. 6.35 reveal that for the device of Fig. 6.34 with $V_{GS} = 8 \text{ V}$, saturation occurs at a level of $V_{DS} = 6 \text{ V}$. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{\text{sat}}} = V_{GS} - V_T \quad (6.14)$$

Obviously, therefore, for a fixed value of V_T , the higher the level of V_{GS} , the greater is the saturation level for V_{DS} , as shown in Fig. 6.34 by the locus of saturation levels.



The level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:
For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

FIG. 6.35

Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2 \text{ V}$ and $k = 0.278 \times 10^{-3} \text{ A/V}^2$.

V_{DS}

Characteristics for an n-channel enhancement-type MOSFET from the drain characteristics

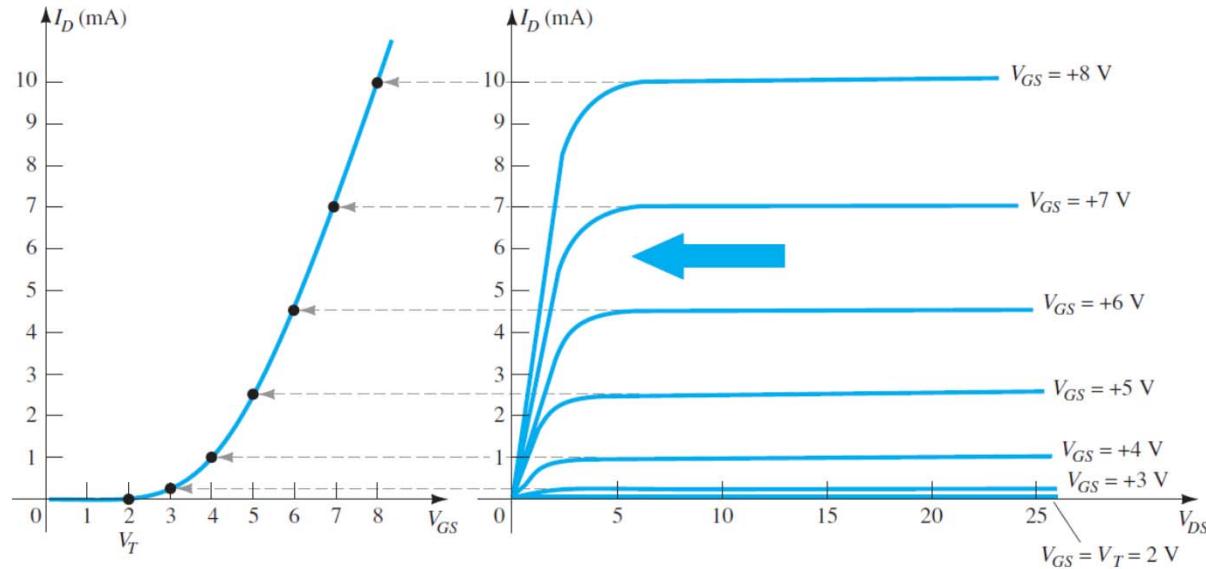


FIG. 6.36
Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

For levels of $V_{GS} \geq V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Characteristics for an n-channel enhancement-type MOSFET from the drain characteristics

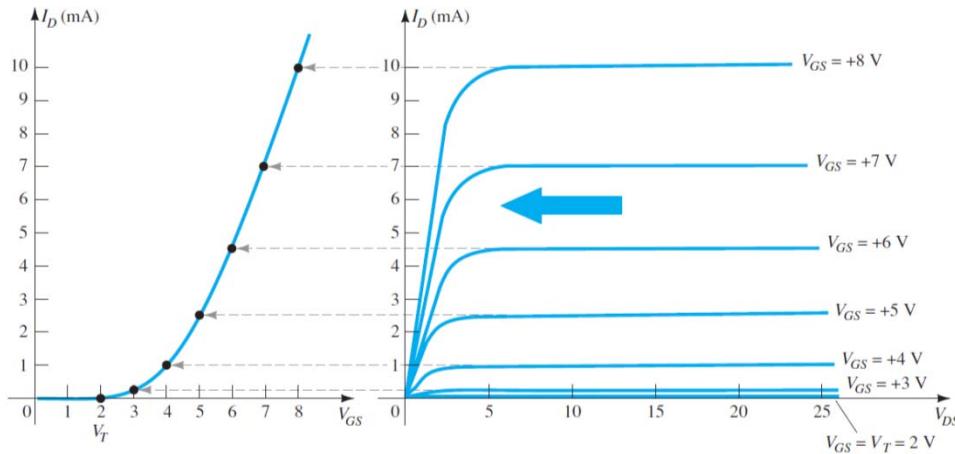


FIG. 6.36

Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.

- The k term is a constant that is a function of the construction of the device.
- The value of k can be determined from the following equation

$$k = \frac{I_{D(\text{on})}}{(V_{G_S(\text{on})} - V_T)^2}$$

- where $I_{D(\text{on})}$ and $V_{G_S(\text{on})}$ are the values for each at a particular point on the characteristics of the device.

Substituting $I_{D(\text{on})} = 10 \text{ mA}$ when $V_{G_S(\text{on})} = 8 \text{ V}$ from the characteristics of Fig. 6.35 yields

$$\begin{aligned} k &= \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2} \\ &= 0.278 \times 10^{-3} \text{ A/V}^2 \end{aligned}$$

and a general equation for I_D for the characteristics of Fig. 6.35 results in

$$I_D = 0.278 \times 10^{-3}(V_{G_S} - 2 \text{ V})^2$$

Substituting $V_{G_S} = 4 \text{ V}$, we find that

$$\begin{aligned} I_D &= 0.278 \times 10^{-3}(4 \text{ V} - 2 \text{ V})^2 = 0.278 \times 10^{-3}(2)^2 \\ &= 0.278 \times 10^{-3}(4) = 1.11 \text{ mA} \end{aligned}$$

Characteristics for an n-channel enhancement-type MOSFET from the drain characteristics

it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. As V_{GS} is increased beyond V_T , the drain current I_D will begin to flow at an increasing rate in accordance with Eq. (6.15).

$$I_D = k(V_{GS} - V_T)^2$$

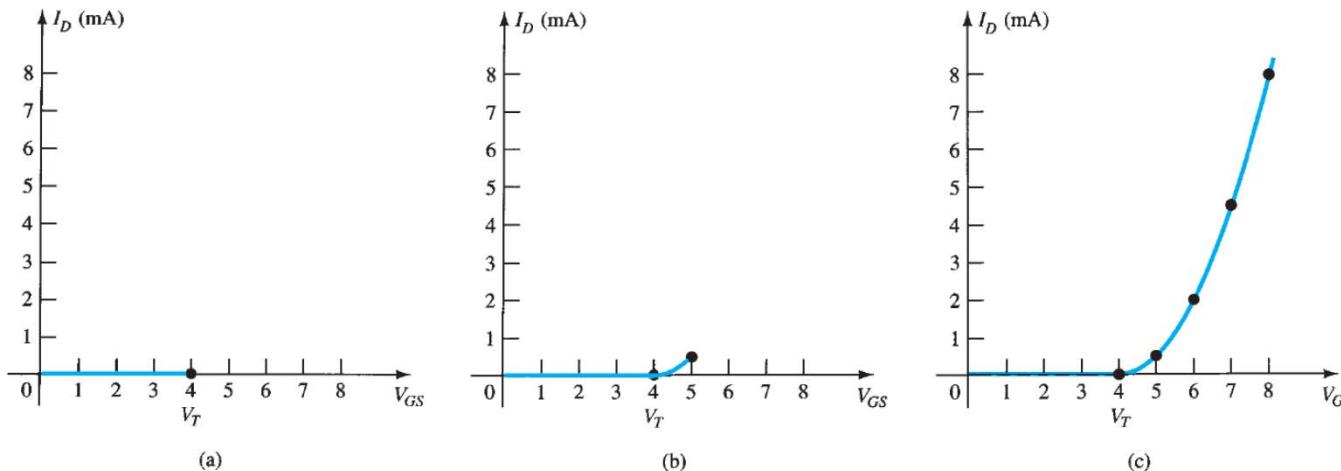


FIG. 6.37

Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3} \text{ A/V}^2$ and $V_T = 4 \text{ V}$.

p -Channel Enhancement-Type MOSFETs

The terminals remain as identified, but all the voltage polarities and the current directions are reversed.

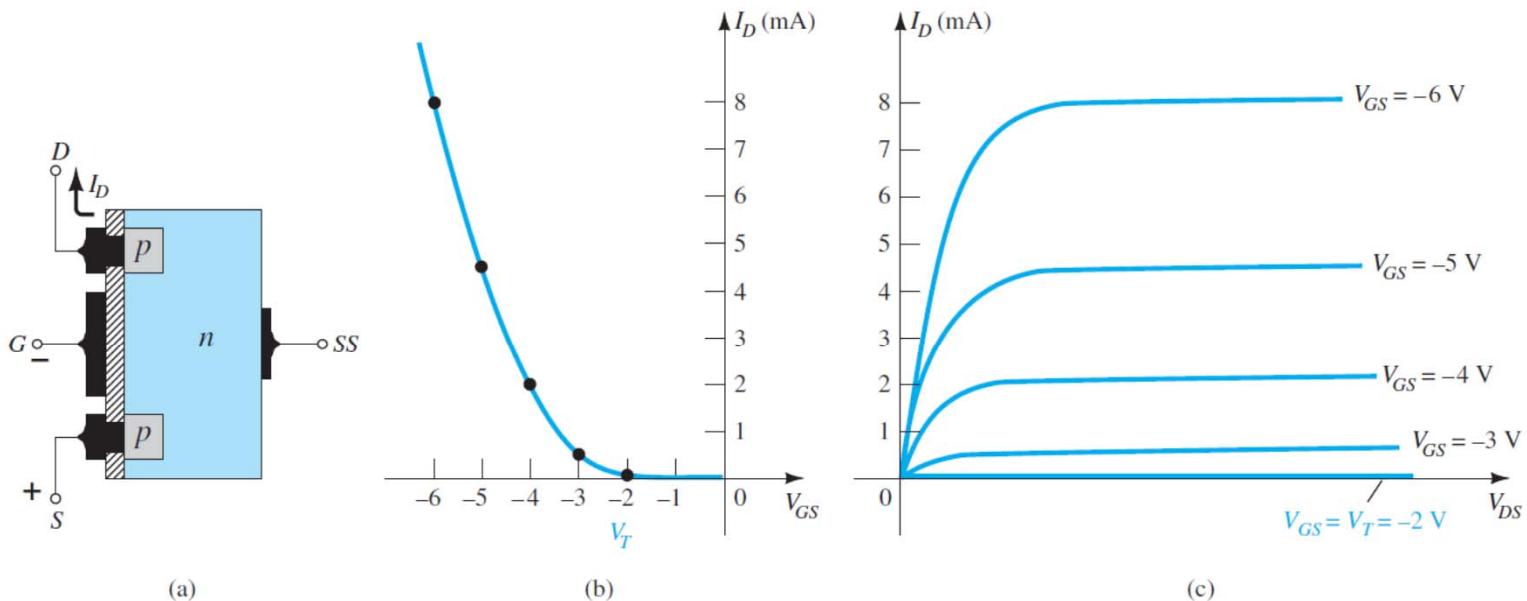


FIG. 6.38
p-Channel enhancement-type MOSFET with $V_T = 2 \text{ V}$ and $k = 0.5 \times 10^{-3} \text{ A/V}^2$.

Specification Sheet

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 1.7	mW mW/ $^\circ\text{C}$
Junction Temperature Range	T_J	175	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +175	$^\circ\text{C}$

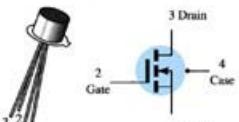
* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10 \mu\text{A}$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	—	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10$ V, $V_{GS} = 0$) $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	I_{DSS}	— —	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 10 \mu\text{A}$)	$V_{GS(th)}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0$ mA, $V_{GS} = 10$ V)	$V_{DS(on)}$	—	1.0	V
On-State Drain Current ($V_{GS} = 10$ V, $V_{DS} = 10$ V)	$I_{D(on)}$	3.0	—	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10$ V, $I_D = 2.0$ mA, $f = 1.0$ kHz)	$ y_{fs} $	1000	—	μmho
Input Capacitance ($V_{DS} = 10$ V, $V_{GS} = 0$, $f = 140$ kHz)	C_{iss}	—	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, $f = 140$ kHz)	C_{trs}	—	1.3	pF
Drain-Substrate Capacitance ($V_{DSUB} = 10$ V, $f = 140$ kHz)	$C_{d(substr)}$	—	5.0	pF
Drain-Source Resistance ($V_{GS} = 10$ V, $I_D = 0$, $f = 1.0$ kHz)	$r_{ds(on)}$	—	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	—	45	ns
Rise Time (Fig. 6)	t_r	—	65	ns
Turn-Off Delay (Fig. 7) (See Figure 9; Times Circuit Determined)	t_{d2}	—	60	ns
Fall Time (Fig. 8)	t_f	—	100	ns

2N4351

CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET
SWITCHING
N-CHANNEL - ENHANCEMENT

EXAMPLE 6.4 Using the data provided on the specification sheet of Fig. 6.40 and an average threshold voltage of $V_{GS(\text{Th})} = 3$ V, determine:

- The resulting value of k for the MOSFET.
- The transfer characteristics

Solution:

$$\begin{aligned}\text{a. Eq. (6.16): } k &= \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \\ &= \frac{3 \text{ mA}}{(10 \text{ V} - 3 \text{ V})^2} = \frac{3 \text{ mA}}{(7 \text{ V})^2} = \frac{3 \times 10^{-3}}{49} \text{ A/V}^2 \\ &= \mathbf{0.061 \times 10^{-3} \text{ A/V}^2}\end{aligned}$$

$$\begin{aligned}\text{b. Eq. (6.15): } I_D &= k(V_{GS} - V_T)^2 \\ &= 0.061 \times 10^{-3}(V_{GS} - 3 \text{ V})^2\end{aligned}$$

For $V_{GS} = 5$ V,

$$\begin{aligned}I_D &= 0.061 \times 10^{-3}(5 \text{ V} - 3 \text{ V})^2 = 0.061 \times 10^{-3}(2)^2 \\ &= 0.061 \times 10^{-3}(4) = 0.244 \text{ mA}\end{aligned}$$

For $V_{GS} = 8, 10, 12$, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 6.41.

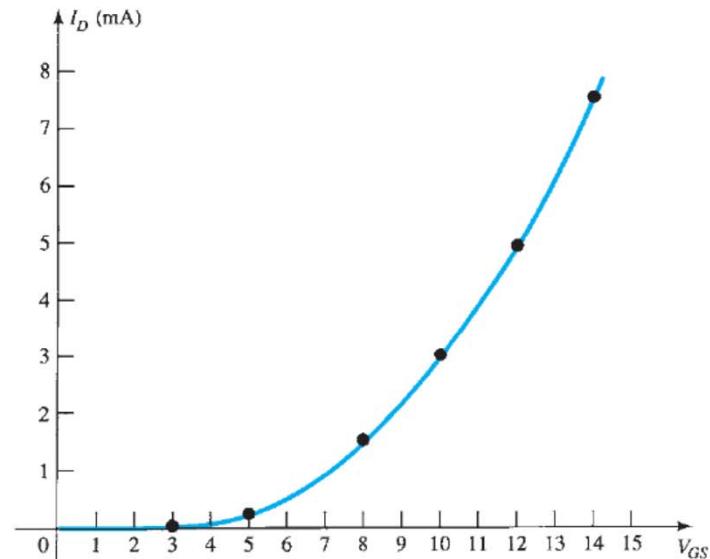


FIG. 6.41

Solution to Example 6.4.

p -Channel Enhancement-Type MOSFETs

The terminals remain as identified, but all the voltage polarities and the current directions are reversed.

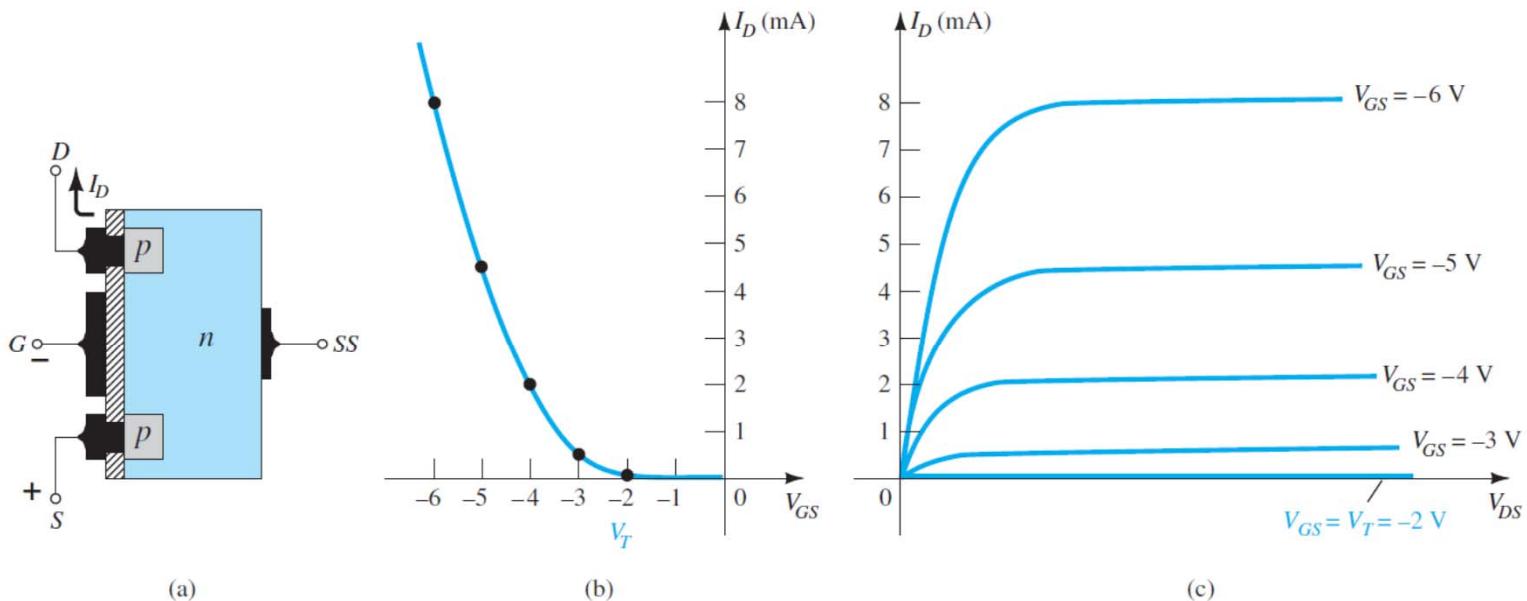
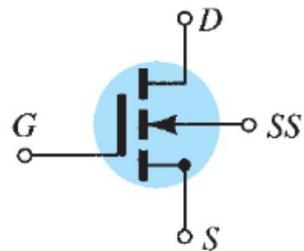


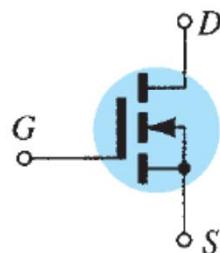
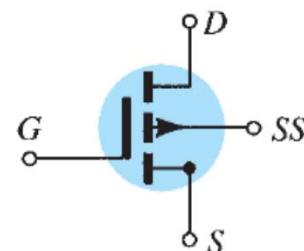
FIG. 6.38
p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V².

Symbols, Specification Sheets, and Case Construction

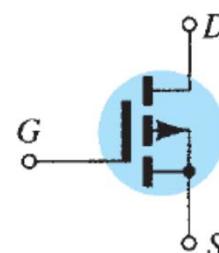
n-channel



p-channel



(a)



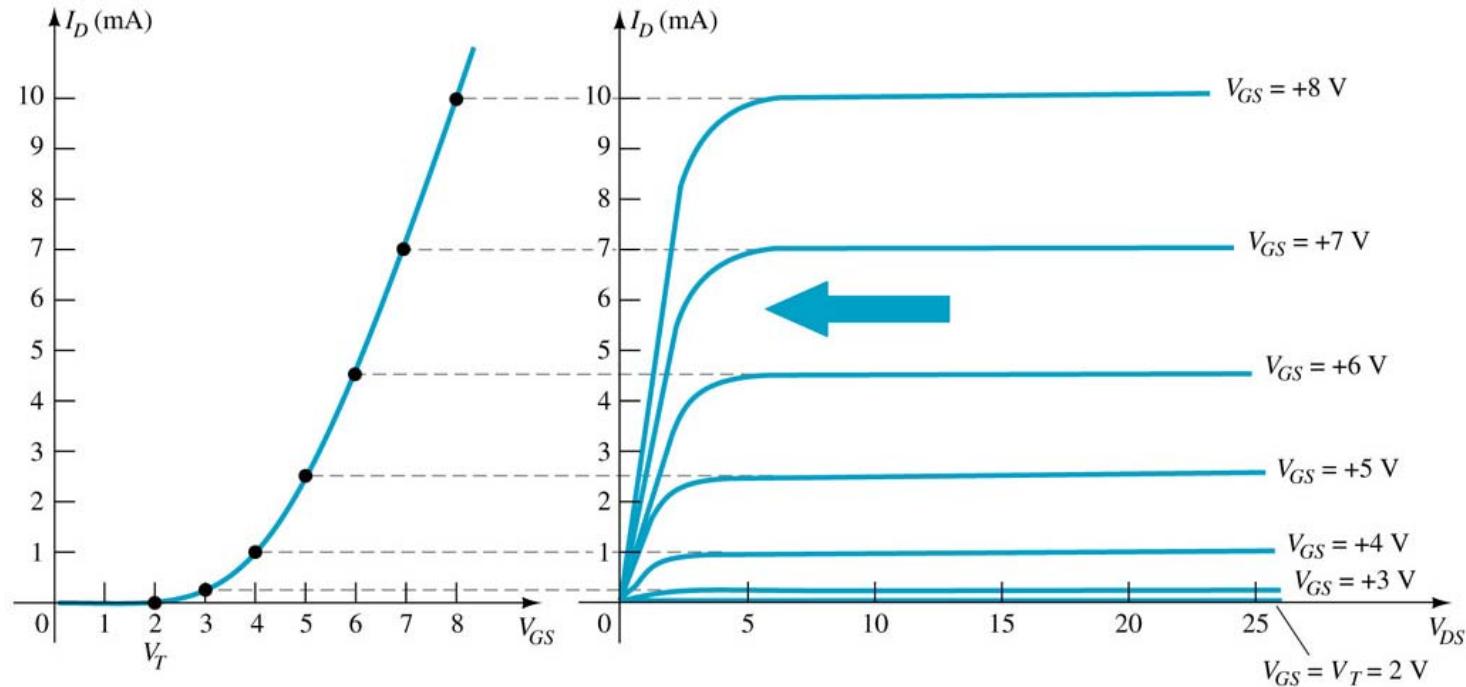
(b)

FIG. 6.39

Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.

Wrap up: Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive

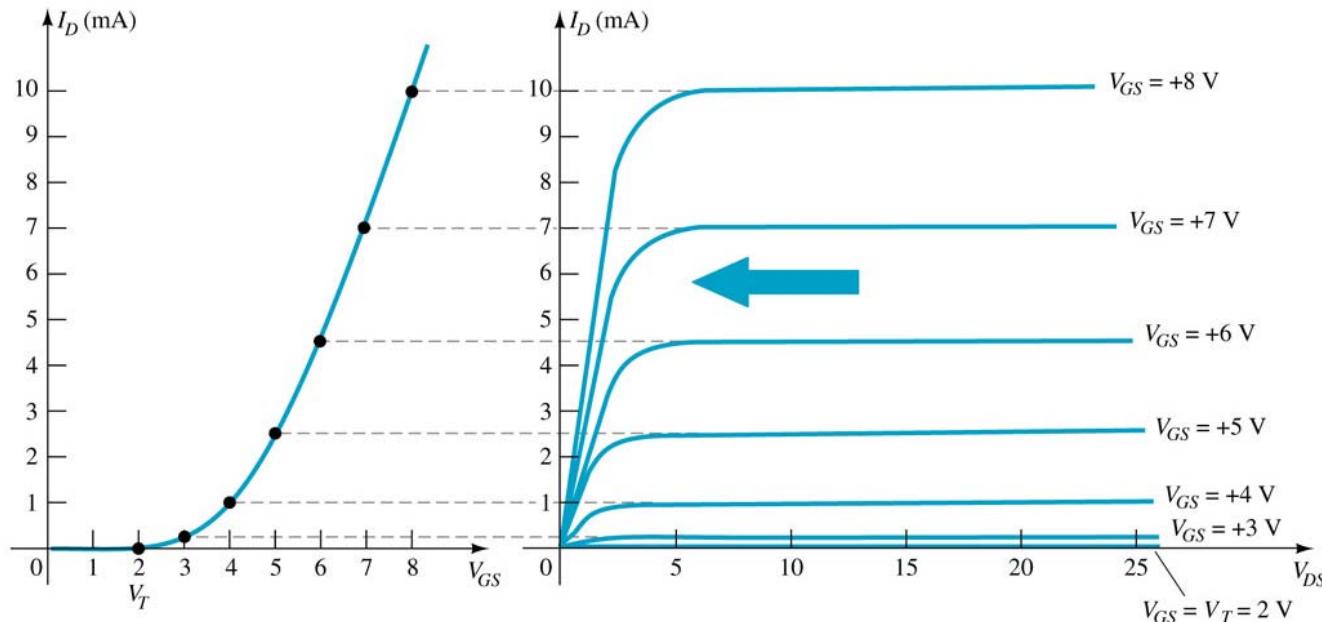
$I_{DSS} = 0$ when $V_{GS} < V_T$

As V_{GS} increases above V_T , I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

Wrap up: Transfer Curve



- To determine \$ID\$ given \$VGS\$:
- where \$V_T\$ = threshold voltage or voltage at which the MOSFET turns on.
- \$k\$ = constant found in the specification sheet
- The PSpice determination of \$k\$ is based on the geometry of the device:

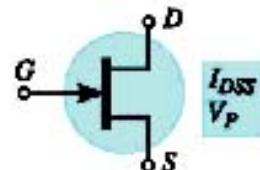
$$k = \left(\frac{W}{L} \right) \left(\frac{KP}{2} \right) \quad \text{where } KP = \mu_n C_{ox}$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \quad I_D = k (V_{GS} - V_T)^2$$

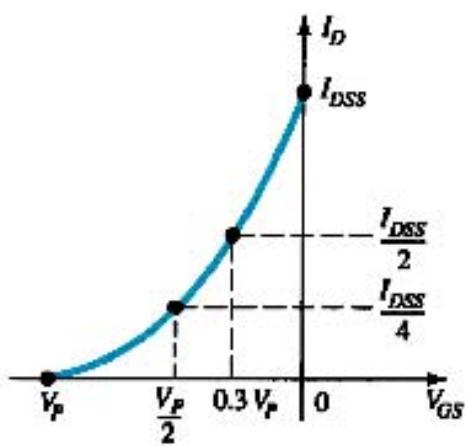
Summary Table

JFET

$$I_G = 0 \text{ A}, I_D = I_S$$

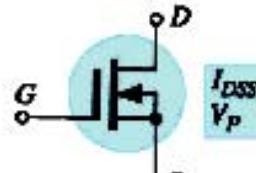


$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

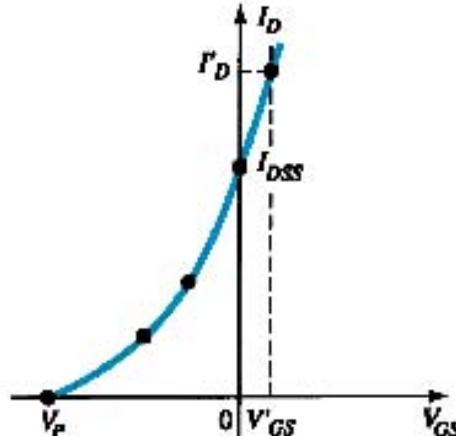


D-MOSFET

$$I_G = 0 \text{ A}, I_D = I_S$$

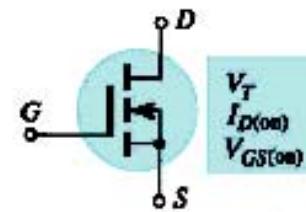


$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



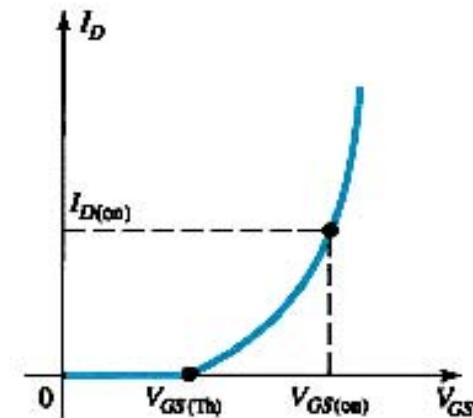
E-MOSFET

$$I_G = 0 \text{ A}, I_D = I_S$$

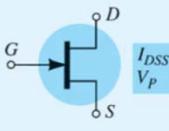
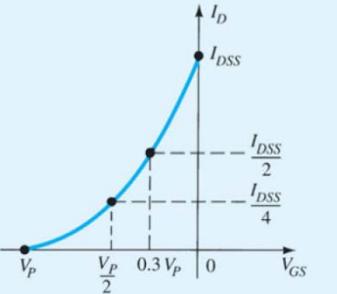
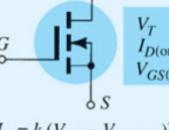
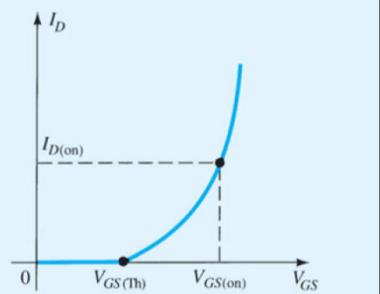


$$I_D = k (V_{GS} - V_{GS(\text{Th})})^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$



Summary Table

Type	Symbol and Basic Relationships	Transfer Curve
JFET (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$	
MOSFET enhancement type (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = k (V_{GS} - V_{GS(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$	

JFET:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}|_{V_{GS}=0 \text{ V}}, \quad I_D = 0 \text{ mA}|_{V_{GS}=V_P}, \quad I_D = \frac{I_{DSS}}{4} \Big|_{V_{GS}=V_P/2}, \quad V_{GS} \cong 0.3V_P|_{I_D=I_{DSS}/2}$$

$$V_{GS} = V_P \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS} I_D$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$