

# MSP430FR413x Mixed-Signal Microcontrollers

## 1 Features

- Embedded microcontroller
  - 16-bit RISC architecture up to 16 MHz
  - Wide supply voltage range from 3.6 V down to 1.8 V (minimum supply voltage is restricted by SVS levels, see the [Section 8.12.1.1](#))
- Optimized low-power modes (at 3 V)
  - Active mode: 126  $\mu$ A/MHz
  - Standby mode: <1  $\mu$ A with real-time clock (RTC) counter and liquid crystal display (LCD)
  - Shutdown (LPM4.5): 15 nA
- High-performance analog
  - 10-channel 10-bit analog-to-digital converter (ADC)
    - Internal 1.5-V reference
    - Sample-and-hold 200 ksp/s
  - Low-power LCD driver
    - Supports up to 4×36- or 8×32-segment LCD configuration
    - On-chip charge pump to keep LCD active in standby mode (LPM3.5)
    - Each LCD pin software configurable as SEG or COM
    - Contrast control from 2.6 V to 3.5 V by 0.06-V steps
- Low-power ferroelectric RAM (FRAM)
  - Up to 15.5KB of nonvolatile memory
  - Built-in error correction code (ECC)
  - Configurable write protection
  - Unified memory of program, constants, and storage
  - 10<sup>15</sup> write cycle endurance
  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals
  - IR modulation logic
  - Two 16-bit timers with three capture/compare registers each (Timer\_A3)
  - One 16-bit counter-only RTC counter
  - 16-bit cyclic redundancy checker (CRC)
- Enhanced serial communications
  - Enhanced USCI A (eUSCI\_A) supports UART, IrDA, and SPI
  - Enhanced USCI B (eUSCI\_B) supports SPI and I<sup>2</sup>C
- Clock system (CS)
  - On-chip 32-kHz RC oscillator (REFO)
  - On-chip 16-MHz digitally controlled oscillator (DCO) with frequency-locked loop (FLL)
    - $\pm 1\%$  accuracy with on-chip reference at room temperature
  - On-chip very low-frequency 10-kHz oscillator (VLO)
  - On-chip high-frequency modulation oscillator clock (MODCLK)
  - External 32-kHz crystal oscillator (XT1)
  - Programmable MCLK prescaler of 1 to 128
  - SMCLK derived from MCLK with programmable prescaler of 1, 2, 4, or 8
- General input/output and pin functionality
  - 60 I/Os on 64-pin package
  - 16 interrupt pins (P1 and P2) can wake MCU from LPMs
  - All I/Os are capacitive touch I/O
- Development tools and software
  - Development kits ([MSP-EXP430FR4133 LaunchPad™ development kit](#) and [MSP-TS430PM64D target development board](#))
  - Free software ([MSP430Ware™ software](#))
- Family members (also see [Section 6](#))
  - MSP430FR4133: 15KB of program FRAM + 512B of information FRAM + 2KB of RAM
  - MSP430FR4132: 8KB of program FRAM + 512B of information FRAM + 1KB of RAM
  - MSP430FR4131: 4KB of program FRAM + 512B of information FRAM + 512B of RAM
- Package options
  - 64 pin: LQFP (PM)
  - 56 pin: TSSOP (G56)
  - 48 pin: TSSOP (G48)

## 2 Applications

- Remote controls
- Thermostats
- Water meters
- Heat meters
- Gas meters
- One-time password tokens
- Blood glucose monitors
- Blood pressure monitors

## 3 Description

MSP430FR41xx ultra-low-power (ULP) microcontroller family supports low-cost LCD applications that benefit from an integrated 10-bit ADC such as remote controls, thermostats, smart meters, blood glucose monitors, and blood pressure monitors. The MCUs feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device



to wake up from low-power modes to active mode in less than 10  $\mu$ s. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications.

The MSP430™ FRAM microcontroller platform combines uniquely embedded ferroelectric random access memory (FRAM) and a holistic ultra-low-power system architecture, allowing system designers to increase performance while lowering energy consumption. FRAM technology combines the low-energy fast writes, flexibility, and endurance of RAM with the nonvolatile behavior of flash.

MSP430FR41x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. Development kits for the MSP430FR41xx include the [MSP-EXP430FR4133](#) LaunchPad™ development kit and the [MSP-TS430PM64D](#) 64-pin target development board. TI also provides free [MSP430Ware™](#) software, which is available as a component of Code Composer Studio™ IDE desktop and cloud versions within TI Resource Explorer. MSP430 MCUs are also supported by extensive online collateral, such as our [housekeeping example series](#), [MSP Academy training](#), and online support through the [TI E2E™ support forums](#).

For complete module descriptions, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

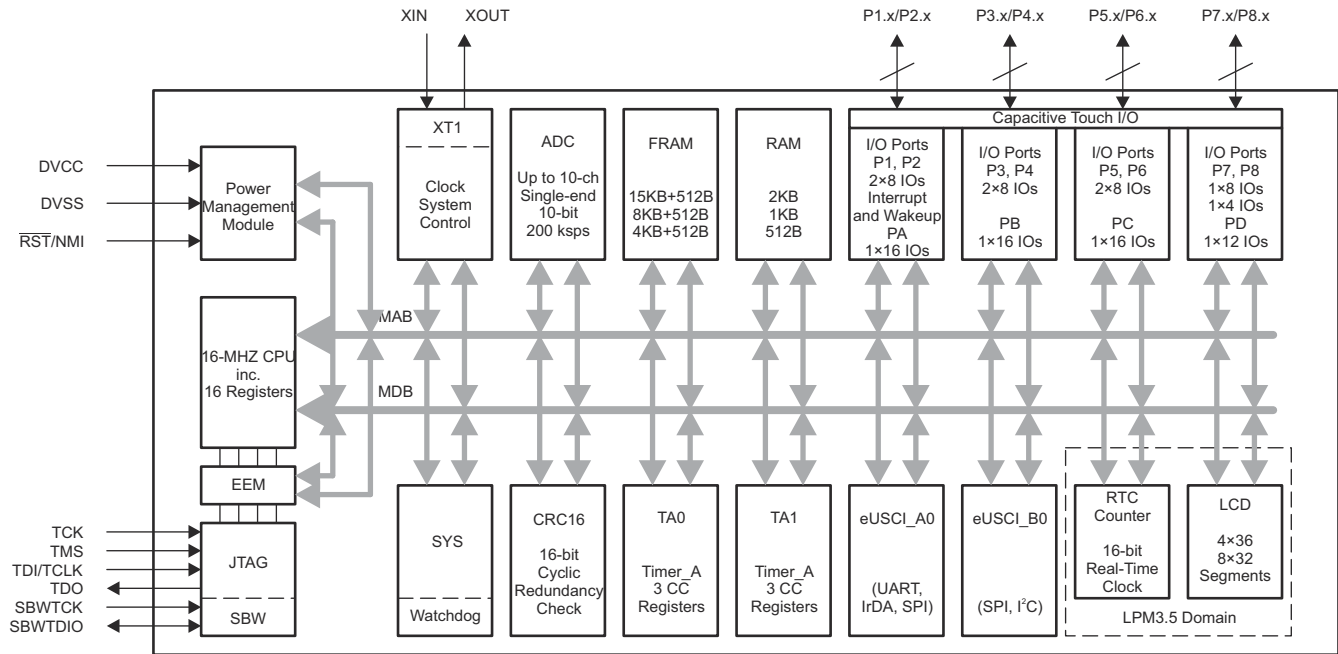
#### Device Information

| PART NUMBER <sup>(1)</sup> | PACKAGE    | BODY SIZE <sup>(2)</sup> |
|----------------------------|------------|--------------------------|
| MSP430FR4133IPM            | LQFP (64)  | 10 mm × 10 mm            |
| MSP430FR4133IG56           | TSSOP (56) | 14 mm × 6.1 mm           |
| MSP430FR4133IG48           | TSSOP (48) | 12.5 mm × 6.1 mm         |

- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 12](#), or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 12](#).

## 4 Functional Block Diagram

Figure 4-1 shows the functional block diagram.



**Figure 4-1. Functional Block Diagram**

- The device has one main power pair of DVCC and DVSS that supplies both digital and analog modules. Recommended bypass and decouple capacitors are 4.7  $\mu$ F to 10  $\mu$ F and 0.1  $\mu$ F, respectively, with  $\pm 5\%$  accuracy.
- P1 and P2 feature the pin-interrupt function and can wake the MCU from LPM3.5.
- Each Timer\_A3 has three CC registers, but only the CCR1 and CCR2 are externally connected. CCR0 registers can only be used for internal period timing and interrupt generation.
- In LPM3.5, the RTC counter and the LCD can be functional while the rest of peripherals are off.
- All I/Os can be configured as Capacitive Touch I/Os.

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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision E to revision F

| Changes from December 9, 2019 to December 8, 2021   | Page |
|---|------|
| • Updated the numbering format for tables, figures, and cross references throughout the document..... | 1    |
| • Added <a href="#">Section 10.2.3.1 Generate Accurate PWM Using Internal Oscillator</a> .....        | 83   |

Changes from revision D to revision E

| Changes from January 22, 2019 to December 9, 2019  | Page |
|--|------|
| • Changed the note that begins "Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset..." in <a href="#">Section 8.3, Recommended Operating Conditions</a> .....                                 | 15   |
| • Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in <a href="#">Section 8.3, Recommended Operating Conditions</a> .....                                   | 15   |
| • Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in <a href="#">Section 8.3, Recommended Operating Conditions</a> .....   | 15   |
| • Added the note "See <a href="#">MSP430 32-kHz Crystal Oscillators</a> for details on crystal section, layout, and testing" to <a href="#">Section 8.12.3.1, XT1 Crystal Oscillator (Low Frequency)</a> ..... | 23   |
| • Changed the note that begins "Requires external capacitors at both terminals..." in <a href="#">Section 8.12.3.1, XT1 Crystal Oscillator (Low Frequency)</a> .....   | 23   |
| • Added the $t_{(int)}$ parameter in <a href="#">Section 8.12.4.1, Digital Inputs</a> .....  | 26   |
| • Added the $t_{TA, cap}$ parameter in <a href="#">Section 8.12.5.1, Timer_A</a> .....   | 27   |
| • Corrected the test conditions for the $R_{I, MUX}$ parameter in <a href="#">Section 8.12.7.1, ADC, Power Supply and Input Range Conditions</a> .....   | 33   |
| • Added the note that begins " $t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in <a href="#">Section 8.12.7.2, ADC, 10-Bit Timing Parameters</a> ....  | 33   |

Changes from revision C to revision D

| Changes from August 30, 2018 to January 21, 2019  | Page |
|---|------|
| • Throughout the document, changed Modulation Oscillator (MODOSC) to Modulation Oscillator Clock (MODCLK) .....   | 1    |
| • Added "or memory corruption" in table that starts "Stresses beyond those listed..." of <a href="#">Section 8.1, Absolute Maximum Ratings</a> .....  | 15   |
| • Added note of VLO clock frequency shift in LPM3 and LPM4 mode in <a href="#">Section 8.12.3.4, Internal Very-Low-Power Low-Frequency Oscillator (VLO)</a> .....                             | 24   |
| • Changed from $R_I$ to $R_{I, MUX}$ in <a href="#">Section 8.12.7.1, ADC, Power Supply and Input Range Conditions</a> .....  | 33   |
| • Added $R_{I, Misc}$ TYP value 34kΩ in <a href="#">Section 8.12.7.1, ADC, Power Supply and Input Range Conditions</a> .....  | 33   |
| • Removed ADCDIV from the conversion time formula because ADCCLK is after division in <a href="#">Section 8.12.7.2, ADC, 10-Bit Timing Parameters</a> .....                                   | 33   |
| • Added formula for $R_I$ calculation in <a href="#">Section 8.12.7.2, ADC, 10-Bit Timing Parameters</a> .....  | 33   |
| • Remove description of "±3°C" in table note that starts "The device descriptor structure ..." of <a href="#">Section 8.12.7.3, ADC, 10-Bit Linearity Parameters</a> .....                    | 34   |
| • Add "10b" for ADCSEL bit in <a href="#">Table 9-6, Clock Distribution</a> .....   | 41   |
| • Added "Clock Distribution Block Diagram" in <a href="#">Section 9.9.2, Clock System (CS) and Clock Distribution</a> .....   | 41   |
| • Corrected bitfield from IRDSEL to IRDSSEL in <a href="#">Section 9.9.8, Timers (Timer0_A3, Timer1_A3)</a> , in the description that starts "The interconnection of Timer0_A3 and ..." ..... | 46   |
| • Corrected the ADCINCHx column heading in <a href="#">Table 9-12, ADC Channel Connections</a> .....  | 48   |
| • Added word "Sensor" in <a href="#">Table 9-27, Device Descriptors</a> .....   | 67   |
| • Added word "Sensor" in <a href="#">Table 9-27, Device Descriptors</a> .....   | 67   |

Changes from revision B to revision C

| Changes from August 15, 2015 to August 29, 2018  | Page |
|--|------|
| • Editorial changes and additional information in <a href="#">Section 1, Features</a> , <a href="#">Section 2, Applications</a> , and <a href="#">Section 3, Description</a> ..... | 1    |
| • Updated <a href="#">Section 6.1, Related Products</a> .....  | 7    |
| • Added note to $V_{SVSH-}$ and $V_{SVSH+}$ parameters in <a href="#">Section 8.12.1.1, PMM, SVS and BOR</a> .....   | 21   |
| • Changed all instances of "bootstrap loader" to "bootloader" .....  | 39   |
| • Updates to text and figure in <a href="#">Section 11.2, Device Nomenclature</a> .....  | 85   |

Changes from revision A to revision B

| Changes from December 20, 2014 to August 14, 2015   | Page |
|---|------|
| • Changed "Standby Mode" current consumption from 770 nA to 1 $\mu$ A .....   | 1    |
| • Added <a href="#">Section 8.2, ESD Ratings</a> .....  | 15   |
| • Added $I_{LPM3.5}$ , LCD, CP TYP values at $-40^{\circ}\text{C}$ (0.90 $\mu$ A) and at $85^{\circ}\text{C}$ (1.27 $\mu$ A) .....  | 18   |
| • Added the paragraph that starts "The graphs in this section..." .....   | 19   |
| • Changed all graphs in <a href="#">Section 8.9, Typical Characteristics, Low-Power Mode Supply Currents</a> , for new measurements .....   | 19   |
| • Added $V_{REF, 1.2V}$ parameter to <a href="#">Section 8.12.1.1, PMM, SVS and BOR</a> .....   | 21   |
| • Changed $t_{STE,LEAD}$ MIN value at 2 V from 40 ns to 50 ns .....   | 30   |
| • Changed $t_{STE,LEAD}$ MIN value at 3 V from 24 ns to 45 ns .....   | 30   |
| • Changed $t_{VALID,SO}$ MAX value at 2 V from 55 ns to 65 ns .....   | 30   |
| • Changed $t_{VALID,SO}$ MAX value at 3 V from 30 ns to 40 ns .....   | 30   |
| • Changed $f_{ADCOSC}$ TYP value from 4.5 MHz to 5.0 MHz .....  | 33   |
| • In <a href="#">Table 9-1, Operating Modes</a> , changed the entry for "Power Consumption at $25^{\circ}\text{C}$ , 3 V" in AM from 100 $\mu$ A/MHz to 126 $\mu$ A/MHz .....                       | 37   |
| • In <a href="#">Table 9-1, Operating Modes</a> , added "with RTC only" to the entry for "Power Consumption at $25^{\circ}\text{C}$ , 3 V" in LPM3.5 .....  | 37   |
| • In <a href="#">Table 9-2, Interrupt Sources, Flags, and Vectors</a> , removed "FRAM access time error" (ACCTEIFG) from the "System NMI" row .....   | 38   |
| • In <a href="#">Table 9-8, System Module Interrupt Vector Registers</a> , changed the interrupt event in the SYSSNIV row with a VALUE of 06h from "ACCTEIFG access time error" to "Reserved" ..... | 43   |
| • In <a href="#">Table 9-27, Device Descriptors</a> , added note to "CRC value" .....   | 67   |

Changes from initial release to revision A

| Changes from October 3, 2014 to December 19, 2014   | Page |
|---|------|
| • Moved $T_{stg}$ to <i>Absolute Maximum Ratings</i> table and added note (3) .....                             | 15   |
| • Changed link to BSL user's guide in <a href="#">Section 9.4</a> .....   | 39   |
| • Added note (1) to <a href="#">Table 9-6</a> .....   | 41   |
| • Changed the values of ADC Calibration Tag and ADC Calibration Length in the ADC Calibration row .....         | 67   |
| • Added Calibration Tag, Calibration Length, and 1.5-V Reference in the Reference and DCO Calibration row ..... | 67   |
| • Added row for BSL memory to <a href="#">Table 9-28</a> .....  | 68   |

## 6 Device Comparison

Table 6-1 summarizes the features of the available family members.

**Table 6-1. Device Comparison**

| DEVICE <sup>(1) (2)</sup> | PROGRAM FRAM<br>+ INFORMATION<br>FRAM (BYTES) | SRAM<br>(BYTES) | TA0, TA1               | eUSCI_A | eUSCI_B | 10-BIT ADC<br>CHANNELS | LCD<br>SEGMENTS  | I/O | PACKAGE<br>TYPE     |
|---------------------------|---|-----------------|------------------------|---------|---------|------------------------|------------------|-----|---------------------|
| MSP430FR4133IPM           | 15360 + 512                                   | 2048            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 10                     | 4 × 36<br>8 × 32 | 60  | 64 PM<br>(LQFP)     |
| MSP430FR4132IPM           | 8192 + 512                                    | 1024            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 10                     | 4 × 36<br>8 × 32 | 60  | 64 PM<br>(LQFP)     |
| MSP430FR4131IPM           | 4096 + 512                                    | 512             | 3 × CCR <sup>(3)</sup> | 1       | 1       | 10                     | 4 × 36<br>8 × 32 | 60  | 64 PM<br>(LQFP)     |
| MSP430FR4133IG56          | 15360 + 512                                   | 2048            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 30<br>8 × 26 | 52  | 56 DGG<br>(TSSOP56) |
| MSP430FR4132IG56          | 8192 + 512                                    | 1024            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 30<br>8 × 26 | 52  | 56 DGG<br>(TSSOP56) |
| MSP430FR4131IG56          | 4096 + 512                                    | 512             | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 30<br>8 × 26 | 52  | 56 DGG<br>(TSSOP56) |
| MSP430FR4133IG48          | 15360 + 512                                   | 2048            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 24<br>8 × 20 | 44  | 48 DGG<br>(TSSOP48) |
| MSP430FR4132IG48          | 8192 + 512                                    | 1024            | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 24<br>8 × 20 | 44  | 48 DGG<br>(TSSOP48) |
| MSP430FR4131IG48          | 4096 + 512                                    | 512             | 3 × CCR <sup>(3)</sup> | 1       | 1       | 8                      | 4 × 24<br>8 × 20 | 44  | 48 DGG<br>(TSSOP48) |

- (1) For the most current device, package, and ordering information, see the *Package Option Addendum* in Section 12, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

### 6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

[TI 16-bit and 32-bit microcontrollers](#)

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## 7 Terminal Configuration and Functions

### 7.1 Pin Diagrams

Figure 7-1 shows the pinout of the 64-pin PM package.

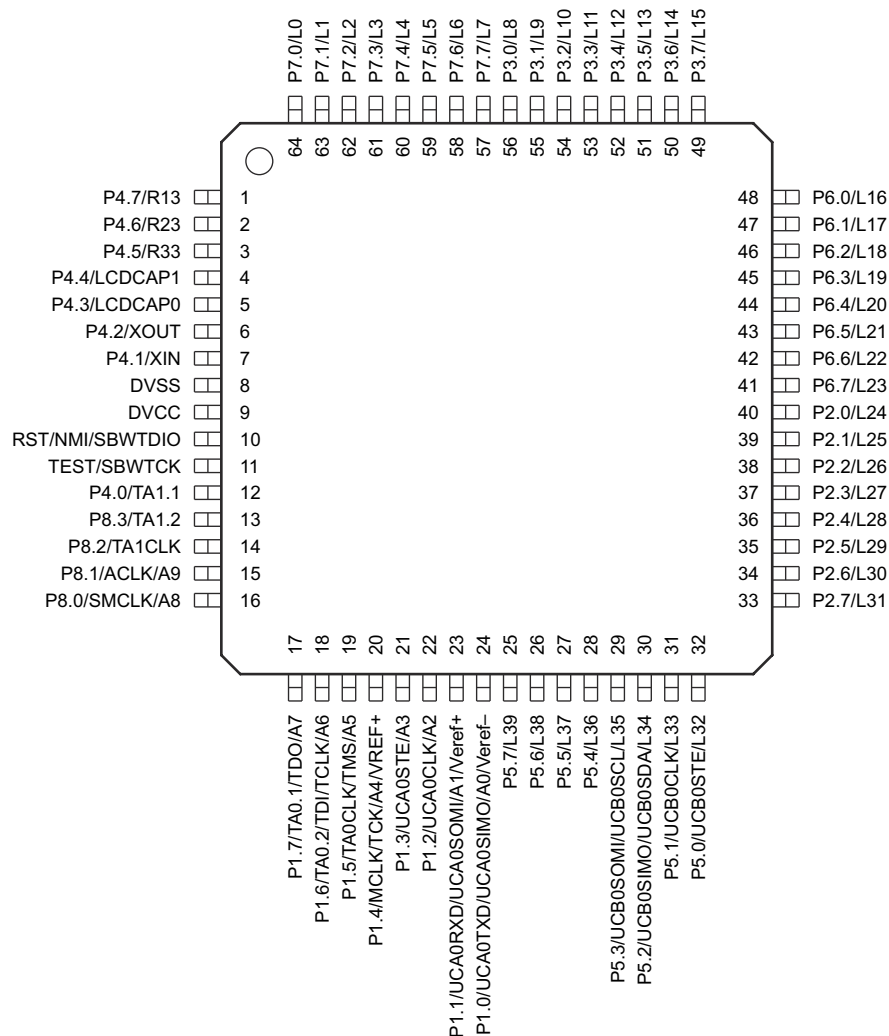
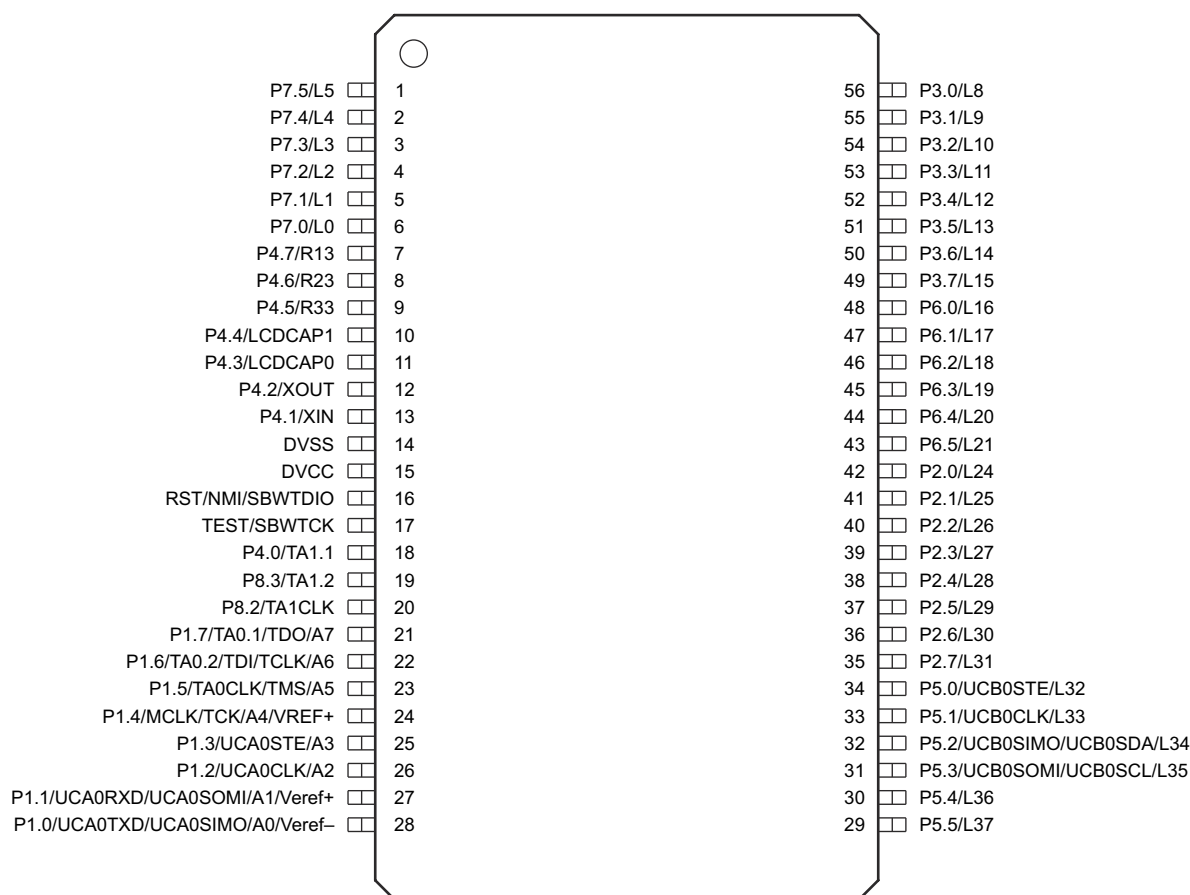


Figure 7-1. 64-Pin PM (LQFP) (Top View)

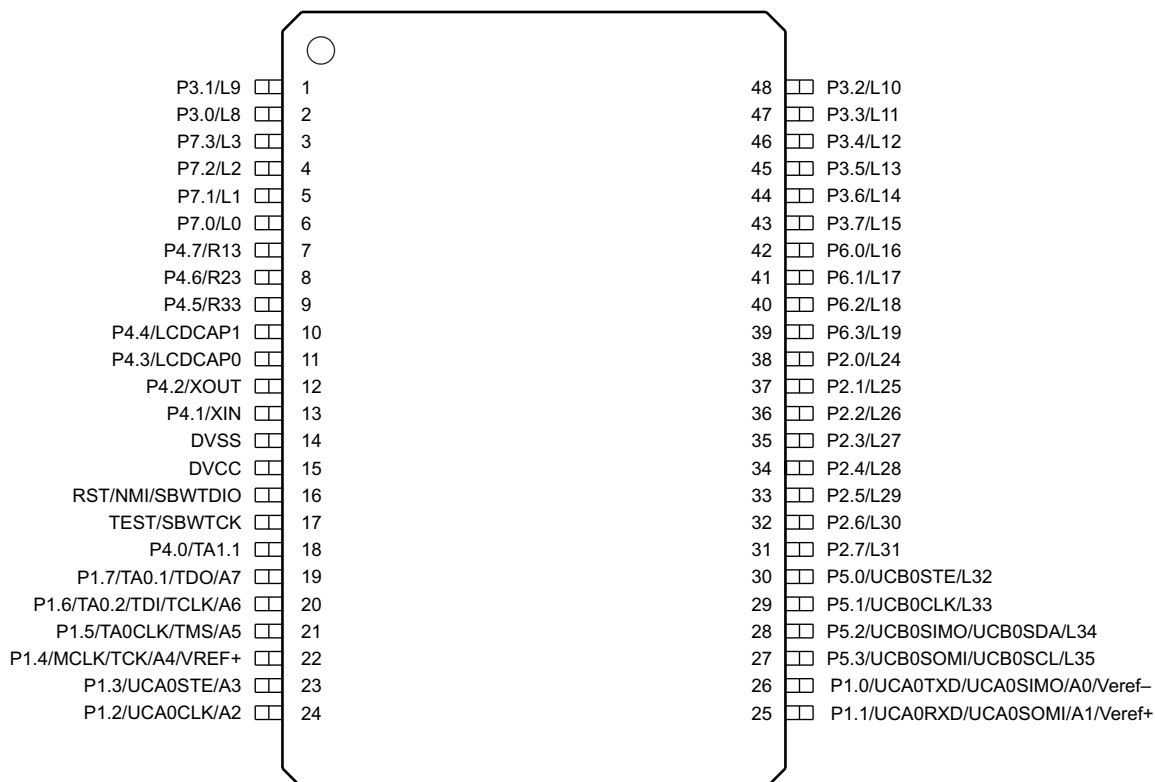


Figure 7-2 shows the pinout of the 56-pin DGG package.



**Figure 7-2. 56-Pin DGG (TSSOP) (Top View)**

Figure 7-3 shows the pinout of the 48-pin DGG package.



**Figure 7-3. 48-Pin DGG (TSSOP) Designation**

## 7.2 Signal Descriptions

Section 7.2 describes the signals for all device variants and package options.

**Table 7-1. Signal Descriptions**

| NAME                         | PACKAGE SUFFIX |     |     | I/O | DESCRIPTION  |
|------------------------------|----------------|-----|-----|-----|--|
|                              | PM             | G56 | G48 |     |  |
| P4.7/R13                     | 1              | 7   | 7   | I/O | General-purpose I/O<br>Input/output port of third most positive analog LCD voltage V4  |
| P4.6/R23                     | 2              | 8   | 8   | I/O | General-purpose I/O<br>Input/output port of second most positive analog LCD voltage V2   |
| P4.5/R33                     | 3              | 9   | 9   | I/O | General-purpose I/O<br>Input/output port of first most positive analog LCD voltage V1  |
| P4.4/LCDCAP1                 | 4              | 10  | 10  | I/O | General-purpose I/O<br>LCD charge pump external port connecting to LCDCAP0 pin by 0.1-μF capacitor   |
| P4.3/LCDCAP0                 | 5              | 11  | 11  | I/O | General-purpose I/O<br>LCD charge pump external port connecting to LCDCAP1 pin by 0.1-μF capacitor   |
| P4.2/XOUT                    | 6              | 12  | 12  | I/O | General-purpose I/O<br>Output terminal for crystal oscillator  |
| P4.1/XIN                     | 7              | 13  | 13  | I/O | General-purpose I/O<br>Input terminal for crystal oscillator   |
| DVSS                         | 8              | 14  | 14  |     | Power ground   |
| DVCC                         | 9              | 15  | 15  |     | Power supply   |
| RST/NMI/SBWTIO               | 10             | 16  | 16  | I/O | Reset input active low<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output   |
| TEST/SBWTK                   | 11             | 17  | 17  | I   | Test Mode pin – selected digital I/O on JTAG pins<br>Spy-Bi-Wire input clock   |
| P4.0/TA1.1                   | 12             | 18  | 18  | I/O | General-purpose I/O<br>Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs  |
| P8.3/TA1.2 <sup>(1)</sup>    | 13             | 19  | –   | I/O | General-purpose I/O<br>Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs  |
| P8.2/TA1CLK <sup>(1)</sup>   | 14             | 20  | –   | I/O | General-purpose I/O<br>Timer clock input TACLK for TA1   |
| P8.1/ACLK/A9 <sup>(1)</sup>  | 15             | –   | –   | I/O | General-purpose I/O<br>ACLK output<br>Analog input A9  |
| P8.0/SMCLK/A8 <sup>(1)</sup> | 16             | –   | –   | I/O | General-purpose I/O<br>SMCLK output<br>Analog input A8   |
| P1.7/TA0.1/TDO/A7            | 17             | 21  | 19  | I/O | General-purpose I/O <sup>(2)</sup><br>Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs<br>Test data output<br>Analog input A7                    |
| P1.6/TA0.2/TDI/TCLK/A6       | 18             | 22  | 20  | I/O | General-purpose I/O <sup>(2)</sup><br>Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs<br>Test data input or test clock input<br>Analog input A6 |
| P1.5/TA0CLK/TMS/A5           | 19             | 23  | 21  | I/O | General-purpose I/O <sup>(2)</sup><br>Timer clock input TACLK for TA0<br>Test mode select<br>Analog input A5   |
| P1.4/MCLK/TCK/A4/VREF+       | 20             | 24  | 22  | I/O | General-purpose I/O <sup>(2)</sup><br>MCLK output<br>Test clock<br>Analog input A4<br>Output of positive reference voltage with ground as reference        |
| P1.3/UCA0STE/A3              | 21             | 25  | 23  | I/O | General-purpose I/O<br>eUSCI_A0 SPI slave transmit enable<br>Analog input A3   |

Table 7-1. Signal Descriptions (continued)

| TERMINAL<br>NAME                     | PACKAGE SUFFIX |     |     | I/O | DESCRIPTION   |
|--------------------------------------|----------------|-----|-----|-----|---|
|                                      | PM             | G56 | G48 |     |   |
| P1.2/UCA0CLK/A2                      | 22             | 26  | 24  | I/O | General-purpose I/O<br>eUSCI_A0 SPI clock input/output<br>Analog input A2   |
| P1.1/UCA0RXD/UCA0SOMI/ A1/<br>Veref+ | 23             | 27  | 25  | I/O | General-purpose I/O<br>eUSCI_A0 UART receive data<br>eUSCI_A0 SPI slave out/master in<br>Analog input A1, and ADC positive reference  |
| P1.0/UCA0TXD/UCA0SIMO/ A0/<br>Veref- | 24             | 28  | 26  | I/O | General-purpose I/O<br>eUSCI_A0 UART transmit data<br>eUSCI_A0 SPI slave in/master out<br>Analog input A0, and ADC negative reference |
| P5.7/L39 <sup>(1)</sup>              | 25             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P5.6/L38 <sup>(1)</sup>              | 26             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P5.5/L37 <sup>(1)</sup>              | 27             | 29  | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P5.4/L36 <sup>(1)</sup>              | 28             | 30  | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P5.3/UCB0SOMI/UCB0SCL/L35            | 29             | 31  | 27  | I/O | General-purpose I/O<br>eUSCI_B0 SPI slave out/master in; eUSCI_B0 I2C clock<br>LCD drive pin; either segment or common output         |
| P5.2/UCB0SIMO/UCB0SDA/L34            | 30             | 32  | 28  | I/O | General-purpose I/O<br>eUSCI_B0 SPI slave in/master out; eUSCI_B0 I2C data<br>LCD drive pin; either segment or common output          |
| P5.1/UCB0CLK/L33                     | 31             | 33  | 29  | I/O | General-purpose I/O<br>eUSCI_B0 clock input/output<br>LCD drive pin; either segment or common output                                  |
| P5.0/UCB0STE/L32                     | 32             | 34  | 30  | I/O | General-purpose I/O<br>eUSCI_B0 slave transmit enable<br>LCD drive pin; either segment or common output                               |
| P2.7/L31                             | 33             | 35  | 31  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.6/L30                             | 34             | 36  | 32  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.5/L29                             | 35             | 37  | 33  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.4/L28                             | 36             | 38  | 34  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.3/L27                             | 37             | 39  | 35  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.2/L26                             | 38             | 40  | 36  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.1/L25                             | 39             | 41  | 37  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P2.0/L24                             | 40             | 42  | 38  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.7/L23 <sup>(1)</sup>              | 41             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.6/L22 <sup>(1)</sup>              | 42             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.5/L21 <sup>(1)</sup>              | 43             | 43  | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.4/L20 <sup>(1)</sup>              | 44             | 44  | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.3/L19                             | 45             | 45  | 39  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |
| P6.2/L18                             | 46             | 46  | 40  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output   |

**Table 7-1. Signal Descriptions (continued)**

| TERMINAL               |                |     |     | I/O | DESCRIPTION   |
|------------------------|----------------|-----|-----|-----|---|
| NAME                   | PACKAGE SUFFIX |     |     |     |   |
|                        | PM             | G56 | G48 |     |   |
| P6.1/L17               | 47             | 47  | 41  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P6.0/L16               | 48             | 48  | 42  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.7/L15               | 49             | 49  | 43  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.6/L14               | 50             | 50  | 44  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.5/L13               | 51             | 51  | 45  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.4/L12               | 52             | 52  | 46  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.3/L11               | 53             | 53  | 47  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.2/L10               | 54             | 54  | 48  | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.1/L9                | 55             | 55  | 1   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P3.0/L8                | 56             | 56  | 2   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.7/L7 <sup>(1)</sup> | 57             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.6/L6 <sup>(1)</sup> | 58             | –   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.5/L5 <sup>(1)</sup> | 59             | 1   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.4/L4 <sup>(1)</sup> | 60             | 2   | –   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.3/L3                | 61             | 3   | 3   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.2/L2                | 62             | 4   | 4   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.1/L1                | 63             | 5   | 5   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |
| P7.0/L0                | 64             | 6   | 6   | I/O | General-purpose I/O<br>LCD drive pin; either segment or common output |

(1) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.

(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

## 7.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 9.9.13](#).

## 7.4 Connection of Unused Pins

Table 7-2 shows the correct termination of unused pins.

**Table 7-2. Connection of Unused Pins**

| PIN <sup>(1)</sup> | POTENTIAL | COMMENT  |
|--------------------|-----------|--|
| Px.0 to Px.7       | Open      | Switched to port function, output direction (PxDIR.n = 1)                            |
| RST/NMI            | DVCC      | 47-kΩ pullup or internal pullup selected with 10-nF (1.1-nF) pulldown <sup>(2)</sup> |
| TEST               | Open      | This pin always has an internal pulldown enabled.                                    |

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  | MIN  | MAX                                | UNIT |
|--|------|------------------------------------|------|
| Voltage applied at DVCC pin to V <sub>SS</sub>       | −0.3 | 4.1                                | V    |
| Voltage applied to any pin <sup>(2)</sup>            | −0.3 | V <sub>CC</sub> + 0.3<br>(4.1 Max) | V    |
| Diode current at any device pin                      |      | ±2                                 | mA   |
| Maximum junction temperature, T <sub>J</sub>         |      | 85                                 | °C   |
| Storage temperature, T <sub>stg</sub> <sup>(3)</sup> | −40  | 125                                | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage or memory corruption to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V<sub>SS</sub>.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 8.2 ESD Ratings

|  |  | VALUE | UNIT |
|--|--|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 | V    |
|  | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

### 8.3 Recommended Operating Conditions

Typical values are specified at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C (unless otherwise noted)

|                     |   | MIN   | NOM | MAX               | UNIT |
|---------------------|---|---|-----|-------------------|------|
| V <sub>CC</sub>     | Supply voltage applied at DVCC pin <sup>(1) (2) (3)</sup>       | 1.8 <sup>(6)</sup>                                    |     | 3.6               | V    |
| V <sub>SS</sub>     | Supply voltage applied at DVSS pin                              |   | 0   |                   | V    |
| T <sub>A</sub>      | Operating free-air temperature                                  | −40   |     | 85                | °C   |
| T <sub>J</sub>      | Operating junction temperature                                  | −40   |     | 85                | °C   |
| C <sub>DVCC</sub>   | Recommended capacitor at DVCC <sup>(5)</sup>                    | 4.7   | 10  |                   | μF   |
| f <sub>SYSTEM</sub> | Processor frequency (maximum MCLK frequency) <sup>(6) (4)</sup> | No FRAM wait states<br>(NWAITSx = 0)                  |     | 8                 | MHz  |
|                     |   | With FRAM wait states<br>(NWAITSx = 1) <sup>(7)</sup> |     | 16 <sup>(8)</sup> |      |
| f <sub>ACLK</sub>   | Maximum ACLK frequency  |   |     | 40                | kHz  |
| f <sub>SMCLK</sub>  | Maximum SMCLK frequency   |   |     | 16 <sup>(8)</sup> | MHz  |

- (1) Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C<sub>DVCC</sub> limits the slopes accordingly.
- (2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
- (6) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in [Section 8.12.1.1](#).
- (7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
- (8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.



## 8.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

See (1)

| PARAMETER                           | EXECUTION MEMORY             | TEST CONDITIONS | Frequency (f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |     |   |     |   |      | UNIT |
|-------------------------------------|------------------------------|-----------------|---|-----|---|-----|---|------|------|
|                                     |                              |                 | 1 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 8 MHz<br>0 WAIT STATES<br>(NWAITS <sub>x</sub> = 0) |     | 16 MHz<br>1 WAIT STATE<br>(NWAITS <sub>x</sub> = 1) |      |      |
|                                     |                              |                 | TYP   | MAX | TYP   | MAX | TYP   | MAX  |      |
| I <sub>AM, FRAM</sub> (0%)          | FRAM<br>0% cache hit ratio   | 3 V, 25°C       | 504   |     | 2874  |     | 3156  | 3700 | μA   |
|                                     |                              | 3 V, 85°C       | 516   |     | 2919  |     | 3205  |      |      |
| I <sub>AM, FRAM</sub> (100%)        | FRAM<br>100% cache hit ratio | 3 V, 25°C       | 209   |     | 633   |     | 1056  | 1298 | μA   |
|                                     |                              | 3 V, 85°C       | 217   |     | 647   |     | 1074  |      |      |
| I <sub>AM, RAM</sub> <sup>(2)</sup> | RAM                          | 3 V, 25°C       | 231   |     | 809   |     | 1450  |      | μA   |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current. Characterized with program executing typical data processing.

$f_{ACLK} = 32786$  Hz,  $f_{MCLK} = f_{SMCLK} = f_{DCO}$  at specified frequency

Program and data entirely reside in FRAM. All execution is from FRAM.

(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

## 8.5 Active Mode Supply Current Per MHz

$V_{CC} = 3$  V,  $T_A = 25^\circ C$  (unless otherwise noted)

| PARAMETER          | TEST CONDITIONS  | TYP | UNIT        |
|--------------------|--|-----|-------------|
| $dI_{AM, FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states (1) | 126 | $\mu A/MHz$ |

(1) All peripherals are turned on in default settings.

## 8.6 Low-Power Mode LPM0 Supply Currents Into $V_{CC}$ Excluding External Current

$V_{CC} = 3$  V,  $T_A = 25^\circ C$  (unless otherwise noted) (1) (2)

| PARAMETER  | V <sub>CC</sub> | FREQUENCY (f <sub>SMCLK</sub> ) |     |       |     |        |     | UNIT |
|--|-----------------|---------------------------------|-----|-------|-----|--------|-----|------|
|  |                 | 1 MHz                           |     | 8 MHz |     | 16 MHz |     |      |
|  |                 | TYP                             | MAX | TYP   | MAX | TYP    | MAX |      |
| I <sub>LPM0</sub> Low-power mode LPM0 supply current | 2 V             | 158                             |     | 307   |     | 415    |     | μA   |
|  | 3 V             | 169                             |     | 318   |     | 427    |     |      |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32786$  Hz,  $f_{MCLK} = 0$  MHz,  $f_{SMCLK}$  at specified frequency.

## 8.7 Low-Power Mode LPM3, LPM4 Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER         |   | $V_{CC}$ | –40°C |     | 25°C |      | 85°C |     | UNIT    |
|-------------------|---|----------|-------|-----|------|------|------|-----|---------|
|                   |   |          | TYP   | MAX | TYP  | MAX  | TYP  | MAX |         |
| $I_{LPM3,XT1}$    | Low-power mode 3, includes SVS <sup>(2) (3) (4)</sup> | 3 V      | 1.13  |     | 1.31 | 1.99 | 3.00 |     | $\mu A$ |
|                   |   | 2 V      | 1.06  |     | 1.21 |      | 2.94 |     |         |
| $I_{LPM3,VLO}$    | Low-power mode 3, VLO, excludes SVS <sup>(5)</sup>    | 3 V      | 0.92  |     | 1.00 | 1.75 | 2.89 |     | $\mu A$ |
|                   |   | 2 V      | 0.86  |     | 1.00 |      | 2.75 |     |         |
| $I_{LPM3,LCD,CP}$ | Low-power mode 3, LCD, excludes SVS <sup>(6)</sup>    | 3 V      | 1.07  |     | 1.25 |      | 3.04 |     | $\mu A$ |
| $I_{LPM3,RTC}$    | Low-power mode 3, RTC, excludes SVS <sup>(7)</sup>    | 3 V      | 1.08  |     | 1.25 |      | 3.04 |     | $\mu A$ |
| $I_{LPM4,SVS}$    | Low-power mode 4, includes SVS                        | 3 V      | 0.65  |     | 0.75 |      | 1.88 |     | $\mu A$ |
|                   |   | 2 V      | 0.63  |     | 0.73 |      | 1.85 |     |         |
| $I_{LPM4}$        | Low-power mode 4, excludes SVS                        | 3 V      | 0.51  |     | 0.58 |      | 1.51 |     | $\mu A$ |
|                   |   | 2 V      | 0.50  |     | 0.57 |      | 1.49 |     |         |

(1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current

(2) Not applicable for devices with HF crystal oscillator only.

(3) Characterized with a Golledge MS1V-TK/I\_32.768KHZ crystal with a load capacitance chosen to closely match the required load.

(4) **Low-power mode 3, includes SVS** test conditions:

Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz

(5) **Low-power mode 3, VLO, excludes SVS** test conditions:

Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz

(6) LCD works in LPM3 if internal charge pump and  $V_{REF}$  switch mode are enabled. LCD driver pins are configured as 4 × 36 at 32-Hz frame frequency with external 32768-Hz clock source.

(7) RTC periodically wakes up every second with external 32768-Hz as source.

## 8.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |   | $V_{CC}$ | –40°C |     | 25°C  |       | 85°C  |       | UNIT    |
|-----------------------|---|----------|-------|-----|-------|-------|-------|-------|---------|
|                       |   |          | TYP   | MAX | TYP   | MAX   | TYP   | MAX   |         |
| $I_{LPM3.5, XT1}$     | Low-power mode 3.5, includes SVS <sup>(1) (2) (3)</sup><br>(also see <a href="#">Figure 8-3</a> ) | 3 V      | 0.71  |     | 0.77  | 1.25  | 1.06  | 2.06  | $\mu A$ |
|                       |   | 2 V      | 0.66  |     | 0.70  |       | 0.95  |       |         |
| $I_{LPM3.5, LCD, CP}$ | Low-power mode 3.5, excludes SVS <sup>(6)</sup>   | 3 V      | 0.90  |     | 0.94  |       | 1.27  |       | $\mu A$ |
| $I_{LPM4.5, SVS}$     | Low-power mode 4.5, includes SVS <sup>(4)</sup>   | 3 V      | 0.23  |     | 0.25  | 0.375 | 0.32  | 0.43  | $\mu A$ |
|                       |   | 2 V      | 0.20  |     | 0.20  |       | 0.24  |       |         |
| $I_{LPM4.5}$          | Low-power mode 4.5, excludes SVS <sup>(5)</sup>   | 3 V      | 0.010 |     | 0.015 | 0.070 | 0.073 | 0.140 | $\mu A$ |
|                       |   | 2 V      | 0.008 |     | 0.013 |       | 0.060 |       |         |

(1) Not applicable for devices with HF crystal oscillator only.

(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance chosen to closely match the required load.

(3) **Low-power mode 3.5, includes SVS** test conditions:

Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 32768$  Hz,  $f_{ACLK} = f_{XT1}$ ,  $f_{MCLK} = f_{SMCLK} = 0$  MHz

(4) **Low-power mode 4.5, includes SVS** test conditions:

Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz

(5) **Low-power mode 4.5, excludes SVS** test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.

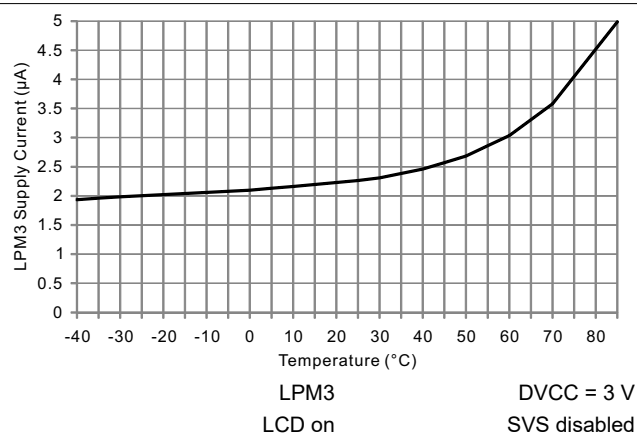
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 0$  Hz,  $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz

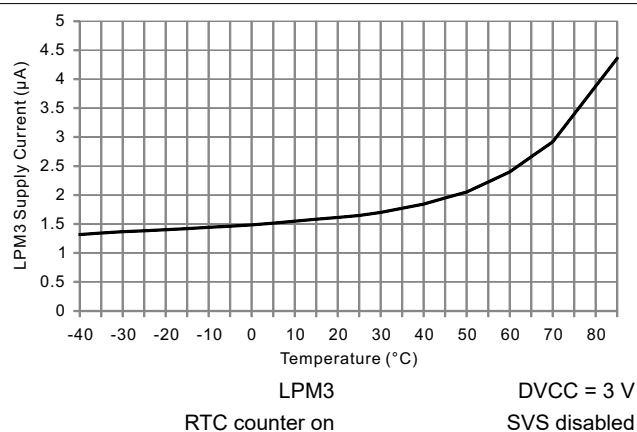
(6) LCD works in LPM3.5 if the internal charge pump and VREF switch mode are enabled. The LCD driver pins are configured as 4x36 at 32-Hz frame frequency with an external 32768-Hz clock source.

## 8.9 Typical Characteristics, Low-Power Mode Supply Currents

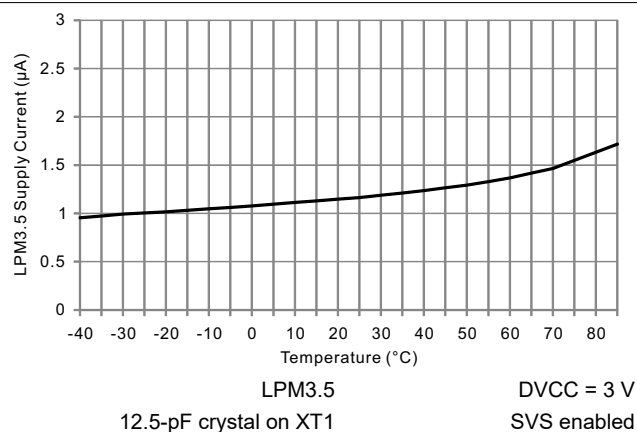
The graphs in this section show only board-level test result on a small number of samples. A MS1V-T1K crystal from Micro-Crystal was populated for 32-kHz clock generation. LCD is configured in 4xCOM mode without LCD panel populated.



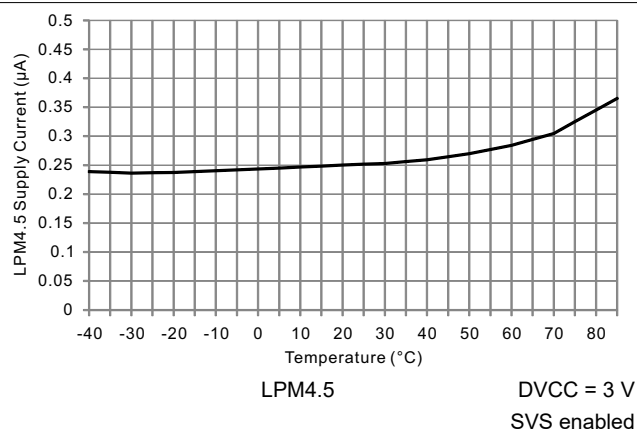
**Figure 8-1. LPM3 Supply Current vs Temperature**



**Figure 8-2. LPM3 Supply Current vs Temperature**



**Figure 8-3. LPM3.5 Supply Current vs Temperature**



**Figure 8-4. LPM4.5 Supply Current vs Temperature**

## 8.10 Current Consumption Per Module

| MODULE  | TEST CONDITIONS                  | REFERENCE CLOCK    | TYP | UNIT   |
|---------|----------------------------------|--------------------|-----|--------|
| Timer_A |                                  | Module input clock | 5   | μA/MHz |
| eUSCI_A | UART mode                        | Module input clock | 7   | μA/MHz |
| eUSCI_A | SPI mode                         | Module input clock | 5   | μA/MHz |
| eUSCI_B | SPI mode                         | Module input clock | 5   | μA/MHz |
| eUSCI_B | I <sup>2</sup> C mode, 100 kbaud | Module input clock | 5   | μA/MHz |
| RTC     |                                  | 32 kHz             | 85  | nA     |
| CRC     | From start to end of operation   | MCLK               | 8.5 | μA/MHz |

## 8.11 Thermal Characteristics

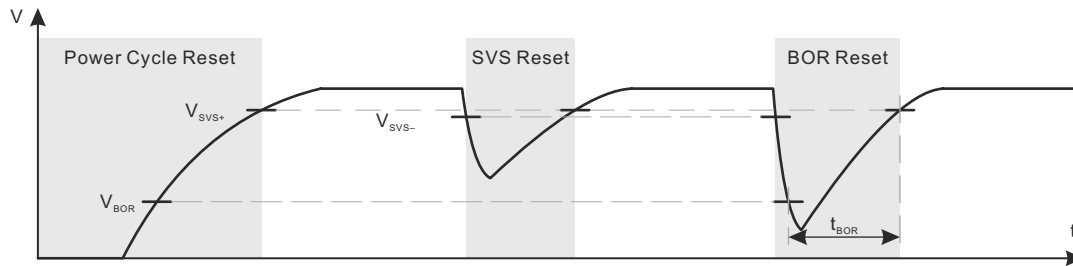
| PARAMETER            |  |                  | VALUE | UNIT |
|----------------------|--|------------------|-------|------|
| $\theta_{JA}$        | Junction-to-ambient thermal resistance, still air <sup>(1)</sup> | LQFP-64 (PM)     | 61.7  | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance <sup>(2)</sup>         |                  | 25.4  | °C/W |
| $\theta_{JB}$        | Junction-to-board thermal resistance <sup>(3)</sup>              |                  | 32.7  | °C/W |
| $\Psi_{JB}$          | Junction-to-board thermal characterization parameter             |                  | 32.4  | °C/W |
| $\Psi_{JT}$          | Junction-to-top thermal characterization parameter               |                  | 2.5   | °C/W |
| $\theta_{JA}$        | Junction-to-ambient thermal resistance, still air <sup>(1)</sup> | TSSOP-56 (DGG56) | 62.4  | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance <sup>(2)</sup>         |                  | 18.7  | °C/W |
| $\theta_{JB}$        | Junction-to-board thermal resistance <sup>(3)</sup>              |                  | 31.4  | °C/W |
| $\Psi_{JB}$          | Junction-to-board thermal characterization parameter             |                  | 31.1  | °C/W |
| $\Psi_{JT}$          | Junction-to-top thermal characterization parameter               |                  | 0.8   | °C/W |
| $\theta_{JA}$        | Junction-to-ambient thermal resistance, still air <sup>(1)</sup> | TSSOP-48 (DGG48) | 68.9  | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance <sup>(2)</sup>         |                  | 23    | °C/W |
| $\theta_{JB}$        | Junction-to-board thermal resistance <sup>(3)</sup>              |                  | 35.8  | °C/W |
| $\Psi_{JB}$          | Junction-to-board thermal characterization parameter             |                  | 35.3  | °C/W |
| $\Psi_{JT}$          | Junction-to-top thermal characterization parameter               |                  | 1.1   | °C/W |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold place fixture to control the PCB temperature, as described in JESD51-8.

## 8.12 Timing and Switching Characteristics

### 8.12.1 Power Supply Sequencing

Figure 8-5 shows the power cycle, SVS, and BOR reset conditions.



**Figure 8-5. Power Cycle, SVS, and BOR Reset Conditions**

Section 8.12.1.1 lists the characteristics of the SVS and BOR.

#### 8.12.1.1 PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  |   | TEST CONDITIONS         | MIN   | TYP  | MAX   | UNIT |
|----------------------------|---|-------------------------|-------|------|-------|------|
| V <sub>BOR, safe</sub>     | Safe BOR power-down level <sup>(1)</sup>              |                         | 0.1   |      |       | V    |
| t <sub>BOR, safe</sub>     | Safe BOR reset delay <sup>(2)</sup>                   |                         | 10    |      |       | ms   |
| I <sub>SVSH, AM</sub>      | SVS <sub>H</sub> current consumption, active mode     | V <sub>CC</sub> = 3.6 V |       |      | 1.5   | μA   |
| I <sub>SVSH, LPM</sub>     | SVS <sub>H</sub> current consumption, low-power modes | V <sub>CC</sub> = 3.6 V |       | 240  |       | nA   |
| V <sub>SVSH-</sub>         | SVS <sub>H</sub> power-down level <sup>(4)</sup>      |                         | 1.71  | 1.81 | 1.87  | V    |
| V <sub>SVSH+</sub>         | SVS <sub>H</sub> power-up level <sup>(4)</sup>        |                         | 1.76  | 1.88 | 1.99  | V    |
| V <sub>SVSH_hys</sub>      | SVS <sub>H</sub> hysteresis                           |                         |       | 70   |       | mV   |
| t <sub>PD, SVSH, AM</sub>  | SVS <sub>H</sub> propagation delay, active mode       |                         |       |      | 10    | μs   |
| t <sub>PD, SVSH, LPM</sub> | SVS <sub>H</sub> propagation delay, low-power modes   |                         |       |      | 100   | μs   |
| V <sub>REF, 1.2V</sub>     | 1.2-V REF voltage <sup>(3)</sup>                      |                         | 1.158 | 1.20 | 1.242 | V    |

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.

(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V<sub>SVSH+</sub>.

(3) This is a characterized result with external 1-mA load to ground from –40°C to 85°C.

(4) For additional information, see the [Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO reference design](#).

## 8.12.2 Reset Timing

Section 8.12.2.1 lists the device wake-up times.

### 8.12.2.1 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |   | TEST CONDITIONS | V <sub>CC</sub> | MIN | TYP | MAX                           | UNIT |
|-----------------------------|---|-----------------|-----------------|-----|-----|-------------------------------|------|
| t <sub>WAKE-UP FRAM</sub>   | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wake-up <sup>(1)</sup> |                 | 3 V             |     | 10  |                               | μs   |
| t <sub>WAKE-UP LPM0</sub>   | Wake-up time from LPM0 to active mode <sup>(1)</sup>  |                 | 3 V             |     |     | 200 ns + 2.5/f <sub>DCO</sub> |      |
| t <sub>WAKE-UP LPM3</sub>   | Wake-up time from LPM3 to active mode <sup>(2)</sup>  |                 | 3 V             |     | 10  |                               | μs   |
| t <sub>WAKE-UP LPM4</sub>   | Wake-up time from LPM4 to active mode   |                 | 3 V             |     | 10  |                               | μs   |
| t <sub>WAKE-UP LPM3.5</sub> | Wake-up time from LPM3.5 to active mode <sup>(2)</sup>  |                 | 3 V             |     | 350 |                               | μs   |
| t <sub>WAKE-UP LPM4.5</sub> | Wake-up time from LPM4.5 to active mode <sup>(2)</sup>  | SVSHE = 1       | 3 V             |     | 350 |                               | μs   |
|                             |   | SVSHE = 0       | 3 V             |     | 1   |                               | ms   |
| t <sub>WAKE-UP-RESET</sub>  | Wake-up time from RST or BOR event to active mode <sup>(2)</sup>  |                 | 3 V             |     | 1   |                               | ms   |
| t <sub>RESET</sub>          | Pulse duration required at RST/NMI pin to accept a reset  |                 | 3 V             | 2   |     |                               | μs   |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.



## 8.12.3 Clock Specifications

Section 8.12.3.1 lists the characteristics of XT1.

### 8.12.3.1 XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                | TEST CONDITIONS  | V <sub>CC</sub>  | MIN | TYP   | MAX  | UNIT |
|--------------------------|--|--|-----|-------|------|------|
| f <sub>XT1, LF</sub>     | XT1 oscillator crystal, low frequency                    | LFXTBYPASS = 0   |     | 32768 |      | Hz   |
| DC <sub>XT1, LF</sub>    | XT1 oscillator LF duty cycle                             | Measured at MCLK, f <sub>LFXT</sub> = 32768 Hz   | 30% |       | 70%  |      |
| f <sub>XT1, SW</sub>     | XT1 oscillator logic-level square-wave input frequency   | LFXTBYPASS = 1 <sup>(3) (4)</sup>  |     | 32768 |      | Hz   |
| DC <sub>XT1, SW</sub>    | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1   | 40% |       | 60%  |      |
| OA <sub>LFXT</sub>       | Oscillation allowance for LF crystals <sup>(5)</sup>     | LFXTBYPASS = 0, LFXTDRIVE = {3}, f <sub>LFXT</sub> = 32768 Hz, C <sub>L, eff</sub> = 12.5 pF                       |     | 200   |      | kΩ   |
| C <sub>L, eff</sub>      | Integrated effective load capacitance <sup>(6)</sup>     | See <sup>(7)</sup>   |     | 1     |      | pF   |
| t <sub>START, LFXT</sub> | Start-up time <sup>(9)</sup>                             | f <sub>OSC</sub> = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T <sub>A</sub> = 25°C, C <sub>L, eff</sub> = 12.5 pF |     | 1000  |      | ms   |
| f <sub>Fault, LFXT</sub> | Oscillator fault frequency <sup>(10)</sup>               | XTS = 0 <sup>(8)</sup>   | 0   |       | 3500 | Hz   |

- (1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) See [MSP430 32-kHz Crystal Oscillators](#) for details on crystal section, layout, and testing.
- (3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DC<sub>LFXT, SW</sub>.
- (4) Maximum frequency of operation of the entire device cannot be exceeded.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  - For LFXTDRIVE = {0}, C<sub>L, eff</sub> = 3.7 pF.
  - For LFXTDRIVE = {1}, 6 pF ≤ C<sub>L, eff</sub> ≤ 9 pF.
  - For LFXTDRIVE = {2}, 6 pF ≤ C<sub>L, eff</sub> ≤ 10 pF.
  - For LFXTDRIVE = {3}, 6 pF ≤ C<sub>L, eff</sub> ≤ 12 pF.
- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
- (7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.
- (9) Includes startup counter of 1024 clock cycles.
- (10) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.

### 8.12.3.2 DCO FLL, Frequency

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER              |   | TEST CONDITIONS                                      | V <sub>CC</sub> | MIN   | TYP    | MAX  | UNIT |
|------------------------|---|--|-----------------|-------|--------|------|------|
| f <sub>DCO, FLL</sub>  | FLL lock frequency, 16 MHz, 25°C          | Measured at MCLK, Internal trimmed REFO as reference | 3 V             | –1.0% |        | 1.0% |      |
|                        | FLL lock frequency, 16 MHz, –40°C to 85°C |  | 3 V             | –2.0% |        | 2.0% |      |
|                        | FLL lock frequency, 16 MHz, –40°C to 85°C | Measured at MCLK, XT1 crystal as reference           | 3 V             | –0.5% |        | 0.5% |      |
| f <sub>DUTY</sub>      | Duty cycle                                | Measured at MCLK, XT1 crystal as reference           | 3 V             | 40%   | 50%    | 60%  |      |
| Jitter <sub>cc</sub>   | Cycle-to-cycle jitter, 16 MHz             |  | 3 V             |       | 0.25%  |      |      |
| Jitter <sub>long</sub> | Long-term jitter, 16 MHz                  |  | 3 V             |       | 0.022% |      |      |
| t <sub>FLL, lock</sub> | FLL lock time                             |  | 3 V             |       | 120    |      | ms   |

Section 8.12.3.3 lists the characteristics of the REFO.

### 8.12.3.3 REFO

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER                            |                                     | TEST CONDITIONS                         | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|--------------------------------------|-------------------------------------|---|-----------------|-------|-------|-------|------|
| I <sub>REFO</sub>                    | REFO oscillator current consumption | T <sub>A</sub> = 25°C                   | 3 V             |       | 15    |       | μA   |
| f <sub>REFO</sub>                    | REFO calibrated frequency           | Measured at MCLK                        | 3 V             |       | 32768 |       | Hz   |
|                                      | REFO absolute calibrated tolerance  | T <sub>A</sub> = –40°C to 85°C          | 1.8 V to 3.6 V  | –3.5% |       | +3.5% |      |
| df <sub>REFO</sub> /dT               | REFO frequency temperature drift    | Measured at MCLK <sup>(1)</sup>         | 3 V             |       | 0.01  |       | %/°C |
| df <sub>REFO</sub> /dV <sub>CC</sub> | REFO frequency supply voltage drift | Measured at MCLK at 25°C <sup>(2)</sup> | 1.8 V to 3.6 V  |       | 1     |       | %/V  |
| f <sub>DC</sub>                      | REFO duty cycle                     | Measured at MCLK                        | 1.8 V to 3.6 V  | 40%   | 50%   | 60%   |      |
| t <sub>START</sub>                   | REFO startup time                   | 40% to 60% duty cycle                   |                 |       | 50    |       | μs   |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Section 8.12.3.4 lists the characteristics of the VLO.

### 8.12.3.4 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                      | Measured at MCLK                | 3 V             |     | 10  |     | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | Measured at MCLK <sup>(1)</sup> | 3 V             |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | Measured at MCLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 4   |     | %/V  |
| f <sub>VLO,DC</sub>                 | Duty cycle                         | Measured at MCLK                | 3 V             |     | 50% |     |      |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

#### Note

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Section 8.12.3.4).

Section 8.12.3.5 lists the characteristics of the MODCLK.

### 8.12.3.5 Module Oscillator Clock (MODCLK)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                             |                                       | V <sub>CC</sub> | MIN | TYP   | MAX | UNIT |
|---------------------------------------|---------------------------------------|-----------------|-----|-------|-----|------|
| f <sub>MODCLK</sub>                   | MODCLK frequency                      | 3 V             | 3.8 | 4.8   | 5.8 | MHz  |
| f <sub>MODCLK</sub> /dT               | MODCLK frequency temperature drift    | 3 V             |     | 0.102 |     | %/°C |
| f <sub>MODCLK</sub> /dV <sub>CC</sub> | MODCLK frequency supply voltage drift | 1.8 V to 3.6 V  |     | 1.02  |     | %/V  |
| f <sub>MODCLK,DC</sub>                | Duty cycle                            | 3 V             | 40% | 50%   | 60% |      |

## 8.12.4 Digital I/Os

Section 8.12.4.1 lists the characteristics of the digital inputs.

### 8.12.4.1 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|---|--|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage   |  | 2 V             | 0.90 |     | 1.50 | V    |
|   |  | 3 V             | 1.35 |     | 2.25 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage   |  | 2 V             | 0.50 |     | 1.10 | V    |
|   |  | 3 V             | 0.75 |     | 1.65 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> )                                    |  | 2 V             | 0.3  |     | 0.8  | V    |
|   |  | 3 V             | 0.4  |     | 1.2  |      |
| R <sub>Pull</sub> Pullup or pulldown resistor   | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I,dig</sub> Input capacitance, digital only port pins  | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |      | 3   |      | pF   |
| C <sub>I,ana</sub> Input capacitance, port pins with shared analog functions  | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>   |                 |      | 5   |      | pF   |
| I <sub>lkg</sub> (P <sub>x,y</sub> ) High-impedance leakage current (also see (1) and (2))                          |  | 2 V, 3 V        | –20  |     | +20  | nA   |
| t <sub>(int)</sub> External interrupt timing (external trigger pulse duration to set interrupt flag) <sup>(3)</sup> | Ports with interrupt capability (see block diagram and terminal function descriptions)           | 2 V, 3 V        | 50   |     |      | ns   |

- (1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pins, unless otherwise noted.
- (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
- (3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

Section 8.12.4.2 lists the characteristics of the digital outputs.

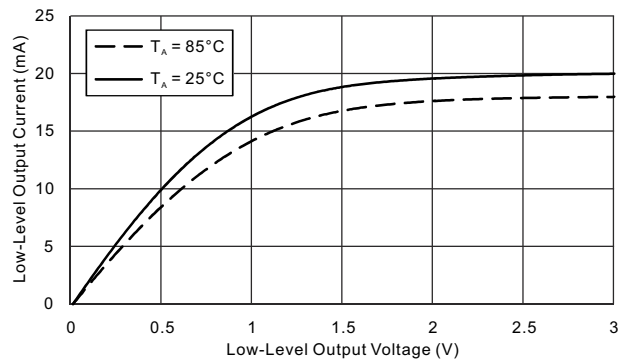
### 8.12.4.2 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

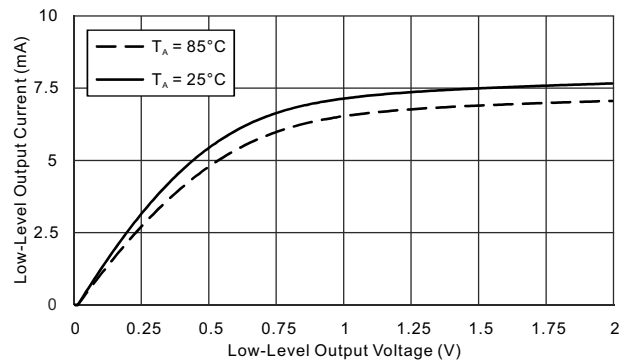
| PARAMETER   | TEST CONDITIONS                             | V <sub>CC</sub> | MIN | TYP | MAX  | UNIT |
|---|---|-----------------|-----|-----|------|------|
| V <sub>OH</sub> High-level output voltage                           | I <sub>(OHmax)</sub> = –3 mA <sup>(1)</sup> | 2 V             | 1.4 |     | 2.0  | V    |
|   | I <sub>(OHmax)</sub> = –5 mA <sup>(1)</sup> | 3 V             | 2.4 |     | 3.0  |      |
| V <sub>OL</sub> Low-level output voltage                            | I <sub>(OLmax)</sub> = 3 mA <sup>(1)</sup>  | 2 V             | 0.0 |     | 0.60 | V    |
|   | I <sub>(OHmax)</sub> = 5 mA <sup>(1)</sup>  | 3 V             | 0.0 |     | 0.60 |      |
| f <sub>Port_CLK</sub> Clock output frequency                        | C <sub>L</sub> = 20 pF <sup>(2)</sup>       | 2 V             | 16  |     |      | MHz  |
|   |   | 3 V             | 16  |     |      |      |
| t <sub>rise,dig</sub> Port output rise time, digital only port pins | C <sub>L</sub> = 20 pF                      | 2 V             |     | 10  |      | ns   |
|   |   | 3 V             |     | 7   |      |      |
| t <sub>fall,dig</sub> Port output fall time, digital only port pins | C <sub>L</sub> = 20 pF                      | 2 V             |     | 10  |      | ns   |
|   |   | 3 V             |     | 5   |      |      |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

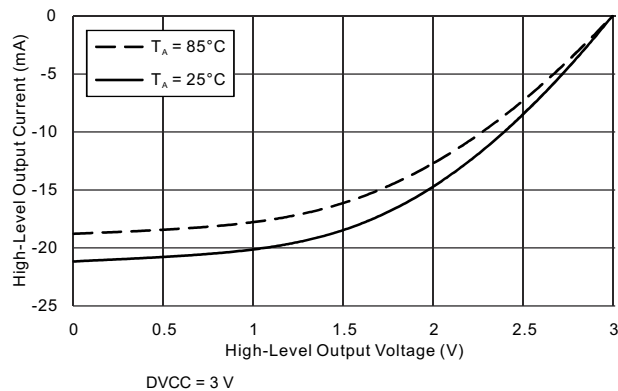
### 8.12.4.3 Digital I/O Typical Characteristics



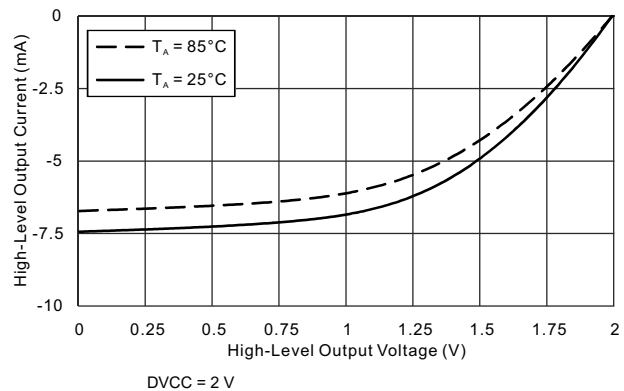
**Figure 8-6. Typical Low-Level Output Current vs Low-Level Output Voltage**



**Figure 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage**



**Figure 8-8. Typical High-Level Output Current vs High-Level Output Voltage**



**Figure 8-9. Typical High-Level Output Current vs High-Level Output Voltage**

### 8.12.5 Timer\_A

Section 8.12.5.1 lists the operating frequency of Timer\_A.

#### 8.12.5.1 Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS   | V <sub>CC</sub> | MIN | MAX | UNIT |
|---|---|-----------------|-----|-----|------|
| f <sub>TA</sub> Timer_A input clock frequency | Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ±10% | 2 V, 3 V        |     | 16  | MHz  |
| t <sub>TA,cap</sub> Timer_A capture timing    | All capture inputs, minimum pulse duration required for capture   | 2 V, 3 V        | 20  |     | ns   |

## 8.12.6 eUSCI

Section 8.12.6.1 lists the operating conditions of the eUSCI in UART mode.

### 8.12.6.1 eUSCI (UART Mode) Operating Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS  | V <sub>CC</sub> | MIN | MAX | UNIT |
|--|--|-----------------|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency                         | Internal: SMCLK, MODCLK<br>External: UCLK<br>Duty cycle = 50% ±10% | 2 V, 3 V        |     | 16  | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals baud rate in Mbaud) |  | 2 V, 3 V        |     | 5   | MHz  |

Section 8.12.6.2 lists the switching characteristics of the eUSCI in UART mode.

### 8.12.6.2 eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS | V <sub>CC</sub> | TYP | UNIT |
|--|-----------------|-----------------|-----|------|
| t <sub>t</sub> UART receive deglitch time <sup>(1)</sup> | UCGLITx = 0     | 2 V, 3 V        | 12  | ns   |
|  | UCGLITx = 1     |                 | 40  |      |
|  | UCGLITx = 2     |                 | 68  |      |
|  | UCGLITx = 3     |                 | 110 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

Section 8.12.6.3 lists the operating conditions of the eUSCI in SPI master mode.

### 8.12.6.3 eUSCI (SPI Master Mode) Operating Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                      | TEST CONDITIONS                                  | MIN | MAX | UNIT |
|--|--|-----|-----|------|
| f <sub>eUSCI</sub> eUSCI input clock frequency | Internal: SMCLK, MODCLK<br>Duty cycle = 50% ±10% |     | 8   | MHz  |

Section 8.12.6.4 lists the switching characteristics of the eUSCI in SPI master mode.

### 8.12.6.4 eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

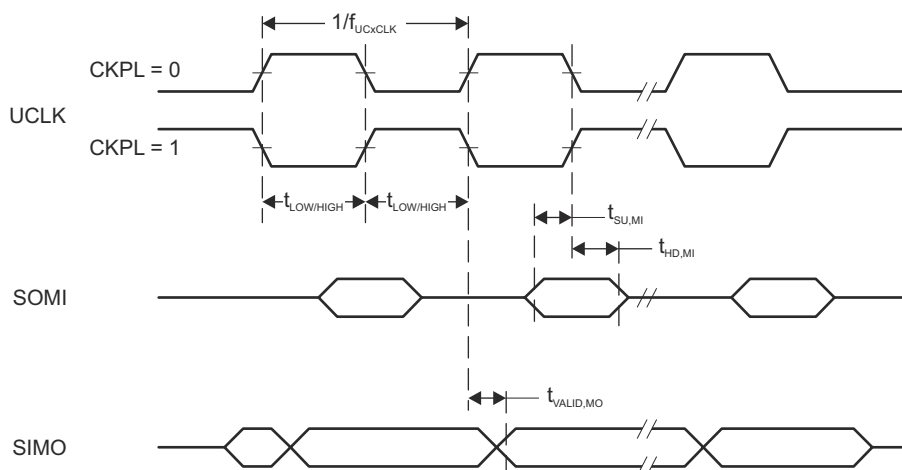
| PARAMETER  | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | MAX | UNIT          |
|--|--|-----------------|-----|-----|---------------|
| t <sub>STE,LEAD</sub> STE lead time, STE active to clock         | UCSTEM = 1, UCMODEx = 01 or 10                     |                 | 1   |     | UCxCLK cycles |
| t <sub>STE,LAG</sub> STE lag time, Last clock to STE inactive    | UCSTEM = 1, UCMODEx = 01 or 10                     |                 | 1   |     | UCxCLK cycles |
| t <sub>SU,MI</sub> SOMI input data setup time                    |  | 2 V             | 45  |     | ns            |
|  |  | 3 V             | 35  |     |               |
| t <sub>HD,MI</sub> SOMI input data hold time                     |  | 2 V             | 0   |     | ns            |
|  |  | 3 V             | 0   |     |               |
| t <sub>VALID,MO</sub> SIMO output data valid time <sup>(2)</sup> | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | 2 V             |     | 20  | ns            |
|  |  | 3 V             |     | 20  |               |
| t <sub>HD,MO</sub> SIMO output data hold time <sup>(3)</sup>     | C <sub>L</sub> = 20 pF                             | 2 V             | 0   |     | ns            |
|  |  | 3 V             | 0   |     |               |

- (1) f<sub>UCxCLK</sub> = 1/2t<sub>LO/HI</sub> with t<sub>LO/HI</sub> = max(t<sub>VALID,MO</sub>(eUSCI) + t<sub>SU,SI</sub>(Slave), t<sub>SU,MI</sub>(eUSCI) + t<sub>VALID,SO</sub>(Slave))

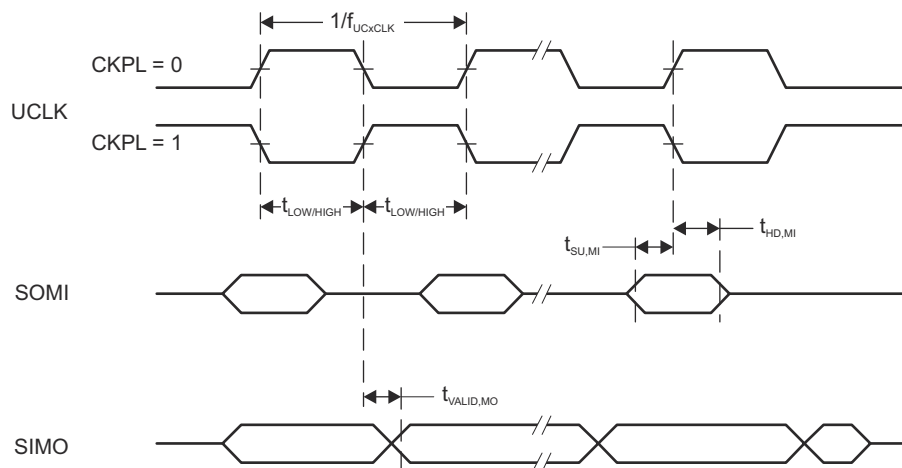
For the slave parameters t<sub>SU,SI</sub>(Slave) and t<sub>VALID,SO</sub>(Slave) see the SPI parameters of the attached slave.

- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-10 and Figure 8-11.

- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 8-10](#) and [Figure 8-11](#).



**Figure 8-10. SPI Master Mode, CKPH = 0**



**Figure 8-11. SPI Master Mode, CKPH = 1**



Section 8.12.6.5 lists the switching characteristics of the eUSCI in SPI slave mode.

#### 8.12.6.5 eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

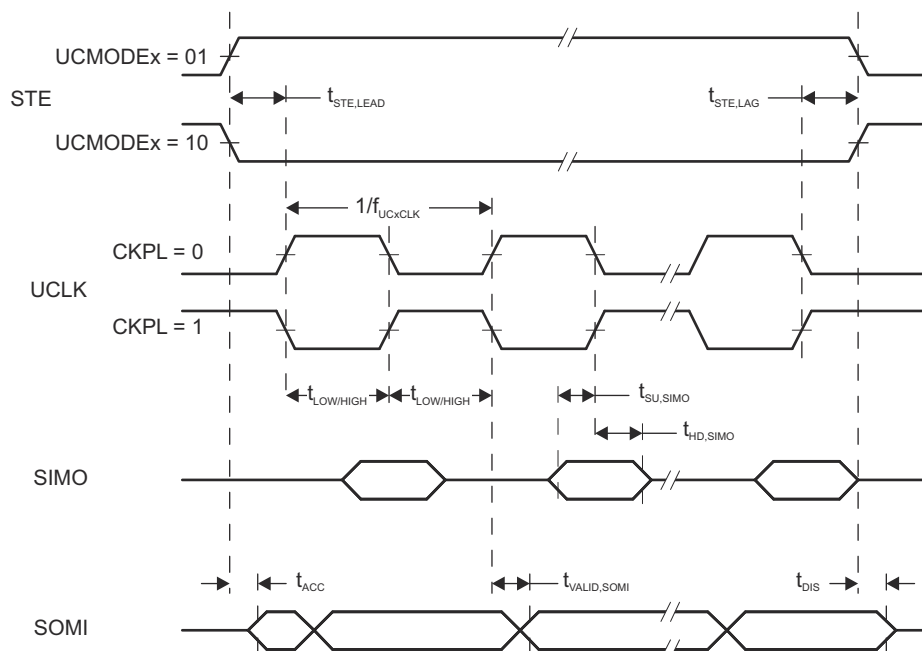
| PARAMETER             |   | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|------|
| t <sub>STE,LEAD</sub> | STE lead time, STE active to clock                    |  | 2 V             | 55  |     | ns   |
|                       |   |  | 3 V             | 45  |     |      |
| t <sub>STE,LAG</sub>  | STE lag time, Last clock to STE inactive              |  | 2 V             | 20  |     | ns   |
|                       |   |  | 3 V             | 20  |     |      |
| t <sub>STE,ACC</sub>  | STE access time, STE active to SOMI data out          |  | 2 V             |     | 65  | ns   |
|                       |   |  | 3 V             |     | 40  |      |
| t <sub>STE,DIS</sub>  | STE disable time, STE inactive to SOMI high impedance |  | 2 V             |     | 40  | ns   |
|                       |   |  | 3 V             |     | 35  |      |
| t <sub>SU,SI</sub>    | SIMO input data setup time                            |  | 2 V             | 4   |     | ns   |
|                       |   |  | 3 V             | 4   |     |      |
| t <sub>HD,SI</sub>    | SIMO input data hold time                             |  | 2 V             | 12  |     | ns   |
|                       |   |  | 3 V             | 12  |     |      |
| t <sub>VALID,SO</sub> | SOMI output data valid time <sup>(2)</sup>            | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2 V             |     | 65  | ns   |
|                       |   |  | 3 V             |     | 40  |      |
| t <sub>HD,SO</sub>    | SOMI output data hold time <sup>(3)</sup>             | C <sub>L</sub> = 20 pF                             | 2 V             | 5   |     | ns   |
|                       |   |  | 3 V             | 5   |     |      |

(1)  $f_{UCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$

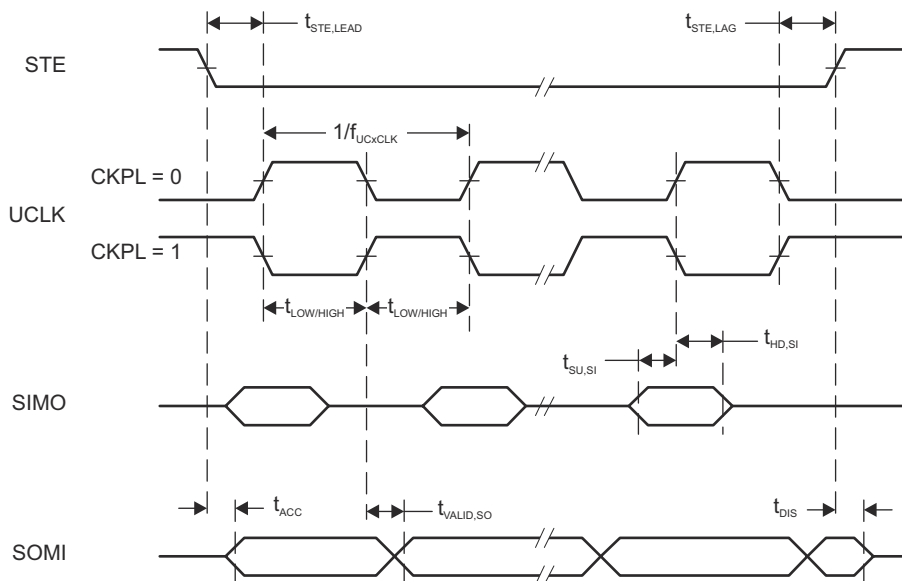
For the master parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$ , see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 8-12 and Figure 8-13.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 8-12 and Figure 8-13.



**Figure 8-12. SPI Slave Mode, CKPH = 0**



**Figure 8-13. SPI Slave Mode, CKPH = 1**

Section 8.12.6.6 lists the switching characteristics of the eUSCI in I<sup>2</sup>C mode.

#### 8.12.6.6 eUSCI (I<sup>2</sup>C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-14)

| PARAMETER            | TEST CONDITIONS   | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|----------------------|---|-----------------|------|-----|-----|------|
| f <sub>eUSCI</sub>   | eUSCI input clock frequency<br>Internal: SMCLK, MODCLK<br>External: UCLK<br>Duty cycle = 50% ±10% |                 |      |     | 16  | MHz  |
| f <sub>SCL</sub>     | SCL clock frequency   | 2 V, 3 V        | 0    |     | 400 | kHz  |
| t <sub>HD,STA</sub>  | Hold time (repeated) START  | 2 V, 3 V        | 4.0  |     |     | μs   |
|                      | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz  |                 | 0.6  |     |     |      |
| t <sub>SU,STA</sub>  | Setup time for a repeated START   | 2 V, 3 V        | 4.7  |     |     | μs   |
|                      | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz  |                 | 0.6  |     |     |      |
| t <sub>HD,DAT</sub>  | Data hold time  | 2 V, 3 V        | 0    |     |     | ns   |
| t <sub>SU,DAT</sub>  | Data setup time   | 2 V, 3 V        | 250  |     |     | ns   |
| t <sub>SU,STO</sub>  | Setup time for STOP   | 2 V, 3 V        | 4.0  |     |     | μs   |
|                      | f <sub>SCL</sub> = 100 kHz<br>f <sub>SCL</sub> > 100 kHz  |                 | 0.6  |     |     |      |
| t <sub>SP</sub>      | Pulse duration of spikes suppressed by input filter   | 2 V, 3 V        | 50   |     | 600 | ns   |
|                      | UCGLITx = 1   |                 | 25   |     | 300 |      |
|                      | UCGLITx = 2   |                 | 12.5 |     | 150 |      |
|                      | UCGLITx = 3   |                 | 6.3  |     | 75  |      |
| t <sub>TIMEOUT</sub> | Clock low time-out  | 2 V, 3 V        |      | 27  |     | ms   |
|                      | UCCLTOx = 2   |                 |      | 30  |     |      |
|                      | UCCLTOx = 3   |                 |      | 33  |     |      |

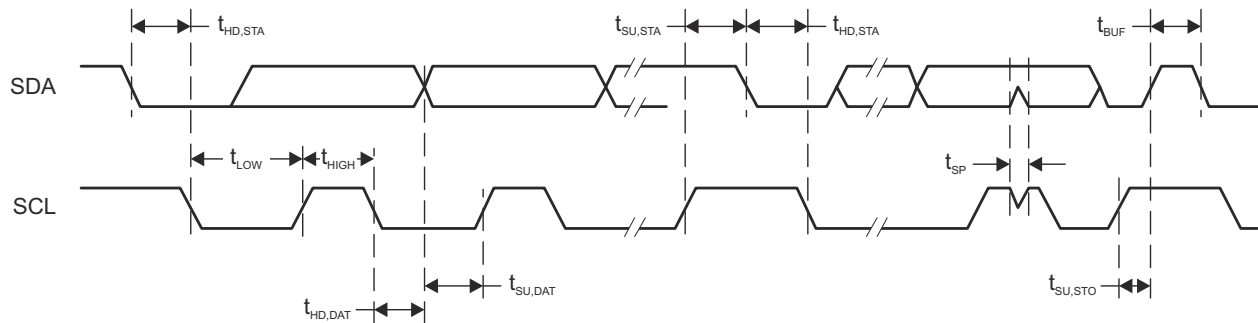


Figure 8-14. I<sup>2</sup>C Mode Timing

## 8.12.7 ADC

Section 8.12.7.1 lists the power supply and input conditions of the ADC.

### 8.12.7.1 ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS   | V <sub>CC</sub>  | MIN   | TYP | MAX              | UNIT |
|---------------------|---|--|-------|-----|------------------|------|
| DV <sub>CC</sub>    | ADC supply voltage  |  | 2.0   |     | 3.6              | V    |
| V <sub>(Ax)</sub>   | Analog input voltage range  | All ADC pins   | 0     |     | DV <sub>CC</sub> | V    |
| I <sub>ADC</sub>    | Operating supply current into DV <sub>CC</sub> terminal, reference current not included, repeat-single-channel mode | f <sub>ADCCLK</sub> = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b                | 2 V   | 185 |                  | μA   |
|                     |   |  | 3 V   | 207 |                  |      |
| C <sub>I</sub>      | Input capacitance   | Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad | 2.2 V | 1.6 | 2.0              | pF   |
| R <sub>I,MUX</sub>  | Input MUX ON resistance   | DV <sub>CC</sub> = 2 V, 0 V ≤ V <sub>Ax</sub> ≤ DV <sub>CC</sub>   |       |     | 2                | kΩ   |
| R <sub>I,Misc</sub> | Input miscellaneous resistance  |  |       | 34  |                  | kΩ   |

Section 8.12.7.2 lists the timing parameters of the ADC.

### 8.12.7.2 ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                  | TEST CONDITIONS  | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|----------------------|----------------------------------|--|-----------------|------|-----|------|------|
| f <sub>ADCCLK</sub>  |                                  | For specified performance of ADC linearity parameters  | 2 V to 3.6 V    | 0.45 | 5   | 5.5  | MHz  |
| f <sub>ADCOSC</sub>  | Internal ADC oscillator (MODCLK) | ADCDIV = 0, f <sub>ADCCLK</sub> = f <sub>ADCOSC</sub>  | 2 V to 3.6 V    | 4.5  | 5.0 | 5.5  | MHz  |
| t <sub>CONVERT</sub> | Conversion time                  | REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f <sub>ADCOSC</sub> = 4.5 MHz to 5.5 MHz  | 2 V to 3.6 V    | 2.18 |     | 2.67 | μs   |
|                      |                                  | External f <sub>ADCCLK</sub> from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0  | 2 V to 3.6 V    |      | (1) |      |      |
| t <sub>ADCON</sub>   | Turn-on settling time of the ADC | The error in a conversion started after t <sub>ADCON</sub> is less than ±0.5 LSB, Reference and input signal already settled                               |                 |      |     | 100  | ns   |
| t <sub>Sample</sub>  | Sampling time                    | R <sub>S</sub> = 1000 Ω, R <sub>I</sub> (2) = 36000 Ω, C <sub>I</sub> = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB(3) | 2 V             | 1.5  |     |      | μs   |
|                      |                                  |  | 3 V             | 2.0  |     |      |      |

(1)  $12 \times 1/f_{ADCCLK}$

(2)  $R_I = R_{I,MUX} + R_{I,Misc}$

(3)  $t_{Sample} = \ln(2^{n+1}) \times \tau$ , where n = ADC resolution,  $\tau = (R_I + R_S) \times C_I$

Section 8.12.7.3 lists the linearity parameters of the ADC.

### 8.12.7.3 ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |   | TEST CONDITIONS  | V <sub>CC</sub> | MIN   | TYP   | MAX  | UNIT  |
|---------------------------------|---|--|-----------------|-------|-------|------|-------|
| E <sub>I</sub>                  | Integral linearity error (10-bit mode)            | V <sub>DVCC</sub> as reference   | 2.4 V to 3.6 V  | –2    |       | 2    | LSB   |
|                                 | Integral linearity error (8-bit mode)             |  | 2 V to 3.6 V    | –2    |       | 2    |       |
| E <sub>D</sub>                  | Differential linearity error (10-bit mode)        | V <sub>DVCC</sub> as reference   | 2.4 V to 3.6 V  | –1    |       | 1    | LSB   |
|                                 | Differential linearity error (8-bit mode)         |  | 2 V to 3.6 V    | –1    |       | 1    |       |
| E <sub>O</sub>                  | Offset error (10-bit mode)                        | V <sub>DVCC</sub> as reference   | 2.4 V to 3.6 V  | –6.5  |       | 6.5  | mV    |
|                                 | Offset error (8-bit mode)                         |  | 2 V to 3.6 V    | –6.5  |       | 6.5  |       |
| E <sub>G</sub>                  | Gain error (10-bit mode)                          | V <sub>DVCC</sub> as reference   | 2.4 V to 3.6 V  | –2.0  |       | 2.0  | LSB   |
|                                 |   | Internal 1.5-V reference   |                 | –3.0% |       | 3.0% |       |
|                                 | Gain error (8-bit mode)                           | V <sub>DVCC</sub> as reference   | 2 V to 3.6 V    | –2.0  |       | 2.0  | LSB   |
|                                 |   | Internal 1.5-V reference   |                 | –3.0% |       | 3.0% |       |
| E <sub>T</sub>                  | Total unadjusted error (10-bit mode)              | V <sub>DVCC</sub> as reference   | 2.4 V to 3.6 V  | –2.0  |       | 2.0  | LSB   |
|                                 |   | Internal 1.5-V reference   |                 | –3.0% |       | 3.0% |       |
|                                 | Total unadjusted error (8-bit mode)               | V <sub>DVCC</sub> as reference   | 2 V to 3.6 V    | –2.0  |       | 2.0  | LSB   |
|                                 |   | Internal 1.5-V reference   |                 | –3.0% |       | 3.0% |       |
| V <sub>SENSOR</sub>             | See (1)   | ADCON = 1, INCH = 0Ch, T <sub>A</sub> = 0°C  | 3 V             |       | 1.013 |      | mV    |
| TC <sub>SENSOR</sub>            | See (2)   | ADCON = 1, INCH = 0Ch  | 3 V             |       | 3.35  |      | mV/°C |
| t <sub>SENSOR</sub><br>(sample) | Sample time required if channel 12 is selected(3) | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, AM and all LPM above LPM3 | 3 V             |       | 30    |      | μs    |
|                                 |   | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, LPM3                      | 3 V             |       | 100   |      |       |

- (1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for 30°C and 85°C for each of the available reference voltage levels. The sensor voltage can be computed as  $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, } ^\circ\text{C}) + V_{SENSOR}$ , where TC<sub>SENSOR</sub> and V<sub>SENSOR</sub> can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor-on time t<sub>SENSOR(on)</sub>.

## 8.12.8 LCD Controller

Section 8.12.8.1 lists the operating conditions of the LCD controller.

### 8.12.8.1 LCD Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS  | MIN   | NOM | MAX | UNIT          |
|-------------------------|--|---|-----|-----|---------------|
| $V_{CC,LCD,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$             | LCDPEN = 1, $0000 < VLCDx \leq 1111$ ,<br>LCDREFEN = 1 (charge pump enabled,<br>$V_{LCD} \leq 3.6\text{ V}$ ) |     |     | V             |
| $V_{CC,LCD,ext.\ bias}$ | Supply voltage range, external biasing, charge pump enabled                        | LCDPEN = 1, LCDREFEN = 0  |     |     | V             |
| $V_{CC,LCD,VLCDEXT}$    | Supply voltage range, external LCD voltage, external biasing, charge pump disabled | LCDPEN = 0, LCDSELVDD = 0   |     |     | V             |
| $V_{R33}$               | External LCD voltage at LCDCAP/R33, external biasing, charge pump disabled         | LCDPEN = 0, LCDSELVDD = 0   |     |     | V             |
| $C_{LDCAP}$             |  | 0.1   |     |     | $\mu\text{F}$ |
| $C_{R33}$               |  | 0.1   |     |     | $\mu\text{F}$ |
| $C_{R23}$               |  | 0.1   |     |     | $\mu\text{F}$ |
| $C_{R13}$               |  | 0.1   |     |     | $\mu\text{F}$ |
| $f_{Frame}$             | LCD frame frequency range  | $f_{LCD} = 2 \times \text{mux} \times f_{FRAME}$ with<br>mux = 1 (static), 2, 3, 4                            |     |     | Hz            |
| $f_{CLK,in}$            | ACLK input frequency range   | 30 32 40  |     |     | kHz           |
| $C_{Panel}$             | Panel capacitance  | 32-Hz frame frequency   |     |     | pF            |
| $V_{R33}$               | Analog input voltage at R33  | LCDPEN = 0, LCDSELVDD = 0,<br>LCDREFEN = 0  |     |     | V             |
| $V_{R23,1/3bias}$       | Analog input voltage at R23  | LCDPEN = 0, LCDSELVDD = 0,<br>LCDREFEN = 0  |     |     | V             |
| $V_{R13,1/3bias}$       | Analog input voltage at R13 with 1/3 biasing                                       | 0.0 1.2   |     |     | V             |
| $V_{LCDREF/R13}$        | External LCD reference voltage applied at LCDREF/R13                               | LCDPEN = 1, LCDSELVDD = 0,<br>LCDREFEN = 0  |     |     | V             |

## 8.12.9 FRAM

Section 8.12.9.1 lists the characteristics of the FRAM.

### 8.12.9.1 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                |                         | TEST CONDITIONS       | MIN              | MAX | UNIT   |
|--------------------------|-------------------------|-----------------------|------------------|-----|--------|
| Read and write endurance |                         |                       | 10 <sup>15</sup> |     | cycles |
| t <sub>Retention</sub>   | Data retention duration | T <sub>J</sub> = 25°C | 100              |     | years  |
|                          |                         | T <sub>J</sub> = 70°C | 40               |     |        |
|                          |                         | T <sub>J</sub> = 85°C | 10               |     |        |

## 8.12.10 Emulation and Debug

Section 8.12.10.1 lists the characteristics of the JTAG and SBW interface.

### 8.12.10.1 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |  | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f <sub>SBW</sub>      | Spy-Bi-Wire input frequency  | 2 V, 3 V        | 0     |     | 10  | MHz  |
| t <sub>SBW,Low</sub>  | Spy-Bi-Wire low clock pulse duration   | 2 V, 3 V        | 0.028 |     | 15  | μs   |
| t <sub>SBW,En</sub>   | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup> | 2 V, 3 V        |       |     | 110 | μs   |
| t <sub>SBW,Rst</sub>  | Spy-Bi-Wire return to normal operation time  |                 | 15    |     | 100 | μs   |
| f <sub>TCK</sub>      | TCK input frequency, 4-wire JTAG <sup>(2)</sup>                                      | 2 V             | 0     |     | 16  | MHz  |
|                       |  | 3 V             | 0     |     | 16  | MHz  |
| R <sub>internal</sub> | Internal pulldown resistance on TEST   | 2 V, 3 V        | 20    | 35  | 50  | kΩ   |

(1) Tools that access the Spy-Bi-Wire interface must wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.



## 9 Detailed Description

### 9.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

### 9.2 Operating Modes

The devices have one active mode and several software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power mode LPM0 or LPM3, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

**Table 9-1. Operating Modes**

| MODE                           |           | AM              | LPM0            | LPM3               | LPM4               | LPM3.5                   | LPM4.5            |
|--------------------------------|-----------|-----------------|-----------------|--------------------|--------------------|--------------------------|-------------------|
|                                |           | ACTIVE MODE     | CPU OFF         | STANDBY            | OFF                | ONLY RTC COUNTER AND LCD | SHUTDOWN          |
| Maximum System Clock           |           | 16 MHz          | 16 MHz          | 40 kHz             | 0                  | 40 kHz                   | 0                 |
| Power Consumption at 25°C, 3 V |           | 126 µA/MHz      | 20 µA/MHz       | 1.2 µA             | 0.6 µA without SVS | 0.77 µA with RTC only    | 13 nA without SVS |
| Wake-up time                   |           | N/A             | Instant         | 10 µs              | 10 µs              | 150 µs                   | 150 µs            |
| Wake-up events                 |           | N/A             | All             | All                | I/O                | RTC Counter I/O          | I/O               |
| Power                          | Regulator | Full Regulation | Full Regulation | Partial Power Down | Partial Power Down | Partial Power Down       | Power Down        |
|                                | SVS       | On              | On              | Optional           | Optional           | Optional                 | Optional          |
|                                | Brown Out | On              | On              | On                 | On                 | On                       | On                |
| Clock                          | MCLK      | Active          | Off             | Off                | Off                | Off                      | Off               |
|                                | SMCLK     | Optional        | Optional        | Off                | Off                | Off                      | Off               |
|                                | FLL       | Optional        | Optional        | Off                | Off                | Off                      | Off               |
|                                | DCO       | Optional        | Optional        | Off                | Off                | Off                      | Off               |
|                                | MODCLK    | Optional        | Optional        | Off                | Off                | Off                      | Off               |
|                                | REFO      | Optional        | Optional        | Optional           | Off                | Off                      | Off               |
|                                | ACLK      | Optional        | Optional        | Optional           | Off                | Off                      | Off               |
|                                | XT1CLK    | Optional        | Optional        | Optional           | Off                | Optional                 | Off               |
| Core                           | VLOCLK    | Optional        | Optional        | Optional           | Off                | Optional                 | Off               |
|                                | CPU       | On              | Off             | Off                | Off                | Off                      | Off               |
|                                | FRAM      | On              | On              | Off                | Off                | Off                      | Off               |
|                                | RAM       | On              | On              | On                 | On                 | Off                      | Off               |
| Backup Memory <sup>(1)</sup>   |           | On              | On              | On                 | On                 | On                       | Off               |

**Table 9-1. Operating Modes (continued)**

| MODE        |                              | AM          | LPM0     | LPM3       | LPM4       | LPM3.5                   | LPM4.5     |
|-------------|------------------------------|-------------|----------|------------|------------|--------------------------|------------|
|             |                              | ACTIVE MODE | CPU OFF  | STANDBY    | OFF        | ONLY RTC COUNTER AND LCD | SHUTDOWN   |
| Peripherals | Timer0_A3                    | Optional    | Optional | Optional   | Off        | Off                      | Off        |
|             | Timer1_A3                    | Optional    | Optional | Optional   | Off        | Off                      | Off        |
|             | WDT                          | Optional    | Optional | Optional   | Off        | Off                      | Off        |
|             | eUSCI_A0                     | Optional    | Optional | Off        | Off        | Off                      | Off        |
|             | eUSCI_B0                     | Optional    | Optional | Off        | Off        | Off                      | Off        |
|             | CRC                          | Optional    | Optional | Off        | Off        | Off                      | Off        |
|             | ADC                          | Optional    | Optional | Optional   | Off        | Off                      | Off        |
|             | LCD                          | Optional    | Optional | Optional   | Off        | Optional                 | Off        |
|             | RTC Counter                  | Optional    | Optional | Optional   | Off        | Optional                 | Off        |
| I/O         | General Digital Input/Output | On          | Optional | State Held | State Held | State Held               | State Held |
|             | Capacitive Touch I/O         | Optional    | Optional | Optional   | Off        | Off                      | Off        |

- (1) Backup memory contains one 32-byte register in the peripheral memory space. See [Table 9-29](#) and [Table 9-48](#) for its memory allocation.

### 9.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 9-2. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE  | INTERRUPT FLAG  | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|---|---|------------------|--------------|-------------|
| <b>System Reset</b><br>Power-up, Brownout, Supply Supervisor<br>External Reset RST<br>Watchdog Time-out, Key Violation<br>FRAM uncorrectable bit error detection<br>Software POR,<br>FLL unlock error | SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>PMMPORIFG, PMMBORIFG<br>SYSRSTIV<br>FLLUNLOCKIFG                | Reset            | FFFEh        | 63, Highest |
| <b>System NMI</b><br>Vacant Memory Access<br>JTAG Mailbox<br>FRAM bit error detection   | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>CBDIFG, UBDIFG   | Nonmaskable      | FFFCh        | 62          |
| <b>User NMI</b><br>External NMI<br>Oscillator Fault   | NMIIFG<br>OFIFG   | Nonmaskable      | FFFAh        | 61          |
| Timer0_A3   | TA0CCR0 CCIFG0  | Maskable         | FFF8h        | 60          |
| Timer0_A3   | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)  | Maskable         | FFF6h        | 59          |
| Timer1_A3   | TA1CCR0 CCIFG0  | Maskable         | FFF4h        | 58          |
| Timer1_A3   | TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV)  | Maskable         | FFF2h        | 57          |
| RTC Counter   | RTCIFG  | Maskable         | FFF0h        | 56          |
| Watchdog Timer Interval mode  | WDTIFG  | Maskable         | FFEEh        | 55          |
| eUSCI_A0 Receive or Transmit  | UCTXCPITFG, UCSTTIFG, UCRXIFG,<br>UCTXIFG (UART mode)<br>UCRXIFG, UCTXIFG (SPI mode)<br>(UCA0IV)) | Maskable         | FFEEh        | 54          |

**Table 9-2. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE             | INTERRUPT FLAG  | SYSTEM INTERRUPT | WORD ADDRESS  | PRIORITY   |
|------------------------------|---|------------------|---------------|------------|
| eUSCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG,<br>UCSTPIFG, UCRXIFG0, UCTXIFG0,<br>UCRXIFG1, UCTXIFG1, UCRXIFG2,<br>UCTXIFG2, UCRXIFG3, UCTXIFG3,<br>UCCNTIFG, UCBIT9IFG (I2C mode)<br>(UCB0IV) | Maskable         | FFEAh         | 53         |
| ADC                          | ADCIFG0, ADCINIFG, ADCLOIFG,<br>ADCHIFG, ADCTOVIFG, ADCOVIFG<br>(ADCIV)   | Maskable         | FFE8h         | 52         |
| P1                           | P1IFG.0 to P1IFG.7 (P1IV)   | Maskable         | FFE6h         | 51         |
| P2                           | P2IFG.0 to P2IFG.7 (P2IV)   | Maskable         | FFE4h         | 50         |
| LCD                          | LCDBLKOFFIFG, LCDBLKONIFG,<br>LCDFRMIFG (LCDEIV)  | Maskable         | FFE2h         | 49, Lowest |
| Reserved                     | Reserved  | Maskable         | FFE0h to FF8h |            |
| Signatures                   | BSL Signature 2   |                  | 0FF86h        |            |
|                              | BSL Signature 1   |                  | 0FF84h        |            |
|                              | JTAG Signature 2  |                  | 0FF82h        |            |
|                              | JTAG Signature 1  |                  | 0FF80h        |            |

## 9.4 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using a UART serial interface. Access to the device memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins as shown in [Table 9-3](#). BSL entry requires a specific entry sequence on the RST/NMI/SBWDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the [MSP430 FRAM Devices Bootloader \(BSL\) User's Guide](#).

**Table 9-3. BSL Pin Requirements and Functions**

| DEVICE SIGNAL  | BSL FUNCTION          |
|----------------|-----------------------|
| RST/NMI/SBWDIO | Entry sequence signal |
| TEST/SBWTCK    | Entry sequence signal |
| P1.0           | Data transmit         |
| P1.1           | Data receive          |
| VCC            | Power supply          |
| VSS            | Ground supply         |

## 9.5 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in [Table 9-4](#). For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

**Table 9-4. JTAG Pin Requirements and Function**

| DEVICE SIGNAL          | DIRECTION | JTAG FUNCTION              |
|------------------------|-----------|----------------------------|
| P1.4/MCLK/TCK/A4/VREF+ | IN        | JTAG clock input           |
| P1.5/TA0CLK/TMS/A5     | IN        | JTAG state control         |
| P1.6/TA0.2/TDI/TCLK/A6 | IN        | JTAG data input/TCLK input |
| P1.7/TA0.1/TDO/A7      | OUT       | JTAG data output           |
| TEST/SBWTK             | IN        | Enable JTAG pins           |
| RST/NMI/SBWDIO         | IN        | External reset             |
| VCC                    |           | Power supply               |
| VSS                    |           | Ground supply              |

## 9.6 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 9-5](#) shows the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#).

**Table 9-5. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL  | DIRECTION | SBW FUNCTION                  |
|----------------|-----------|-------------------------------|
| TEST/SBWTK     | IN        | Spy-Bi-Wire clock input       |
| RST/NMI/SBWDIO | IN, OUT   | Spy-Bi-Wire data input/output |
| VCC            |           | Power supply                  |
| VSS            |           | Ground supply                 |

## 9.7 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction code (ECC) generation

## 9.8 Memory Protection

The device features memory protection that can restrict user access and enable write protection:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits in System Configuration register 0. For more detailed information, see the SYS chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

### Note

The FRAM is protected by default on PUC. To write to FRAM during code execution, the application must first clear the corresponding PFWP or DFWP bit in System Configuration Register 0 to unprotect the FRAM.

## 9.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

### 9.9.1 Power Management Module (PMM) and On-Chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as [Equation 1](#) by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5 \text{ V}) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when the ADC channel 4 is selected as the function. For more detailed information, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

### 9.9.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODCLK). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

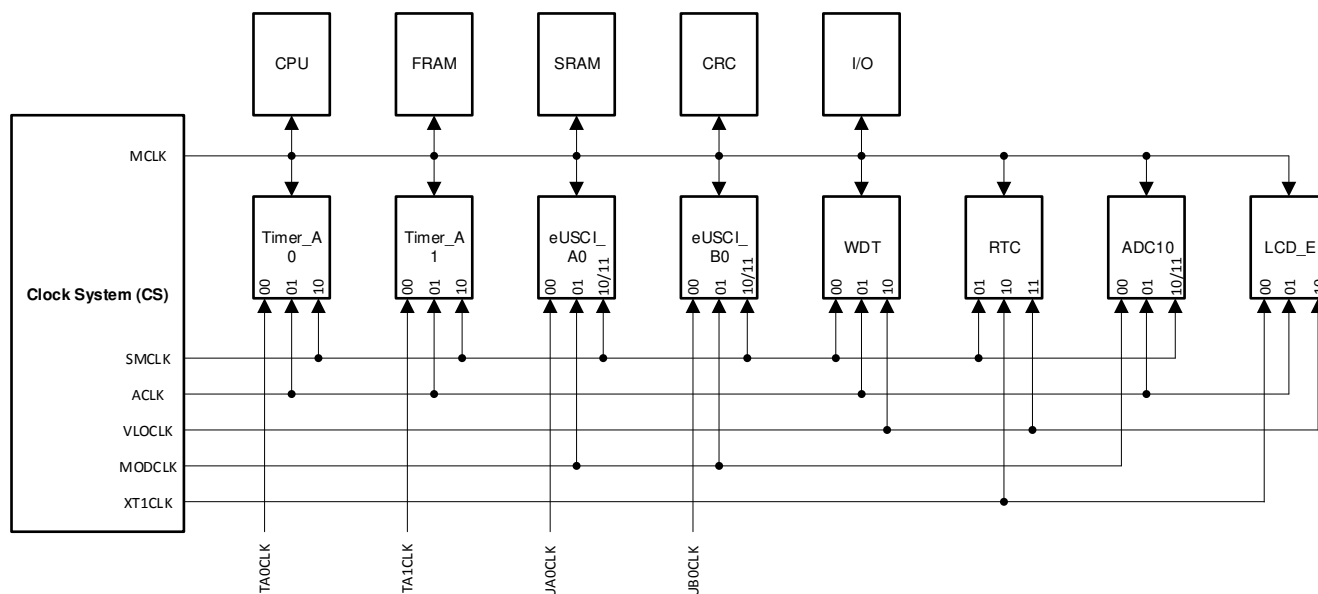
- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODCLK can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. [Table 9-6](#) shows the clock distribution used in this device.

**Table 9-6. Clock Distribution**

|                    | CLOCK<br>SOURCE<br>SELECT<br>BITS | MCLK            | SMCLK           | ACLK         | MODCLK     | XT1CLK <sup>(1)</sup> | VLOCLK      | EXTERNAL PIN      |
|--------------------|-----------------------------------|-----------------|-----------------|--------------|------------|-----------------------|-------------|-------------------|
| Frequency<br>Range |                                   | DC to<br>16 MHz | DC to<br>16 MHz | DC to 40 kHz | 5 MHz ±10% | DC to 40 kHz          | 10 kHz ±50% |                   |
| CPU                | N/A                               | Default         |                 |              |            |                       |             |                   |
| FRAM               | N/A                               | Default         |                 |              |            |                       |             |                   |
| RAM                | N/A                               | Default         |                 |              |            |                       |             |                   |
| CRC                | N/A                               | Default         |                 |              |            |                       |             |                   |
| I/O                | N/A                               | Default         |                 |              |            |                       |             |                   |
| TA0                | TASSEL                            |                 | 10b             | 01b          |            |                       |             | 00b (TA0CLK pin)  |
| TA1                | TASSEL                            |                 | 10b             | 01b          |            |                       |             | 00b (TA1CLK pin)  |
| eUSCI_A0           | UCSSELx                           |                 | 10b or 11b      |              | 01b        |                       |             | 00b (UCA0CLK pin) |
| eUSCI_B0           | UCSSELx                           |                 | 10b or 11b      |              | 01b        |                       |             | 00b (UCB0CLK pin) |
| WDT                | WDTSEL                            |                 | 00b             | 01b          |            |                       | 10b         |                   |
| ADC                | ADCSEL                            |                 | 10b or 11b      | 01b          | 00b        |                       |             |                   |
| LCD                | LCDSEL                            |                 |                 | 01b          |            | 00b                   | 10b         |                   |
| RTC                | RTCSS                             |                 | 01b             |              |            | 10b                   | 11b         |                   |

(1) To enable XT1 functionality, configure P4SEL0.1 (XIN) and P4SEL0.2 (XOUT) before configuring the Clock System registers.

**Figure 9-1. Clock Distribution Block Diagram**

### 9.9.3 General-Purpose Input/Output Port (I/O)

Up to 60 I/O ports are implemented.

- P1, P2, P3, P4, P5, P6, and P7 are full 8-bit ports; P8 has 4 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

- Capacitive Touch IO functionality is supported on all pins.

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#### Note

##### Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

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#### 9.9.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

**Table 9-7. WDT Clocks**

| WDTSEL | NORMAL OPERATION<br>(WATCHDOG AND INTERVAL TIMER<br>MODE) |
|--------|---|
| 00     | SMCLK   |
| 01     | ACLK  |
| 10     | VLOCLK  |
| 11     | VLOCLK  |

#### 9.9.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These include Power-On Reset (POR) and Power-Up Clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application.

**Table 9-8. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT                          | VALUE      | PRIORITY |
|---------------------------|---------|--|------------|----------|
| SYSRSTIV, System Reset    | 015Eh   | No interrupt pending                     | 00h        |          |
|                           |         | Brownout (BOR)                           | 02h        | Highest  |
|                           |         | RSTIFG RST/NMI (BOR)                     | 04h        |          |
|                           |         | PMMSWBOR software BOR (BOR)              | 06h        |          |
|                           |         | LPMx.5 wakeup (BOR)                      | 08h        |          |
|                           |         | Security violation (BOR)                 | 0Ah        |          |
|                           |         | Reserved                                 | 0Ch        |          |
|                           |         | SVSHIFG SVSH event (BOR)                 | 0Eh        |          |
|                           |         | Reserved                                 | 10h        |          |
|                           |         | Reserved                                 | 12h        |          |
|                           |         | PMMSWPOR software POR (POR)              | 14h        |          |
|                           |         | WDTIFG watchdog time-out (PUC)           | 16h        |          |
|                           |         | WDTPW password violation (PUC)           | 18h        |          |
|                           |         | FRCTLPW password violation (PUC)         | 1Ah        |          |
|                           |         | Uncorrectable FRAM bit error detection   | 1Ch        |          |
|                           |         | Peripheral area fetch (PUC)              | 1Eh        |          |
|                           |         | PMMPW PMM password violation (PUC)       | 20h        |          |
|                           |         | Reserved                                 | 22h        |          |
|                           |         | FLL unlock (PUC)                         | 24h        |          |
|                           |         | Reserved                                 | 26h to 3Eh | Lowest   |
| SYSSNIV, System NMI       | 015Ch   | No interrupt pending                     | 00h        |          |
|                           |         | SVS low-power reset entry                | 02h        | Highest  |
|                           |         | Uncorrectable FRAM bit error detection   | 04h        |          |
|                           |         | Reserved                                 | 06h        |          |
|                           |         | Reserved                                 | 08h        |          |
|                           |         | Reserved                                 | 0Ah        |          |
|                           |         | Reserved                                 | 0Ch        |          |
|                           |         | Reserved                                 | 0Eh        |          |
|                           |         | Reserved                                 | 10h        |          |
|                           |         | VMAIFG Vacant memory access              | 12h        |          |
|                           |         | JMBINIFG JTAG mailbox input              | 14h        |          |
|                           |         | JMBOUTIFG JTAG mailbox output            | 16h        |          |
|                           |         | Correctable FRAM bit error detection     | 18h        |          |
|                           |         | Reserved                                 | 1Ah to 1Eh | Lowest   |
| SYSUNIV, User NMI         | 015Ah   | No interrupt pending                     | 00h        |          |
|                           |         | NMIIFG NMI pin or SVS <sub>H</sub> event | 02h        | Highest  |
|                           |         | OFIFG oscillator fault                   | 04h        |          |
|                           |         | Reserved                                 | 06h to 1Eh | Lowest   |

### 9.9.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of  $x^{16} + x^{12} + x^5 + 1$ .



### 9.9.7 Enhanced Universal Serial Communication Interface (eUSCI\_A0, eUSCI\_B0)

The eUSCI modules are used for serial data communications. The eUSCI\_A module supports either UART or SPI communications. The eUSCI\_B module supports either SPI or I<sup>2</sup>C communications. Additionally, eUSCI\_A supports automatic baud-rate detection and IrDA.

**Table 9-9. eUSCI Pin Configurations**

| eUSCI_A0 | PIN  | UART             | SPI  |
|----------|------|------------------|------|
|          | P1.0 | TXD              | SIMO |
|          | P1.1 | RXD              | SOMI |
|          | P1.2 |                  | SCLK |
|          | P1.3 |                  | STE  |
| eUSCI_B0 | PIN  | I <sup>2</sup> C | SPI  |
|          | P5.0 |                  | STE  |
|          | P5.1 |                  | SCLK |
|          | P5.2 | SDA              | SIMO |
|          | P5.3 | SCL              | SOMI |

### 9.9.8 Timers (Timer0\_A3, Timer1\_A3)

The Timer0\_A3 and Timer1\_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA1 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up Mode, they can be used to set the overflow value of the counter.

**Table 9-10. Timer0\_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL                  | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL                                  |
|----------|--------------------------------------|-------------------|--------------|----------------------|---|
| P1.5     | TA0CLK                               | TACLK             | Timer        | N/A                  |   |
|          | ACLK (internal)                      | ACLK              |              |                      |   |
|          | SMCLK (internal)                     | SMCLK             |              |                      |   |
|          | from Capacitive Touch IO (internal)  | INCLK             |              |                      |   |
|          |                                      | CCI0A             | CCR0         | TA0                  |   |
|          |                                      | CCI0B             |              |                      | Timer1_A3 CCI0B input                                 |
|          | DVSS                                 | GND               |              |                      |   |
|          | DVCC                                 | VCC               |              |                      |   |
| P1.7     | TA0.1                                | CCI1A             | CCR1         | TA1                  | TA0.1   |
|          | from RTC (internal)                  | CCI1B             |              |                      | Timer1_A3 CCI1B input                                 |
|          | DVSS                                 | GND               |              |                      |   |
|          | DVCC                                 | VCC               |              |                      |   |
| P1.6     | TA0.2                                | CCI2A             | CCR2         | TA2                  | TA0.2   |
|          | from Capacitive Touch I/O (internal) | CCI2B             |              |                      | Timer1_A3 INCLK<br>Timer1_A3 CCI2B input,<br>IR Input |
|          | DVSS                                 | GND               |              |                      |   |
|          | DVCC                                 | VCC               |              |                      |   |

**Table 9-11. Timer1\_A3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL               | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|----------|-----------------------------------|-------------------|--------------|----------------------|----------------------|
| P8.2     | TA1CLK                            | TACLK             | Timer        | N/A                  |                      |
|          | ACLK (internal)                   | ACLK              |              |                      |                      |
|          | SMCLK (internal)                  | SMCLK             |              |                      |                      |
|          | Timer0_A3 CCR2B output (internal) | INCLK             |              |                      |                      |
|          |                                   | CCI0A             | CCR0         | TA0                  |                      |
|          | Timer0_A3 CCR0B output (internal) | CCI0B             |              |                      |                      |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |
| P4.0     | TA1.1                             | CCI1A             | CCR1         | TA1                  | TA1.1                |
|          | Timer0_A3 CCR1B output (internal) | CCI1B             |              |                      | to ADC trigger       |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |
| P8.3     | TA1.2                             | CCI2A             | CCR2         | TA2                  | TA1.2                |
|          | Timer0_A3 CCR2B output (internal) | CCI2B             |              |                      | IR Input             |
|          | DVSS                              | GND               |              |                      |                      |
|          | DVCC                              | VCC               |              |                      |                      |

The interconnection of Timer0\_A3 and Timer1\_A3 can be used to modulate the eUSCI\_A pin of UCA0TXD/ UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

### 9.9.9 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0\_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

### 9.9.10 10-Bit Analog Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and four internal inputs (see [Table 9-12](#)).

**Table 9-12. ADC Channel Connections**

| ADCINCHx | ADC CHANNELS               | EXTERNAL PIN OUT    |
|----------|----------------------------|---------------------|
| 0        | A0/V <sub>ref</sub> –      | P1.0                |
| 1        | A1/V <sub>ref</sub> +      | P1.1                |
| 2        | A2                         | P1.2                |
| 3        | A3                         | P1.3                |
| 4        | A4 <sup>(2)</sup>          | P1.4                |
| 5        | A5                         | P1.5                |
| 6        | A6                         | P1.6                |
| 7        | A7                         | P1.7                |
| 8        | A8                         | P8.0 <sup>(1)</sup> |
| 9        | A9                         | P8.1 <sup>(1)</sup> |
| 10       | Not Used                   | N/A                 |
| 11       | Not Used                   | N/A                 |
| 12       | On-chip Temperature Sensor | N/A                 |
| 13       | Reference Voltage (1.5 V)  | N/A                 |
| 14       | DVSS                       | N/A                 |
| 15       | DVCC                       | N/A                 |

(1) P8.0 and P8.1 are only available in the LQFP-64 package.

(2) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.

The AD conversion can be started by software or a hardware trigger. [Table 9-13](#) shows the trigger sources that are available.

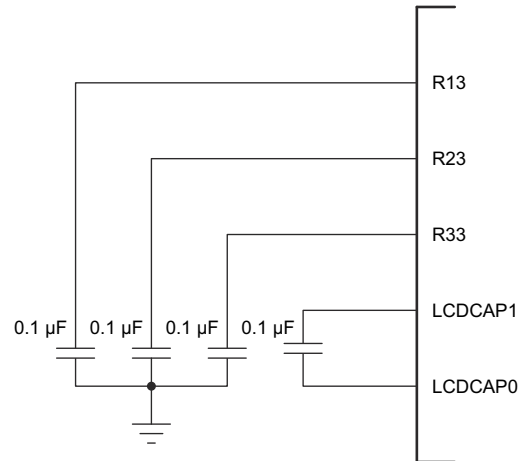
**Table 9-13. ADC Trigger Signal Connections**

| ADCSHSx |         | TRIGGER SOURCE               |
|---------|---------|------------------------------|
| Binary  | Decimal |                              |
| 00      | 0       | ADCSC bit (software trigger) |
| 01      | 1       | RTC event                    |
| 10      | 2       | TA1.1B                       |
| 11      | 3       | TA1.2B                       |

### 9.9.11 Liquid Crystal Display (LCD)

The LCD driver generates the segment and common signals to drive segment liquid crystal display (LCD) glass. The LCD controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, up to 8-mux LCDs are supported. The module can provide an LCD voltage independent from the main supply voltage with its integrated charge pump. The LCD display contrast can be trimmed by setting the LCD drive voltage. The LCD module can be fully functional in any power mode from AM to LPM3.5.

When supplied by the on-chip charge pump with on-chip regulator reference, the LCD driver needs five pins and four external 0.1-μF capacitors to achieve low-power consumption during operation. Figure 9-2 shows the recommended connections.



**Figure 9-2. LCD Power Supply Configuration With On-Chip Charge Pump and Regulator Reference**

The LCD contains 20 16-bit words (40 bytes) display memory. The use of memory is flexible, depending on the selected mode:

- 4-mux mode
  - LCDM0 to LCDM19 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 20 bytes).
  - LCDBM0 to LCDBM19 can be used for LCD blinking contents. If it is not used as blinking, the corresponding LCDBMx can be used for user data (up to 20 bytes).
- 8-mux mode
  - LCDM0 to LCDM39 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 40 bytes).

### 9.9.12 Embedded Emulation Module (EEM)

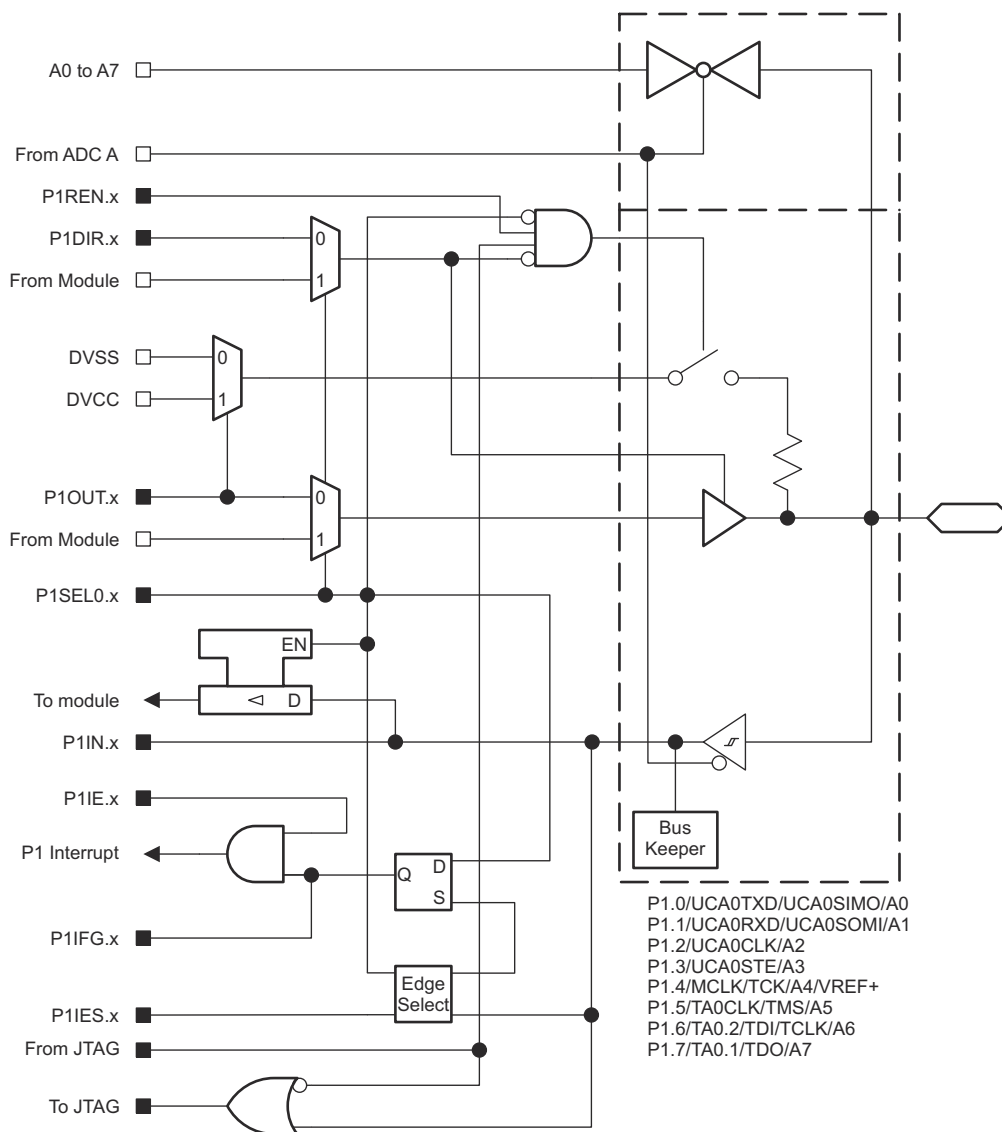
The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

## 9.9.13 Input/Output Schematics

### 9.9.13.1 Port P1 Input/Output With Schmitt Trigger

Figure 9-3 shows the port schematic. Table 9-14 summarizes the selection of the pin functions.



**Figure 9-3. Port P1 Input/Output With Schmitt Trigger**

**Table 9-14. Port P1 Pin Functions**

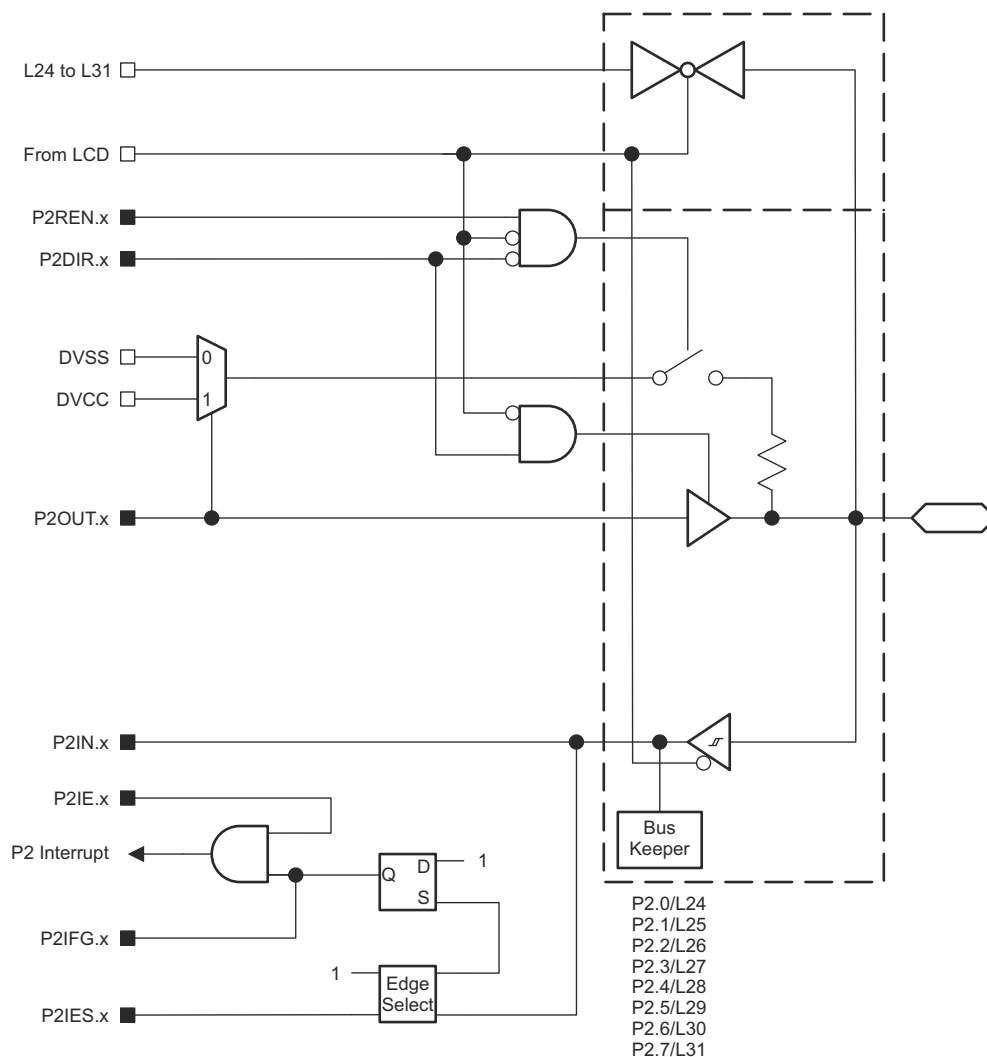
| PIN NAME (P1.x)              | x | FUNCTION         | CONTROL BITS AND SIGNALS <sup>(2)</sup> |          |                         |          |
|------------------------------|---|------------------|---|----------|-------------------------|----------|
|                              |   |                  | P1DIR.x                                 | P1SEL0.x | ADCPCTLx <sup>(1)</sup> | JTAG     |
| P1.0/UCA0TXD/<br>UCA0SIMO/A0 | 0 | P1.0 (I/O)       | I: 0; O: 1                              | 0        | 0                       | N/A      |
|                              |   | UCA0TXD/UCA0SIMO | X                                       | 1        | 0                       | N/A      |
|                              |   | A0               | X                                       | X        | 1 (x = 0)               | N/A      |
| P1.1/UCA0RXD/<br>UCA0SOMI/A1 | 1 | P1.1 (I/O)       | I: 0; O: 1                              | 0        | 0                       | N/A      |
|                              |   | UCA0RXD/UCA0SOMI | X                                       | 1        | 0                       | N/A      |
|                              |   | A1               | X                                       | X        | 1 (x = 1)               | N/A      |
| P1.2/UCA0CLK/A2              | 2 | P1.2 (I/O)       | I: 0; O: 1                              | 0        | 0                       | N/A      |
|                              |   | UCA0CLK          | X                                       | 1        | 0                       | N/A      |
|                              |   | A2               | X                                       | X        | 1 (x = 2)               | N/A      |
| P1.3/UCA0STE/A3              | 3 | P1.3 (I/O)       | I: 0; O: 1                              | 0        | 0                       | N/A      |
|                              |   | UCA0STE          | X                                       | 1        | 0                       | N/A      |
|                              |   | A3               | X                                       | X        | 1 (x = 3)               | N/A      |
| P1.4/MCLK/TCK/A4/<br>VREF+   | 4 | P1.4 (I/O)       | I: 0; O: 1                              | 0        | 0                       | Disabled |
|                              |   | VSS              | 0                                       | 1        | 0                       | Disabled |
|                              |   | MCLK             | 1                                       |          |                         |          |
|                              |   | A4, VREF+        | X                                       | X        | 1 (x = 4)               | Disabled |
|                              |   | JTAG TCK         | X                                       | X        | X                       | TCK      |
| P1.5/TA0CLK/TMS/A5           | 5 | P1.5 (I/O)       | I: 0; O: 1                              | 0        | 0                       | Disabled |
|                              |   | TA0CLK           | 0                                       | 1        | 0                       | Disabled |
|                              |   | VSS              | 1                                       |          |                         |          |
|                              |   | A5               | X                                       | X        | 1 (x = 5)               | Disabled |
|                              |   | JTAG TMS         | X                                       | X        | X                       | TMS      |
| P1.6/TA0.2/TDI/TCLK/ A6      | 6 | P1.6 (I/O)       | I: 0; O: 1                              | 0        | 0                       | Disabled |
|                              |   | TA0.CCI2A        | 0                                       | 1        | 0                       | Disabled |
|                              |   | TA0.2            | 1                                       |          |                         |          |
|                              |   | A6               | X                                       | X        | 1 (x = 6)               | Disabled |
|                              |   | JTAG TDI/TCLK    | X                                       | X        | X                       | TDI/TCLK |
| P1.7/TA0.1/TDO/A7            | 7 | P1.7 (I/O)       | I: 0; O: 1                              | 0        | 0                       | Disabled |
|                              |   | TA0.CCI1A        | 0                                       | 1        | 0                       | Disabled |
|                              |   | TA0.1            | 1                                       |          |                         |          |
|                              |   | A7               | X                                       | X        | 1 (x = 7)               | Disabled |
|                              |   | JTAG TDO         | X                                       | X        | X                       | TDO      |

(1) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

(2) X = don't care

### 9.9.13.2 Port P2 Input/Output With Schmitt Trigger

Figure 9-4 shows the port schematic. Table 9-15 summarizes the selection of the pin functions.



**Figure 9-4. Port P2 Input/Output With Schmitt Trigger**



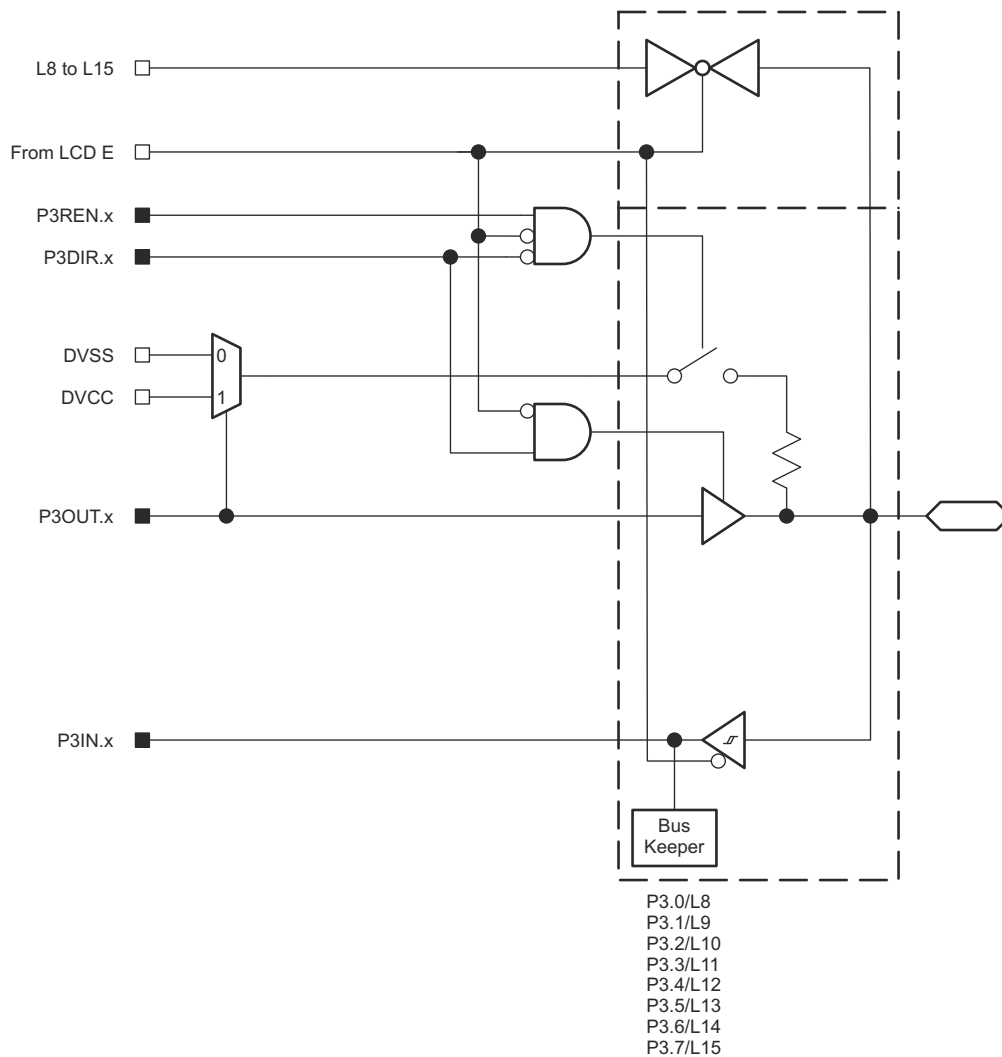
**Table 9-15. Port P2 Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |            |
|-----------------|---|------------|---|------------|
|                 |   |            | P2DIR.x                                 | LCDSy      |
| P2.0/L24        | 0 | P2.0 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L24        | X                                       | 1 (y = 24) |
| P2.1/L25        | 1 | P2.1 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L25        | X                                       | 1 (y = 25) |
| P2.2/L26        | 2 | P2.2 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L26        | X                                       | 1 (y = 26) |
| P2.3/L27        | 3 | P2.3 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L27        | X                                       | 1 (y = 27) |
| P2.4/L28        | 4 | P2.4 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L28        | X                                       | 1 (y = 28) |
| P2.5/L29        | 5 | P2.5 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L29        | X                                       | 1 (y = 29) |
| P2.6/L30        | 6 | P2.6 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L30        | X                                       | 1 (y = 30) |
| P2.7/L31        | 7 | P2.7 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L31        | X                                       | 1 (y = 31) |

(1) X= don't care

### 9.9.13.3 Port P3 Input/Output With Schmitt Trigger

Figure 9-5 shows the port schematic. Table 9-16 summarizes the selection of the pin functions.



**Figure 9-5. Port P3 Input/Output With Schmitt Trigger**

**Table 9-16. Port P3 Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |            |
|-----------------|---|------------|---|------------|
|                 |   |            | P3DIR.x                                 | LCDSy      |
| P3.0/L8         | 0 | P3.0 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L8         | X                                       | 1 (y = 8)  |
| P3.1/L9         | 1 | P3.1 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L9         | X                                       | 1 (y = 9)  |
| P3.2/L10        | 2 | P3.2 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L10        | X                                       | 1 (y = 10) |
| P3.3/L11        | 3 | P3.3 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L11        | X                                       | 1 (y = 11) |
| P3.4/L12        | 4 | P3.4 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L12        | X                                       | 1 (y = 12) |
| P3.5/L13        | 5 | P3.5 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L13        | X                                       | 1 (y = 13) |
| P3.6/L14        | 6 | P3.6 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L14        | X                                       | 1 (y = 14) |
| P3.7/L15        | 7 | P3.7 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L15        | X                                       | 1 (y = 15) |

(1) X= don't care

### 9.9.13.4 Port P4.0 Input/Output With Schmitt Trigger

Figure 9-6 shows the port schematic. Table 9-17 summarizes the selection of the pin functions.

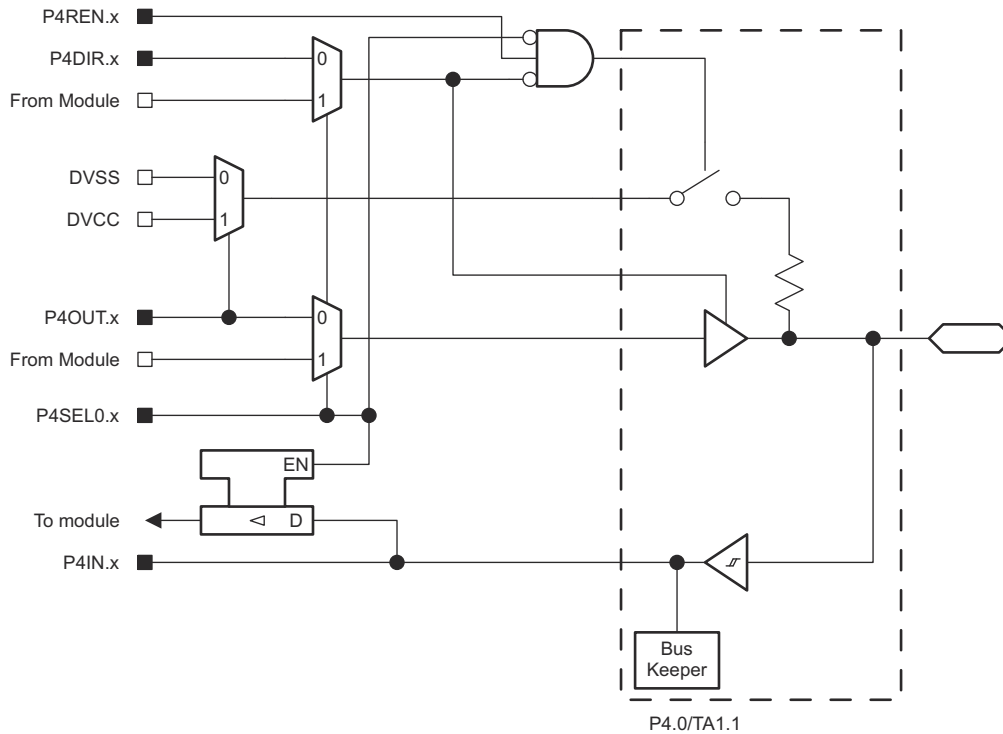


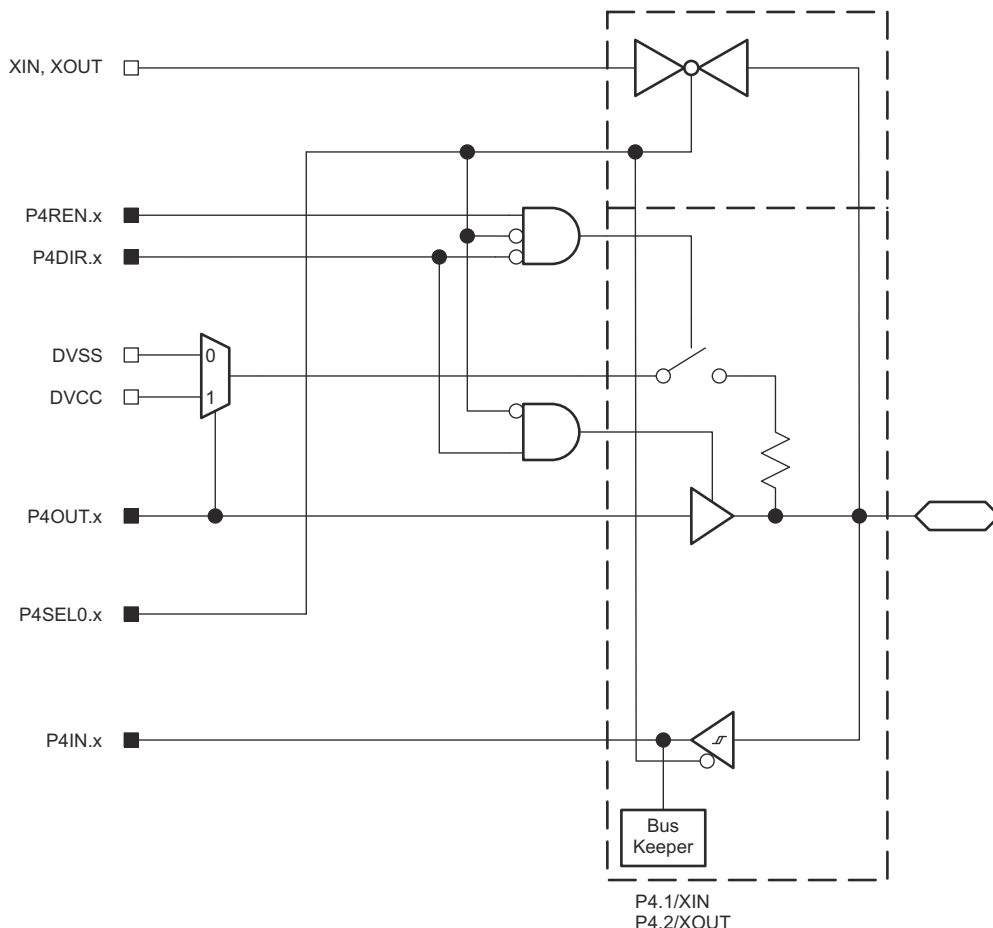
Figure 9-6. Port P4.0 Input/Output With Schmitt Trigger

Table 9-17. Port P4.0 Pin Functions

| PIN NAME (P4.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS |          |
|-----------------|---|------------|--------------------------|----------|
|                 |   |            | P4DIR.x                  | P4SEL0.x |
| P4.0/TA1.1      | 0 | P4.0 (I/O) | I: 0; O: 1               | 0        |
|                 |   | TA1.CCI1A  | 0                        | 1        |
|                 |   | TA1.1      | 1                        |          |

### 9.9.13.5 Port P4.1 and P4.2 Input/Output With Schmitt Trigger

Figure 9-7 shows the port schematic. Table 9-18 summarizes the selection of the pin functions.



**Figure 9-7. Port P4.1 and P4.2 Input/Output With Schmitt Trigger**

**Table 9-18. Port P4.1 and P4.2 Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |
|-----------------|---|------------|---|----------|
|                 |   |            | P4DIR.x                                 | P4SEL0.x |
| P4.1/XIN        | 1 | P4.1 (I/O) | I: 0; O: 1                              | 0        |
|                 |   | XIN        | X                                       | 1        |
| P4.2/XOUT       | 2 | P4.2 (I/O) | I: 0; O: 1                              | 0        |
|                 |   | XOUT       | X                                       | 1        |

(1) X= don't care

### 9.9.13.6 Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

Figure 9-8 shows the port schematic. Table 9-19 summarizes the selection of the pin functions.

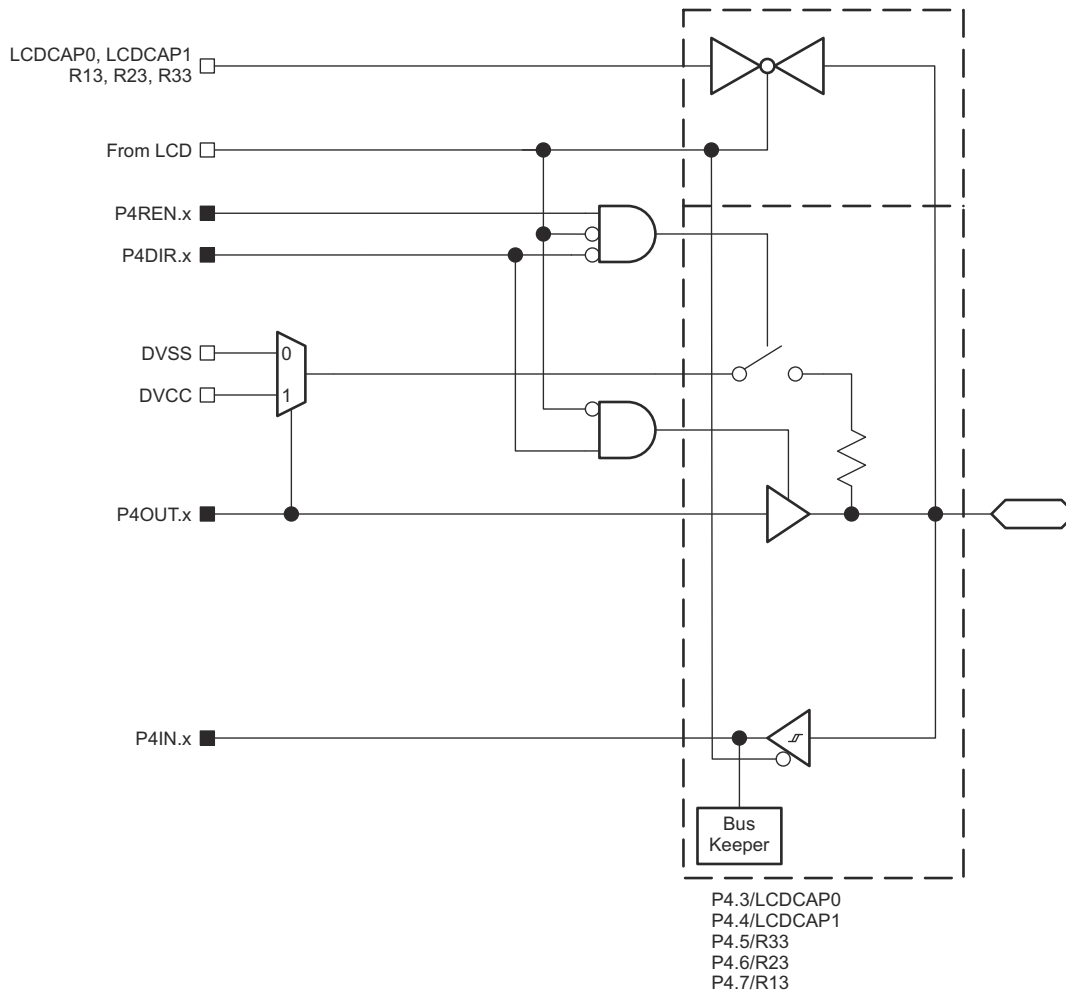


Figure 9-8. Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

Table 9-19. Port P4.3, P4.4, P4.5, P4.6, and P4.7 Pin Functions

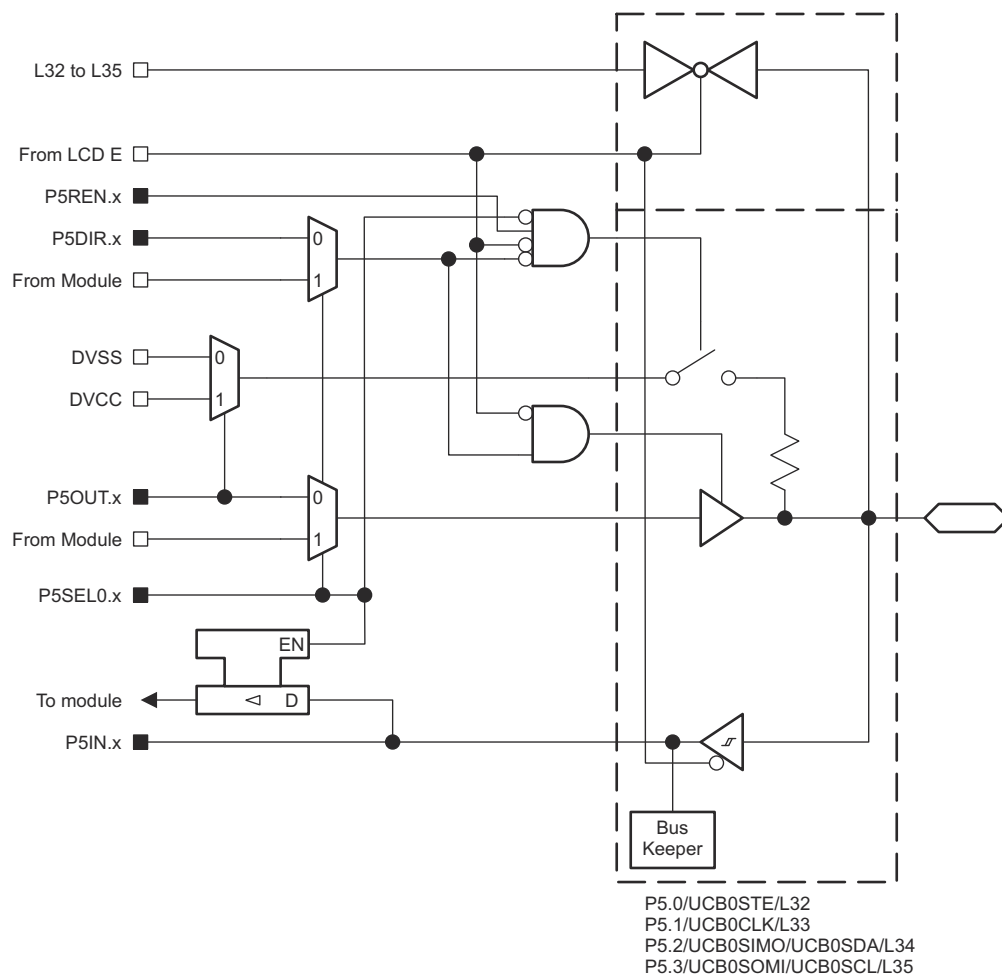
| PIN NAME (P4.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |                        |
|-----------------|---|------------|---|------------------------|
|                 |   |            | P4DIR.x                                 | LCDPCTL <sup>(2)</sup> |
| P4.3/LCDCAP0    | 3 | P4.3 (I/O) | I: 0; O: 1                              | X                      |
|                 |   | LDCAP0     | X                                       | 1                      |
| P4.4/LCDCAP1    | 4 | P4.4 (I/O) | I: 0; O: 1                              | 0                      |
|                 |   | LDCAP1     | X                                       | 1                      |
| P4.5/R33        | 5 | P4.5 (I/O) | I: 0; O: 1                              | 0                      |
|                 |   | R33        | X                                       | 1                      |
| P4.6/R23        | 6 | P4.6 (I/O) | I: 0; O: 1                              | 0                      |
|                 |   | R23        | X                                       | 1                      |
| P4.7/R13        | 7 | P4.7 (I/O) | I: 0; O: 1                              | 0                      |
|                 |   | R13        | X                                       | 1                      |

(1) X= don't care

(2) Setting the LCDPCTL bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

### 9.9.13.7 Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

Figure 9-9 shows the port schematic. Table 9-20 summarizes the selection of the pin functions.



**Figure 9-9. Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger**

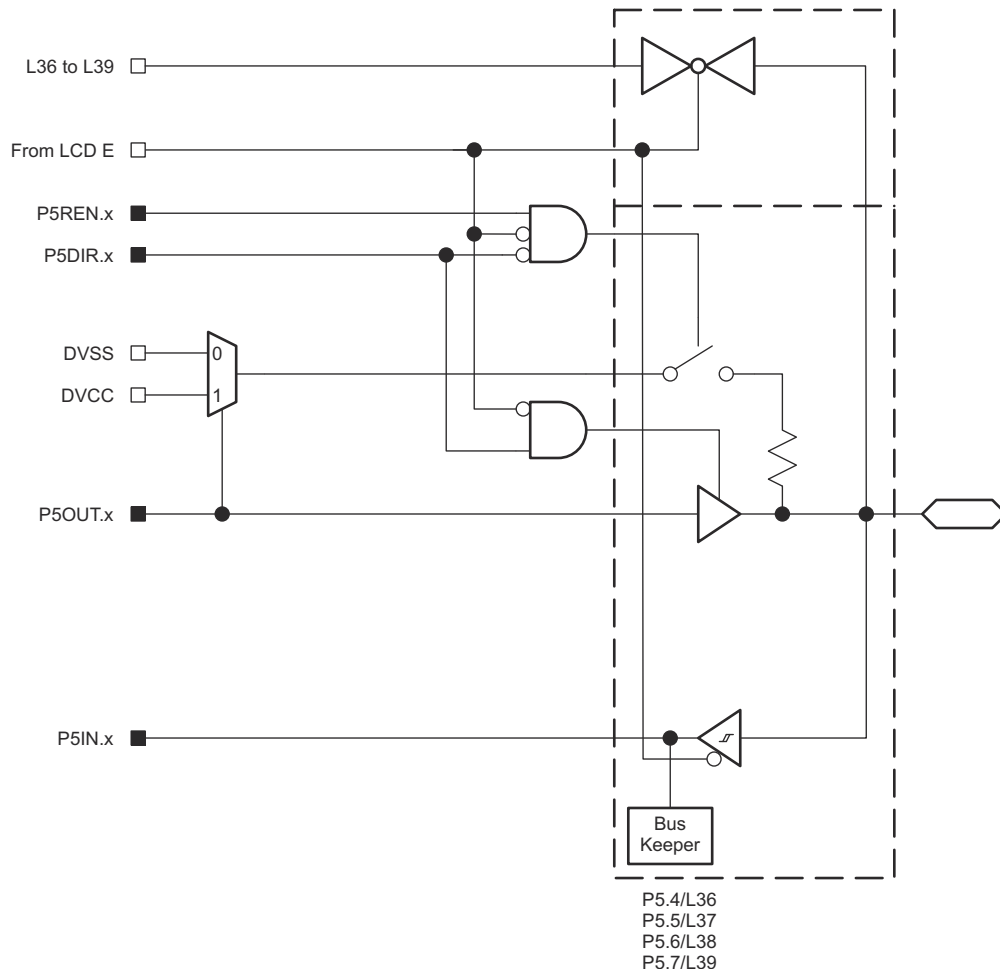
**Table 9-20. Port P5.0, P5.1, P5.2, and P5.3 Pin Functions**

| PIN NAME (P5.x)               | x | FUNCTION         | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |            |
|-------------------------------|---|------------------|---|----------|------------|
|                               |   |                  | P5DIR.x                                 | P5SEL0.x | LCDSy      |
| P5.0/UCB0STE/L32              | 0 | P5.0 (I/O)       | I: 0; O: 1                              | 0        | 0          |
|                               |   | UCB0STE          | 0                                       | 1        | 0          |
|                               |   | L32              | X                                       | X        | 1 (y = 32) |
| P5.1/UCB0CLK/L33              | 1 | P5.1 (I/O)       | I: 0; O: 1                              | 0        | 0          |
|                               |   | UCB0CLK          | 0                                       | 1        | 0          |
|                               |   | L33              | X                                       | X        | 1 (y = 33) |
| P5.2/UCB0SIMO/<br>UCB0SDA/L34 | 2 | P5.2 (I/O)       | I: 0; O: 1                              | 0        | 0          |
|                               |   | UCB0SIMO/UCB0SDA | 0                                       | 1        | 0          |
|                               |   | L34              | X                                       | X        | 1 (y = 34) |
| P5.3/UCB0SOMI/<br>UCB0SCL/L35 | 3 | P5.3 (I/O)       | I: 0; O: 1                              | 0        | 0          |
|                               |   | UCB0SOMI/UCB0SCL | 0                                       | 1        | 0          |
|                               |   | L35              | X                                       | X        | 1 (y = 35) |

(1) X= don't care

### 9.9.13.8 Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

Figure 9-10 shows the port schematic. Table 9-21 summarizes the selection of the pin functions.



**Figure 9-10. Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger**

**Table 9-21. Port P5.4, P5.5, P5.6, and P5.7 Pin Functions**

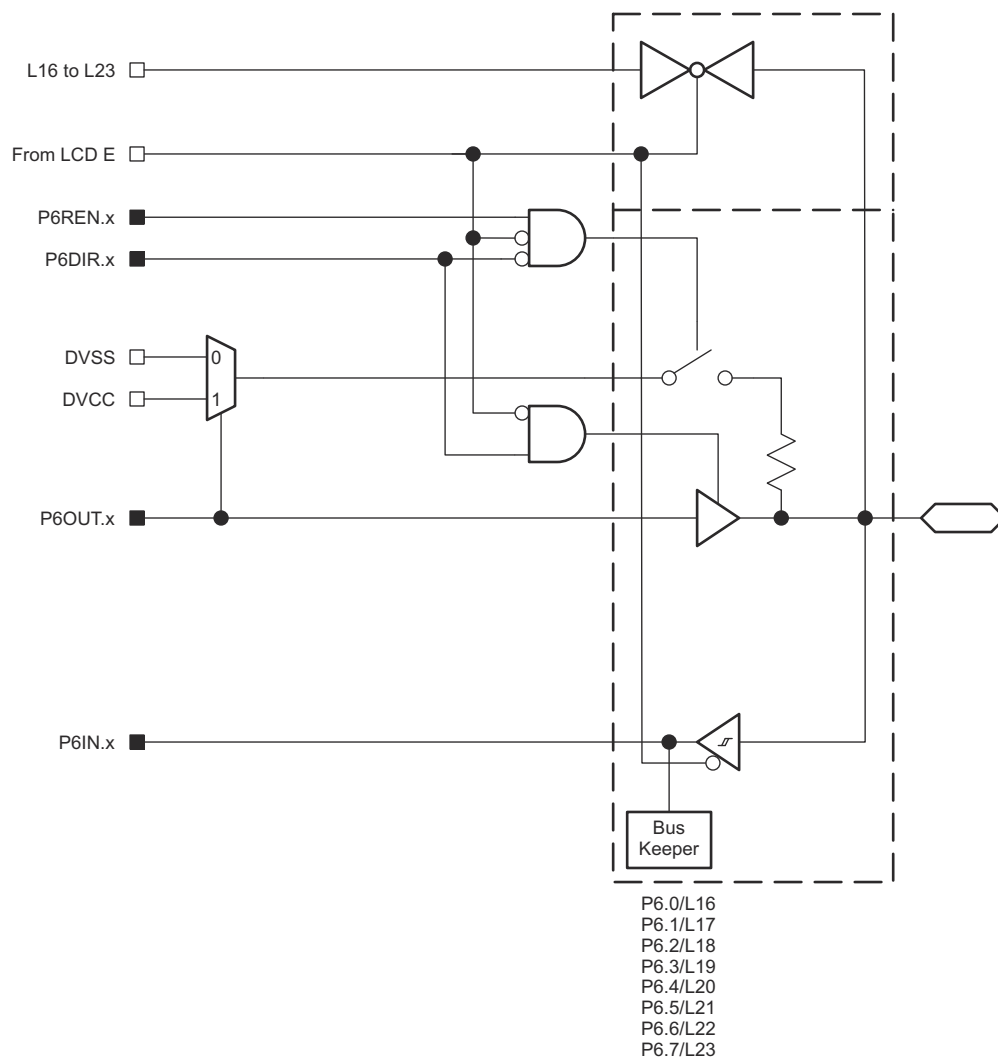
| PIN NAME (P5.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |            |
|-----------------|---|------------|---|------------|
|                 |   |            | P5DIR.x                                 | LCDSy      |
| P5.4/L36        | 4 | P5.4 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L36        | X                                       | 1 (y = 36) |
| P5.5/L37        | 5 | P5.5 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L37        | X                                       | 1 (y = 37) |
| P5.6/L38        | 6 | P5.6 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L38        | X                                       | 1 (y = 38) |
| P5.7/L39        | 7 | P5.7 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L39        | X                                       | 1 (y = 39) |

(1) X= don't care



### 9.9.13.9 Port P6 Input/Output With Schmitt Trigger

Figure 9-11 shows the port schematic. Table 9-22 summarizes the selection of the pin functions.



**Figure 9-11. Port P6 Input/Output With Schmitt Trigger**

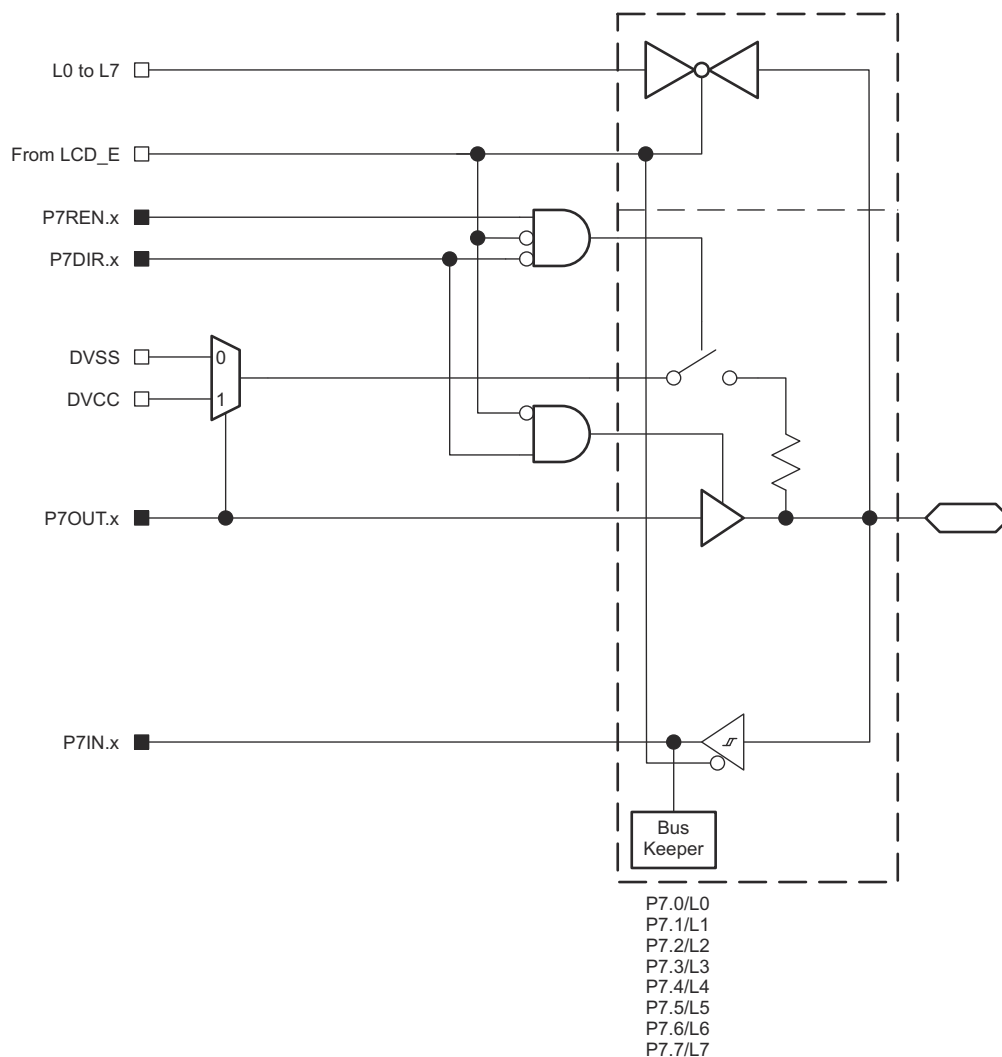
**Table 9-22. Port P6 Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |            |
|-----------------|---|------------|---|------------|
|                 |   |            | P6DIR.x                                 | LCDSy      |
| P6.0/L16        | 0 | P6.0 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L16        | X                                       | 1 (y = 16) |
| P6.1/L17        | 1 | P6.1 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L17        | X                                       | 1 (y = 17) |
| P6.2/L18        | 2 | P6.2 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L18        | X                                       | 1 (y = 18) |
| P6.3/L19        | 3 | P6.3 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L19        | X                                       | 1 (y = 19) |
| P6.4/L20        | 4 | P6.4 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L20        | X                                       | 1 (y = 20) |
| P6.5/L21        | 5 | P6.5 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L21        | X                                       | 1 (y = 21) |
| P6.6/L22        | 6 | P6.6 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L22        | X                                       | 1 (y = 22) |
| P6.7/L23        | 7 | P6.7 (I/O) | I: 0; O: 1                              | 0          |
|                 |   | L23        | X                                       | 1 (y = 23) |

(1) X= don't care

### 9.9.13.10 Port P7 Input/Output With Schmitt Trigger

Figure 9-12 shows the port schematic. Table 9-23 summarizes the selection of the pin functions.



**Figure 9-12. Port P7 Input/Output With Schmitt Trigger**

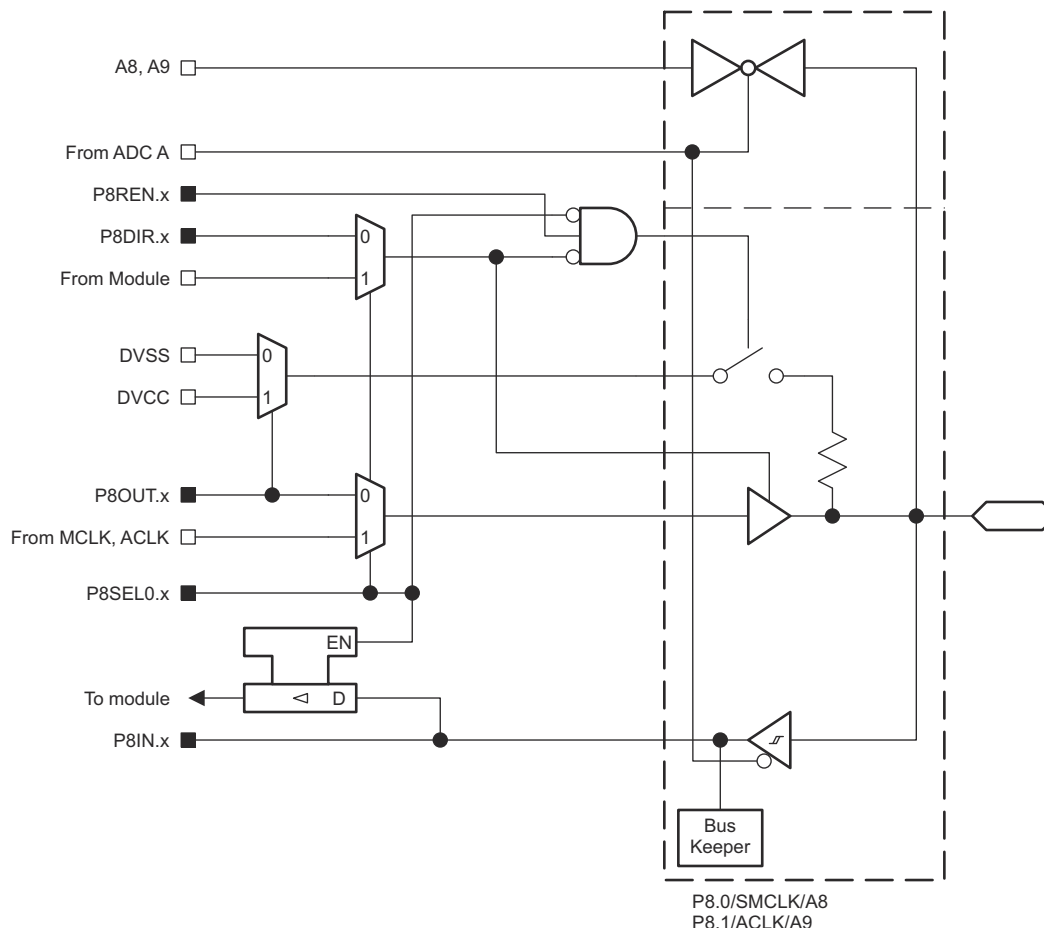
**Table 9-23. Port P7 Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |           |
|-----------------|---|------------|---|-----------|
|                 |   |            | P7DIR.x                                 | LCDSy     |
| P7.0/L0         | 0 | P7.0 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L0         | X                                       | 1 (y = 0) |
| P7.1/L1         | 1 | P7.1 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L1         | X                                       | 1 (y = 1) |
| P7.2/L2         | 2 | P7.2 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L2         | X                                       | 1 (y = 2) |
| P7.3/L3         | 3 | P7.3 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L3         | X                                       | 1 (y = 3) |
| P7.4/L4         | 4 | P7.4 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L4         | X                                       | 1 (y = 4) |
| P7.5/L5         | 5 | P7.5 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L5         | X                                       | 1 (y = 5) |
| P7.6/L6         | 6 | P7.6 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L6         | X                                       | 1 (y = 6) |
| P7.7/L7         | 7 | P7.7 (I/O) | I: 0; O: 1                              | 0         |
|                 |   | L7         | X                                       | 1 (y = 7) |

(1) X= don't care

### 9.9.13.11 Port P8.0 and P8.1 Input/Output With Schmitt Trigger

Figure 9-13 shows the port schematic. Table 9-24 summarizes the selection of the pin functions.



**Figure 9-13. Port P8.0 and P8.1 Input/Output With Schmitt Trigger**

**Table 9-24. Port P8.0 and P8.1 Pin Functions**

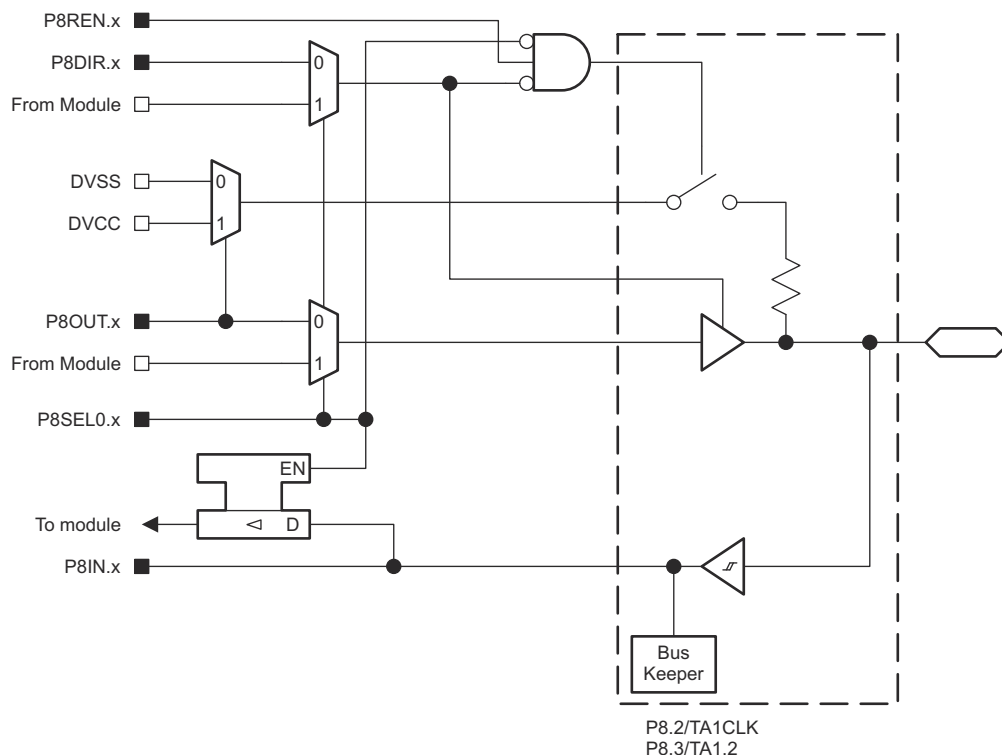
| PIN NAME (P8.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS <sup>(1)</sup> |          |                         |
|-----------------|---|------------|---|----------|-------------------------|
|                 |   |            | P8DIR.x                                 | P8SEL0.x | ADCPCTLx <sup>(2)</sup> |
| P8.0/SMCLK/A8   | 0 | P8.0 (I/O) | I: 0; O: 1                              | 0        | 0                       |
|                 |   | VSS        | 0                                       | 1        | 0                       |
|                 |   | SMCLK      | 1                                       |          |                         |
|                 |   | A8         | X                                       | X        | 1 (x = 8)               |
| P8.1/ACLK/A9    | 1 | P8.1 (I/O) | I: 0; O: 1                              | 0        | 0                       |
|                 |   | VSS        | 0                                       | 1        | 0                       |
|                 |   | ACLK       | 1                                       |          |                         |
|                 |   | A9         | X                                       | X        | 1 (x = 9)               |

(1) X= don't care

(2) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

### 9.9.13.12 Port P8.2 and P8.3 Input/Output With Schmitt Trigger

Figure 9-14 shows the port schematic. Table 9-25 summarizes the selection of the pin functions.



### Figure 9-14. Port P8.2 and P8.3 Input/Output With Schmitt Trigger

### Table 9-25. Port P8.2 and P8.3 Pin Functions

| PIN NAME (P8.x) | x | FUNCTION   | CONTROL BITS AND SIGNALS |          |
|-----------------|---|------------|--------------------------|----------|
|                 |   |            | P8DIR.x                  | P8SEL0.x |
| P8.2/TA1CLK     | 2 | P8.2 (I/O) | I: 0; O: 1               | 0        |
|                 |   | TA1 CLK    | 0                        | 1        |
|                 |   | VSS        | 1                        |          |
| P8.3/TA1.2      | 3 | P8.3 (I/O) | I: 0; O: 1               | 0        |
|                 |   | TA1.CCI2A  | 0                        | 1        |
|                 |   | TA1.2      | 1                        |          |

## 9.10 Device Descriptors (TLV)

[Table 9-26](#) lists the Device IDs of the MSP430FR413x devices. [Table 9-27](#) lists the contents of the device descriptor tag-length-value (TLV) structure for the MSP430FR413x devices.

**Table 9-26. Device IDs**

| DEVICE       | DEVICE ID |       |
|--------------|-----------|-------|
|              | 1A04h     | 1A05h |
| MSP430FR4133 | F0h       | 81h   |
| MSP430FR4132 | F1h       | 81h   |
| MSP430FR4131 | F2h       | 81h   |

**Table 9-27. Device Descriptors**

|                   | DESCRIPTION                                 | MSP430FR413x |                                |
|-------------------|---|--------------|--------------------------------|
|                   |   | ADDRESS      | VALUE                          |
| Information Block | Info length                                 | 1A00h        | 06h                            |
|                   | CRC length                                  | 1A01h        | 06h                            |
|                   | CRC value <sup>(2)</sup>                    | 1A02h        | Per unit                       |
|                   |   | 1A03h        | Per unit                       |
|                   | Device ID                                   | 1A04h        | See <a href="#">Table 9-26</a> |
|                   |   | 1A05h        |                                |
|                   | Hardware revision                           | 1A06h        | Per unit                       |
| Die Record        | Firmware revision                           | 1A07h        | Per unit                       |
|                   | Die Record Tag                              | 1A08h        | 08h                            |
|                   | Die Record length                           | 1A09h        | 0Ah                            |
|                   | Lot Wafer ID                                | 1A0Ah        | Per unit                       |
|                   |   | 1A0Bh        | Per unit                       |
|                   |   | 1A0Ch        | Per unit                       |
|                   |   | 1A0Dh        | Per unit                       |
|                   | Die X position                              | 1A0Eh        | Per unit                       |
|                   |   | 1A0Fh        | Per unit                       |
|                   | Die Y position                              | 1A10h        | Per unit                       |
|                   |   | 1A11h        | Per unit                       |
| ADC Calibration   | Test Result                                 | 1A12h        | Per unit                       |
|                   |   | 1A13h        | Per unit                       |
|                   | ADC Calibration Tag                         | 1A14h        | 11h                            |
|                   | ADC Calibration Length                      | 1A15h        | 08h                            |
|                   | ADC Gain Factor                             | 1A16h        | Per unit                       |
|                   |   | 1A17h        | Per unit                       |
|                   | ADC Offset                                  | 1A18h        | Per unit                       |
|                   |   | 1A19h        | Per unit                       |
|                   | ADC 1.5-V Reference Temperature Sensor 30°C | 1A1Ah        | Per unit                       |
|                   |   | 1A1Bh        | Per unit                       |
|                   | ADC 1.5-V Reference Temperature Sensor 85°C | 1A1Ch        | Per unit                       |
|                   |   | 1A1Dh        | Per unit                       |

**Table 9-27. Device Descriptors (continued)**

|                               | DESCRIPTION  | MSP430FR413x |          |
|-------------------------------|--|--------------|----------|
|                               |  | ADDRESS      | VALUE    |
| Reference and DCO Calibration | Calibration Tag  | 1A1Eh        | 12h      |
|                               | Calibration Length   | 1A1Fh        | 04h      |
|                               | 1.5-V Reference Factor                                       | 1A20h        | Per unit |
|                               |  | 1A21h        | Per unit |
|                               | DCO Tap Settings for 16 MHz, Temperature 30°C <sup>(1)</sup> | 1A22h        | Per unit |
|                               |  | 1A23h        | Per unit |

- (1) This value can be directly loaded into DCO bits in CSCTL0 register to get accurate 16-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. It is also suggested to use predivider to decrease the frequency if the temperature drift might result an overshoot beyond 16 MHz.
- (2) The CRC value covers the checksum from 1A04h to 1A77h by applying the CRC-CCITT-16 polynomial of  $x^{16} + x^{12} + x^5 + 1$ .

## 9.11 Memory

Table 9-28 shows the memory organization of the MSP430FR413x devices.

**Table 9-28. Memory Organization**

|  | ACCESS   | MSP430FR4133                             | MSP430FR4132                            | MSP430FR4131                            |
|--|--|--|---|---|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Read/Write<br>(Optional Write Protect)<br><sup>(1)</sup> | 15KB<br>FFFFh to FF80h<br>FFFFh to C400h | 8KB<br>FFFFh to FF80h<br>FFFFh to E000h | 4KB<br>FFFFh to FF80h<br>FFFFh to F000h |
| RAM  | Read/Write   | 2KB<br>27FFh to 2000h                    | 1KB<br>23FFh to 2000h                   | 512 bytes<br>21FFh to 2000h             |
| Information Memory (FRAM)  | Read/Write<br>(Optional Write Protect)<br><sup>(2)</sup> | 512 bytes<br>19FFh to 1800h              | 512 bytes<br>19FFh to 1800h             | 512 bytes<br>19FFh to 1800h             |
| Bootloader (BSL) Memory (ROM)  | Read only  | 1KB<br>13FFh to 1000h                    | 1KB<br>13FFh to 1000h                   | 1KB<br>13FFh to 1000h                   |
| Peripherals  | Read/Write   | 4KB<br>0FFFh to 0000h                    | 4KB<br>0FFFh to 0000h                   | 4KB<br>0FFFh to 0000h                   |

- (1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#) for more details.
- (2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#) for more details.



### 9.11.1 Peripheral File Map

[Table 9-29](#) shows the base address and the memory size of the registers of each peripheral, and [Table 9-30](#) through [Table 9-49](#) show all of the available registers for each peripheral and their address offsets.

**Table 9-29. Peripherals Summary**

| MODULE NAME  | BASE ADDRESS | SIZE  |
|--|--------------|-------|
| Special Functions (see <a href="#">Table 9-30</a> )    | 0100h        | 0010h |
| PMM (see <a href="#">Table 9-31</a> )                  | 0120h        | 0020h |
| SYS (see <a href="#">Table 9-32</a> )                  | 0140h        | 0030h |
| CS (see <a href="#">Table 9-33</a> )                   | 0180h        | 0020h |
| FRAM (see <a href="#">Table 9-34</a> )                 | 01A0h        | 0010h |
| CRC (see <a href="#">Table 9-35</a> )                  | 01C0h        | 0008h |
| WDT (see <a href="#">Table 9-36</a> )                  | 01CCh        | 0002h |
| Port P1, P2 (see <a href="#">Table 9-37</a> )          | 0200h        | 0020h |
| Port P3, P4 (see <a href="#">Table 9-38</a> )          | 0220h        | 0020h |
| Port P5, P6 (see <a href="#">Table 9-39</a> )          | 0240h        | 0020h |
| Port P7, P8 (see <a href="#">Table 9-40</a> )          | 0260h        | 0020h |
| Capacitive Touch I/O (see <a href="#">Table 9-41</a> ) | 02E0h        | 0010h |
| Timer0_A3 (see <a href="#">Table 9-42</a> )            | 0300h        | 0030h |
| Timer1_A3 (see <a href="#">Table 9-43</a> )            | 0340h        | 0030h |
| RTC (see <a href="#">Table 9-44</a> )                  | 03C0h        | 0010h |
| eUSCI_A0 (see <a href="#">Table 9-45</a> )             | 0500h        | 0020h |
| eUSCI_B0 (see <a href="#">Table 9-46</a> )             | 0540h        | 0030h |
| LCD (see <a href="#">Table 9-47</a> )                  | 0600h        | 0060h |
| Backup Memory (see <a href="#">Table 9-48</a> )        | 0660h        | 0020h |
| ADC (see <a href="#">Table 9-49</a> )                  | 0700h        | 0040h |

**Table 9-30. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable  | SFRIE1   | 00h    |
| SFR interrupt flag    | SFRIFG1  | 02h    |
| SFR reset pin control | SFRRPCR  | 04h    |

**Table 9-31. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| PMM control 0        | PMMCTL0  | 00h    |
| PMM control 1        | PMMCTL1  | 02h    |
| PMM control 2        | PMMCTL2  | 04h    |
| PMM interrupt flags  | PMMIFG   | 0Ah    |
| PM5 Control 0        | PM5CTL0  | 10h    |

**Table 9-32. SYS Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| System control                | SYCTL     | 00h    |
| Bootloader configuration area | SYSBSLC   | 02h    |
| JTAG mailbox control          | SYSJMBC   | 06h    |
| JTAG mailbox input 0          | SYSJMBI0  | 08h    |
| JTAG mailbox input 1          | SYSJMBI1  | 0Ah    |
| JTAG mailbox output 0         | SYSJMBO0  | 0Ch    |
| JTAG mailbox output 1         | SYSJMBO1  | 0Eh    |
| Bus Error vector generator    | SYSBERRIV | 18h    |
| User NMI vector generator     | SYSUNIV   | 1Ah    |
| System NMI vector generator   | SYSSNIV   | 1Ch    |
| Reset vector generator        | SYSRSTIV  | 1Eh    |
| System configuration 0        | SYSCFG0   | 20h    |
| System configuration 1        | SYSCFG1   | 22h    |
| System configuration 2        | SYSCFG2   | 24h    |

**Table 9-33. CS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| CS control register 0 | CSCTL0   | 00h    |
| CS control register 1 | CSCTL1   | 02h    |
| CS control register 2 | CSCTL2   | 04h    |
| CS control register 3 | CSCTL3   | 06h    |
| CS control register 4 | CSCTL4   | 08h    |
| CS control register 5 | CSCTL5   | 0Ah    |
| CS control register 6 | CSCTL6   | 0Ch    |
| CS control register 7 | CSCTL7   | 0Eh    |
| CS control register 8 | CSCTL8   | 10h    |

**Table 9-34. FRAM Registers (Base Address: 01A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| FRAM control 0       | FRCTL0   | 00h    |
| General control 0    | GCCTL0   | 04h    |
| General control 1    | GCCTL1   | 06h    |

**Table 9-35. CRC Registers (Base Address: 01C0h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRC16DI   | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**Table 9-36. WDT Registers (Base Address: 01CCh)**

| REGISTER DESCRIPTION   | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL   | 00h    |

**Table 9-37. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION               | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P1 input                      | P1IN     | 00h    |
| Port P1 output                     | P1OUT    | 02h    |
| Port P1 direction                  | P1DIR    | 04h    |
| Port P1 pulling register enable    | P1REN    | 06h    |
| Port P1 selection 0                | P1SEL0   | 0Ah    |
| Port P1 interrupt vector word      | P1IV     | 0Eh    |
| Port P1 interrupt edge select      | P1IES    | 18h    |
| Port P1 interrupt enable           | P1IE     | 1Ah    |
| Port P1 interrupt flag             | P1IFG    | 1Ch    |
| Port P2 input                      | P2IN     | 01h    |
| Port P2 output                     | P2OUT    | 03h    |
| Port P2 direction                  | P2DIR    | 05h    |
| Port P2 pulling register enable    | P2REN    | 07h    |
| Port P2 selection 0 <sup>(1)</sup> | P2SEL0   | 0Bh    |
| Port P2 interrupt vector word      | P2IV     | 1Eh    |
| Port P2 interrupt edge select      | P2IES    | 19h    |
| Port P2 interrupt enable           | P2IE     | 1Bh    |
| Port P2 interrupt flag             | P2IFG    | 1Dh    |

(1) Port P2 selection register does not feature any valid bits. P2SEL0 presents for 16-bit Port A operation with P1SEL0.

**Table 9-38. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION               | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P3 input                      | P3IN     | 00h    |
| Port P3 output                     | P3OUT    | 02h    |
| Port P3 direction                  | P3DIR    | 04h    |
| Port P3 pulling register enable    | P3REN    | 06h    |
| Port P3 selection 0 <sup>(1)</sup> | P3SEL0   | 0Ah    |
| Port P4 input                      | P4IN     | 01h    |
| Port P4 output                     | P4OUT    | 03h    |
| Port P4 direction                  | P4DIR    | 05h    |
| Port P4 pulling register enable    | P4REN    | 07h    |
| Port P4 selection 0                | P4SEL0   | 0Bh    |

(1) Port P3 selection register does not feature any valid bits. P3SEL0 presents for 16-bit Port B operation with P4SEL0.

**Table 9-39. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Port P5 input        | P5IN     | 00h    |

**Table 9-39. Port P5, P6 Registers (Base Address: 0240h) (continued)**

| REGISTER DESCRIPTION               | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P5 output                     | P5OUT    | 02h    |
| Port P5 direction                  | P5DIR    | 04h    |
| Port P5 pulling register enable    | P5REN    | 06h    |
| Port P5 selection 0                | P5SEL0   | 0Ah    |
| Port P6 input                      | P6IN     | 01h    |
| Port P6 output                     | P6OUT    | 03h    |
| Port P6 direction                  | P6DIR    | 05h    |
| Port P6 pulling register enable    | P6REN    | 07h    |
| Port P6 selection 0 <sup>(1)</sup> | P6SEL0   | 0Bh    |

(1) Port P6 selection register does not feature any valid bits. P6SEL0 presents for 16-bit Port C operation with P5SEL0.

**Table 9-40. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION               | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P7 input                      | P7IN     | 00h    |
| Port P7 output                     | P7OUT    | 02h    |
| Port P7 direction                  | P7DIR    | 04h    |
| Port P7 pulling register enable    | P7REN    | 06h    |
| Port P7 selection 0 <sup>(1)</sup> | P7SEL0   | 0Ah    |
| Port P8 input                      | P8IN     | 01h    |
| Port P8 output                     | P8OUT    | 03h    |
| Port P8 direction                  | P8DIR    | 05h    |
| Port P8 pulling register enable    | P8REN    | 07h    |
| Port P8 selection 0                | P8SEL0   | 0Bh    |

(1) Port P7 selection register does not feature any valid bits. P7SEL0 presents for 16-bit Port D operation with P8SEL0.

**Table 9-41. Capacitive Touch IO Registers (Base Address: 02E0h)**

| REGISTER DESCRIPTION          | REGISTER   | OFFSET |
|-------------------------------|------------|--------|
| Capacitive Touch IO 0 control | CAPTIO0CTL | 0Eh    |

**Table 9-42. Timer0\_A3 Registers (Base Address: 0300h)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control                | TA0CTL   | 00h    |
| Capture/compare control 0  | TA0CCTL0 | 02h    |
| Capture/compare control 1  | TA0CCTL1 | 04h    |
| Capture/compare control 2  | TA0CCTL2 | 06h    |
| TA0 counter register       | TA0R     | 10h    |
| Capture/compare register 0 | TA0CCR0  | 12h    |
| Capture/compare register 1 | TA0CCR1  | 14h    |
| Capture/compare register 2 | TA0CCR2  | 16h    |
| TA0 expansion register 0   | TA0EX0   | 20h    |
| TA0 interrupt vector       | TA0IV    | 2Eh    |

**Table 9-43. Timer1\_A3 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control               | TA1CTL   | 00h    |
| Capture/compare control 0 | TA1CCTL0 | 02h    |
| Capture/compare control 1 | TA1CCTL1 | 04h    |
| Capture/compare control 2 | TA1CCTL2 | 06h    |

**Table 9-43. Timer1\_A3 Registers (Base Address: 0340h) (continued)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 counter register       | TA1R     | 10h    |
| Capture/compare register 0 | TA1CCR0  | 12h    |
| Capture/compare register 1 | TA1CCR1  | 14h    |
| Capture/compare register 2 | TA1CCR2  | 16h    |
| TA1 expansion register 0   | TA1EX0   | 20h    |
| TA1 interrupt vector       | TA1IV    | 2Eh    |

**Table 9-44. RTC Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RTC control          | RTCCTL   | 00h    |
| RTC interrupt vector | RTCIV    | 04h    |
| RTC modulo           | RTCMOD   | 08h    |
| RTC counter          | RTCCNT   | 0Ch    |

**Table 9-45. eUSCI\_A0 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION          | REGISTER    | OFFSET |
|-------------------------------|-------------|--------|
| eUSCI_A control word 0        | UCA0CTLW0   | 00h    |
| eUSCI_A control word 1        | UCA0CTLW1   | 02h    |
| eUSCI_A control rate 0        | UCA0BR0     | 06h    |
| eUSCI_A control rate 1        | UCA0BR1     | 07h    |
| eUSCI_A modulation control    | UCA0MCTLW   | 08h    |
| eUSCI_A status                | UCA0STAT    | 0Ah    |
| eUSCI_A receive buffer        | UCA0RXBUF   | 0Ch    |
| eUSCI_A transmit buffer       | UCA0TXBUF   | 0Eh    |
| eUSCI_A LIN control           | UCA0ABCTL   | 10h    |
| eUSCI_A IrDA transmit control | IUCA0IRTCTL | 12h    |
| eUSCI_A IrDA receive control  | IUCA0IRRCTL | 13h    |
| eUSCI_A interrupt enable      | UCA0IE      | 1Ah    |
| eUSCI_A interrupt flags       | UCA0IFG     | 1Ch    |
| eUSCI_A interrupt vector word | UCA0IV      | 1Eh    |

**Table 9-46. eUSCI\_B0 Registers (Base Address: 0540h)**

| REGISTER DESCRIPTION           | REGISTER    | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0         | UCB0CTLW0   | 00h    |
| eUSCI_B control word 1         | UCB0CTLW1   | 02h    |
| eUSCI_B bit rate 0             | UCB0BR0     | 06h    |
| eUSCI_B bit rate 1             | UCB0BR1     | 07h    |
| eUSCI_B status word            | UCB0STATW   | 08h    |
| eUSCI_B byte counter threshold | UCB0TBCNT   | 0Ah    |
| eUSCI_B receive buffer         | UCB0RXBUF   | 0Ch    |
| eUSCI_B transmit buffer        | UCB0TXBUF   | 0Eh    |
| eUSCI_B I2C own address 0      | UCB0I2COA0  | 14h    |
| eUSCI_B I2C own address 1      | UCB0I2COA1  | 16h    |
| eUSCI_B I2C own address 2      | UCB0I2COA2  | 18h    |
| eUSCI_B I2C own address 3      | UCB0I2COA3  | 1Ah    |
| eUSCI_B receive address        | UCB0ADDRX   | 1Ch    |
| eUSCI_B address mask           | UCB0ADDMASK | 1Eh    |
| eUSCI_B I2C slave address      | UCB0I2CSA   | 20h    |
| eUSCI_B interrupt enable       | UCB0IE      | 2Ah    |
| eUSCI_B interrupt flags        | UCB0IFG     | 2Ch    |
| eUSCI_B interrupt vector word  | UCB0IV      | 2Eh    |

**Table 9-47. LCD Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION                              | REGISTER  | OFFSET |
|---|-----------|--------|
| LCD control register 0                            | LCDCTL0   | 00h    |
| LCD control register 1                            | LCDCTL1   | 02h    |
| LCD blink control register                        | LCDBLKCTL | 04h    |
| LCD memory control register                       | LCDMEMCTL | 06h    |
| LCD voltage control register                      | LCDVCTL   | 08h    |
| LCD port control 0                                | LCDPCTL0  | 0Ah    |
| LCD port control 1                                | LCDPCTL1  | 0Ch    |
| LCD port control 2                                | LCDPCTL2  | 0Eh    |
| LCD COM/SEG select register                       | LCDCSS0   | 14h    |
| LCD COM/SEG select register                       | LCDCSS1   | 16h    |
| LCD COM/SEG select register                       | LCDCSS2   | 18h    |
| LCD interrupt vector                              | LCDIV     | 1Eh    |
| <b>Display memory Static and 2 to 4 mux modes</b> |           |        |
| LCD memory 0                                      | LCDM0     | 20h    |
| LCD memory 1                                      | LCDM1     | 21h    |
| LCD memory 2                                      | LCDM2     | 22h    |
| ⋮   | ⋮         | ⋮      |
| LCD memory 19                                     | LCDM19    | 33h    |
| Reserved <sup>(1)</sup>                           |           | 34h    |
| ⋮   | ⋮         | ⋮      |
| Reserved <sup>(1)</sup>                           |           | 3Fh    |

**Table 9-47. LCD Registers (Base Address: 0600h) (continued)**

| REGISTER DESCRIPTION                                   | REGISTER | OFFSET |
|--|----------|--------|
| <b>Blinking memory for Static and 2 to 4 mux modes</b> |          |        |
| LCD blinking memory 0                                  | LCDBM0   | 40h    |
| LCD blinking memory 1                                  | LCDBM1   | 41h    |
| ⋮  | ⋮        | ⋮      |
| LCD blinking memory 19                                 | LCDBM19  | 53h    |
| Reserved <sup>(1)</sup>                                |          | 54h    |
| ⋮  | ⋮        | ⋮      |
| Reserved <sup>(1)</sup>                                |          | 5Fh    |
| <b>Display memory for 5 to 8 mux modes</b>             |          |        |
| LCD memory 0   | LCDM0    | 20h    |
| LCD memory 1   | LCDM1    | 21h    |
| LCD memory 2   | LCDM2    | 22h    |
| ⋮  | ⋮        | ⋮      |
| LCD memory 39  | LCDM39   | 47h    |
| Reserved <sup>(2)</sup>                                |          | 48h    |
| ⋮  | ⋮        | ⋮      |
| Reserved <sup>(2)</sup>                                |          | 5Fh    |

(1) In static and 2-mux to 4-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

(2) In 5-mux to 8-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

**Table 9-48. Backup Memory Registers (Base Address: 0660h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Backup memory 0      | BAKMEM0  | 00h    |
| Backup memory 1      | BAKMEM1  | 02h    |
| Backup memory 2      | BAKMEM2  | 04h    |
| Backup memory 3      | BAKMEM3  | 06h    |
| Backup memory 4      | BAKMEM4  | 08h    |
| Backup memory 5      | BAKMEM5  | 0Ah    |
| Backup memory 6      | BAKMEM6  | 0Ch    |
| Backup memory 7      | BAKMEM7  | 0Eh    |
| Backup memory 8      | BAKMEM8  | 10h    |
| Backup memory 9      | BAKMEM9  | 12h    |
| Backup memory 10     | BAKMEM10 | 14h    |
| Backup memory 11     | BAKMEM11 | 16h    |
| Backup memory 12     | BAKMEM12 | 18h    |
| Backup memory 13     | BAKMEM13 | 1Ah    |
| Backup memory 14     | BAKMEM14 | 1Ch    |
| Backup memory 15     | BAKMEM15 | 1Eh    |

**Table 9-49. ADC Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION                 | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| ADC control register 0               | ADCCTL0  | 00h    |
| ADC control register 1               | ADCCTL1  | 02h    |
| ADC control register 2               | ADCCTL2  | 04h    |
| ADC window comparator low threshold  | ADCLO    | 06h    |
| ADC window comparator high threshold | ADCHI    | 08h    |
| ADC memory control register 0        | ADCMCTL0 | 0Ah    |
| ADC conversion memory register       | ADCMEM0  | 12h    |
| ADC interrupt enable                 | ADCIE    | 1Ah    |
| ADC interrupt flags                  | ADCIFG   | 1Ch    |
| ADC interrupt vector word            | ADCIV    | 1Eh    |

## 9.12 Identification

### 9.12.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 11.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [Section 9.10](#).

### 9.12.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 11.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [Section 9.10](#).

### 9.12.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in [MSP430 Programming With the JTAG Interface](#).



## 10 Applications, Implementation, and Layout

### Note

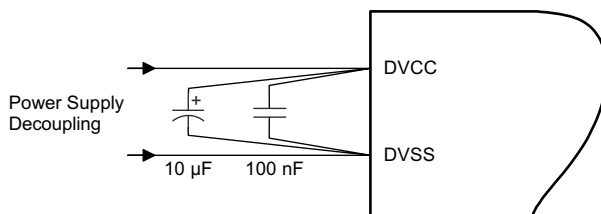
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430FR413x devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

#### 10.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10- $\mu$ F plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins (see [Figure 10-1](#)). Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).



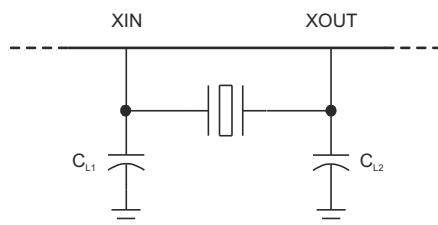
**Figure 10-1. Power Supply Decoupling**

#### 10.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If they are left unused, they must be terminated according to [Section 7.4](#).

[Figure 10-2](#) shows a typical connection diagram.



**Figure 10-2. Typical Crystal Connection**

See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

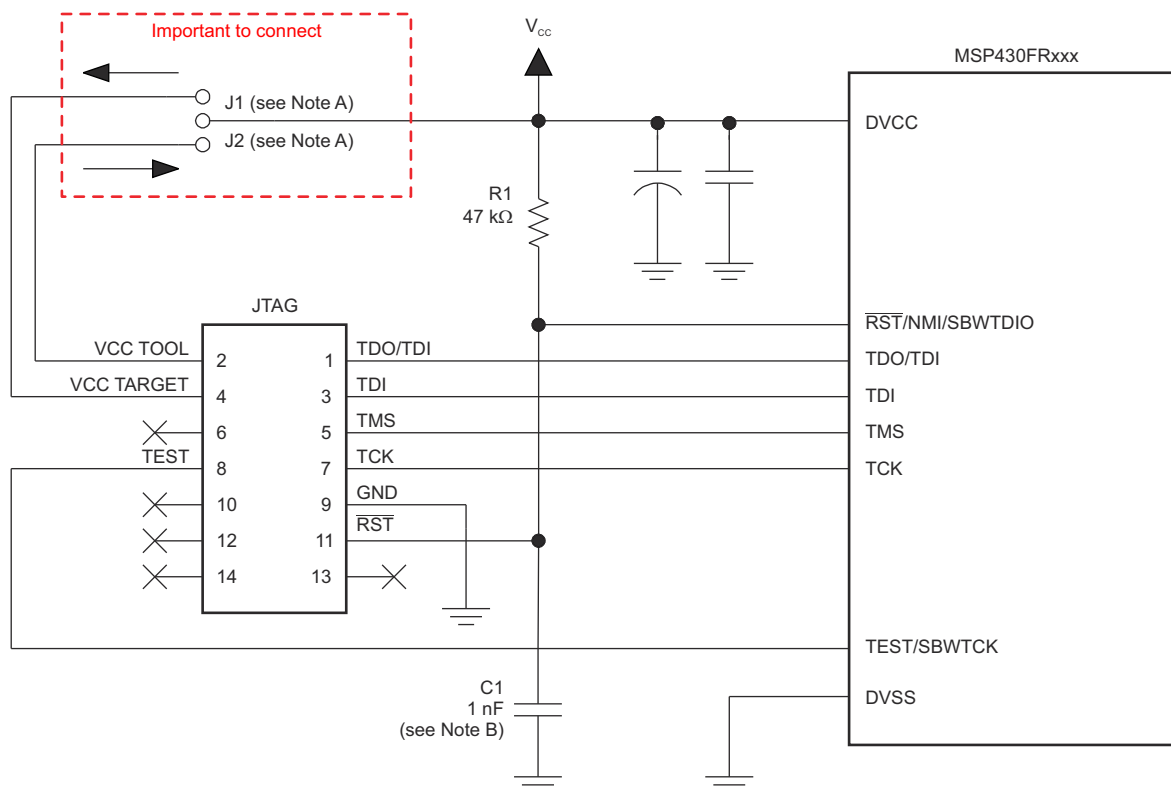
#### 10.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if

desired. Figure 10-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 10-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

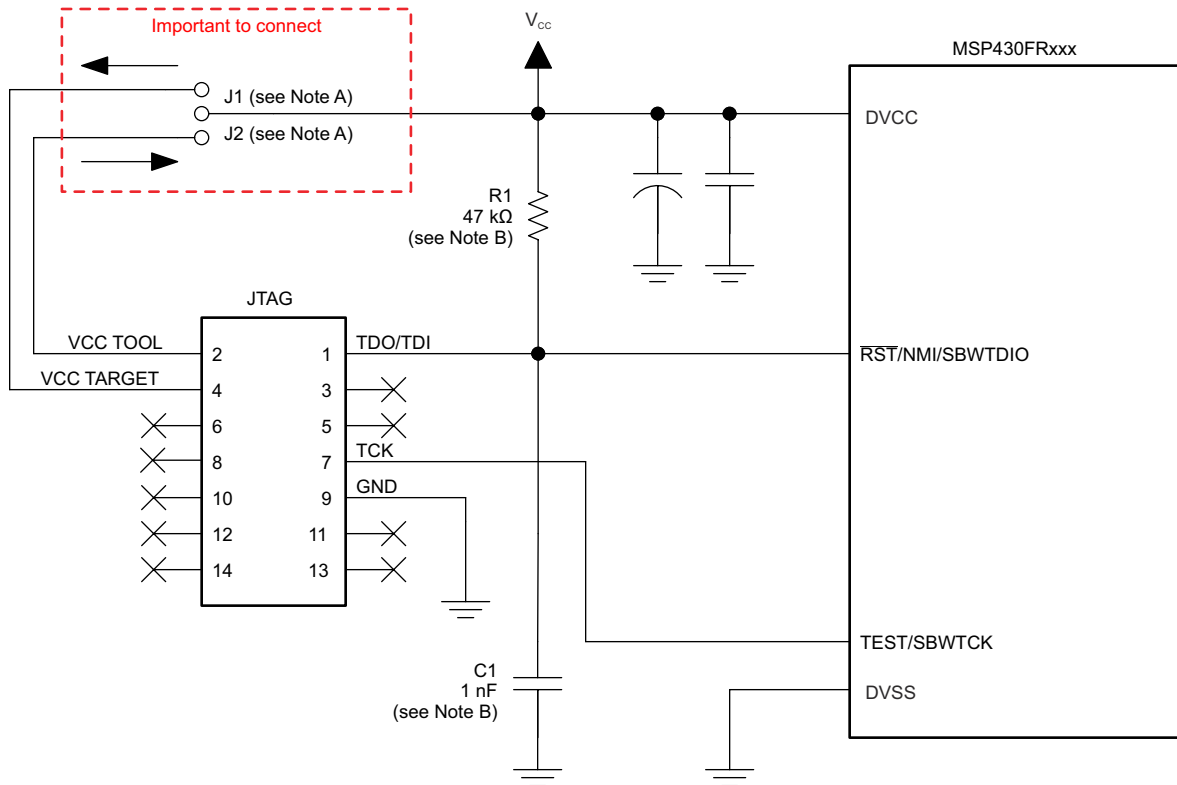
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply  $V_{CC}$  to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a  $V_{CC}$ -sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The  $V_{CC}$ -sense feature senses the local  $V_{CC}$  present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 10-3 and Figure 10-4 show a jumper block that supports both scenarios of supplying  $V_{CC}$  to the target board. If this flexibility is not required, the desired  $V_{CC}$  connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 10-3. Signal Connections for 4-Wire JTAG Communication**



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device  $\overline{\text{RST}}/\text{NMI}/\text{SBWTIO}$  pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

**Figure 10-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

#### 10.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the  $\overline{\text{RST}}/\text{NMI}$  pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the  $\overline{\text{RST}}/\text{NMI}$  pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The  $\overline{\text{RST}}/\text{NMI}$  pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the  $\overline{\text{RST}}/\text{NMI}$  pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the  $\overline{\text{RST}}/\text{NMI}$  pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#) for more information on the referenced control registers and bits.

#### 10.1.5 Unused Pins

For details on the connection of unused pins, see [Section 7.4](#).

## 10.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

## 10.1.7 Do's and Don'ts

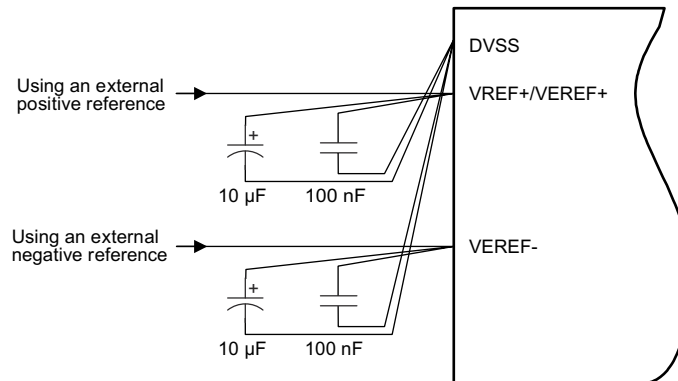
During power up, power down, and device operation, DVCC must not exceed the limits specified in [Section 8.1](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 10.2 Peripheral- and Interface-Specific Design Information

### 10.2.1 ADC Peripheral

#### 10.2.1.1 Partial Schematic

[Figure 10-5](#) shows the recommended circuit for ADC grounding and noise reduction.



**Figure 10-5. ADC Grounding and Noise Considerations**

#### 10.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 10.1.1](#) combined with the connections shown in [Section 10.2.1.1](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

[Figure 10-5](#) shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filters low-frequency ripple. A 100-nF bypass capacitor filters out high-frequency noise.

### 10.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 10-5](#)) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

## 10.2.2 LCD\_E Peripheral

### 10.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, LCD\_E has configurable segment (Sx) or common (COMx) signals connected to the MCU which allows optimal PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for an example of connecting a 4-mux LCD with 27 segment lines that has a total of  $4 \times 27 = 108$  individually addressable LCD segments to an MSP430FR4133, see the [MSP-EXP430FR4133 LaunchPad™ development kit](#) as a reference.

### 10.2.2.2 Design Requirements

Due to the flexibility of the LCD\_E peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments must be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD\_E peripheral module chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#) during the initial design requirements and decision process. [Table 10-1](#) provides a brief overview over different choices that can be made and their impact.

**Table 10-1. LCD\_E Design Options**

| OPTION OR FEATURE        | IMPACT OR USE CASE  |
|--------------------------|---|
| Multiplexed LCD          | <ul style="list-style-type: none"> <li>• Enable displays with more segments</li> <li>• Use fewer device pins</li> <li>• LCD contrast decreases as mux level increases</li> <li>• Power consumption increases with mux level</li> <li>• Requires multiple intermediate bias voltages</li> </ul>  |
| Static LCD               | <ul style="list-style-type: none"> <li>• Limited number of segments that can be addressed</li> <li>• Use a relatively large number of device pins</li> <li>• Use the least amount of power</li> <li>• Use only <math>V_{CC}</math> and GND to drive LCD signals</li> </ul>  |
| Internal Bias Generation | <ul style="list-style-type: none"> <li>• Simpler solution – no external circuitry</li> <li>• Independent of <math>V_{LCD}</math> source</li> <li>• Somewhat higher power consumption</li> </ul>   |
| External Bias Generation | <ul style="list-style-type: none"> <li>• Requires external resistor ladder divider</li> <li>• Resistor size depends on display</li> <li>• Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load)</li> <li>• External resistor ladder divider can be stabilized through capacitors to reduce ripple</li> </ul>                    |
| Internal Charge Pump     | <ul style="list-style-type: none"> <li>• Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications)</li> <li>• Programmable voltage levels allow software-driven contrast control</li> <li>• Requires an external capacitor on the LCDCAP pins</li> <li>• Higher current consumption than simply using <math>V_{CC}</math> for the LCD driver</li> </ul> |

### 10.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD\_E peripheral module and the display itself. Two basic design processes can be employed for this step, although often a balanced co-design approach is recommended:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, LCD\_E offers configurable segment Sx and common COMx signals which are connected to the respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD\_E module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD\_E module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit through a single byte-wide access to an LCDMx register. And consecutive segments are mapped to consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing

computational overhead and optimizing the energy consumption of an application. Establishing of the most convenient memory layout needs to be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see the LCD\_E controller chapter in the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

#### 10.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP0 and LCDCAP1 pins should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace.

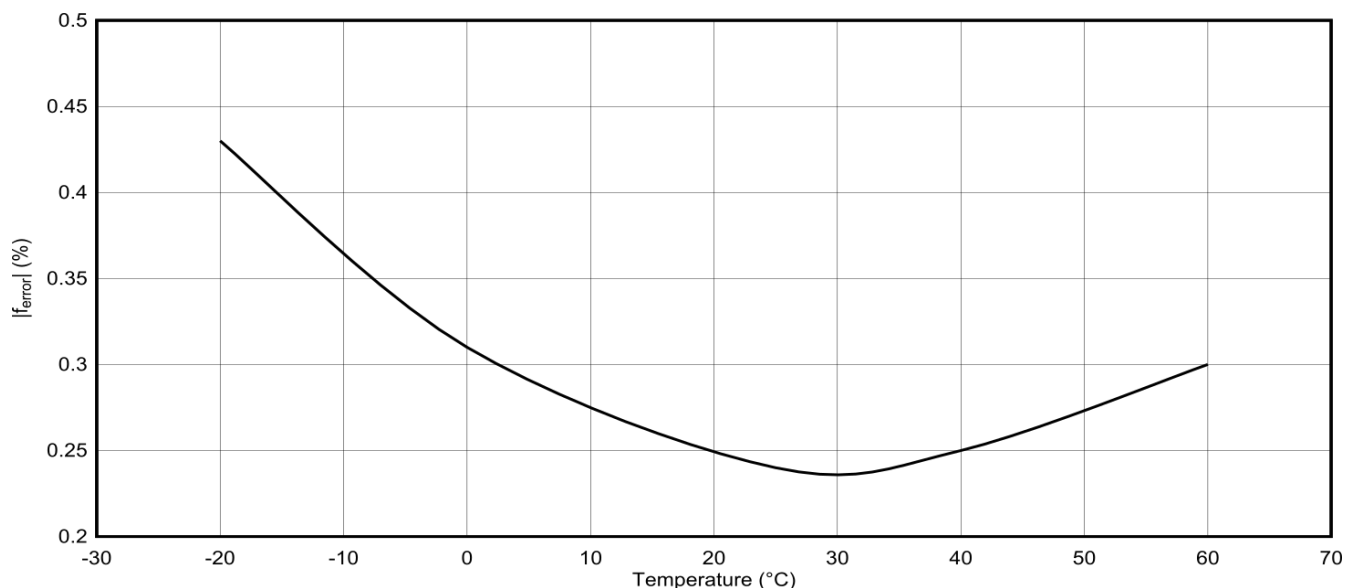
For an example layout of connecting a 4-mux LCD with 27 segments to an MSP430FR4133 and using the charge pump feature, see the [MSP-EXP430FR4133 LaunchPad development kit](#).

### 10.2.3 Timer

#### 10.2.3.1 Generate Accurate PWM Using Internal Oscillator

Generating an accurate PWM signal using the device internal oscillator is an important feature for many cost-sensitive applications in which an external crystal is not desired. The MSP430FR4133 uses an on-chip 32-kHz RC oscillator (REFO) combined with the 16-MHz digitally controlled oscillator (DCO) with frequency-locked loop (FLL) to provide the clock source for the timer peripheral to generate the PWM. The REFO frequency may change across different temperatures. To achieve improved PWM accuracy, application software may periodically measure the device temperature and compute an appropriate timer capture/compare correction value to offset for REFO temperature drift. For more information on how to implement this algorithm refer to [How to Achieve Higher Accuracy Timer with Internal Oscillator on MSP430](#). Figure 10-6 shows the absolute value of a typical error percentage for a 44-kHz PWM signal over the temperature range.

The absolute value error percentages shown below can be interpreted as either positive or negative resulting in a slightly faster or slower PWM frequency.



**Figure 10-6. Calibrated 44-kHz Timer PWM Error Magnitude**

## 10.3 Typical Applications

[Table 10-2](#) lists reference designs that demonstrate use of the MSP430FR413x family of devices in different real-world application scenarios. Consult these designs for additional guidance regarding schematic, layout, and software implementation. For the most up-to-date list of available reference designs, visit [TI reference designs](#).

**Table 10-2. Reference Designs**

| DESIGN NAME  | LINK  |
|--|---|
| Thermostat Implementation With MSP430FR4xx                           | <a href="#">TIDM-FRAM-THERMOSTAT</a>          |
| Water Meter Implementation With MSP430FR4xx                          | <a href="#">TIDM-FRAM-WATERMETER</a>          |
| Remote Controller of Air Conditioner Using Low-Power Microcontroller | <a href="#">TIDM-REMOTE-CONTROLLER-FOR-AC</a> |



## 11 Device and Documentation Support

### 11.1 Getting Started

For an introduction to the MSP430 family of devices and the tools and libraries that are available to help with your development, visit the [MSP430™ ultra-low-power sensing & measurement MCUs overview](#).

### 11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

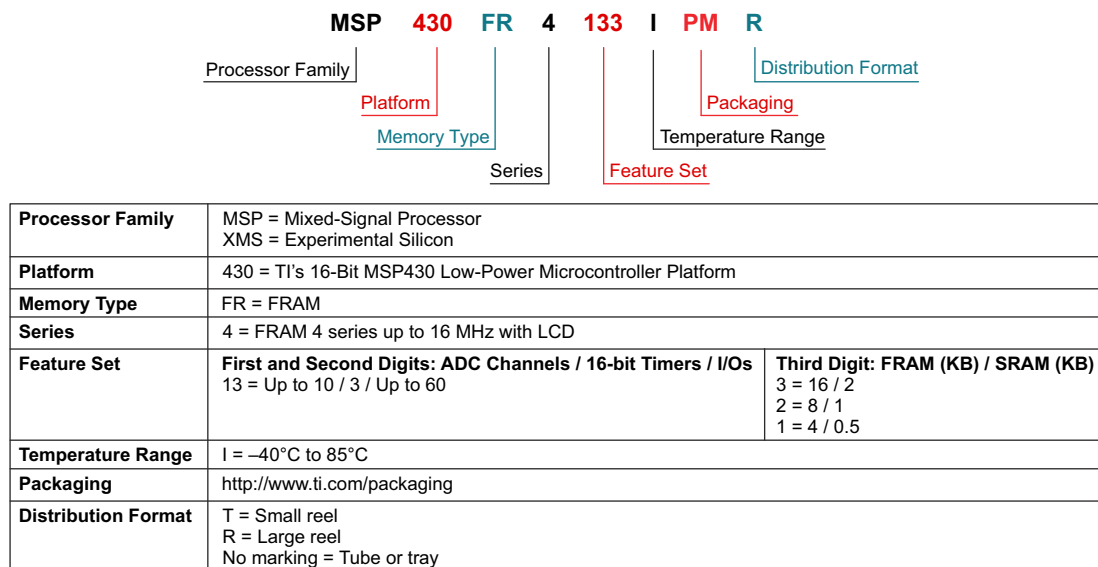
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 11-1](#) provides a legend for reading the complete device name.



**Figure 11-1. Device Nomenclature**

## 11.3 Tools and Software

Table 11-1 lists the debug features supported by the MSP430FR413x microcontrollers. See the [Code Composer Studio IDE for MSP430 MCUs User's Guide](#) for details on the available features.

**Table 11-1. Hardware Features**

| MSP430<br>ARCHITECTURE | 4-WIRE<br>JTAG | 2-WIRE<br>JTAG | BREAK-<br>POINTS<br>(N) | RANGE<br>BREAK-<br>POINTS | CLOCK<br>CONTROL | STATE<br>SEQUENCER | TRACE<br>BUFFER | LPMX.5<br>DEBUGGING<br>SUPPORT |
|------------------------|----------------|----------------|-------------------------|---------------------------|------------------|--------------------|-----------------|--------------------------------|
| MSP430Xv2              | Yes            | Yes            | 3                       | Yes                       | Yes              | No                 | No              | No                             |

### Design Kits and Evaluation Modules

#### MSP430FR4133 LaunchPad Development Kit

The MSP-EXP430FR4133 LaunchPad development kit is an easy-to-use Evaluation Module (EVM) for the MSP430FR4133 microcontroller. It contains everything needed to start developing on the MSP430 ultra-low-power (ULP) FRAM-based microcontroller (MCU) platform, including on-board emulation for programming, debugging, and energy measurements.

#### MSP-TS430PM64D Target Development Board for MSP430FR2x/4x MCUs

The MSP-TS430PM64D is a stand-alone 64-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

#### MSP-FET430U64D Target Development Board (64-pin) and MSP-FET Programmer Bundle for MSP430FR2x/4x MCUs

The MSP-FET430U64D is a bundle containing the MSP-FET emulator and MSP-TS430PM64D 64-pin ZIF socket target board to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

### Software

#### MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

#### MSP430FR413x, MSP430FR203x Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

#### FRAM Embedded Software Utilities for MSP Ultra-Low-Power Microcontrollers

The TI FRAM Utilities software is designed to grow as a collection of embedded software utilities that leverage the ultra-low-power and virtually unlimited write endurance of FRAM. The utilities are available for MSP430FRxx FRAM microcontrollers and provide example code to help start application development.

#### MSP430 Touch Pro GUI

The MSP430 Touch Pro Tool is a PC-based tool that can be used to verify capacitive touch button, slider, and wheel designs. The tool receives and visualizes captouch sensor data to help the user quickly and easily evaluate, diagnose, and tune button, slider, and wheel designs.

## [MSP430 Touch Power Designer GUI](#)

The MSP430 Capacitive Touch Power Designer enables the calculation of the estimated average current draw for a given MSP430 capacitive touch system. By entering system parameters such as operating voltage, frequency, number of buttons, and button gate time, the user can have a power estimate for a given capacitive touch configuration on a given device family in minutes.

## [Digital Signal Processing \(DSP\) Library for MSP Microcontrollers](#)

The Digital Signal Processing library is a set of highly optimized functions to perform many common signal processing operations on fixed-point numbers for MSP430 and MSP432 microcontrollers. This function set is typically used for applications where processing-intensive transforms are done in real-time for minimal energy and with very high accuracy. This optimal use of the MSP intrinsic hardware for fixed-point math allows for significant performance gains.

## [MSP Driver Library](#)

The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

## [MSP EnergyTrace Technology](#)

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low-power consumption.

## [ULP \(Ultra-Low Power\) Advisor](#)

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

## [Fixed Point Math Library for MSP](#)

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

## [Floating Point Math Library for MSP430](#)

Continuing to innovate in the low-power and low-cost microcontroller space, TI provides MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating-point math library of scalar functions is up to 26 times faster than the standard MSP430 math functions. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

## **Development Tools**

### [Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers](#)

Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

## Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

## MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

## MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

## 11.4 Documentation Support

The following documents describe the MSP430FR413x microcontrollers. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

### Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### Errata

#### MSP430FR4133 Device Erratasheet

Describes the known exceptions to the functional specifications.

#### MSP430FR4132 Device Erratasheet

Describes the known exceptions to the functional specifications.

#### MSP430FR4131 Device Erratasheet

Describes the known exceptions to the functional specifications.

### User's Guides

#### MSP430FR4xx and MSP430FR2xx Family User's Guide

Detailed description of all modules and peripherals available in this device family.

#### MSP430 FRAM Device Bootloader (BSL) User's Guide

The bootloader (BSL) on MSP430 MCUs lets users communicate with embedded memory in the MSP430 MCU during the prototyping phase, final production, and in service. Both the programmable memory (FRAM memory) and the data memory (RAM) can be modified as required.

#### MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

## MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

## Application Reports

### MSP430 FRAM Technology – How To and Best Practices

FRAM is a nonvolatile memory technology that behaves similar to SRAM while enabling a whole host of new applications, but also changing the way firmware should be designed. This application report outlines the how to and best practices of using FRAM technology in MSP430 from an embedded software development perspective. It discusses how to implement a memory layout according to application-specific code, constant, data space requirements, and the use of FRAM to optimize application energy consumption.

### MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

### MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.

## 11.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 11.6 Trademarks

LaunchPad™, MSP430Ware™, MSP430™, Code Composer Studio™, TI E2E™, ULP Advisor™, are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

## 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 11.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FR4131IG48  | ACTIVE        | TSSOP        | DGG                | 48   | 40             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4131                  | <a href="#">Samples</a> |
| MSP430FR4131IG48R | ACTIVE        | TSSOP        | DGG                | 48   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4131                  | <a href="#">Samples</a> |
| MSP430FR4131IG56  | ACTIVE        | TSSOP        | DGG                | 56   | 35             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4131                  | <a href="#">Samples</a> |
| MSP430FR4131IG56R | ACTIVE        | TSSOP        | DGG                | 56   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4131                  | <a href="#">Samples</a> |
| MSP430FR4131IPMR  | ACTIVE        | LQFP         | PM                 | 64   | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4131                  | <a href="#">Samples</a> |
| MSP430FR4132IG48  | ACTIVE        | TSSOP        | DGG                | 48   | 40             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4132                  | <a href="#">Samples</a> |
| MSP430FR4132IG48R | ACTIVE        | TSSOP        | DGG                | 48   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4132                  | <a href="#">Samples</a> |
| MSP430FR4132IG56  | ACTIVE        | TSSOP        | DGG                | 56   | 35             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4132                  | <a href="#">Samples</a> |
| MSP430FR4132IG56R | ACTIVE        | TSSOP        | DGG                | 56   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4132                  | <a href="#">Samples</a> |
| MSP430FR4132IPMR  | ACTIVE        | LQFP         | PM                 | 64   | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4132                  | <a href="#">Samples</a> |
| MSP430FR4133IG48  | ACTIVE        | TSSOP        | DGG                | 48   | 40             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |
| MSP430FR4133IG48R | ACTIVE        | TSSOP        | DGG                | 48   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |
| MSP430FR4133IG56  | ACTIVE        | TSSOP        | DGG                | 56   | 35             | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |
| MSP430FR4133IG56R | ACTIVE        | TSSOP        | DGG                | 56   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |
| MSP430FR4133IPM   | ACTIVE        | LQFP         | PM                 | 64   | 160            | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |
| MSP430FR4133IPMR  | ACTIVE        | LQFP         | PM                 | 64   | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | FR4133                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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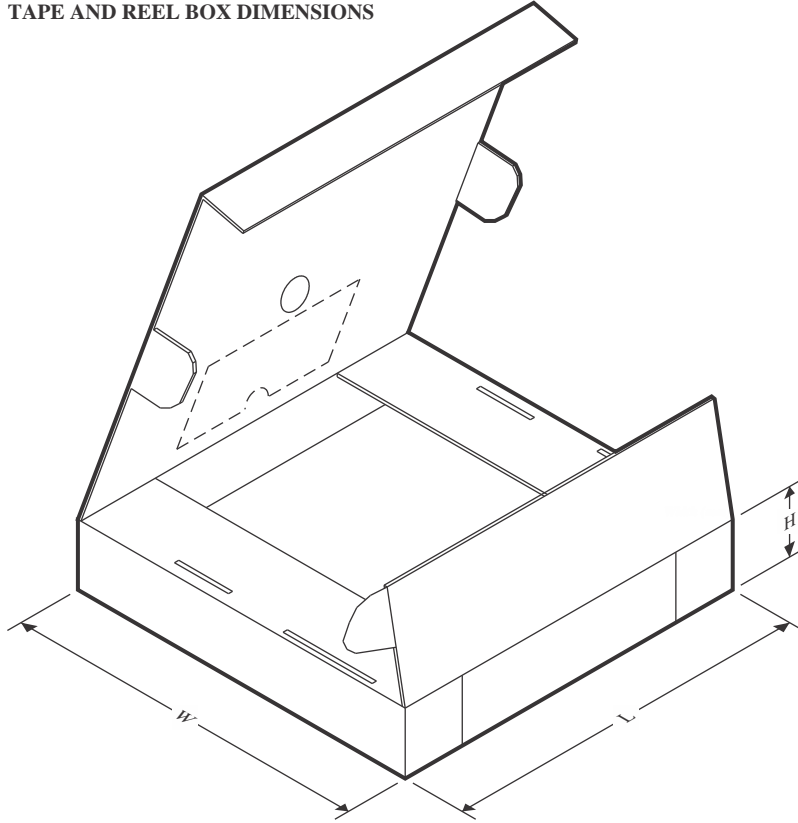
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR4131IG48R | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR4131IG56R | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR4131IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR4132IG48R | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR4132IG56R | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR4132IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430FR4133IG48R | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| MSP430FR4133IPMR  | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |

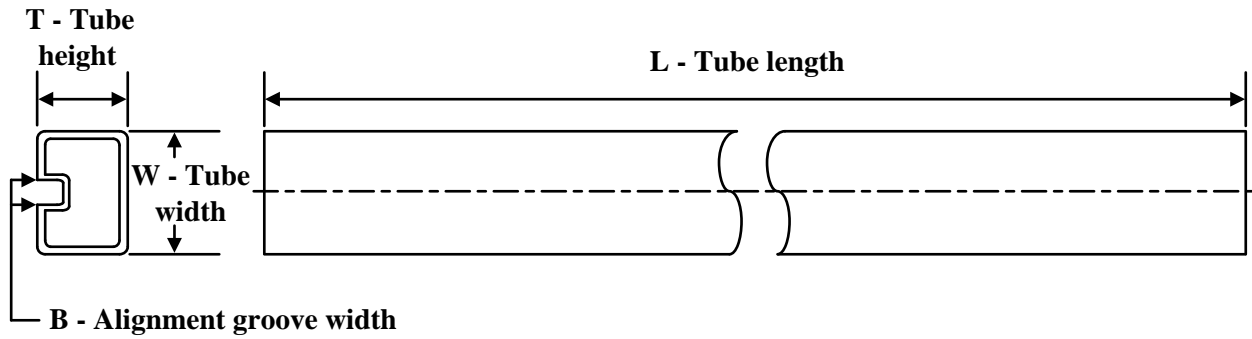
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR4131IG48R | TSSOP        | DGG             | 48   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4131IG56R | TSSOP        | DGG             | 56   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4131IPMR  | LQFP         | PM              | 64   | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4132IG48R | TSSOP        | DGG             | 48   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4132IG56R | TSSOP        | DGG             | 56   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4132IPMR  | LQFP         | PM              | 64   | 1000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4133IG48R | TSSOP        | DGG             | 48   | 2000 | 350.0       | 350.0      | 43.0        |
| MSP430FR4133IPMR  | LQFP         | PM              | 64   | 1000 | 350.0       | 350.0      | 43.0        |

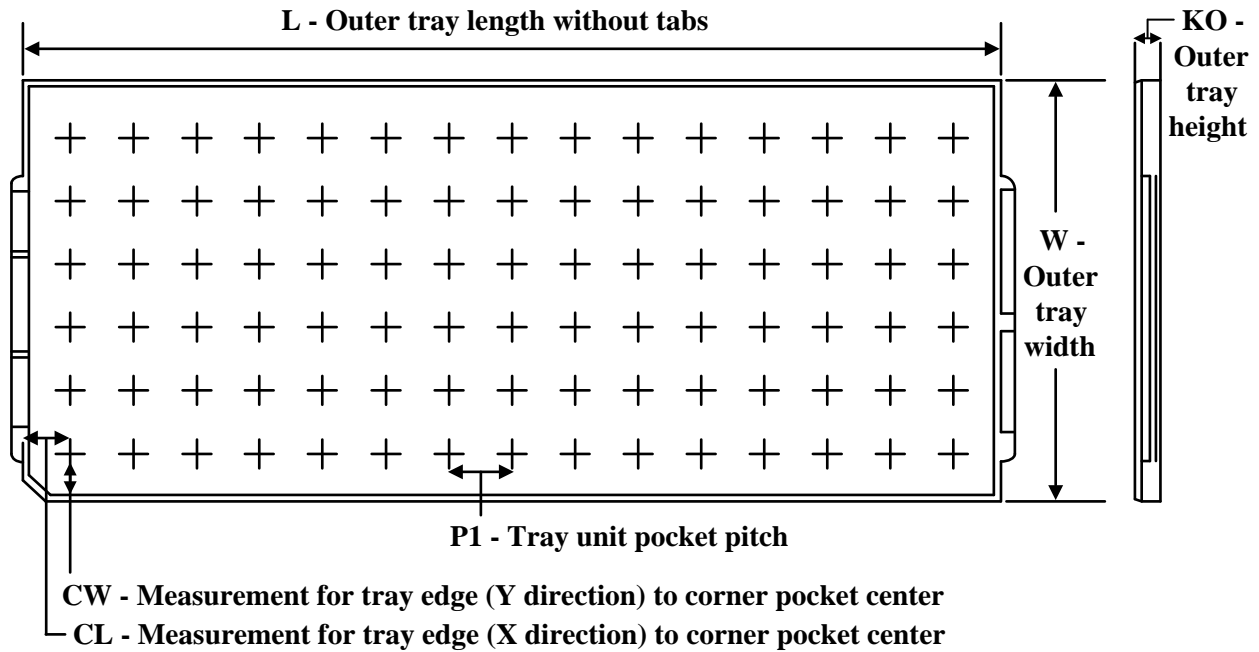
## TUBE



\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MSP430FR4131IG48 | DGG          | TSSOP        | 48   | 40  | 530    | 11.89  | 3600   | 4.9    |
| MSP430FR4131IG56 | DGG          | TSSOP        | 56   | 35  | 530    | 11.89  | 3600   | 4.9    |
| MSP430FR4132IG48 | DGG          | TSSOP        | 48   | 40  | 530    | 11.89  | 3600   | 4.9    |
| MSP430FR4132IG56 | DGG          | TSSOP        | 56   | 35  | 530    | 11.89  | 3600   | 4.9    |
| MSP430FR4133IG48 | DGG          | TSSOP        | 48   | 40  | 530    | 11.89  | 3600   | 4.9    |
| MSP430FR4133IG56 | DGG          | TSSOP        | 56   | 35  | 530    | 11.89  | 3600   | 4.9    |

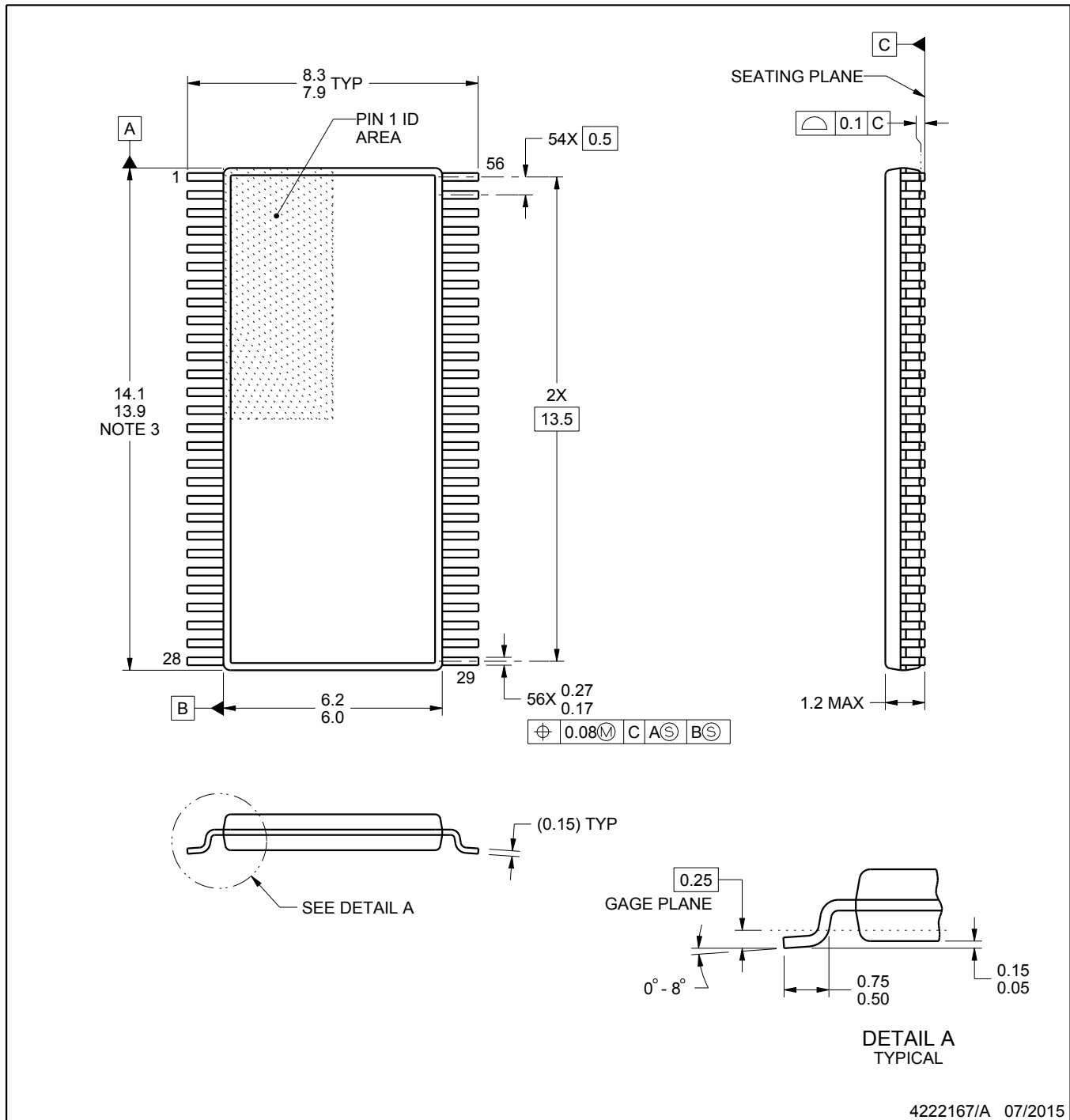
## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| MSP430FR4133IPM | PM           | LQFP         | 64   | 160 | 8 x 20            | 150                  | 315    | 135.9  | 7620    | 15.2    | 13.1    | 13      |



4222167/A 07/2015

## NOTES:

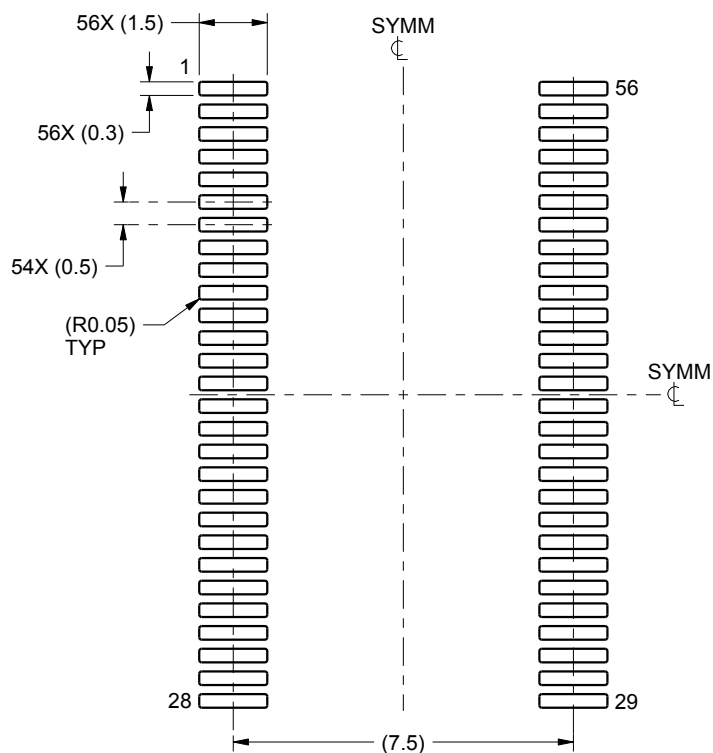
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

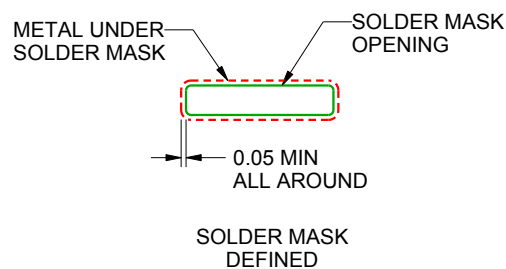
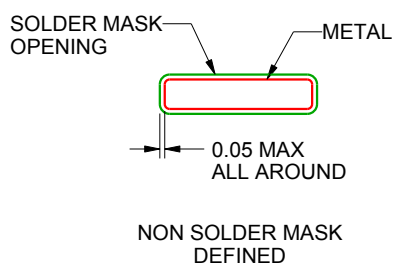
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

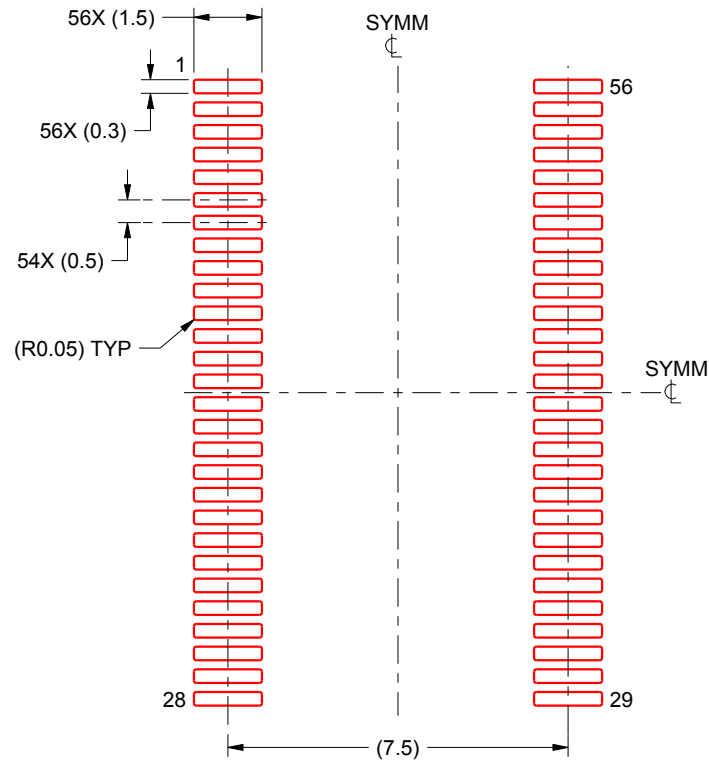
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



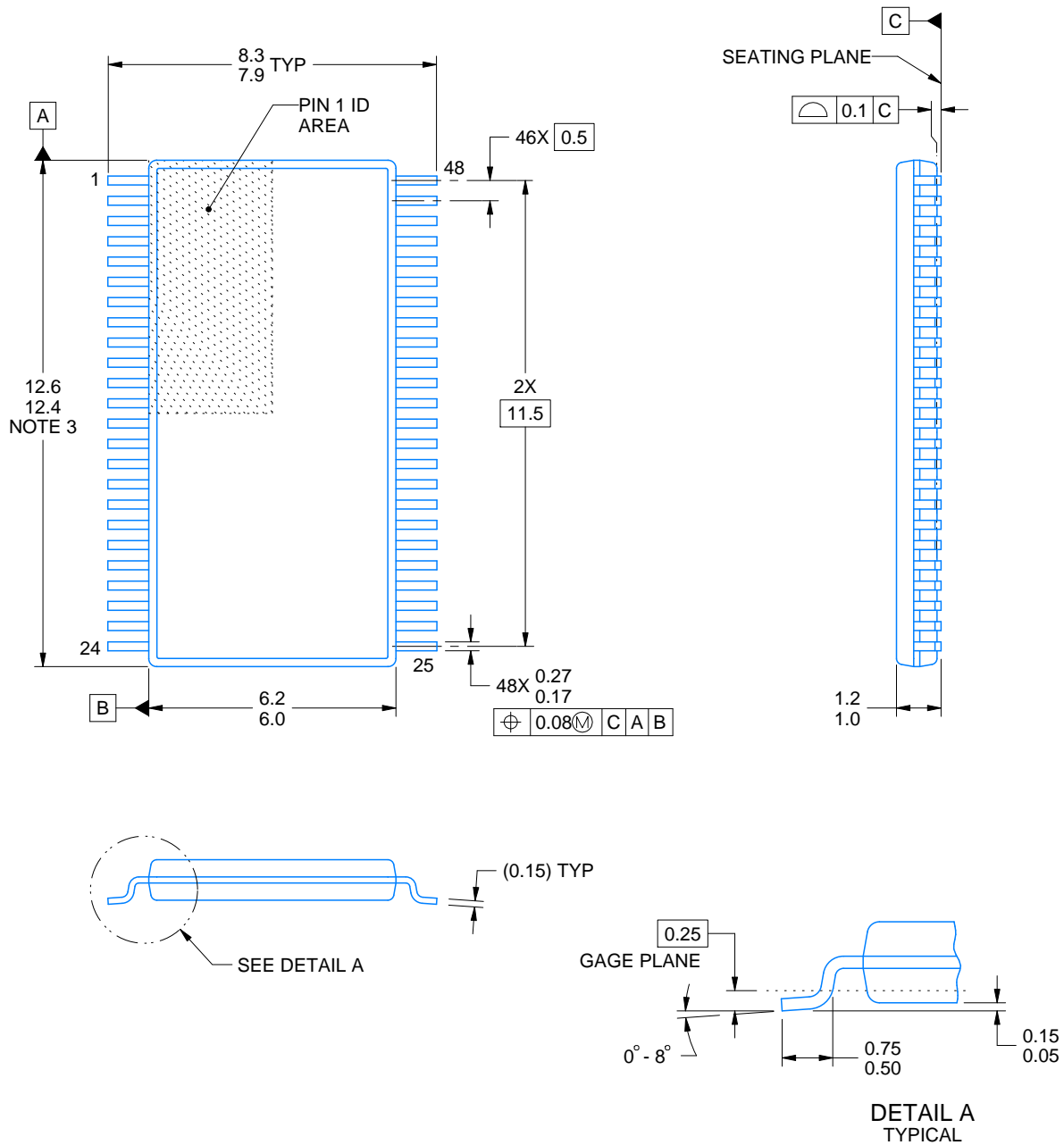
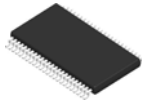
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.





4214859/B 11/2020

## NOTES:

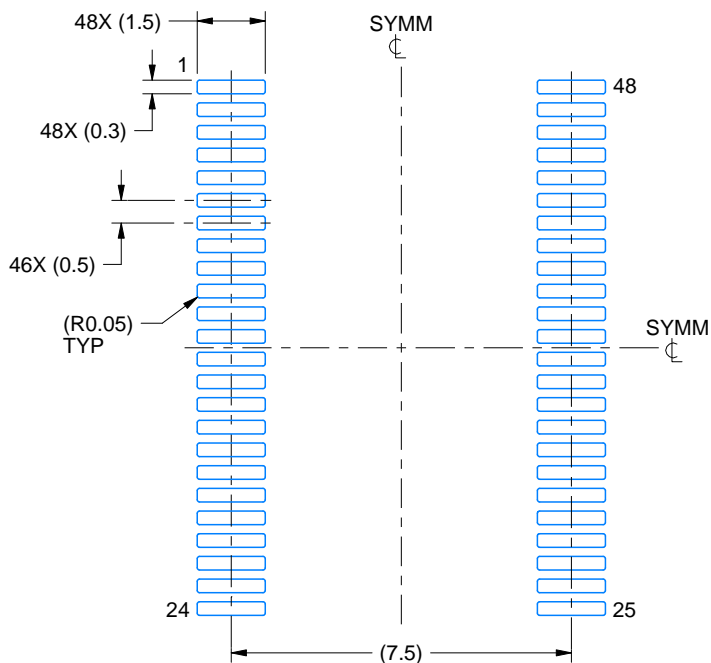
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

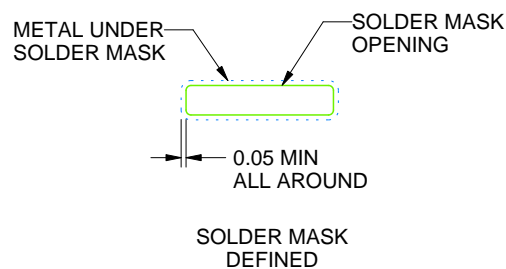
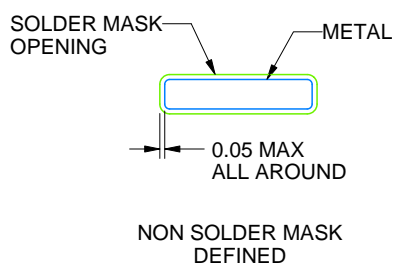
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

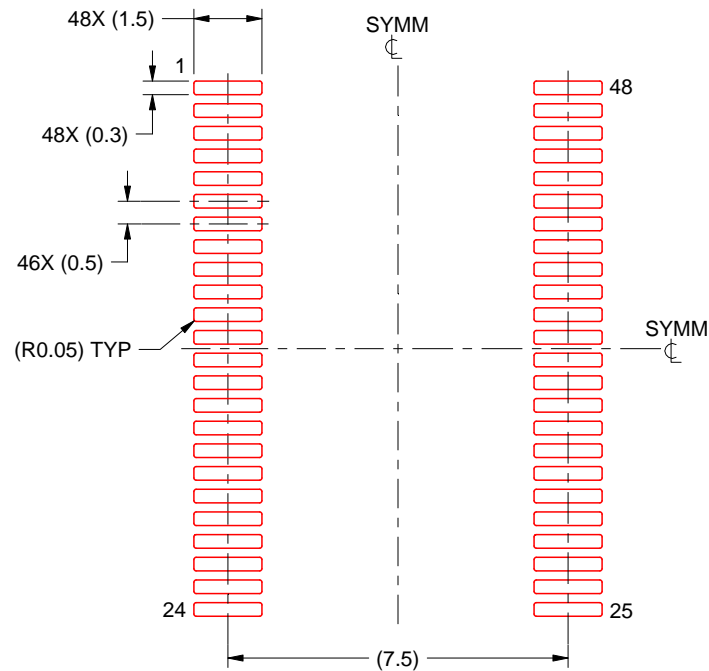
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

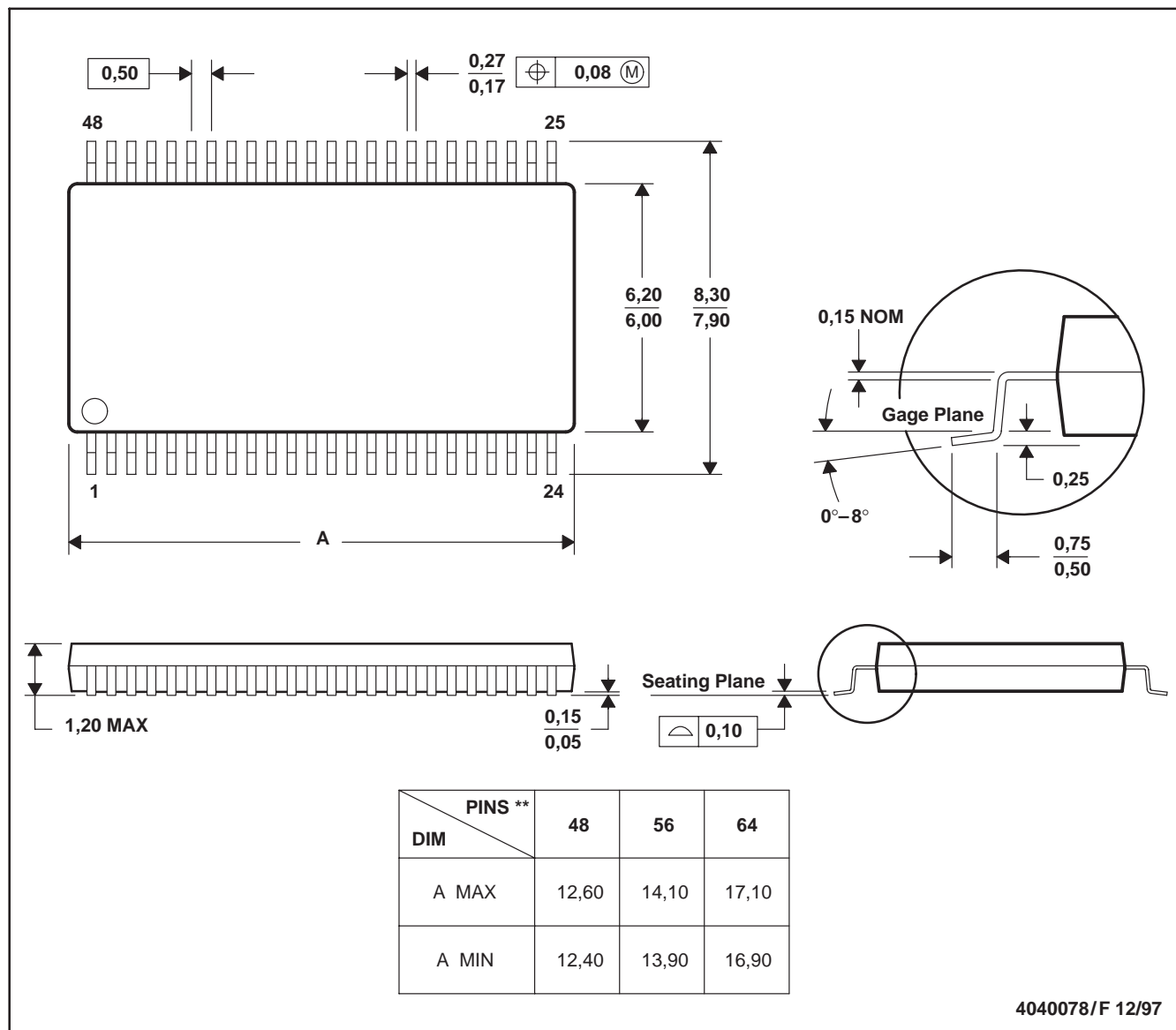
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

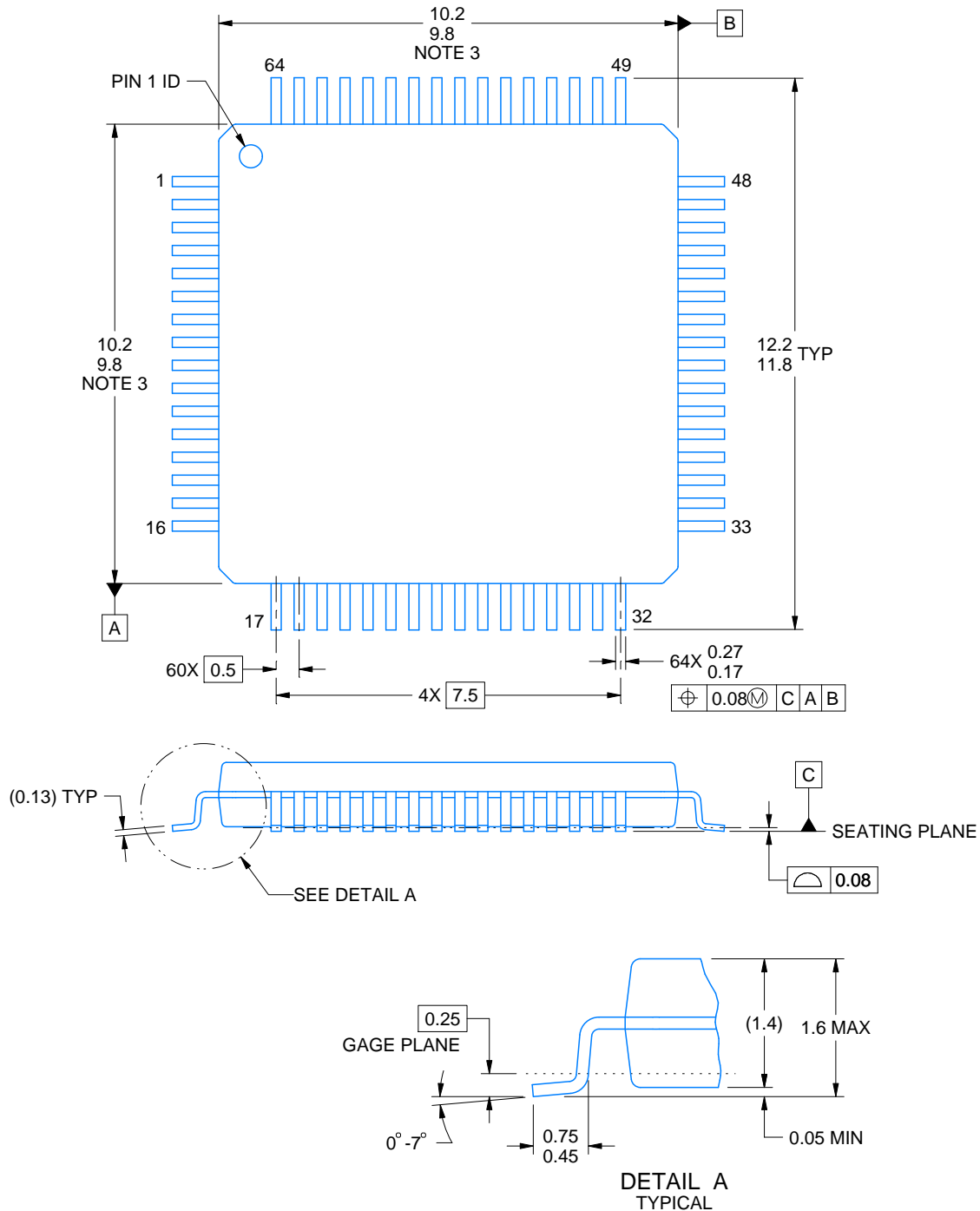
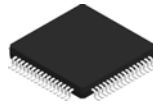
## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



4215162/A 03/2017

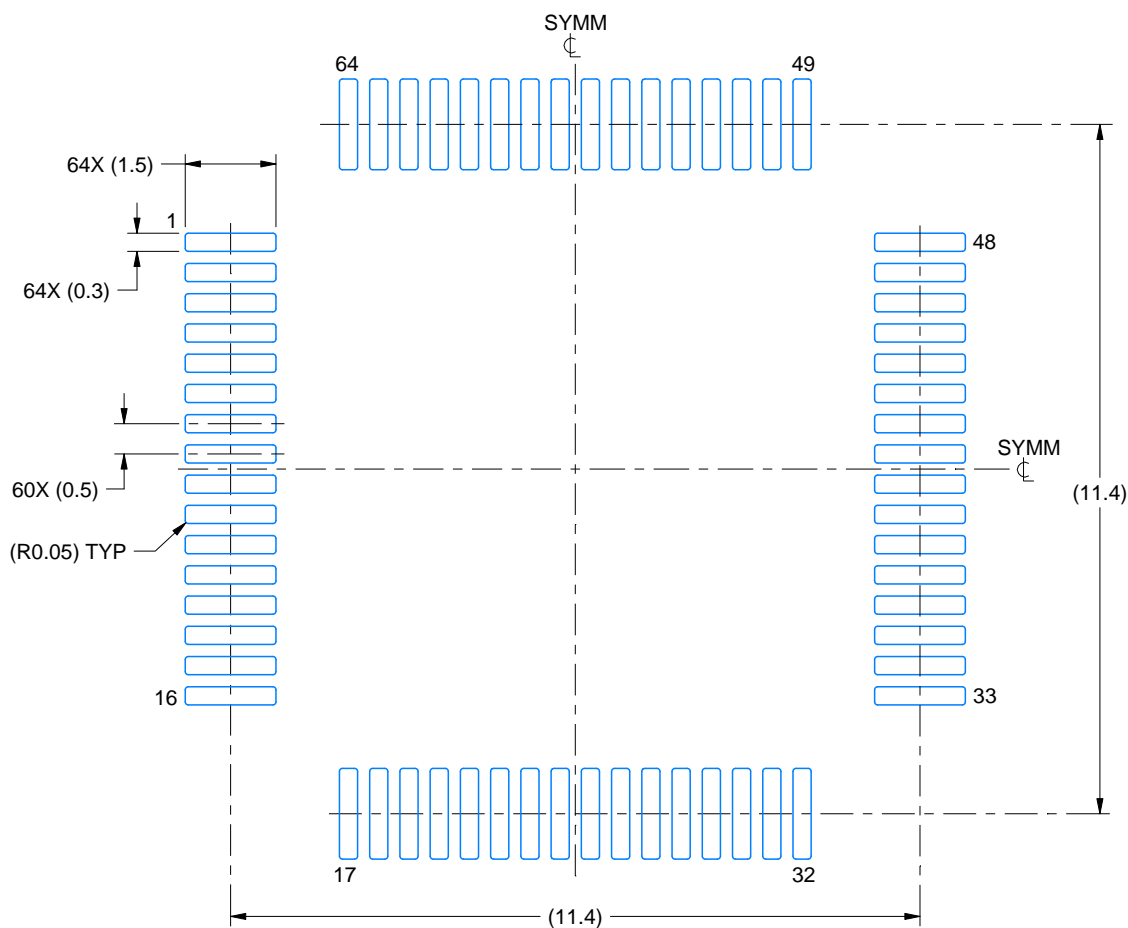
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

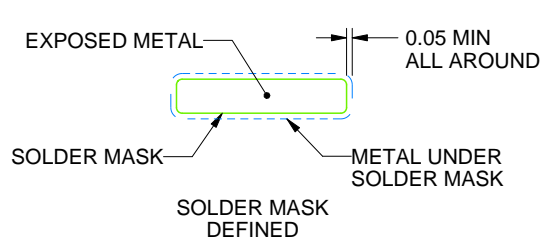
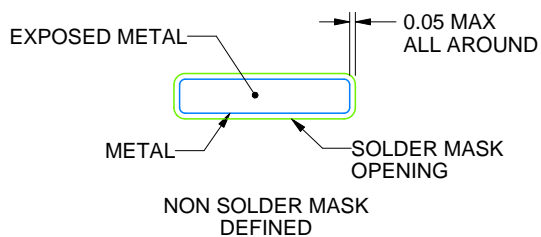
**PM0064A**

**LQFP - 1.6 mm max height**

## PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

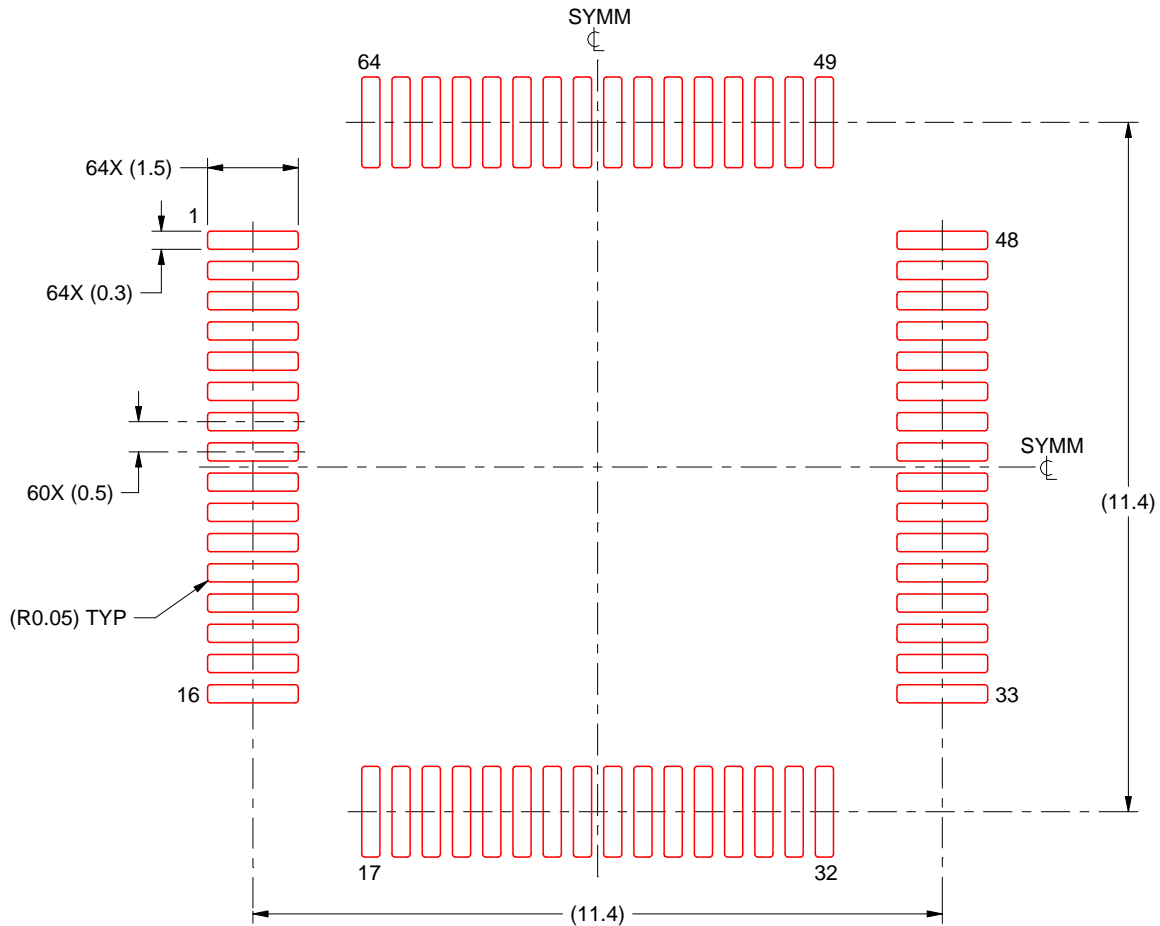
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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