Expanding The Synopsys Primetime Solution With Power Analysis

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Expanding The Synopsys Primetime Solution

"Once again, Synopsys and STMicroelectronics are joining forces to advance timing analysis and signoff," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Expanding our relationship continues the extraordinary success of the PrimeTime and PrimeTime SI solutions, leveraging the more than 10 years of ...

Synopsys Expands Collaboration With STMicroelectronics in ...

The Synopsys PrimeTime static timing analysis solution is the most trusted and advanced timing signoff solution for gate-level designs. It is the standard for gate-level static timing analysis with the capacity and performance for 750+ million instance chips being designed at 10-nm and below.

Overview PrimeTime Suite - Synopsys

Synopsys' PrimeTime static timing analysis tool provides a single, golden, trusted signoff solution for timing, signal integrity, power and variation-aware analysis. It delivers HSPICE® accurate signoff analysis that helps pinpoint problems prior to tapeout thereby reducing risk, ensuring design integrity, and lowering the cost of design.

Static Timing Analysis - PrimeTime - Synopsys

Synopsys today introduced PrimePower, an expanded power analysis solution created to accelerate system-on-chip (SoC) design closure by extending signoff power analysis to drive early design implementation and accurate reliability analysis.

Synopsys Delivers PrimePower Power Analysis to Accelerate ...

Synopsys, Inc. (NASDAQ: SNPS) today announced the availability of its PowerReplay solution to enable early and fast gate-level power analysis with accuracy within 5% of power signoff. Energy efficiency has become a key criterion in complex designs that increasingly need to achieve stricter power targets.

Synopsys: Announces PowerReplay Solution for Early and ...

PrimeTime PX represents a trusted solution, and is an integral part of our design flow from estimations early in the design process to sign-off, contributing to our record of first-time silicon successes.

Synopsys PrimeTime PX Power Analysis Solution Achieves ...

Synopsys 34000-000-S16 PrimeTime: Introduction to Static Timing Analysis Use PrimeTime to perform Static Timing Analysis (STA) on a "Functional Core" prior to Place and Route (P&R).

PrimeTime: Introduction to Static Timing Analysis Workshop

ANSYS and Synopsys to Partner in Accelerating Robust Design Optimization for Next Generation High-Performance Computing, Mobile and Automotive Products. While designers have been using ANSYS and Synopsys tools in combination for years, the integrated solution will enable mutual customers to apply power integrity and reliability signoff technologies earlier in the design flow – empowering them to deliver innovative, high-performance and reliable products faster, while reducing power, area and cost.

ANSYS and Synopsys to Partner in Accelerating Robust ...

Synopsys Delivers PrimePower Power Analysis to Accelerate Robust SoC Design. The new PrimePower solution strengthens the Synopsys Design Platform by not only enabling early RTL-based analysis and optimizations, but also providing a single DNA backbone for power analysis throughout the digital low-power design flow,...

Synopsys Delivers PrimePower Power Analysis to Accelerate ...

"Once again, Synopsys and STMicroelectronics are joining forces to advance timing analysis and sign-off," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Expanding our relationship continues the extraordinary success of the PrimeTime and

PrimeTime SI solutions, leveraging the more than 10 years of ...

Synopsys expands collaboration with STMicroelectronics in ...

• PrimeTime is the Synopsys stand-alone full chip, gate-level static timing analyzer • Widely-adopted in industry and academia, sign-off tools • Controlled by Tool command language (TCL) compatible with DC. Liang Liu, EIT, LTH, Digital IC project and Verification Static Timing Analysis

Digital IC-Project and Verification Static Timing Analysis ...

Synopsys, Inc. SNPS, -0.10% a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced immediate availability of the V1.0 ...

TSMC Certifies Synopsys Digital and Custom Solution for V1 ...

Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced delivery of a comprehensive design implementation solution for TSMC's 16-nanometer (nm) FinFET reference flow.

Synopsys, Inc.: Synopsys Implementation Solution Included ...

Feb. 8, 2018, Synopsys Expands Photonic Design Solution with the Acquisition of PhoeniX Software ARC International [edit] ARC International PLC was the designer of ARC (Argonaut RISC Core) embedded processors, which were widely used in SoC devices for IoT, storage, digital home, mobile, and automotive applications.

Synopsys - Wikipedia

Distributed format enables PrimeTime to annotate each physical segment of the routed netlist (most accurate form of RC back-annotation) C1 C2 R1 C3 R2 C4 R3 U1 U2 U3. . .

STA - Static Timing Analysis - BGU

Synopsys, Inc. SNPS, -1.28% today announced the availability of its PowerReplay solution to enable early and fast gate-level power analysis with accuracy within 5% of power signoff. Energy ...

Synopsys Announces PowerReplay Solution for Early and Fast ...

Synopsys Implementation Solution Included in TSMC 16-nm Reference Flow for FinFET Design MOUNTAIN VIEW, Calif. -- Sept. 23, 2013 -- Synopsys, Inc. (Nasdaq: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced delivery of a comprehensive design implementation ...

Synopsys Implementation Solution Included in TSMC 16-nm ...

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced immediate availability of the V1.0 certified solution for cell-based and custom implementation with the TSMC N16 FinFET process.

TSMC Certifies Synopsys Digital and Custom Solution for V1 ...

Synopsys, Inc. (Nasdaq: SNPS) today announced that its innovative IC Compiler ™ II place-and-route solution with Advanced Fusion technologies has been deployed at Juniper Networks, where it ...

IC Compiler II with Advanced Fusion Technologies Delivers ...

MOUNTAIN VIEW, Calif.—May 13, 2010 —Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that MediaTek Inc., a leading fabless semiconductor company for wireless communications and digital multimedia solutions, has standardised on Synopsys' IC Compiler physical design solution, a key component of the ...

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