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When the parallel load input = 1, the clock pulses go through the AND gate and the data inputs are loaded into the register when the parallel load input = 0, the output of the AND gate remains at 0. 2.10. The buffer gate does not perform logic. It is used for signal amplification of the clock input.

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Set up Karnaugh maps for each output, then develop minimal logic expressions and design the appropriate logic circuits. $X > Y : X \ 1 \ X \ 0 \ Y \ 1 \ Y \ 0 \ 00 \ 01 \ 11 \ 10$ $X = Y : X \ 1 \ X \ 0 \ Y \ 1 \ Y \ 0 \ 00 \ 01 \ 11 \ 10$ $X < Y : X \ 1 \ X \ 0 \ Y \ 1 \ Y \ 0 \ 00 \ 01 \ 11 \ 10$

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