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When the parallel load input = 1, the clock pulses go through the AND gate and the data inputs are loaded into the register when the parallel load input = 0, the output of the AND gate remains at 0.  
2.10. The buffer gate does not perform logic. It is used for signal amplification of the clock input.

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1 int int\_shifts\_are\_arithmetic () 2 { 3 int x = ~0; /\* All 1's \*/ 4 5 return (x >> 1) == x; 6 }  
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