CSE 206 – July 2021

A2

Online on Synchronous Counters

Time: 50 minutes (including upload time) **Full Marks: 12**

Design a synchronous counter with the sequence given below using D Flip-Flops and basic gates. You can only use 74XX series ICs. Failing to adhere to the guidelines and/or make submission in moodle will result in straight ZERO marks.

What Sequence to count:

XXX=The last three digits of your student ID:

- **If XXX%5==0, then 7 – 1 – 3 – 4 – 2 – 0 – 5**
- **If XXX%5==1, then 1 – 0 – 5 – 2 – 6 – 3 – 7**
- **If XXX%5==2, then 2 – 3 – 4 – 6 – 1 – 7 – 5**
- **If XXX%5==3, then 6 – 1 – 7 – 2 – 5 – 3 – 0**
- **If XXX%5==4, then 1 – 6 – 2 – 5 – 3 – 4 – 7**

★ Draw the Transition Table and derive the necessary equations by hand. These should be scanned and converted into a single pdf file.
[Marks: 5]

★ Design the circuit in Logisim using proper IC. Use Edge-Triggered Flip Flops wherever necessary. *[Marks: 5]*

★ *In your Logisim file, clearly mention the sequence mentioned above using a label for facilitating evaluations. For example, like this "**Sequence:** **1 – 0 – 5 – 2 – 6 – 3 – 7**"* [Marks: 2]

Submit the PDF file and the .circ file simulated in Logisim in a single zip file named by your student ID to Moodle.