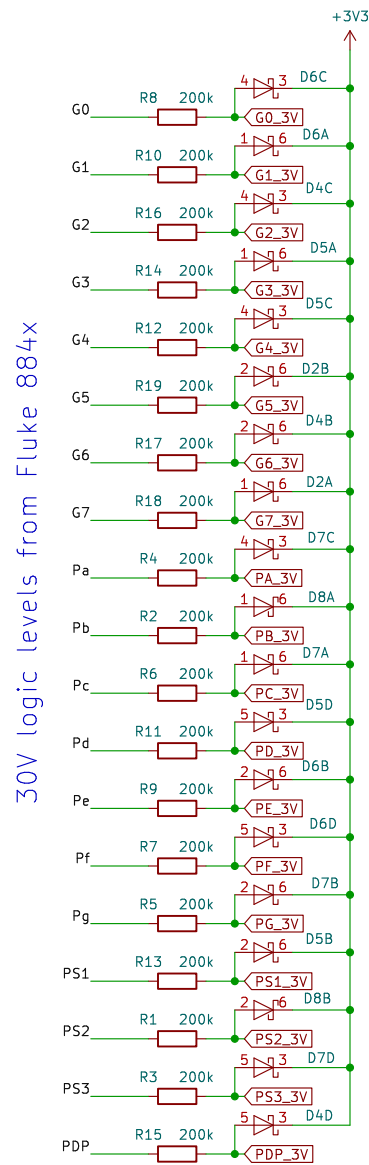



Schematic diagram of the QSPI interface between the J2 connector and the W25Q128JVS memory chip. The J2 connector has pins 1 (USB_BOOT) and 2 (Conn_01x02 GND). The USB_BOOT pin is connected to the QSPI_SS pin of the memory chip through a 1k resistor (R28). The Conn_01x02 GND pin is connected to the GND pin of the memory chip. The memory chip's VCC pin is connected to the 5V supply, and its GND pin is connected to the GND supply. The memory chip's CS pin is connected to the QSPI_SS pin. The memory chip's CLK pin is connected to the QSPI_SCLK pin. The memory chip's DI(100) pin is connected to the QSPI_SD0 pin, and its DO(101) pin is connected to the QSPI_SD1 pin. The memory chip's I02 pin is connected to the QSPI_SD2 pin, and its I03 pin is connected to the QSPI_SD3 pin.



Unused



The diagram shows three unused logic gates. The first is a 4-input OR gate with inputs labeled 4, 3, 2, and 1, and output D8C. The second is a 5-input OR gate with inputs labeled 5, 4, 3, 2, and 1, and output D8D. The third is a 1-input buffer gate with input labeled 1 and output D4A.



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