1. Read: valid bit is 0
   Read Miss:
   1) Cache returns “miss” to processor
   2) Processor will compute instruction addresses, and sends a request to memory to read the appropriate word.
   3) Processor stalls (if it’s main-order processor) at this point
   4) The memory will load the desired line into cache.
   5) Cache adds tag & valid bits & sends desired word to the processor
   6) Processor restart the instruction

2. Read: tags don’t match
   Read Miss:
   1) Cache returns “miss” to processor
   2) Processor will compute instruction addresses, and sends a request to memory to read the appropriate word.
   3) Processor stalls (if it’s main-order processor) at this point
   4) The memory will load the desired line into cache.
   5) Cache adds tag & valid bits & sends desired word to the processor
   6) Processor restart the instruction

3. Write: tags don’t match (write-through and write-allocate)
   Write Miss:
   1) Cache returns ”miss” to processor and write the word with the tag into cache
   2) Processor will compute instruction addresses and sends a request to memory to write the appropriate word into the appropriate address.
   3) Processor stalls (if it’s main-order processor) at this point
   4) Processor restart the instruction

4. Write: tags don’t match (write-through and no-write-allocate)
   5) Cache returns ”miss” to processor and write the word with the tag into cache
   1) Processor will compute instruction addresses and sends a request to memory to write the appropriate word into the appropriate address.
   2) Processor stalls (if it’s main-order processor) at this point
   3) Processor restart the instruction

5. Write: valid bit is 0 (write-back and write-allocate)
   1) Cache returns ”miss” to processor and write the word with the tag into cache
   2) Processor restart the instruction