Lab 4   SRAM Memory Cell Design   ECE334

References:

- Textbook Section
  - 12.2.1 Memory Cell Read/Write Operation

Introduction

In this lab, you will design and simulate an SRAM memory cell using the 0.25um CMOS process and MOSFET models we have used for the previous labs.

Preparation

P1) Design an SRAM memory cell for the 0.25um CMOS process. Determine the dimensions of all 6 transistors in the SRAM cell. For your hand design, you can assume the following conditions:

- Vdd = 2.5V
- Vtn = 0.43 and |Vtp| = 0.62V
- $\mu_n C_{ox} = 88\mu A/V^2$, $\mu_p C_{ox} = 30.67\mu A/V^2$
- Ignore the Body Effect
- Use the minimum channel length of 0.25um for all MOSFETs
- A 1pF load capacitance appears on the bit and bit_b line
- The voltage applied on the bit line (bit or bit_b) during a write operation is precisely 0V or Vdd.

Design notes:

- SRAM cell is symmetrical i.e. N1, N2, P1 are identical to N3, N4, and P2, respectively.

- For **read stability**, the internal node (A or A_b) that is pulling the external bit line (bit or bit_b respectively) LOW should not rise above 0.3V during a read operation. This translates into the following condition $W_{N1 or3} \geq 2.7 W_{N2 or4}$.

- For **write stability**, the internal node (A or A_b) that is being driven LOW should not settle to a value higher than 0.3V during a write operation. This translates into the following condition $W_{N2 or4} \geq 1.2 W_{P1 or2}$.

- The read time is not crucial and so the smallest MOSFETs in the circuit should be made minimum sized (i.e., W= 0.5um for either NMOS or PMOS) in order to minimize the SRAM cell area.

P2) Answer the following design questions:

- 1. Which transistor(s) would you modify in the circuit if you found the read stability condition was violated?
- 2. Which transistor(s) would you modify in the circuit if you found the write stability condition was violated?

P3) Draw a colored stick diagram of your SRAM cell. A sample layout can be found in Figure 11.6a) on the inside book cover, but you are free to explore and create your own layout in order to reduce circuit area. A neat sketch is adequate. Precise dimensions conforming to layout rules are NOT required. You can follow the color scheme used by the book.

P4) Setup your circuit schematic in SUE to simulate the circuit in Figure 1., using the waveforms provided in Figure 2. as your inputs. This simulates a WRITE '1' operation followed by a READ operation. You can use unit-sized inverters for the PRECHARGE and DATA lines.

Hint: the voltage sources named pwl_source in SUE, can help you tailor your input waveforms, as shown in Figure 2.

Laboratory

L1) Use SUE to confirm the design of your SRAM cell. The waveforms shown in Figure 2 simulate a WRITE '1' operation followed by a READ operation. If your design is not working properly, modify your hand design using your answers from P2 to guide you.

If you face convergence problems, you can help HSpice to converge by setting the initial value **(Initial Condition)** stored by the SRAM cell to A='0'. To do this:

Press "t" and click anywhere on the schematic window (You are now in text mode.) Type the following line and press enter:

   ^.   **IC V(A) = 0V**

Another method would be to include the following line to your netlist, after creating it from within SUE.
   ^.   IC V(A) = 0V
where 'A' is the node name for the internal node A in Figure 1. Note that you will need to change the simulation time to 50 nsec. Instructions on how to change the simulation time were given in Lab 3 handout.

L2) Document the simulation results of your working SRAM cell.

- **Measure the read time**, defined as the time from the rising edge of the WORD line to the point where the differential voltage between the bit lines is 200mV as shown in Figure 2.
- Plot the waveforms on the bit lines (bit, bit_b) and internal nodes (A, A_b)

Can you now modify your SRAM cell so that it DOESN'T work?

L3) Change your design so that the read stability condition is violated and the SRAM cell actually switches state during a read operation.
- Plot the waveforms on the bit lines (bit, bit_b) and internal nodes (A, A_b) to document the violation
- Describe how the design has been changed relative to the working design in L2.

L4) Next, modify your design so that the write stability condition is violated and you are no longer able to change the state of the SRAM cell.
- Plot the waveforms on the bit lines (bit, bit_b) and internal nodes (A, A_b) to document the violation
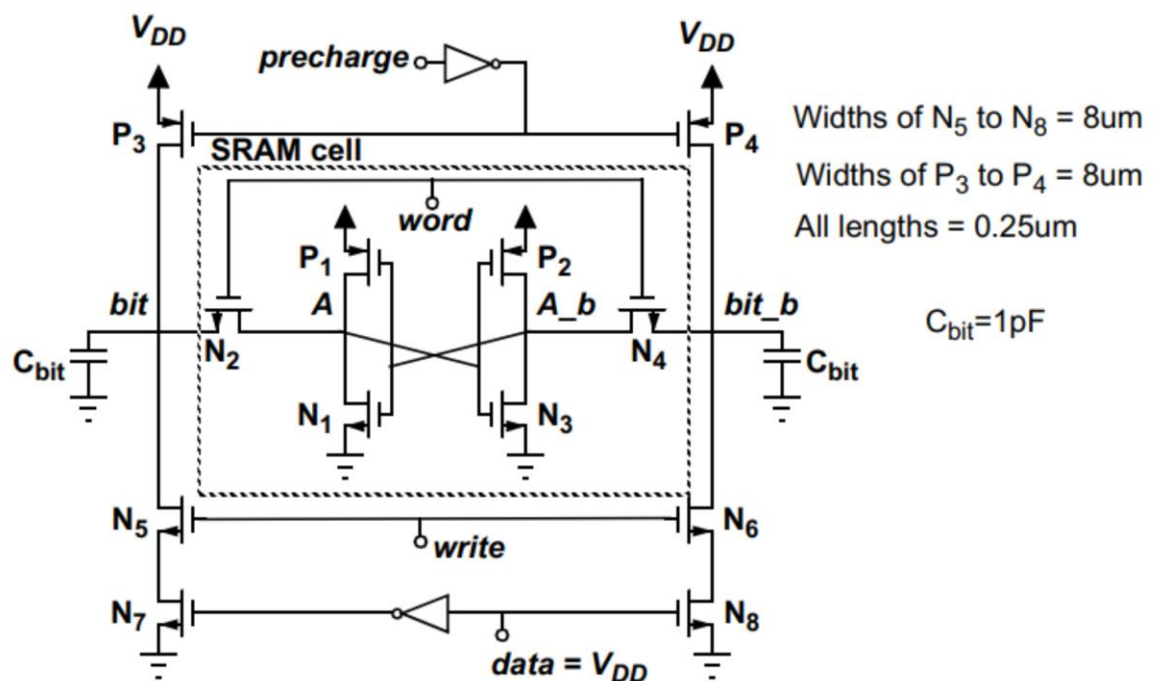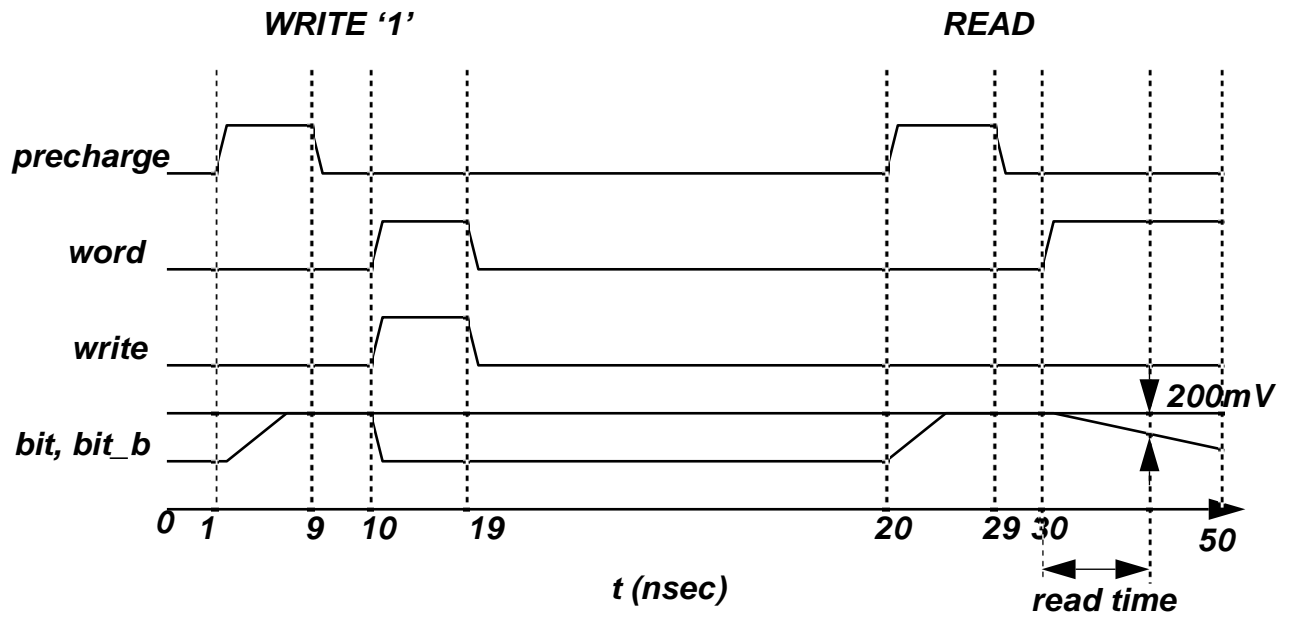- Describe how the design has been changed relative to the working design in L2.

Figure 1: SRAM cell circuit.

Figure 2: Test waveforms