AXI Stream Adapter

Version 1.0

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IP Summary

Introduction

An AXI Stream Adapter IP is a component used in digital systems that converts data width of AXI Stream interfaces. The AXI (Advanced eXtensible Interface) protocol is a widely used standard in the design of high-performance digital systems, particularly in the field of digital signal processing (DSP). AXI Stream is a subset of the AXI protocol, which is optimized for high-speed, unidirectional data transfer. The AXI Stream Adapter IP is typically implemented as a programmable hardware block within a Field Programmable Gate Array (FPGA). This allows designers to easily integrate the AXI Stream Adapter IP into their digital systems, while also customizing its functionality to meet specific requirements. Overall, the AXI Stream Adapter IP is an essential component for high-speed data transfer between different components within a digital system, particularly in the field of DSP.

Features

- AXI Stream one slave and one master interface
- Configurable data width up to 4096 bits
- Supports two modes.i.e. Master Mode or Slave Mode

Overview

AXI Stream Adapter

The AXI Stream Adapter IP core is a part of Raptor Design Suite that enables communication between components with different data interface standards, by translating data from one format to another. The IP core is designed to comply with the AXI Stream specification and can be used in various digital systems. The core can operate in two modes: master mode and slave mode. In master mode, the AXI Stream Adapter IP core acts as the initiator of the data transfer, and in slave mode, it acts as the receiver. The core is configurable to support various data widths.

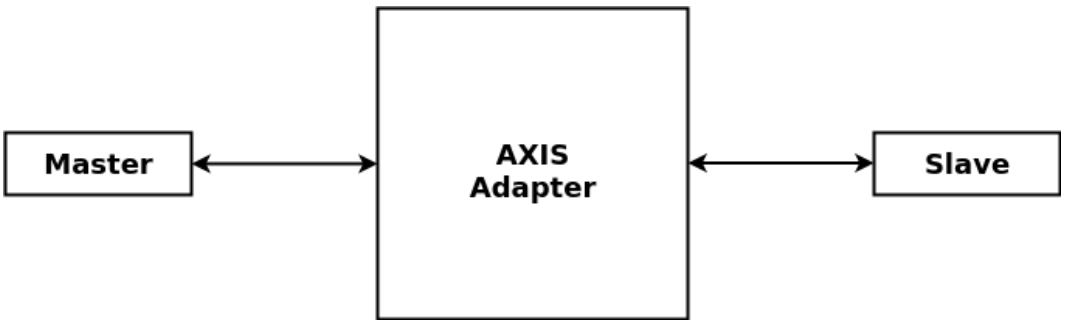

Figure 1: AXI Stream Adapter Block Diagram

IP Specification

Overview

The AXI Stream Adapter IP core typically includes an AXI Stream interface that supports the AXI Stream protocol. It is configurable to support different data widths, ranging from 1 bit to 4096 bits. It can operate in slave mode, where it receives data from the input data stream, or master mode, where it initiates data transfer to the output data stream. It can be customized to support specific system requirements, including setting the data width.

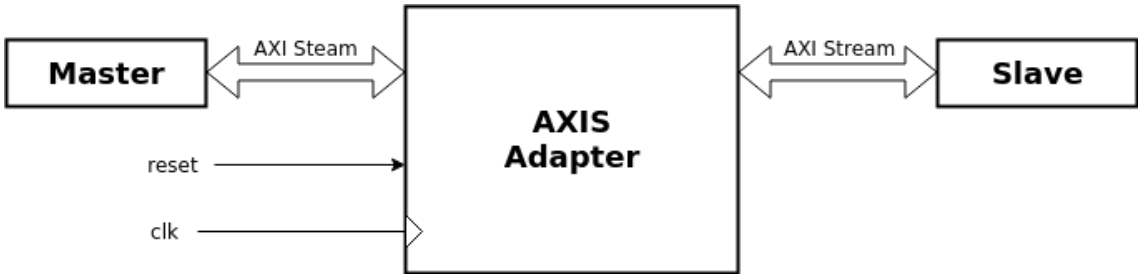

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI Stream Adapter.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI Stream	Verilog	-	CocoTB	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_DATA_WIDTH	1	REGISTERS	33
	M_DATA_WIDTH	1	LUTS	12
	ID_WIDTH	1	-	-
	DEST_WIDTH	1	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_DATA_WIDTH	4096	REGISTERS	9351
	M_DATA_WIDTH	4096	LUTS	4681
	ID_WIDTH	32	-	-
	DEST_WIDTH	32	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI Stream Adapter.

Signal Name	Input/Output	Description
clk	Input	Clock Signal for synchronization
rst	Input	Active Low Reset Signal
AXI Stream Input		
s_axi_tdata	Input	Data Port
s_axis_tkeep	Input	Valid Bytes in Data
s_axis_tvalid	Input	Valid Signal
s_axis_tready	Output	Ready Signal
s_axis_tlast	Input	Last transacton Signal
s_axis_tid	Input	ID Signal
s_axis_tdest	Input	DEST Signal
s_axis_tuser	Input	USER Signal
AXI Stream Output		
m_axi_tdata	Output	Data Port
m_axis_tkeep	Output	Valid Bytes in Data
m_axis_tvalid	Output	Valid Signal
m_axis_tready	Input	Ready Signal
m_axis_tlast	Output	Last transacton Signal
m_axis_tid	Output	ID Signal
m_axis_tdest	Output	DEST Signal
m_axis_tuser	Output	USER Signal

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI Stream Adapter.

Parameter	Values	Default Value	Description
S_DATA_WIDTH	1 - 4096	8	Data Width of Slave Interface
M_DATA_WIDTH	1 - 4096	8	Data Width of Master Interface
ID_WIDTH	1 - 32	8	ID field of AXI Stream
DEST_WIDTH	1 - 32	8	DEST field of AXI Stream
USER_WIDTH	1 - 4096	1	USER field of AXI Stream
ID_EN	True/False	True	ID enable of AXI Stream
DEST_EN	True/False	True	DEST enable of AXI Stream
USER_EN	True/False	True	USER enable of AXI Stream

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI Stream Adapter IP core is a part of the Raptor Design Suite Software. A customized IP can be generated from the Raptor's IP configuration window as shown in figure 3.

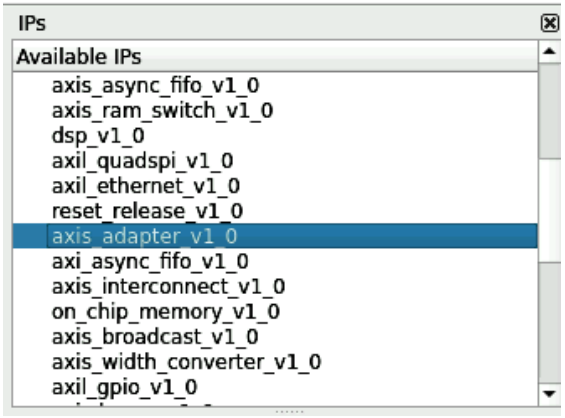

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI Stream Adapter can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

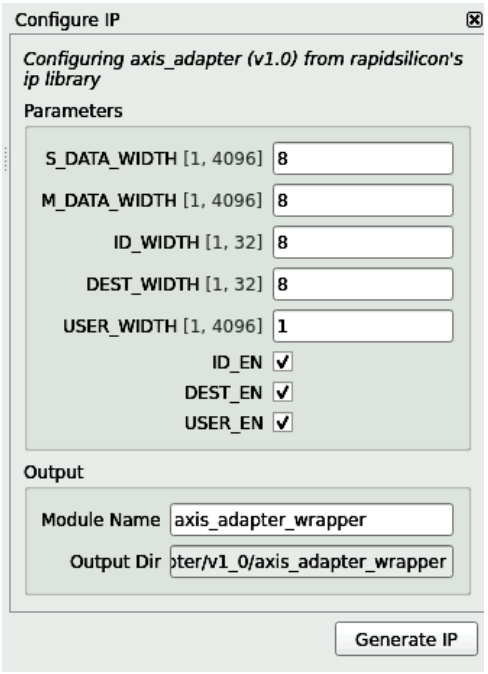

Figure 4: IP Configuration

Test Bench

Test for AXI Stream Adapter

The testbench attached with AXI Stream Adapter is CocoTB based verification environment. The input data is generated using a test data generator module. The input data is written to the input data buffer of the IP core and the output data is read from the output data buffer of the IP core. The output data is compared with the expected output data to verify the correctness of the IP core's operation. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
May 5, 2023	1.0	Initial version AXI Stream Adapter User Guide