AXI RAM
(Beta Release)

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IP Summary

Introduction

The AXI RAM IP Core is a configurable IP block designed for use in FPGA and SoC designs. It provides a simple, high-performance memory interface that supports the AMBA AXI4 protocol, making it easy to integrate with other AXI-compliant IP cores.It can be configured to support a range of memory sizes and data widths. It provides a flexible and efficient solution for integrating FPGA embedded block RAM into the user designs, with a simple and standardized interface that facilitates system-level integration.

Features

- AXI4 (memory mapped) slave interface
- Configurable data width 8, 16, 32, 64 bits
- Supports memory size up to 512 MBytes.
- Compatible with AXI4 Interconnect

Overview

AXI RAM

The AXI RAM IP Core provides a simple and efficient memory interface that supports the widely used AMBA AXI4 protocol. This allows for easy integration with other AXI4-compliant IP cores, simplifying system-level design and verification. It can be customized to support a range of memory sizes and data widths, making it flexible and adaptable to different design requirements. This allows designers to optimize the use of FPGA resources and minimize the cost and complexity of the overall system.

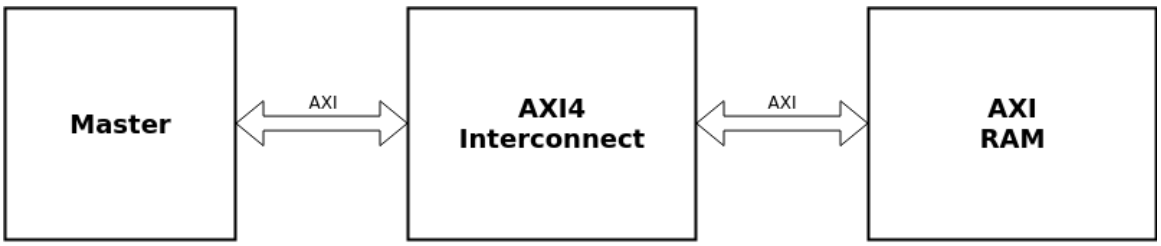

Figure 1: AXI RAM Block Diagram

IP Specification

The AXI RAM IP Core is a simple memory component that supports the ARM Advanced eXtensible Interface (AXI) protocol. It provides a configurable memory block with read and write interfaces that support multiple outstanding transactions. It has configurable memory size and width. This IP Core supports both read and write operations. Read transaction return the data stored in the memory at specific address while write transaction store the data provided at the specific address. It provides a configuration interface to allow user to configure memory size, width and address range. It has a single clock domain and reset signal to initialize the memory to a known state.

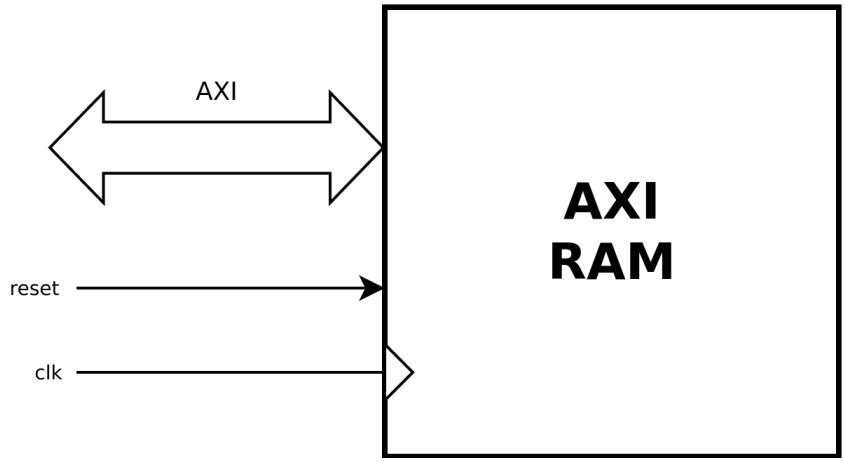

Figure 2: Top Module

Standards

The AXI4 Slave interface is compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXI RAM.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Cocotb	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	8	BRAMS	1
	ADDR_WIDTH	8	REGISTERS	66
	ID_WIDTH	1	LUTS	75
	PIP_OUT	False	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	64	BRAMS	16
	ADDR_WIDTH	16	REGISTERS	256
	ID_WIDTH	8	LUTS	177
	PIP_OUT	True	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI RAM.

Signal Name	I/O	Description
clk	I	Clock Signal of RAM
rst	I	Active High Synchronous Reset Signal
Write Address Channel		
s_axi_awid	I	Write address ID
s_axi_awaddr	I	Write address
s_axi_awlen	I	Burst length
s_axi_awsize	I	Burst size
s_axi_awburst	I	Burst type
s_axi_awlock	I	Lock type
s_axi_awcache	I	Memory type
s_axi_awprot	I	Protection type
s_axi_awvalid	I	Write address valid
s_axi_awready	O	Write address ready
Write Data Channel		
s_axi_wdata	I	Write data
s_axi_wstrb	I	Write strobe
s_axi_wlast	I	Write last
s_axi_wvalid	I	Write valid
s_axi_wready	O	Write ready
Write Response Channel		
s_axi_bid	O	Response ID tag
s_axi_bresp	O	Write response
s_axi_bvalid	O	Write response valid
s_axi_bready	I	Write response ready
Read Address Channel		
s_axi_arid	I	Read address ID
s_axi_araddr	I	Read address
s_axi_arlen	I	Burst length
s_axi_arsize	I	Burst size
s_axi_arburst	I	Burst type
s_axi_arlock	I	Lock type
s_axi_arcache	I	Memory type
s_axi_arprot	I	Protection type
s_axi_arvalid	I	Read address valid
s_axi_arready	O	Read address ready
Read Data Channel		
s_axi_rid	O	Read ID tag
s_axi_rdata	O	Read data
s_axi_rresp	O	Read response

Signal Name	I/O	Description
s_axi_rlast	O	Read last
s_axi_rvalid	O	Read valid
s_axi_rready	I	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI RAM.

Parameter	Values	Default Value	Description
DATA_WIDTH	8, 16, 32, 64	32	Data Width of RAM
ADDR_WIDTH	8,16	16	Address Width of RAM
ID_WIDTH	1-8	8	ID field of RAM
PIP_OUT	True/False	False	Piplelined Output

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI RAM IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in figure 3.

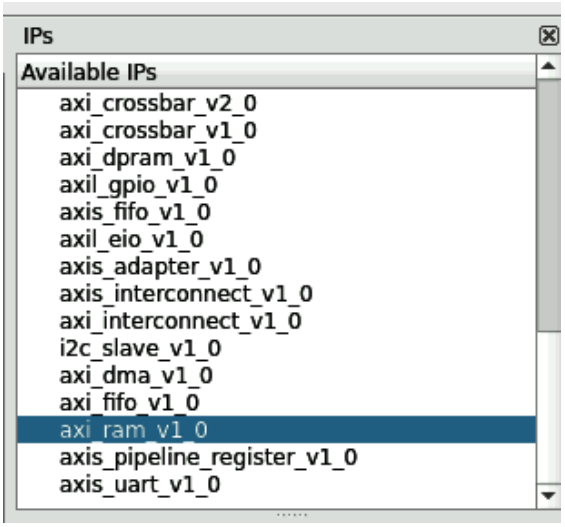

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI RAM can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in Figure 4. In Figure 4, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

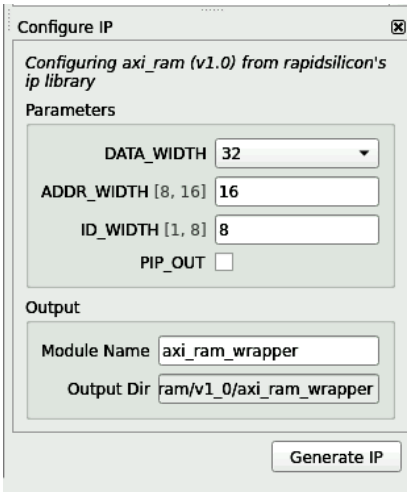

Figure 4: IP Configuration

Test Bench

The AXI RAM IP is provided with a testbench which is based upon Cocotb verification environment. In this test, multiple read/write transactions are performed on memory. The input data is generated using a test data generator module. The output data is compared with the expected output data to verify the correctness of the IP core's operation. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
May 10, 2023	0.1	Initial version AXI RAM User Guide