Reset Release IP V1.0

IP User Guide(Beta Release)

February 2, 2023

RapidSilicon

Contents

Overview

Reset Release IP

Reset Release is added as a processor reset release IP in IP Catalog. It is designed to generate customized resets for a processor based SoC, namely processor, peripherals, buses and interconnects. This offers user access to parameterize the system resets as per his feature needs.

Figure 1. Reset Release IP Block

Features:

- Asynchronous external reset
- Parameterizable pulse width of input resets
- Locked Input
- Reset generation on power up
- Parameterized active-Low reset signal generation for peripherals and interconnects

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IP Specification

Overview

Reset Release IP is a soft IP that offers reset handling mechanism for a processor based system. It generates output resets based upon external resets and lock.

Core Description

The reset release Core has 4 input and 5 output signals. User can configure the core using 5 parameters controlling the outputs. **EXTERNAL RESET WIDTH** tells the window of external reset, number of active Low Peripheral Resets,**PERIPHERAL ARESETN**, number of Interconnects **INTERCONNECTS**, number of bus resets **BUS RESET**, number of Peripheral Resets Active High **PERIPHERAL RESET**.
The reset becomes active six or seven clocks after the input is activated and remains active for five clocks. After ext_reset is inactive for five clocks, the process of exiting the reset begins. If, during this process, ext_reset becomes active for five or more clocks, all outputs will become active again. The External Reset Active Polarity is used to set the logic level that triggers a reset when ext_reset is high on a rising edge of the clock. The Auxiliary Reset Active Polarity is used to set the logic level that triggers a reset when aux_reset is low. The No. of Bus Reset (active-High) and No. of Interconnect Reset (active-Low) are used to generate additional bus_struct_reset and Interconnect Structure Reset signals, which assist with signal loading and routing.

Output reset sequence

1. Interconnects and Bridges(Bus Structures) come out of reset first.
2. After 12 clock cycles Peripherals come out of reset.
3. CPU comes out of reset after 12 more cycles of the peripherals.

IP Support Details

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4-lite	Verilog	-	<verilog	-	-	Raptor	Raptor	Raptor

Resource Utilization

Please note that the utilization and timing figures provided in this section for the Processor System Reset IP core should be considered as estimates, as they are based on its usage in conjunction with other design modules in the FPGA. Once integrated with other designs in the system, the FPGA resource utilization and core timing may differ from the reported results.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	EXT_RESET_WIDTH	5	LUT	31
	PERIPHERAL_ARESETN	1	Registers	19
	INTERCONNETS	1	BRAM	0
	BUS_RESET	1	DSP	0
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	EXT_RESET_WIDTH	10	LUT	31
	PERIPHERAL_ARESETN	10	Registers	19
	INTERCONNETS	10	BRAM	0
	BUS_RESET	10	DSP	0

Ports

Table 2 lists the top interface ports of the Reset Release Core.

Signal Name	I/O	Description
slow_clk	I	Slowest clock of the system
ext_rst	I	External reset of the system
cpu_dbg_rst	I	Processor debug reset
pll_lock	I	Pll Lock
cpu_rst	O	Processor reset generated by IP
periph_aresetn	O	RESETNs for system peripherals
interconnect_aresetn	O	Resets generated for the interconnects used in the system
bus_reset	O	Resets for the buses
periph_reset	O	Resets for system peripherals

Reset Release Interface

Parameters

Table 3 lists the parameters of the Reset Release Core.

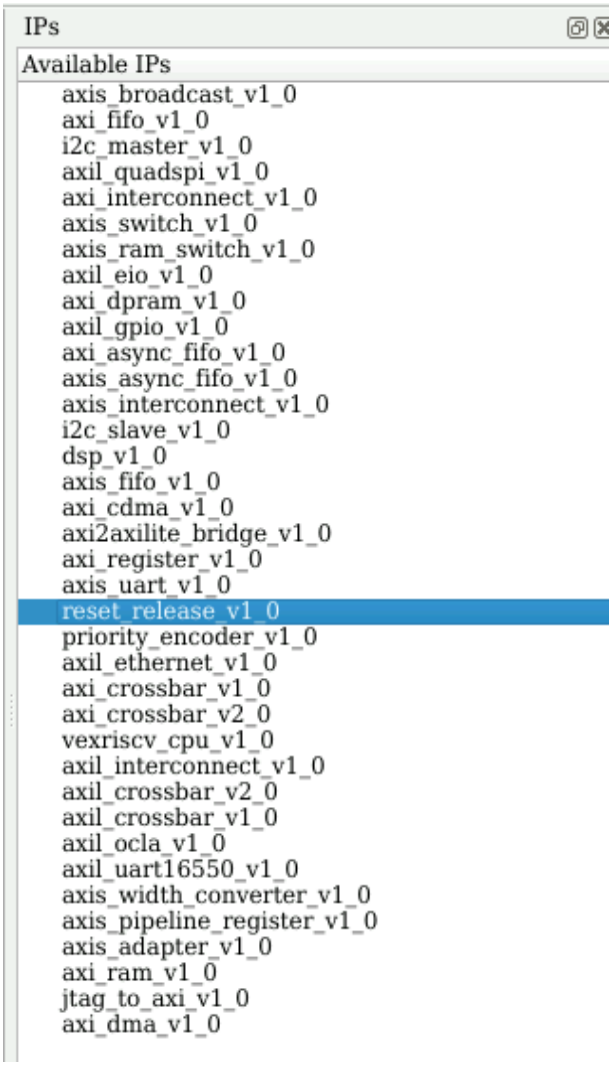
Parameter	Values	Default Value	Description
EXTERNAL RESET WIDTH	4-10	5	External reset window.
PERIPHERAL ARESETN	1-10	1	Number of peripheral resets N.
INTERCONNECTS	1-10	1	Number of Interconnects.
BUS RESET	1-10	1	Number of bus resets.
PERIPHERAL RESET	1-10	1	Probe width in case of value compare mode

Parameters

Design Flow

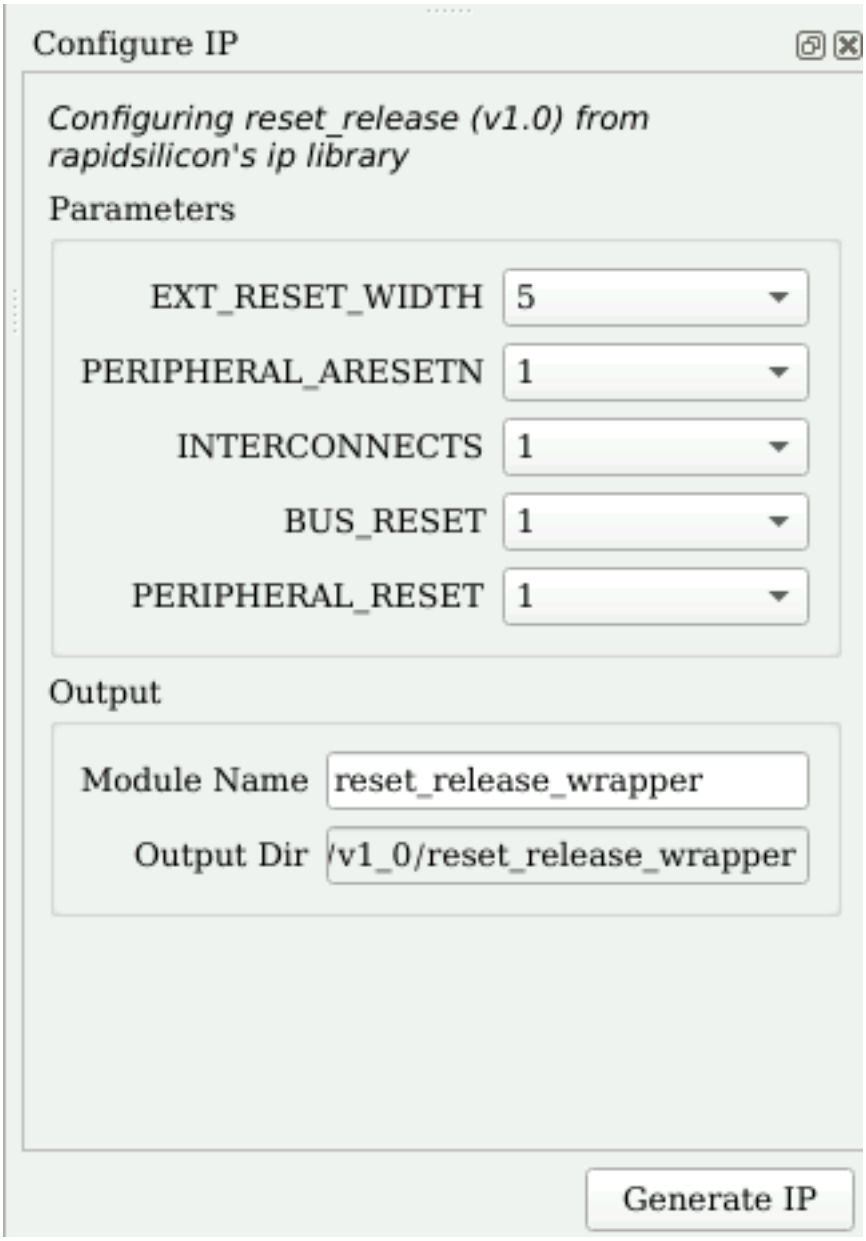
IP Customization and Generation

OCLA IP core is a part of the Raptor Design Suite Software. A customized ocla can be generated from the Raptor's IP configurator window.



IP list

Parameters Customization: From the IP configuration window, the parameters of the OCLA can be configured and OCLA features can be enabled for generating a customized OCLA IP core that suits the user application requirment.

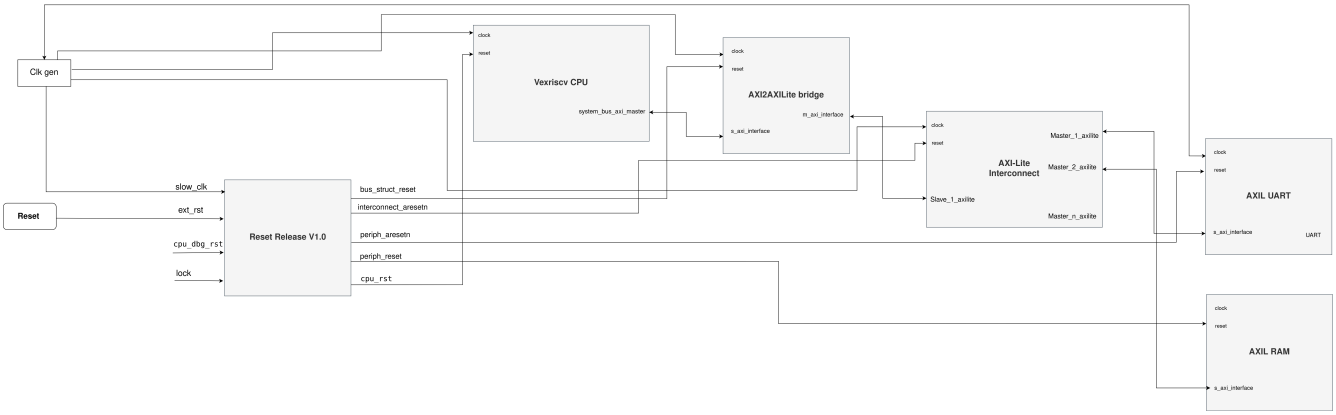


IP Configuration

Example Design

Overview

Reset release IP is an integral part of a processor based SoC. Below shows an example design employing the reset release IP. The reset release IP takes its input from external reset and/or a clock generator. The cpu_reset is fed to Vexriscv cpu, bus_struct_reset is fed to the AXI2AXILite bridge, interconnect_aresetn is fed to the AXILite Interconnect and peripheral resets are fed to AXIL_UART and AXIL_RAM.



Example design employing Reset Realease IP

Synthesis and PnR

Raptor Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post- synthesis and post-route and place netlists can be viewed and analyzed from within the Raptor. The generated bitstream can then be uploaded on an FPGA device to be utilized in hardware application.

Test Bench

The IP package hosts a simple Verilog based test bench that validates design functionality. It can be simulated using Iverilog, Verilator or other simulators.

Revision History

Date	Version	Revisions
February 2, 2023	0.01	Initial version Reset Release IP User Guide