AXI RAM

Version 1.0

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Contents

IP Summary

Introduction

The AXI RAM IP Core is a configurable IP block designed for use in FPGA and SoC designs. It provides a simple, high-performance memory interface that supports the AMBA AXI4 protocol, making it easy to integrate with other AXI-compliant IP cores.It can be configured to support a range of memory sizes and data widths. It provides a flexible and efficient solution for integrating memory into FPGA and SoC designs, with a simple and standardized interface that facilitates system-level integration.

Features

- AXI4 (memory mapped) slave interface
- Configurable data width 8, 16, 32, 64 bits
- Supports memory size up to 512 MBytes.
- Compatible with AXI4 Interconnect

Overview

AXI RAM

The AXI RAM IP Core provides a simple and efficient memory interface that supports the widely used AMBA AXI4 protocol. This allows for easy integration with other AXI4-compliant IP cores, simplifying system-level design and verification. It can be customized to support a range of memory sizes and data widths, making it flexible and adaptable to different design requirements. This allows designers to optimize the use of FPGA resources and minimize the cost and complexity of the overall system.

Figure 1: AXI RAM Block Diagram

IP Specification

Overview

The AXI RAM IP Core is a simple memory component that supports the ARM Advanced eXtensible Interface (AXI) protocol. It provides a configurable memory block with read and write interfaces that support multiple outstanding transactions. It has configurable memory size and width. This IP Core supports both read and write operations. Read transaction return the data stored in the memory at specific address while write transaction store the data provided at the specific address. It provides a configuration interface to allow user to configure memory size, width and address range. It has a single clock domain and reset signal to initialize the memory to a known state.

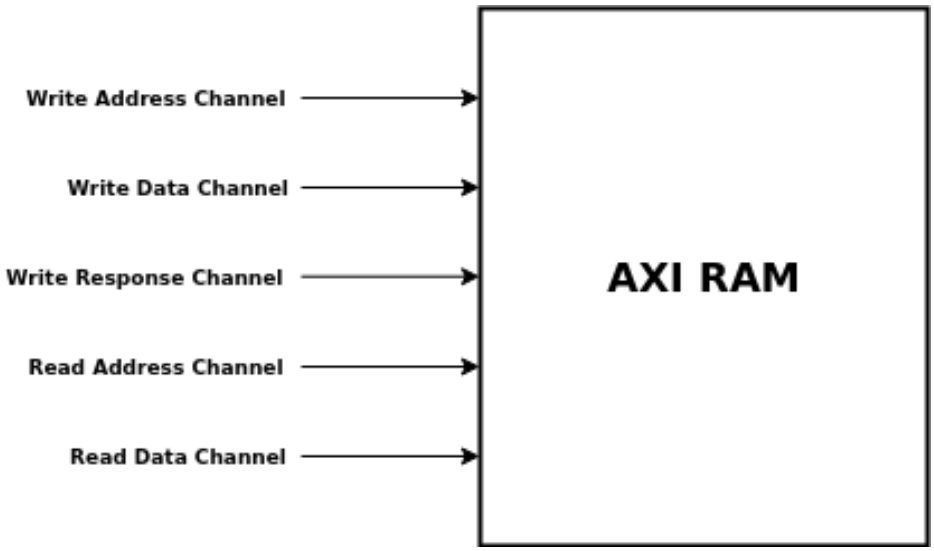

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI RAM.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Verilog	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	8	RAM36K	1
	ADDR_WIDTH	8	REGISTERS	94
	ID_WIDTH	8	-	-
	PIP_OUT	False	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	64	RAM36K	16
	ADDR_WIDTH	16	REGISTERS	256
	ID_WIDTH	8	-	-
	PIP_OUT	True	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI RAM.

Signal Name	Input/Output	Description
clk	Input	Clock Signal for synchronization
rst	Input	Active Low Reset Signal
Write Address Channel		
awid	Input	Write address ID
awaddr	Input	Write address
awlen	Input	Burst length
awsize	Input	Burst size
awburst	Input	Burst type
awlock	Input	Lock type
awcache	Input	Memory type
awprot	Input	Protection type
awvalid	Input	Write address valid
awready	Output	Write address ready
Write Data Channel		
wdata	Input	Write data
wstrb	Input	Write strobe
wlast	Input	Write last
wvalid	Input	Write valid
wready	Output	Write ready
Write Response Channel		
bid	Output	Response ID tag
bresp	Output	Write response
bvalid	Output	Write response valid
bready	Input	Write response ready
Read Address Channel		
arid	Input	Read address ID
araddr	Input	Read address

Signal Name	Input/Output	Description
arlen	Input	Burst length
arsize	Input	Burst size
arburst	Input	Burst type
arlock	Input	Lock type
arcache	Input	Memory type
arprot	Input	Protection type
arvalid	Input	Read address valid
arready	Output	Read address ready
Read Data Channel		
rid	Output	Read ID tag
rdata	Output	Read data
rresp	Output	Read response
rlast	Output	Read last
rvalid	Output	Read valid
rready	Input	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI RAM.

Parameter	Values	Default Value	Description
DATA_WIDTH	8, 16, 32, 64	32	Data Width of RAM
ADDR_WIDTH	8,16	16	Address Width of RAM
ID_WIDTH	1-8	8	ID field of RAM
PIP_OUT	True/False	False	Piplelined Output

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI RAM IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in figure 3.

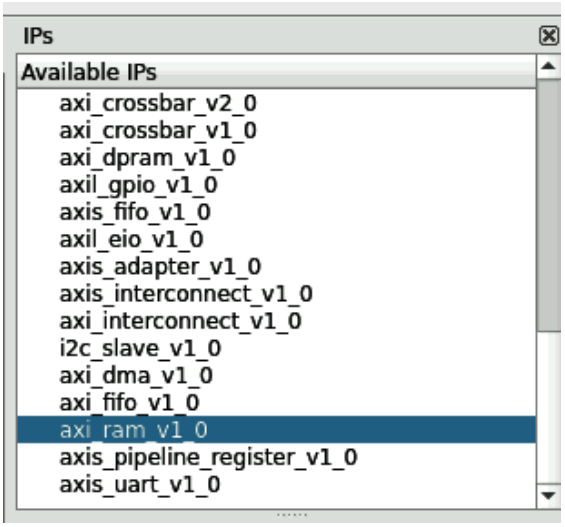

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI RAM can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

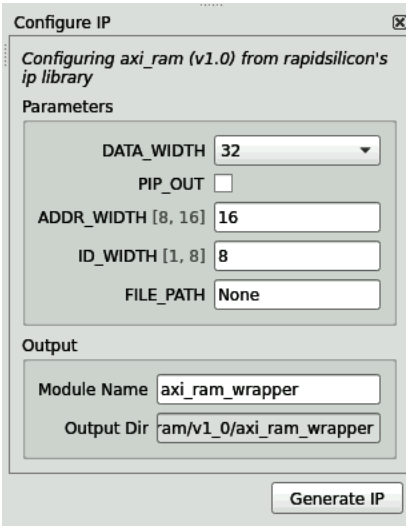

Figure 4: IP Configuration

Test Bench

Test for AXI RAM

The testbench attached with AXI RAM is CocoTB based verification environment. In this test, multiple read/ write tractions are performed by a master IP. The stimulus is generated by environment and test vectors are applied to the design. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
April 26, 2023	1.0	Initial version AXI RAM User Guide