



# **On Chip Memory Generator (Beta Release)**

Version 0.1

November 20, 2023

## Copyright

Copyright © 2021 Rapid Silicon. All rights reserved. This document may not, in whole or part, be reproduced, modified, distributed, or publicly displayed without prior written consent from Rapid Silicon ("Rapid Silicon").

## Trademarks

All Rapid Silicon trademarks are as listed at [www.rapidsilicon.com](http://www.rapidsilicon.com). Synopsys and Synplify Pro are trademarks of Synopsys, Inc. Aldec and Active-HDL are trademarks of Aldec, Inc. Modelsim and Questa are trademarks or registered trademarks of Siemens Industry Software Inc. or its subsidiaries in the United States or other countries. All other trademarks are the property of their respective owners.

## Disclaimers

NO WARRANTIES: THE INFORMATION PROVIDED IN THIS DOCUMENT IS "AS IS" WITHOUT ANY EXPRESS OR IMPLIED WARRANTY OF ANY KIND INCLUDING WARRANTIES OF ACCURACY, COMPLETENESS, MERCHANTABILITY, NONINFRINGEMENT OF INTELLECTUAL PROPERTY, OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL RAPID SILICON OR ITS SUPPLIERS BE LIABLE FOR ANY DAMAGES WHATSOEVER (WHETHER DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL, INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OF OR INABILITY TO USE THE INFORMATION PROVIDED IN THIS DOCUMENT, EVEN IF RAPID SILICON HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. BECAUSE SOME JURISDICTIONS PROHIBIT THE EXCLUSION OR LIMITATION OF CERTAIN LIABILITY, SOME OF THE ABOVE LIMITATIONS MAY NOT APPLY TO YOU.

Rapid Silicon may make changes to these materials, specifications, or information, or to the products described herein, at any time without notice. Rapid Silicon makes no commitment to update this documentation. Rapid Silicon reserves the right to discontinue any product or service without notice and assumes no obligation to correct any errors contained herein or to advise any user of this document of any correction if such be made. Rapid Silicon recommends its customers obtain the latest version of the relevant information to establish that the information being relied upon is current and before ordering any products.

# Contents

<b>IP Summary</b>	<b>3</b>
Introduction . . . . .	3
Features . . . . .	3
<b>Overview</b>	<b>4</b>
On Chip Memory Generator . . . . .	4
<b>IP Specification</b>	<b>5</b>
Memory Types . . . . .	6
Common Clock Versus Uncommon Clock . . . . .	7
Block RAM Versus Distributed RAM . . . . .	8
Memory Initialization . . . . .	9
IP Support Details . . . . .	10
Resource Utilization . . . . .	10
Port List . . . . .	11
Parameters . . . . .	11
<b>Design Flow</b>	<b>12</b>
IP Customization and Generation . . . . .	12
Parameters Customization . . . . .	13
<b>Test Bench</b>	<b>14</b>
<b>Revision History</b>	<b>15</b>

# IP Summary

## Introduction

The On Chip Memory IP Core is a pre-designed and pre-verified memory block that can be easily integrated into FPGA and ASIC designs. It is based on the Block Random Access Memory (BRAM) technology and provides a large amount of memory resources for storing data that is frequently accessed or changed. The On Chip Memory IP Core is customizable in terms of data width and depth, allowing designers to choose the best option for their specific design requirements.

## Features

- On Chip Memory can be configured as Single Port RAM, Simple Dual Port RAM or True Dual Port RAM.
- Support to have multiple read and write ports, allowing multiple operations to occur simultaneously.
- Support configurable width and depth at design time, allowing for flexibility in memory size.
- Support independent clocking on each Port.
- Support to access 1, 2, 4, 8, 9, 16, 18, 32, 36 bit wide memory.
- Support same read/write widths.
- Support mapping feature on Block RAM or Distributed RAM.
- Support memory initialization through file.

# Overview

## On Chip Memory Generator

On Chip Memory Generator is an IP Core that can generate the RTL (register-transfer level) code for on-chip memory components. This generator can be used to create custom memory components with specific parameters, such as size, bit-width, and number of ports, without the need for manual RTL coding. The Figure 1 shows the block diagram of On Chip Memory Generator.

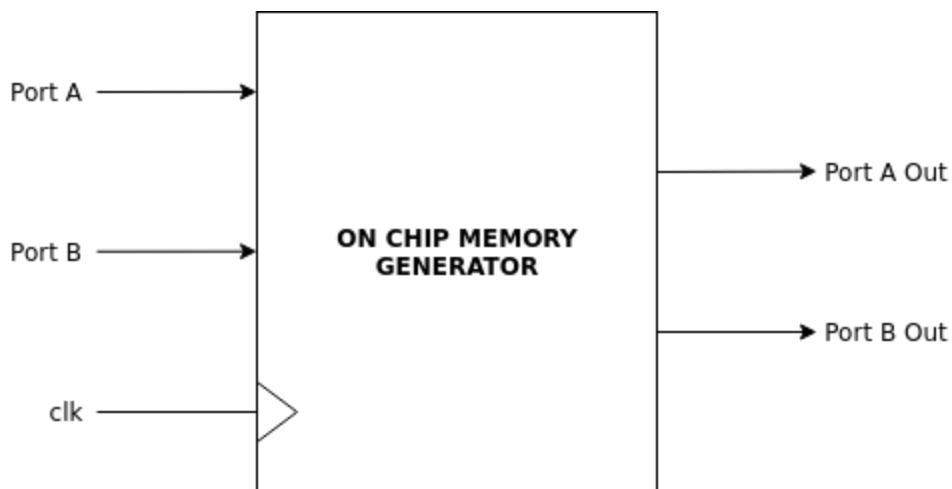


Figure 1: OCM Generator Block Diagram

# IP Specification

On-Chip Memory Generator IP Core with a memory size of 32x1024, data width of 1 to 128 bits, and write depth ranging from 2 to 32768 provides a flexible and scalable memory solution. The IP core supports separate clocks for two ports, allowing for independent control of each port's read and write operations. It also offers three different memory types: Single Port, Simple Dual Port, and True Dual Port. Single Port provides access to the memory through a single clock and data port, Simple Dual Port provides basic two-port functionality with a shared clock, and True Dual Port provides two independent ports with separate clocks for maximum flexibility and performance. This IP core is a versatile and high-performance solution for embedded systems and integrated circuits with memory requirements. The Figure 2 shows the top level diagram of On Chip Memory.

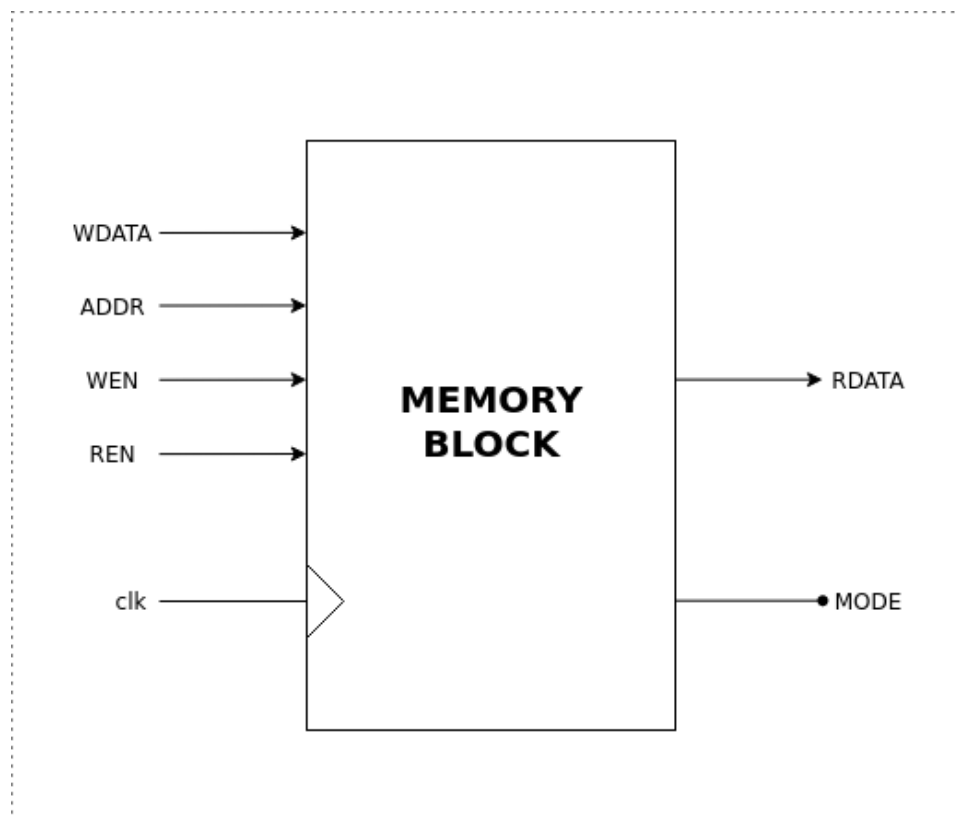


Figure 2: Top Module

## Memory Types

There are three main type of memories. These memories are:

- **Single Port RAM:**

A Single-Port RAM is a type of Random Access Memory that has only one port for reading and writing data. It allows only one operation (read or write) at a time, thus making it less flexible compared to a dual-port RAM which has two ports allowing for both read and write operations to occur simultaneously. Single-port RAM is commonly used in applications where cost and/or chip area are a concern, as they are simpler to implement and consume less resources compared to a dual-port RAM. It is shown in Figure 3.

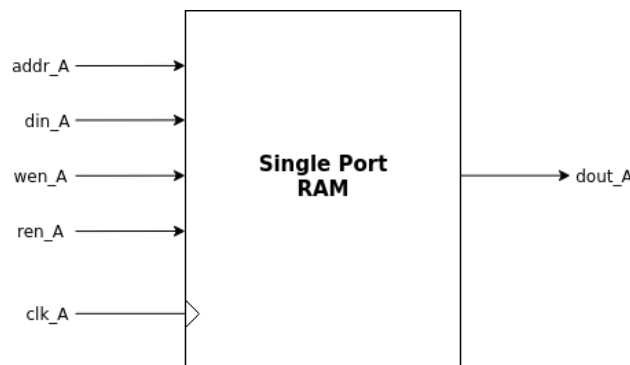


Figure 3: Single Port RAM

- **Simple Dual Port RAM:**

A Simple Dual-Port RAM is a type of Random Access Memory that has two independent ports, allowing for simultaneous read and write operations. This makes it more flexible compared to a single-port RAM, as it can handle multiple access requests at the same time. It is commonly used in applications where multiple processors or systems need to access shared memory simultaneously. It is shown in Figure 4.

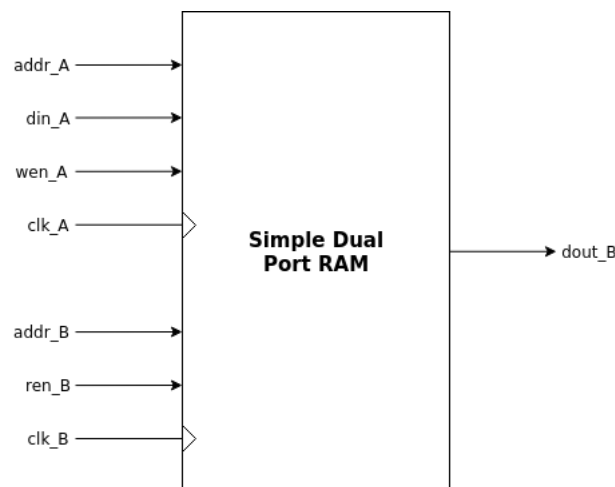


Figure 4: Simple Dual Port RAM

- **True Dual Port RAM:**

A True Dual-Port RAM is a type of Random Access Memory that has two completely

independent ports, allowing for truly simultaneous and non-interfering read and write operations. Unlike a simple dual-port RAM, which may share certain elements such as data buses or address decoders, a true dual-port RAM has completely separate components for each port, allowing for truly independent and parallel access to the memory. True dual-port RAMs are commonly used in applications where the highest level of parallelism is required, such as in high-speed communication systems, real-time video processing, and other high-performance applications. It is shown in Figure 5.

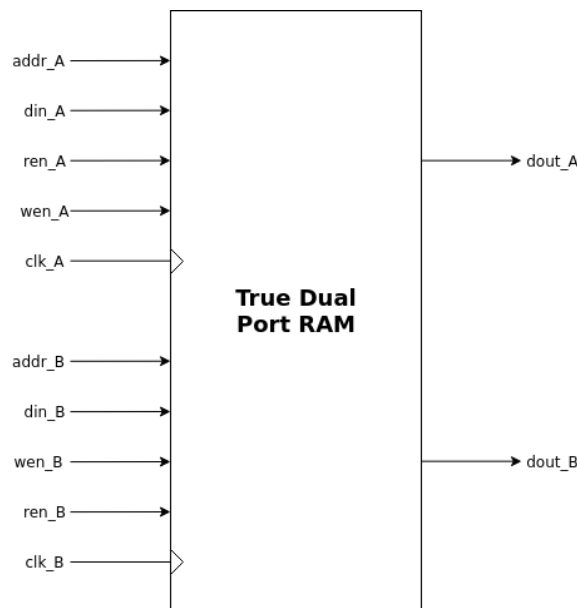


Figure 5: True Dual Port RAM

## Common Clock Versus Uncommon Clock

A common clock refers to a clock signal that is shared among all the memory blocks in the device. In contrast, an uncommon clock refers to a clock signal that is unique to each memory block.

- The use of a common clock in memory blocks has several advantages. First, it simplifies the design and implementation of the memory blocks as there is only one clock signal to manage. Second, it ensures that all the memory blocks are synchronized, which is critical for high-speed data transfer and avoiding errors. However, the disadvantage of using a common clock is that it may limit the flexibility of the design, as all the memory blocks must operate at the same clock frequency.
- The use of an uncommon clock in memory blocks allows for more flexibility in the design, as each memory block can operate at a different clock frequency. This can be useful in designs that require multiple memory blocks with different timing requirements. However, the disadvantage of using an uncommon clock is that it increases the complexity of the design, as each clock signal must be managed independently, and timing issues may arise.

Overall, the choice between using a common clock or an uncommon clock in memories using On Chip Memory Generator depends on the specific requirements of the design. If the design requires all memory blocks to operate at the same frequency, a



common clock may be the best choice. However, if the design requires flexibility in timing requirements, an uncommon clock may be more appropriate.

## **Block RAM Versus Distributed RAM**

Two types of memory blocks that can be generated with On Chip Memory Generator are Block RAM and Distributed RAM. Block RAM is a large, rectangular array of memory cells optimized for high-speed access, while Distributed RAM is a flexible set of smaller, distributed memory cells that are suitable for storing small amounts of data. The choice between these two types of memory blocks depends on the specific requirements of the design.

## Memory Initialization

Memory Initialization is an important feature in memory IPs. This feature allows user to initialize memory by providing the memory file. Supported file formats for On Chip Memory Generator are .hex and .bin. The initialization data is provided in the form of memory lines, where each line corresponds to the data value of a specific memory address. Each memory cell can typically store a fixed number of bits depending upon the user data width. Memory initialization is supported for all the configurations supported by On Chip Memory Generator. To initialize memory correctly, verify that the memory addresses and corresponding data values are accurate and aligned correctly. The Figure 6 shows the memory initialization of On Chip Memory Generator.

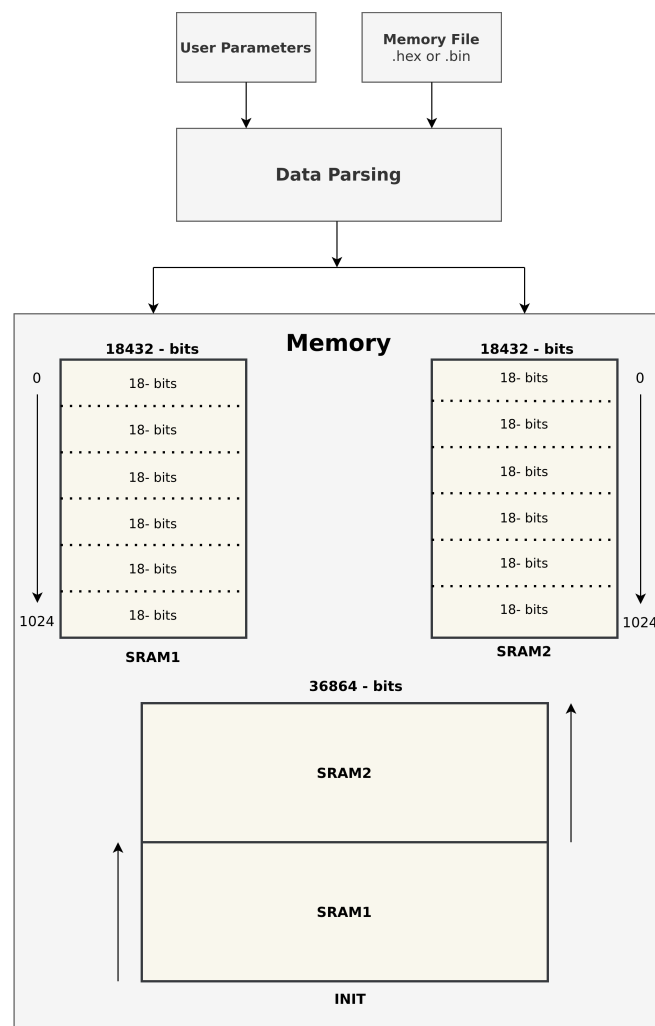


Figure 6: Memory Initialization

**Caution:** Data width and memory addresses in memory file should match the Data Width and Write Depth Parameters of the IP.

## IP Support Details

The Table 1 gives the support details for On Chip Memory.

Compliance		IP Resources				Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Analyze and Elaboration	Simulation	Synthesis
GEMINI	-	Verilog	-	Verilog	BRAM	Raptor	Raptor	Raptor

Table 1: Support Details

## Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			Resource Utilization	
Minimum Resource	Options	Configuration	Resources	Utilized
	MEMORY_TYPE	Single_Port	BRAMS	1
	DATA_WIDTH	32	LUTS	0
	WRITE_DEPTH	1024	REGISTERS	0
	BRAM	TRUE	-	-
Maximum Resource	Options	Configuration	Resources	Utilized
	MEMORY_TYPE	True_Dual_Port	BRAMS	128
	DATA_WIDTH	128	LUTS	0
	WRITE_DEPTH	32768	REGISTERS	0
	BRAM	TRUE	-	-

Table 2: Resource Utilization

## Ports

Table 3 lists the top interface ports of the On Chip Memory.

Signal Name	Input/Output	Description
clk	Input	Clock for Synchronization of two Ports
<b>Port A</b>		
clk_A	Input	Clock for Port A
addr_A	Input	Address Width of Port A
din_A	Input	Input Data of Port A
wen_A	Input	Write Enable to Port A
ren_A	Input	Read Enable to Port A
dout_A	Output	Output Data of Port A
<b>Port B</b>		
clk_B	Input	Clock for Port B
addr_B	Input	Address Width of Port B
din_B	Input	Input Data of Port B
wen_B	Input	Write Enable to Port B
ren_B	Input	Read Enable to Port B
dout_B	Output	Output Data of Port B

Table 3: Ports

## Parameters

Table 4 lists the parameters of the On Chip Memory.

Parameter	Values	Default Value	Description
MEMORY_TYPE	Single Port, Simple Dual Port, True Dual Port	Single Port	Desired Memory Type
DATA_WIDTH	1-128	32	Data Width of Memory
WRITE_DEPTH	2-32768	1024	Depth of Memory
COMMON_CLK	True/False	False	Common Clock for both Ports
BRAM	True/False	False	Block RAM vs Distributed RAM
FILE_PATH	<path>		Path to Pass Memory File for Initialization

Table 4: Parameters

# Design Flow

## IP Customization and Generation

On Chip Memory IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in Figure 7.

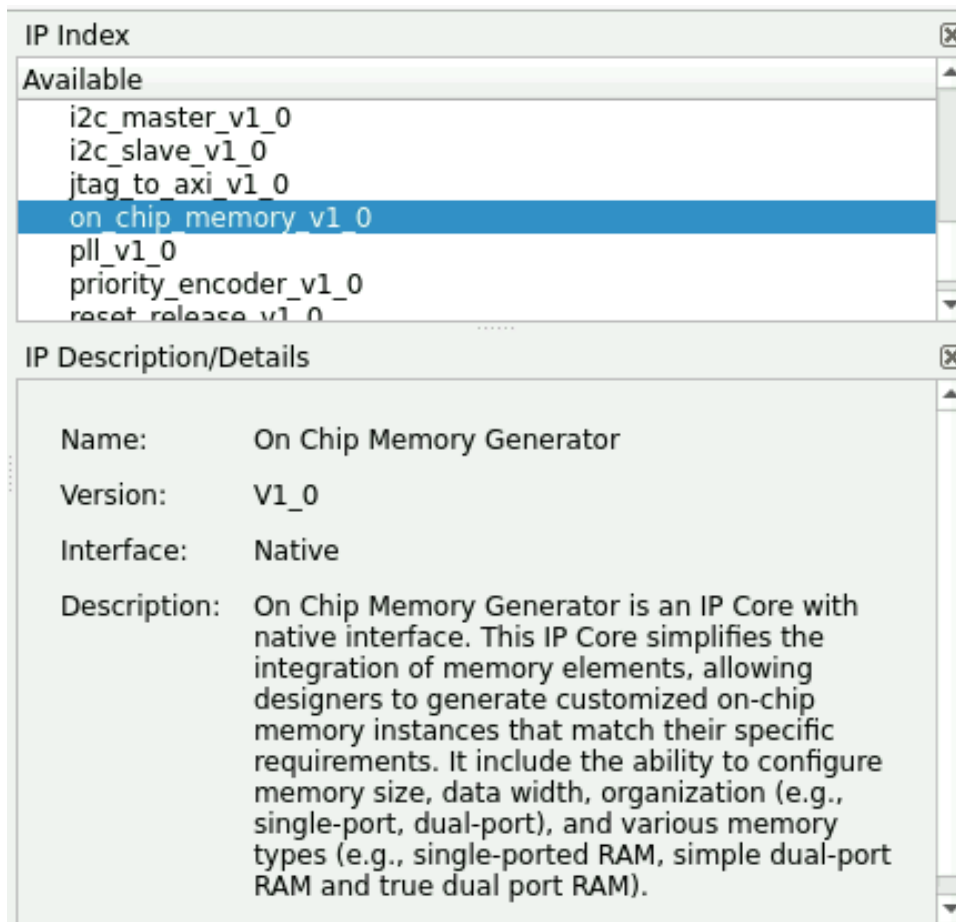
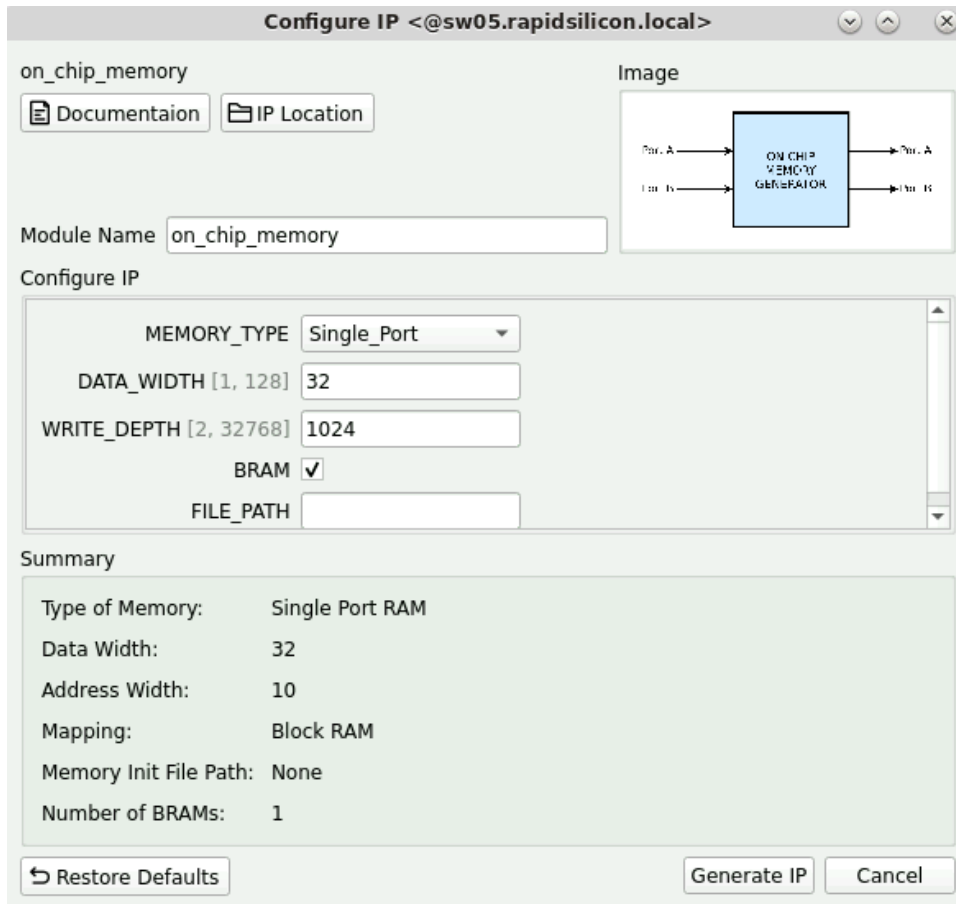


Figure 7: IP List

## Parameters Customization

From the IP configuration window, the parameters of the On Chip Memory can be configured and its features can be enabled for generating a customized On Chip Memory IP core that suits the user application requirements. All parameters are shown in Figure 8. In Figure 8, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.



The screenshot shows the 'Configure IP' window for the On Chip Memory Generator. The window title is 'Configure IP <@sw05.rapidsilicon.local>'. It features a 'Module Name' field set to 'on\_chip\_memory'. The 'Configure IP' section includes a 'MEMORY\_TYPE' dropdown set to 'Single\_Port', a 'DATA\_WIDTH [1, 128]' field set to '32', a 'WRITE\_DEPTH [2, 32768]' field set to '1024', a 'BRAM' checkbox checked, and a 'FILE\_PATH' field. An 'Image' section shows a block diagram of the 'ON CHIP MEMORY GENERATOR' with inputs 'Port A' and 'Port B' and outputs 'Port A' and 'Port B'. A 'Summary' section lists the configuration: 'Type of Memory: Single Port RAM', 'Data Width: 32', 'Address Width: 10', 'Mapping: Block RAM', 'Memory Init File Path: None', and 'Number of BRAMs: 1'. At the bottom are buttons for 'Restore Defaults', 'Generate IP', and 'Cancel'.

Figure 8: IP Configuration

# Test Bench

The testbench attached with On Chip Memory Generator is Single Port RAM 32x1024. It is basically a comparison between the behavioural RTL and the generated RTL. This test provides 1024 random inputs to addr\_A and din\_A of both the RTLs and in the end, it compares all the outputs. If all the outputs match, then test will be passed otherwise it'll be failed. The results of this test are attached below in Figure 9.

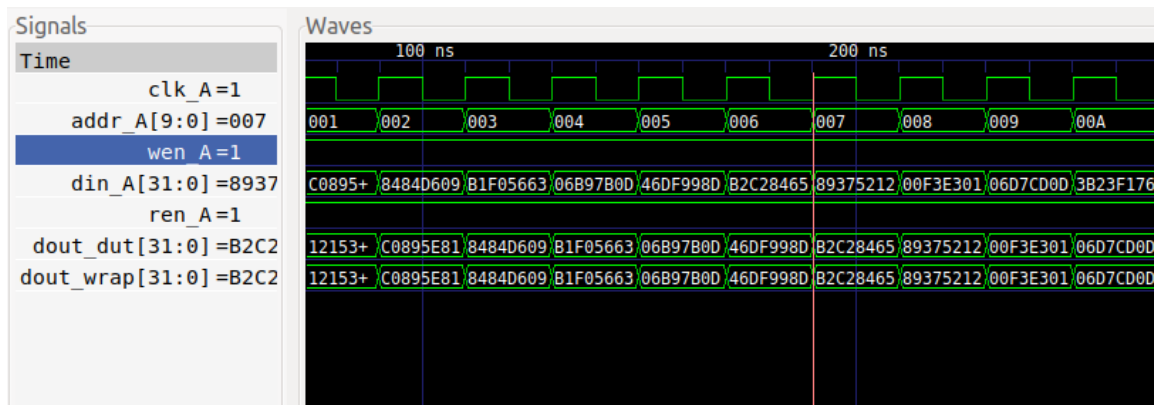


Figure 9: Test Results

# Revision History

Date	Version	Revisions
November 20, 2023	0.1	Initial version On Chip Memory Generator User Guide