AXI Stream Pipeline Register (Beta Release)

Version 0.1

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IP Summary

Introduction

The AXI Stream Pipeline Register is an IP core that can be used to improve the performance and flexibility of AXI Stream interfaces in FPGA designs. It provides a pipeline structure that allows data to be processed concurrently and can be configured with a variable number of stages to optimize performance and reduce latency. It consists of a chain of registers that separate the data into stages. Each stage of the pipeline can be configured as a bypass, simple buffer, or skid buffer register, similar to the AXI Register IP core. This allows designers to choose the appropriate type of register for each stage, depending on the requirements of the design. The main advantage of the AXI Stream Pipeline Register IP core is that it can increase the throughput and reduce the latency of AXI Stream interfaces. By dividing the data into stages, each stage can be processed in parallel, which can increase the overall throughput.

Features

- AXI Stream one master and one slave interface
- Configurable data width 8, 16, 32, 64, 128, 256, 512, 1024 bits
- Support ID width up to 8 bits
- Register options i.e. bypass, simple buffer or skid buffer
- Supports 16 stages of pipelining
- Compatible with AXI Stream Interconnect

Overview

AXI Stream Pipeline Register

The AXI Stream Pipeline Register IP Core is a part of Raptor Design Suite that provides a standard interface for reading and writing registers in a system-on-chip (SoC) design. It uses the AXI Stream protocol, which is an industry-standard communication protocol that enables fast and efficient data transfer between different modules in the SoC. It can be customized to include a specific number of pipeline registers. It simplifies the SoC design process, reduces design time, and ensures compatibility with other AXI Stream-compliant modules in the SoC. It is typically used in high-speed data acquisition systems, image processing applications, and digital signal processing systems. The use of pipeline registers can help to reduce latency and improve system performance in these types of applications.

Figure 1: AXI Stream Pipeline Register Block Diagram

IP Specification

The AXI Stream Pipeline Register IP core is a highly configurable solution for improving the performance and flexibility of AXI Stream interfaces in FPGA designs. It supports the AXI4-Stream protocol and can be customized for various pipeline configurations with up to 16 stages. All pipeline stages can be configured as a bypass, simple buffer, or skid buffer register with single parameter. Additionally, it supports full AXI4-Stream data width up to 1024 bits. These specifications make the AXI Stream Pipeline Register IP core a versatile and configurable solution for improving the performance and flexibility of AXI Stream interfaces in a wide range of applications.

Figure 2: Top Module

Type of Registers

The "REG_TYPE" parameter in an AXI Stream Pipeline Register IP Core specifies how the register behaves when data is written to it. There are three types of registers that can be selected: Bypass, Simple Buffer, and Skid Buffer.

- **Bypass Register:** A Bypass register is the simplest type of register. When data is written to it, the register immediately transfers the data to the output without storing it. This type of register is useful when there is no need to store the data and it can be directly passed on to the next module. The bypass register provides the fastest and most efficient data transfer but does not store the data.
- **Simple Buffer:** A Simple Buffer register stores the data temporarily and releases it when requested. When data is written to a simple buffer register, it is stored in the register and is available for reading until it is overwritten. This type of register is useful when the data needs to be processed before being passed on to the next module. For example, a simple buffer register could be used to store data that needs to be processed by a CPU or a DSP core.
- **Skid Buffer:** A Skid Buffer register is similar to a Simple Buffer register, but it has an additional feature called "skidding." Skidding means that if new data is written to the register before the old data is read, the new data overwrites the old data. This behavior can be useful when only the most recent data needs to be kept. Skid buffer registers are often used in real-time applications, such as video or audio processing, where it is important to have the most recent data.

Pipeline Stages

The number of pipeline registers in the AXI Stream Pipeline Register IP core determines the number of stages in the pipeline structure, and the appropriate number of pipeline registers depends on the specific requirements of the application. The AXI Stream Pipeline Register IP core supports up to 16 pipeline stages, which provides a high degree of flexibility for designers to optimize the performance of the AXI Stream interface.

Standards

The AXI-Stream Master and Slave interfaces are compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXI Stream Pipeline Register.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI Stream	Verilog	-	Cocotb	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2. Other parameters are kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resources	**Options**	**Values**	**Resources**	**Utilized**
	DATA_WIDTH	1	REGISTERS	7
	ID_WIDTH	1	LUTS	2
	DEST_WIDTH	1		
	LENGTH	1		
	REG_TYPE	Simple_Buffer		
Maximum Resources	**Options**	**Values**	**Resources**	**Utilized**
	DATA_WIDTH	1024	REGISTERS	37488
	ID_WIDTH	8	LUTS	18832
	DEST_WIDTH	8		
	LENGTH	16		
	REG_TYPE	Skid_Buffer		

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI Stream Pipeline Register.

Signal Name	I/O	Description
clk	I	Clock Signal for register
rst	I	Active High Synchronous Reset Signal
AXI Stream I		
s_axi_tdata	I	Data Port
s_axis_tkeep	I	Valid Bytes in Data
s_axis_tvalid	I	Valid Signal
s_axis_tready	O	Ready Signal
s_axis_tlast	I	Last transacton Signal
s_axis_tid	I	ID Signal
s_axis_tdest	I	DEST Signal
s_axis_tuser	I	USER Signal
AXI Stream O		
m_axi_tdata	O	Data Port
m_axis_tkeep	O	Valid Bytes in Data
m_axis_tvalid	O	Valid Signal
m_axis_tready	I	Ready Signal
m_axis_tlast	O	Last transaction Signal
m_axis_tid	O	ID Signal
m_axis_tdest	O	DEST Signal
m_axis_tuser	O	USER Signal

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI Stream Pipeline Register.

Parameter	Values	Default Value	Description
REG_TYPE	Bypass, Simple_Buffer, Skid_Buffer	Bypass	Type of Register i.e. bypass, simple buffer or skid buffer
DATA_WIDTH	8, 16, 32, 64, 128, 256, 512, 1024	8	Data Width of Register
ID_WIDTH	1 - 8	8	ID field of Register
DEST_WIDTH	1 - 8	8	DEST field of Register
USER_WIDTH	1 - 1024	1	USER field of Register
LENGTH	1 - 16	1	Number of Pipeline Stages
LAST_EN	True/False	True	Enable for Last Transaction
ID_EN	True/False	True	Enable for ID Field
DEST_EN	True/False	True	Enable for DEST Field
USER_EN	True/False	True	Enable for USER Field

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI Stream Pipeline Register IP core is a part of the Raptor Design Suite Software. A customized register can be generated from the Raptor's IP configuration window as shown in figure 3.

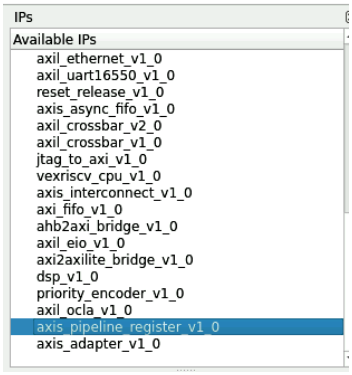

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI Stream Pipeline Register can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in Figure 4. In Figure 4, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

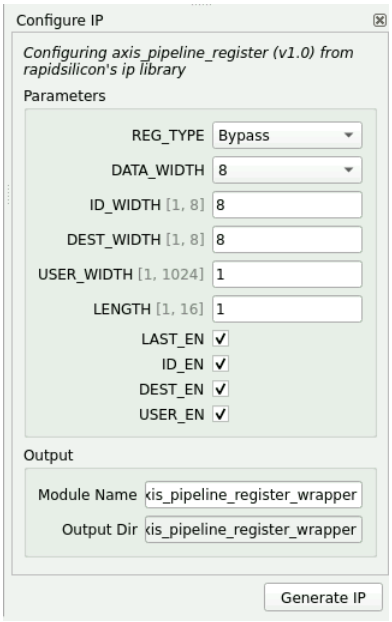

Figure 4: IP Configuration

Test Bench

The AXI Stream Pipeline Register IP is provided with a testbench which is based upon Cocotb verification environment. In this test, slave interface receive frames from master and pass it on to the slave through axis pipeline register. The input data is generated using a test data generator module. The output data is compared with the expected output data to verify the correctness of the IP core's operation. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
May 10, 2023	0.1	Initial version AXI Stream Pipeline Register User Guide