AXI DPRAM

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IP Summary

Introduction

AXI DPRAM (Dual-Port RAM) is a type of memory block that uses the AXI (Advanced eXtensible Interface) protocol for data communication. The AXI protocol is a widely used interface standard for high-speed digital circuits, providing a high-bandwidth, low-latency communication link between hardware components. It is specialized type of RAM that has two independent ports for simultaneous read and write operations from two different sources. This feature allows for greater flexibility and efficiency in data transfer between different hardware components in a digital system. It is particularly useful in applications where multiple components need to access the memory block at the same time, without causing delays or conflicts. One of the key advantages of the AXI DPRAM is its ability to operate at high speeds while maintaining low latency. This makes it ideal for use in high-performance applications where fast data transfer is critical.

Features

- AXI4 (memory mapped) one master and one slave interface
- Configurable data width 8, 16, 32, 64, 128, 256 bits
- Configurable address width 8 to 16 bits
- Support ID width up to 32 bits
- Extra pipeline register for each port.
- Interleaving write and read burst cycles option for each port
- Compatible with AXI4 Interconnect

Overview

AXI DPRAM

The AXI DPRAM IP Core is a part of Raptor Design Suite which is designed to be used in digital systems and is compatible with the AMBA AXI4 (Advanced eXtensible Interface 4) standard. It is a high-performance memory that features two independent data ports, allowing simultaneous read and write access from two different sources. It is commonly used in applications where high-speed data transfer is required, such as in graphics processing, video processing, and networking. It provides efficient data transfer between the memory and other components in the system. It includes features such as burst transfer support, programmable address width and programmable data width.

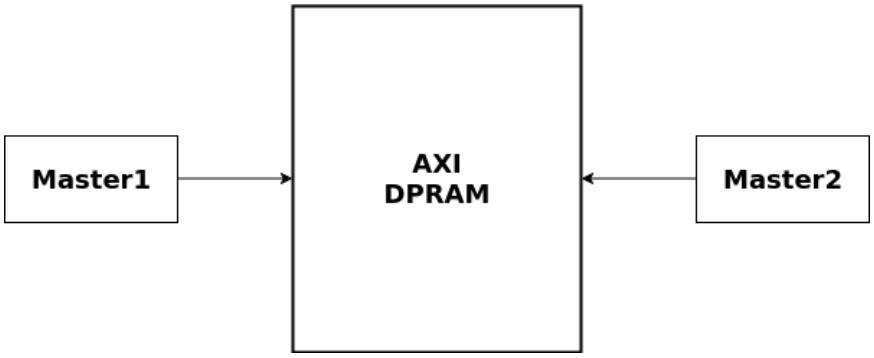

Figure 1: AXI DPRAM Block Diagram

IP Specification

Overview

The AXI DP RAM IP core is a high-performance, dual-port RAM memory block designed for use in FPGAs. It is based on the Advanced Microcontroller Bus Architecture (AMBA) AXI4 protocol and features two independent read/write ports, allowing for simultaneous access by multiple processors or peripherals. It supports a wide range of data widths, from 8 bits to 256 bits, and can be configured for different memory sizes up to a maximum of 16 terabytes. It also includes extra pipeline registers for each port and interleaving write and read burst cycles option for each port. This IP core is commonly used in a wide range of applications, including embedded systems, digital signal processing, network processing, and video processing. It is fully customizable and can be easily integrated into new or existing FPGA designs.

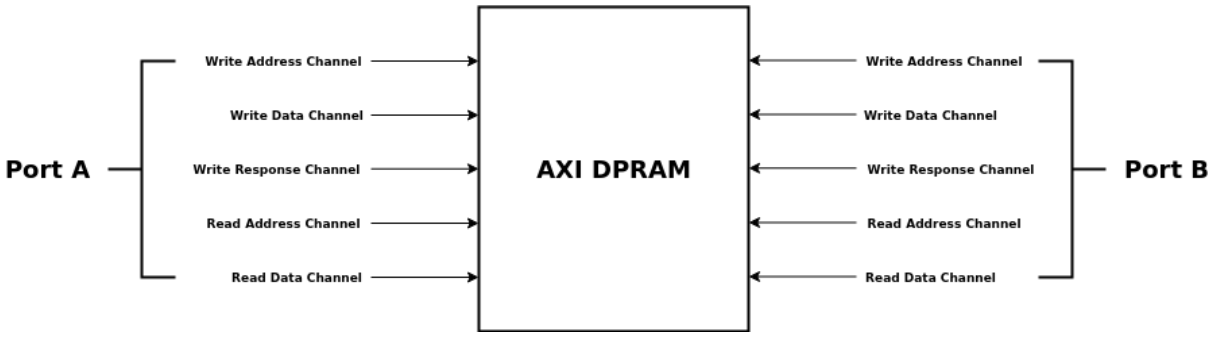

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI DPRAM.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	CocoTB	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2. Other parameters are kept on their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	8	RAM36K	1
	ADDR_WIDTH	8	REGISTERS	162
	ID_WIDTH	8	-	-
	A_PIP_OUT	False	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	256	RAM36K	16
	ADDR_WIDTH	16	REGISTERS	976
	ID_WIDTH	32	-	-
	A_PIP_OUT	True	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI DPRAM.

Signal Name	Input/Output	Description
a_clk	Input	Clock Signal for Port A
b_clk	Input	Clock Signal for Port B
a_rst	Input	Active Low Reset Signal for Port A
b_rst	Input	Active Low Reset Signal for Port B
Write Address Channel		
awid	Input	Write address ID
awaddr	Input	Write address
awlen	Input	Burst length
awsize	Input	Burst size
awburst	Input	Burst type
awlock	Input	Lock type
awcache	Input	Memory type
awprot	Input	Protection type
awvalid	Input	Write address valid
awready	Output	Write address ready
Write Data Channel		
wdata	Input	Write data
wstrb	Input	Write strobe
wlast	Input	Write last
wvalid	Input	Write valid
wready	Output	Write ready
Write Response Channel		
bid	Output	Response ID tag
bresp	Output	Write response
bvalid	Output	Write response valid
bready	Input	Write response ready
Read Address Channel		

Signal Name	Input/Output	Description
arid	Input	Read address ID
araddr	Input	Read address
arlen	Input	Burst length
arsize	Input	Burst size
arburst	Input	Burst type
arlock	Input	Lock type
arcache	Input	Memory type
arprot	Input	Protection type
arvalid	Input	Read address valid
arready	Output	Read address ready
Read Data Channel		
rid	Output	Read ID tag
rdata	Output	Read data
rresp	Output	Read response
rlast	Output	Read last
rvalid	Output	Read valid
rready	Input	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI DPRAM.

Parameter	Values	Default Value	Description
DATA_WIDTH	8, 16, 32, 64, 128, 256	32	Data Width of RAM
ADDR_WIDTH	8 - 16	16	Address Width of RAM
ID_WIDTH	1 - 32	32	ID field of RAM
A_PIP_OUT	True/False	True	Piplelined Output for Port A
B_PIP_OUT	True/False	True	Piplelined Output for Port B
A_INTERLEAVE	True/False	True	Interleave write and read burst cycles on Port A
B_INTERLEAVE	True/False	True	Interleave write and read burst cycles on Port B

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI DPRAM IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in figure 3.

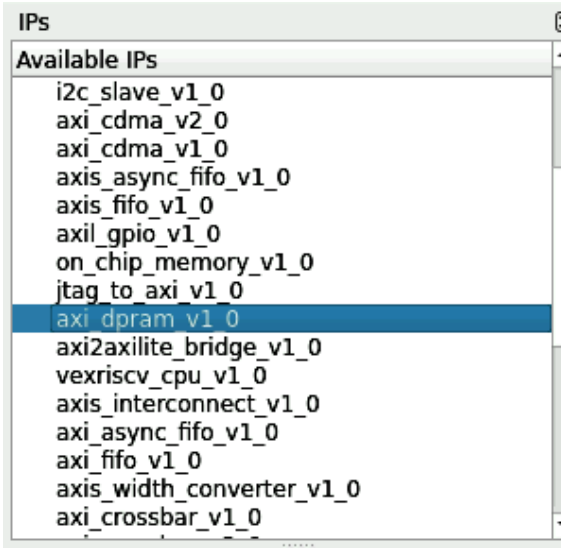

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI DPRAM can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

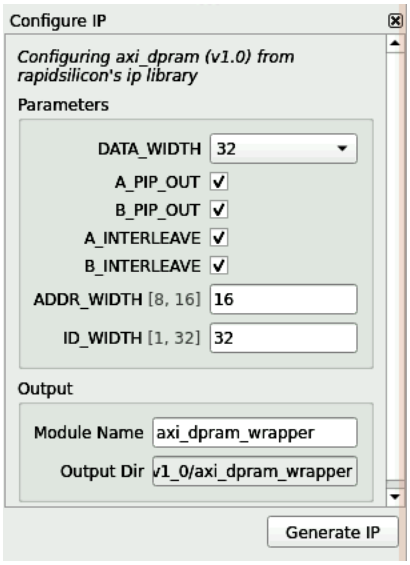

Figure 4: IP Configuration

Test Bench

Test for AXI DPRAM

The testbench attached with AXI DPRAM is CocoTB based verification environment. In this test, multiple read/ write tractions are performed by two masters. The stimulus is generated by environment and test vectors are applied to the design. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
April 27, 2023	1.0	Initial version AXI DPRAM User Guide