Priority Encoder

Version 1.0

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Contents

IP Summary

Introduction

A Priority Encoder IP core is a digital circuit that assigns a priority to a set of input signals and generates a binary code representing the highest-priority signal. Priority encoders are commonly used in digital systems to manage interrupts, data selection, and address decoding. The IP core takes in multiple inputs, and based on their priority, it assigns a unique code to the highest-priority input. This unique code can then be used to select a specific input or to trigger a specific action in the system. The priority encoder IP core is highly configurable, allowing designers to specify the number of inputs and the output code width to match the requirements of the application.

Features

- Support LSB high priority option
- Support 8 bits wide priority encoding

Overview

Priority Encoder

A Priority Encoder IP core is a part of Raptor Design Suite that assigns a priority to a set of input signals and generates a binary code representing the highest-priority signal. This IP core is often used in digital systems to manage interrupts, data selection, and address decoding. It typically consists of a combinational logic circuit that examines the input signals and assigns a priority to them. The output of the combinational logic circuit is a binary code representing the highest-priority input. The number of inputs and the output code width can be specified to match the requirements of the application. The IP core is highly configurable, making it a versatile and flexible solution for digital systems that require efficient management of multiple input signals.

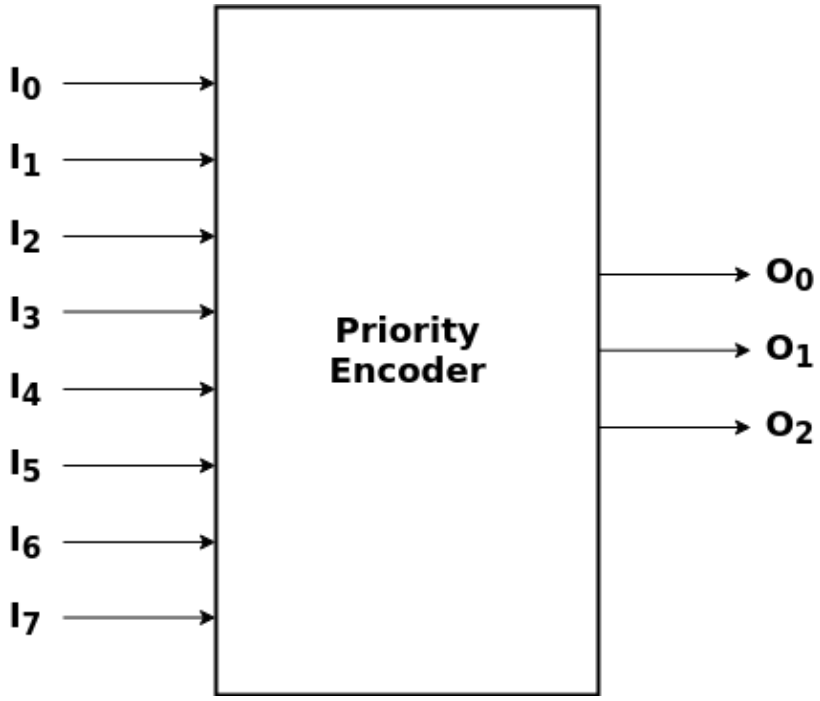

Figure 1: Priority Encoder Block Diagram

IP Specification

Overview

A Priority Encoder IP core is a digital circuit that detects the highest-order bit that is set to 1 in the input and generates a corresponding binary code. Priority encoders are commonly used in microprocessors, where they help in determining the priority of interrupts. The input width of this ip core varies from 2 to 8 depending upon application. The output width depends upon width of input signal. Two priority schemes are supported by this ip core.i.e. LSB Scheme and MSB Scheme.

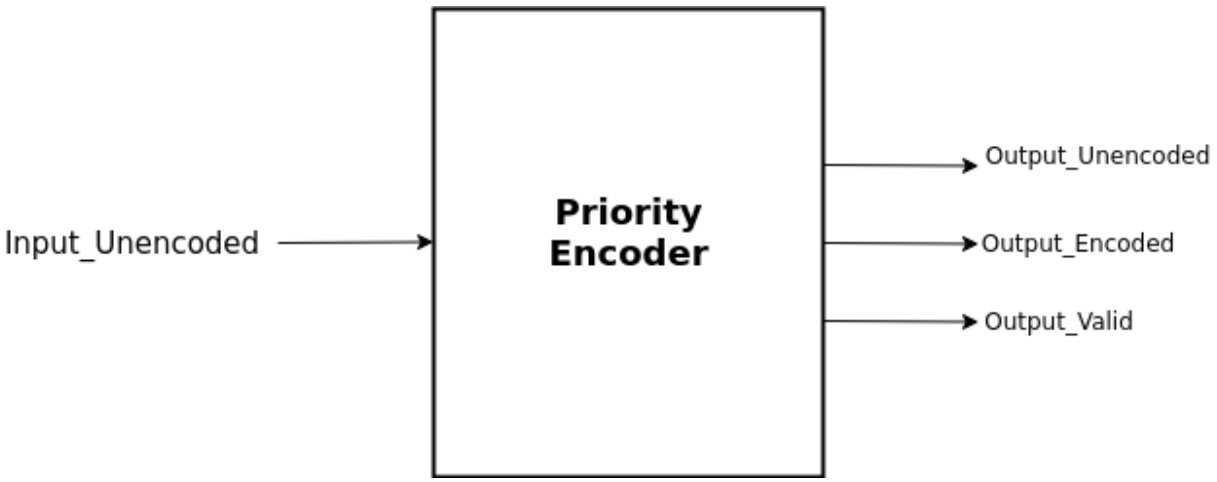

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for Priority Encoder.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	Non-standard	Verilog	-	-	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	WIDTH	2	LUTS	2
	LSB_HIGH_PRIORITY	False	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	WIDTH	8	LUTS	11
	LSB_HIGH_PRIORITY	True	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the Priority Encoder.

Signal Name	Input/Output	Description
input_unencoded	Input	Unencoded input of priority encoder
output_unencoded	Output	Unencoded output of priority encoder
output_valid	Output	Output valid signal
output_encoded	Output	Encoded output of priority encoder

Table 3: Port List

Parameters

Table 4 lists the parameters of the Priority Encoder.

Parameter	Values	Default Value	Description
LSB_HIGH_PRIORITY	True/False	False	Priority Encoding Scheme
WIDTH	2 - 8	4	Width of Input Signal

Table 4: Parameters

Design Flow

IP Customization and Generation

Priority Encoder IP core is a part of the Raptor Design Suite Software. A customized IP can be generated from the Raptor's IP configuration window as shown in figure 3.

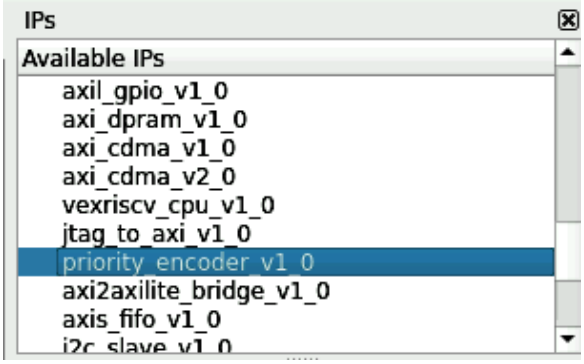

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the Priority Encoder can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

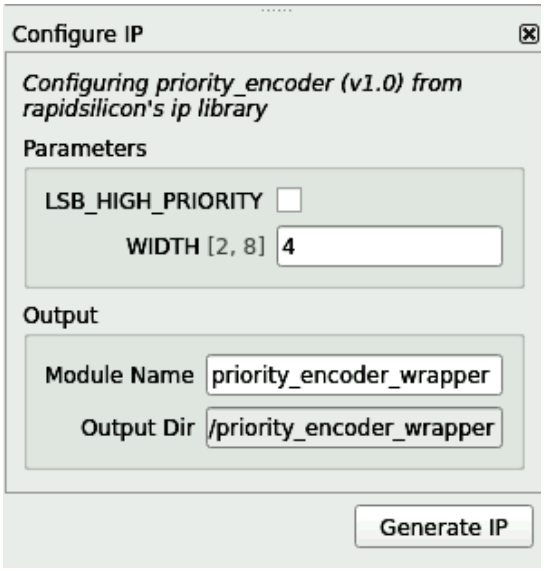

Figure 4: IP Configuration

Test Bench

Test for Priority Encoder

There is no testbench for this IP Core.

Revision History

Date	Version	Revisions
May 3, 2023	1.0	Initial version Priority Encoder User Guide