DSP Generator v1.0

IP User Guide (Beta Release)

January 27, 2023

RapidSilicon

Contents

IP Summary

Introduction

DSP Generator is a unique IP Core that makes it easier to control the dynamic operation of DSP Slice by allowing the use of pre-defined mathematical expressions to specify a variety of operations. Core is generated on the basis of user defined parameters.

Features

- Support for 20-bit and 18-bit operands for multiplication (A*B).
- Support full output width of multiply result (38-bits).
- Support for independent signed or unsigned operands.
- Support Registered inputs for pipelining.
- Support Registered output for pipelining.
- Support three equations:
- (A*B), (A*B+C*D) and (A*B+C*D+E*F+G*H).

Overview

DSP Generator

The DSP Generator facilitates easy customization of the DSP Slice by defining custom instructions. It supports multiple instructions and enables dynamic switching of the instruction being executed during operation. Registered input and registered output is also supported in DSP. The figure 1 shows the block diagram of DSP core.

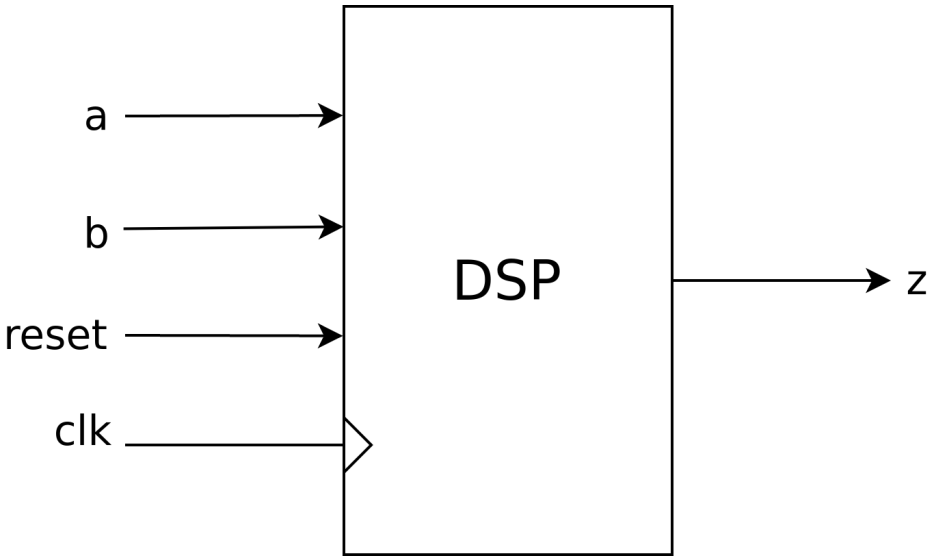

Figure 1. DSP Core Block Diagram

Licensing

IP Specification

Overview

The internal block diagram of the DSP Core in figure 2 consists of several key components, including input a and input b. Input a has a maximum width of 20 bits, while input b has a maximum width of 18 bits. Additionally, the DSP Core includes a reset and clock signal, which are used to control the operation of the system.
Users have the flexibility to change the width of input a and input b using the A_WIDTH and B_WIDTH parameters. This allows for greater control and customization of the DSP Core's operation, depending on the specific requirements of the application.
The output width of the DSP Core is determined based on the provided input widths. The maximum output width is 38 bits, which allows for a wide range of possible output values. Overall, the DSP Core offers a high degree of flexibility and functionality, with the ability to adjust input and output widths and a maximum output width of 38 bits.

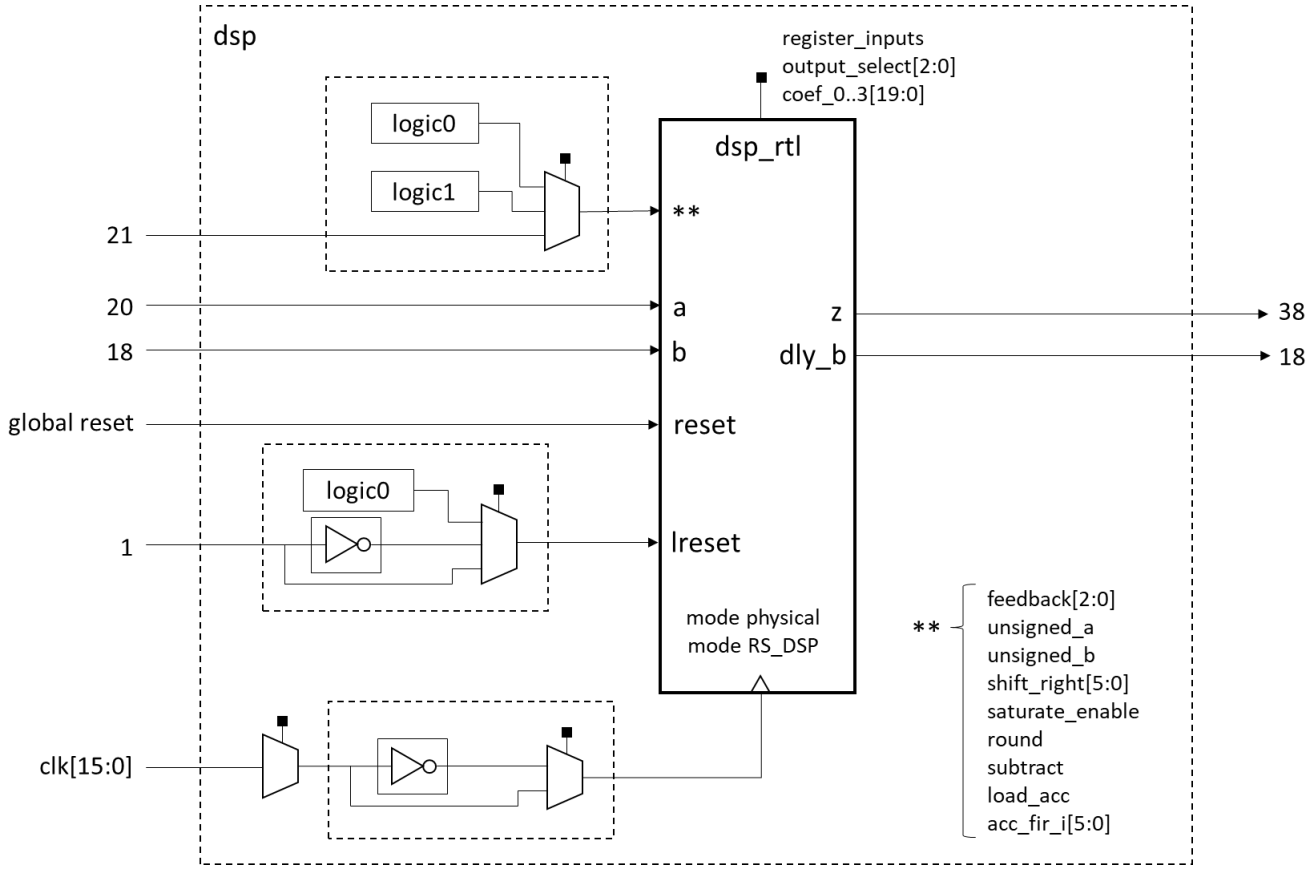

Figure 2. Top Module

IP Support Details

The Table 1 gives the support details for DSP.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	Non-Standard	Verilog	SDC	Verilog	dsp_sim	Raptor	Raptor	Raptor

Table 1. Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	FEATURE	A*B	DSP	1
	A_WIDTH	20	LUT	0
	B_WIDTH	18	CELLS	39
	REG_IN	TRUE	REGISTERS	38
	REG_OUT	TRUE	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	FEATURE	A*B+C*D+E*F+G*H	DSP	4
	A_WIDTH	20	LUT	271
	B_WIDTH	18	CELLS	353
	REG_IN	TRUE	REGISTERS	78
	REG_OUT	TRUE	-	-

Table 2. Resource Utilization

Ports

Table 3 lists the top interface ports of the DSP.

Signal Name	I/O	Description
Global Signals		
clk	I	Clock Port for Synchronization.
reset	I	Reset Port of DSP
z	O	Output Port of DSP
1stDSP		
a	I	Input A Port to 1st DSP Block
b	I	Input B Port to 1st DSP Block
2ndDSP		
c	I	Input A Port to 2nd DSP Block
d	I	Input B Port to 2nd DSP Block
3rdDSP		
e	I	Input A Port to 3rd DSP Block
f	I	Input B Port to 3rd DSP Block
4thDSP		
g	I	Input A Port to 4th DSP Block
h	I	Input B Port to 4th DSP Block

Table 3. DSP Interface

Parameters

Table 4 lists the parameters of the DSP Generator.

Parameter	Values	Default Value	Description
A_WIDTH	1-20	20	Port A width
B_WIDTH	1-18	18	Port B width
C_WIDTH	1-20	20	Port C width
D_WIDTH	1-18	18	Port D width
E_WIDTH	1-20	20	Port E width
F_WIDTH	1-18	18	Port F width
G_WIDTH	1-20	20	Port G width
H_WIDTH	1-18	18	Port H width
UNSIGNED_A	True/False	False	Unsigned value of A
UNSIGNED_B	True/False	False	Unsigned value of B
UNSIGNED_C	True/False	False	Unsigned value of C
UNSIGNED_D	True/False	False	Unsigned value of D
UNSIGNED_E	True/False	False	Unsigned value of E
UNSIGNED_F	True/False	False	Unsigned value of F
UNSIGNED_G	True/False	False	Unsigned value of G
UNSIGNED_H	True/False	False	Unsigned value of H
REG_IN	True/False	False	Registered Input
REG_OUT	True/False	False	Registered Output
FEATURE	A*B A*B+C*D A*B+C*D+E*F+G*H	A*B	Features to be implemented on DSP

Table 4. Parameters

Features Description

1. **A*B**

   A*B is one of the feature of DSP Generator which is used to multiply two numbers. This feature is shown in figure 3.

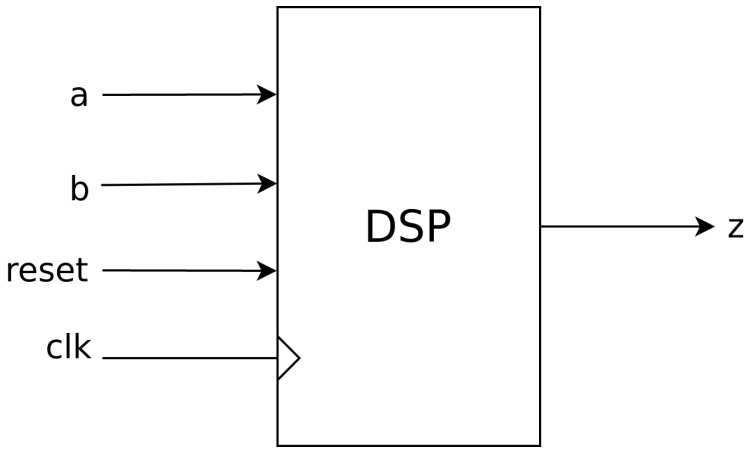

Figure 3. A*B

2. **A*B+C*D**

   A*B+C*D is the second feature of DSP Generator which is used to multiply four numbers. This feature is shown in figure 4.

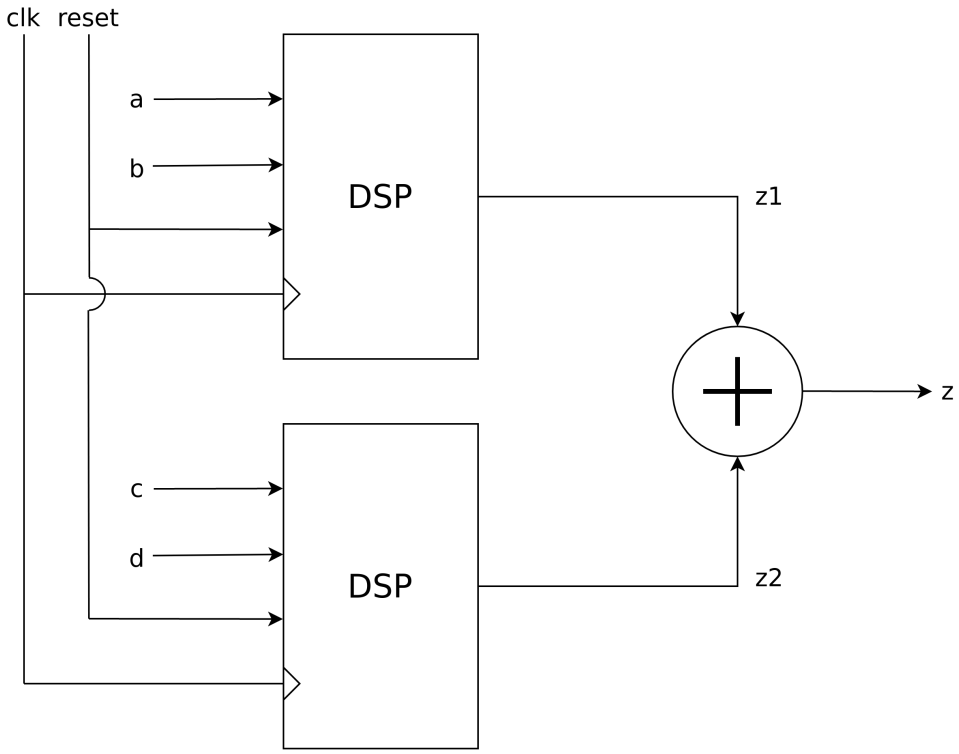

Figure 4. A*B+C*D

Features Description

3. **A*B+C*D+E*F+G*H**

   A*B+C*D+E*F+G*H is the third feature of DSP Generator which is used to multiply eight numbers.This feature is shown in figure 5.

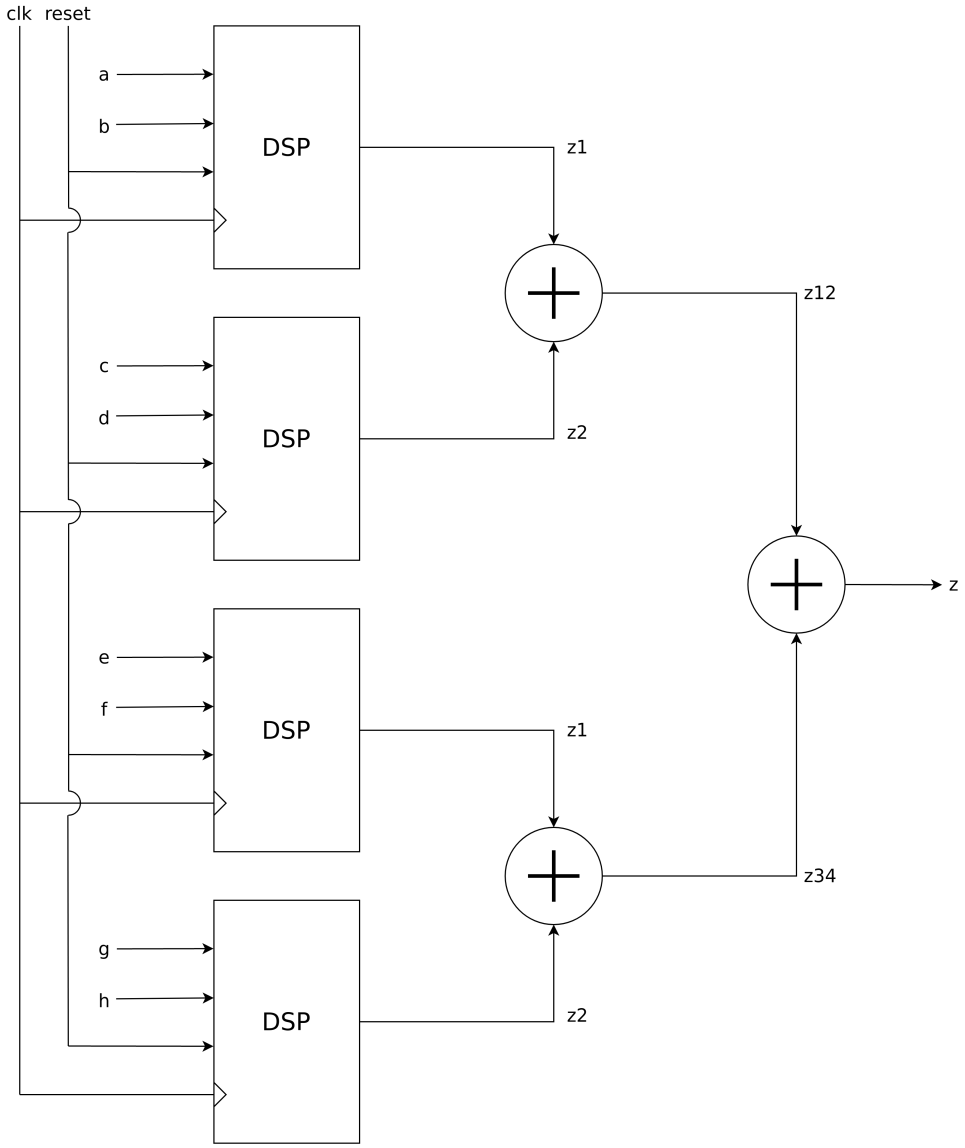

Figure 5. A*B+C*D+E*F+G*H

Design Flow

IP Customization and Generation

DSP IP core is a part of the Raptor Design Suite Software. A customized dsp can be generated from the Raptor's IP configurator window as shown in figure 6.

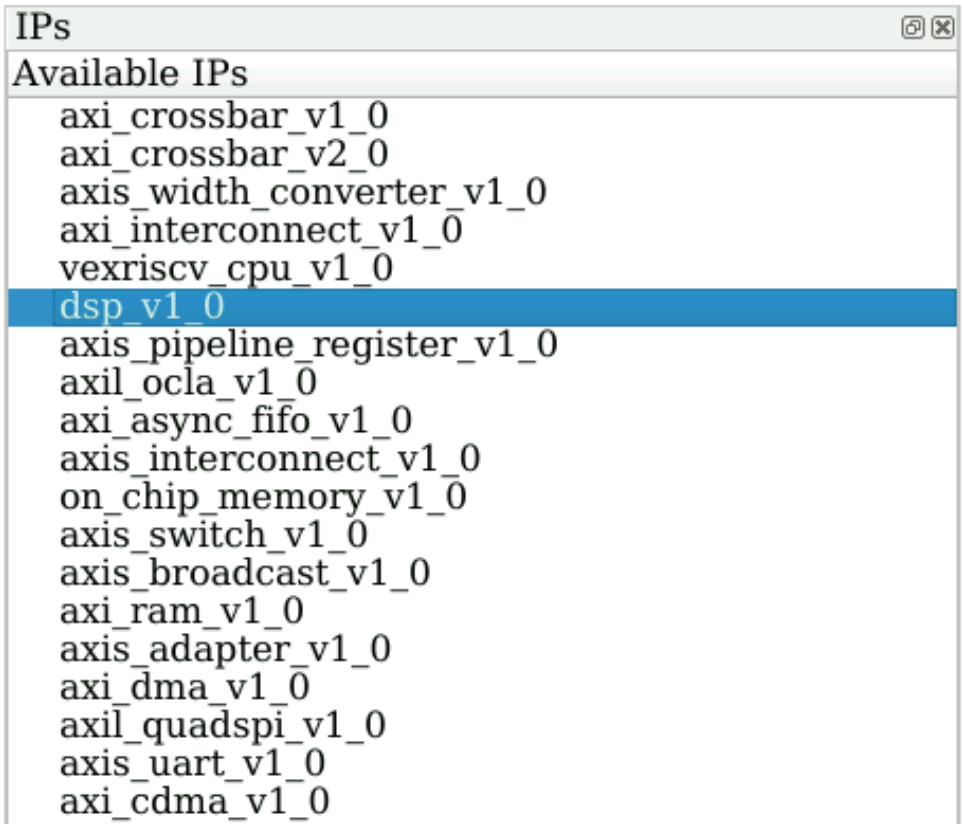

Figure 6. IP list

Parameters Customization: From the IP configuration window, the parameters of the DSP can be configured and DSP features can be enabled for generating a customized DSP IP core that suits the user application requirements. All parameters are shown in figure 7.

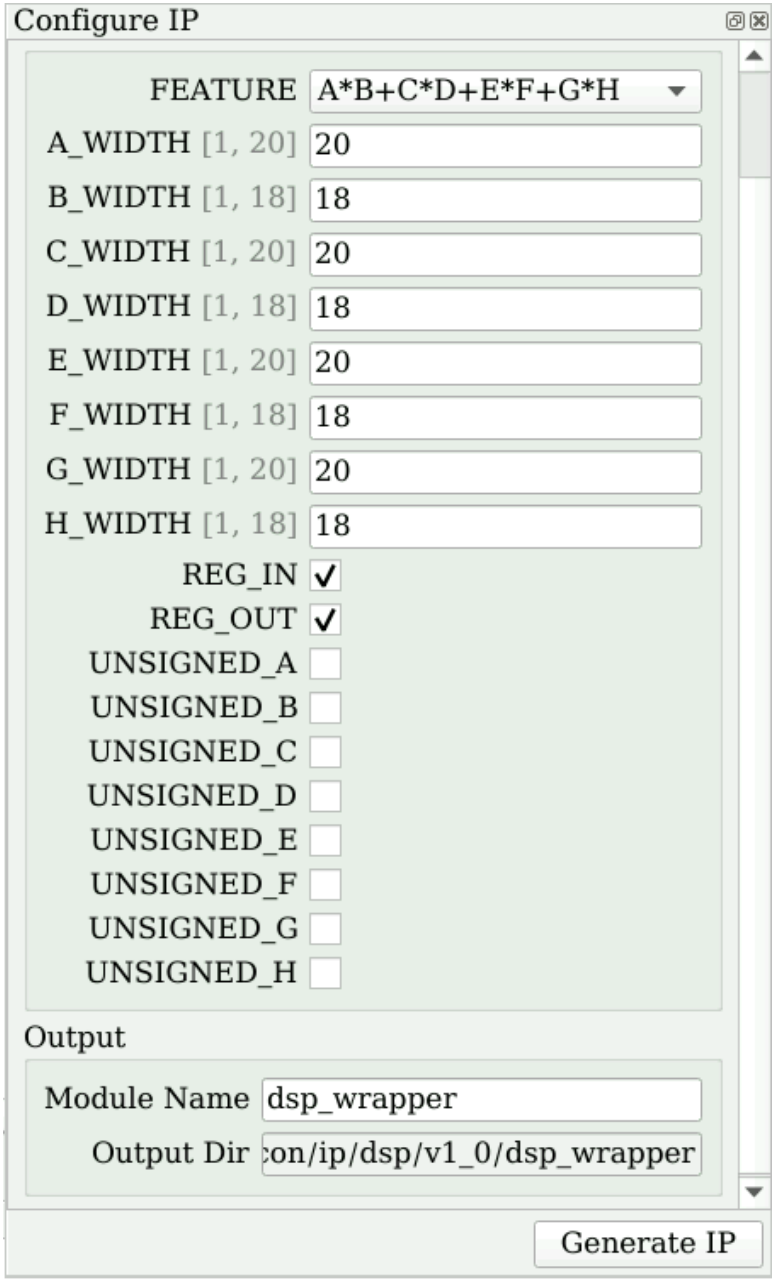

Figure 7. IP Configuration

Test Bench

The testbench attached with DSP Generator is 12x10 multiplication of two inputs. It is basically a comparison between the behavioural RTL and the generated RTL. This test provides 100 random inputs to input a and input b of both the RTLs and in the end, it compares all the outputs. If all the outputs match, then test will be passed otherwise it'll be failed.
The results of this test are attached below in figure 8.

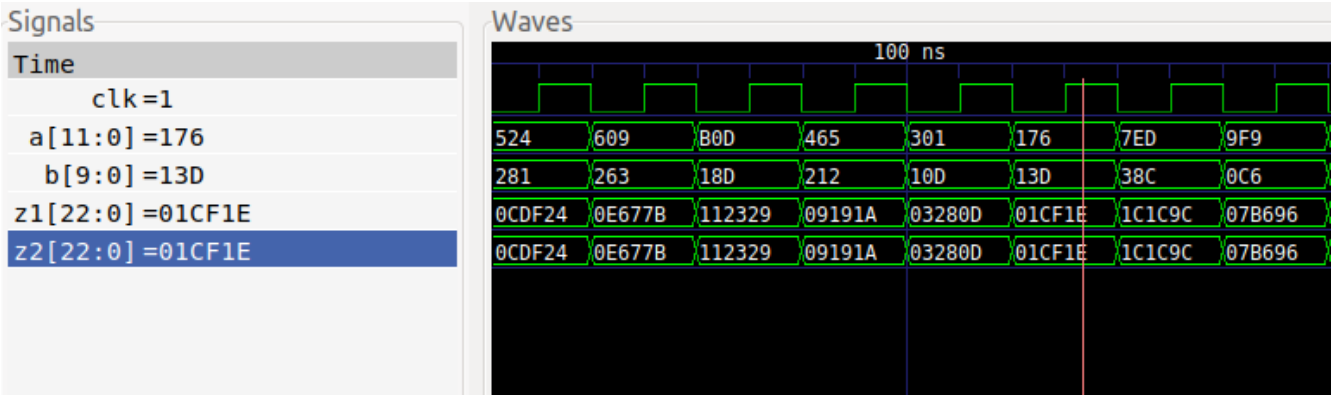

Figure 8. Test Result

Revision History

Date	Version	Revisions
January 27, 2023	0.01	Initial version DSP Generator User Guide Document