Priority Encoder v1.0

IP User Guide (Alpha Release)

January 25, 2023

RapidSilicon

Contents

IP Summary

Introduction

A pipeline register is a type of flip-flop circuit that is used to temporarily store data in a digital system. It is commonly used in computer processors to hold data that is being processed in the pipeline. The data is moved through the pipeline in stages, with each stage performing a specific operation on the data. Pipeline registers are used to hold the data at each stage, allowing the next stage to begin processing the data while the previous stage is still working on it. This helps to increase the overall processing speed of the system by allowing multiple operations to be performed simultaneously. This Priority Encoder IP can be easily integrated in a number of systems. A macro block diagram of this Priority Encoder is shown in Figure 1.

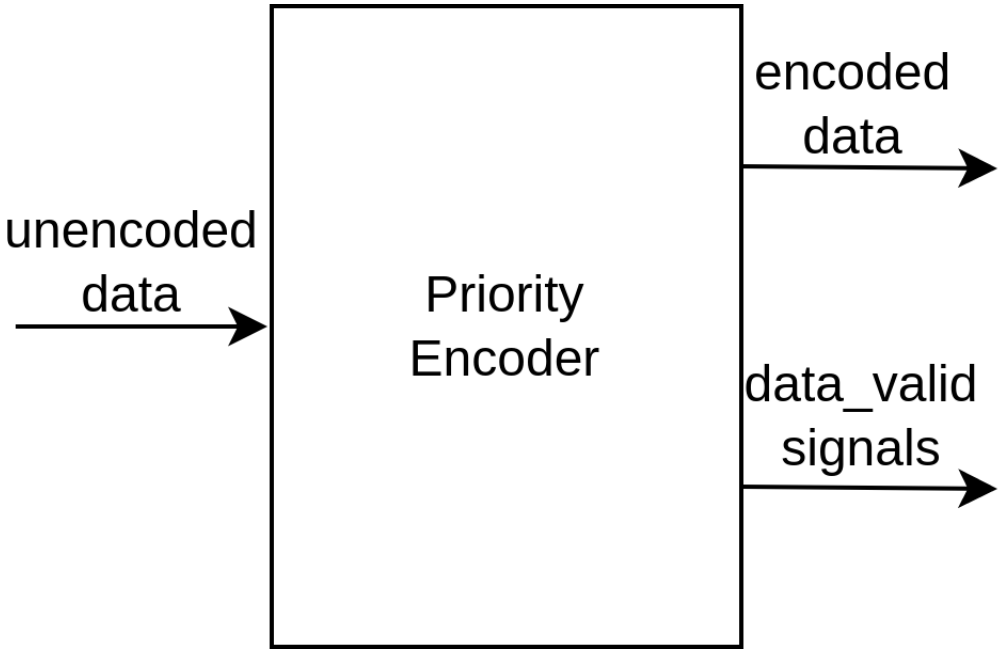

Figure 1. Priority Encoder Block Diagram

Revision History

Date	Version	Revisions
January 25, 2023	0.01	Initial version Priority Encoder User Guide Document