On Chip Memory Generator v1.0

IP User Guide (Beta Release)

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RapidSilicon

Contents

IP Summary

Introduction

The On Chip Memory IP Core is a pre-designed and pre-verified memory block that can be easily integrated into FPGA and ASIC designs. It is based on the Block Random Access Memory (BRAM) technology and provides a large amount of memory resources for storing data that is frequently accessed or changed. The On Chip Memory IP Core is customizable in terms of data width and depth, allowing designers to choose the best option for their specific design requirements.

Features

- On Chip Memory can be configured as Single Port RAM (SP), Simple Dual Port RAM (SDP) or True Dual Port RAM (TDP).
- Support to have multiple read and write ports, allowing multiple operations to occur simultaneously..
- Support configurable width and depth at design time, allowing for flexibility in memory size.
- Support independent clocking on each Port.
- Support to access 32 bit wide memory.
- Support same read/write widths.

Overview

On Chip Memory Generator

On Chip Memory Generator is an IP Core that can generate the RTL (register-transfer level) code for on-chip memory components. This generator can be used to create custom memory components with specific parameters, such as size, bit-width, and number of ports, without the need for manual RTL coding. The figure 1 shows the block diagram of On Chip Memory Generator.

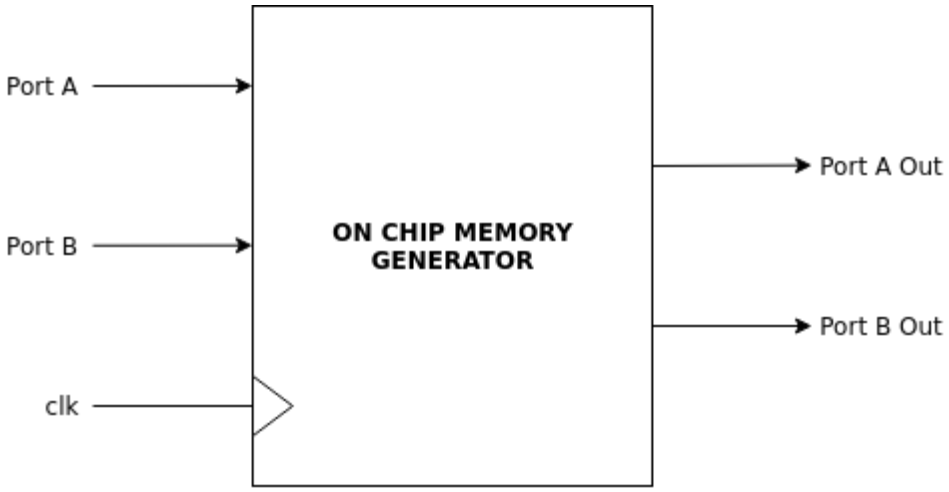

Figure 1. OCM Block Diagram

Licensing

IP Specification

Overview

On-Chip Memory Generator IP Core with a memory size of 32x1024, data width of 32, 64, 96, or 128 bits, and write depth ranging from 2 to 32768 provides a flexible and scalable memory solution. The IP core supports separate clocks for two ports, allowing for independent control of each port's read and write operations. It also offers three different memory types: Single Port, Simple Dual Port, and True Dual Port. Single Port provides access to the memory through a single clock and data port, Simple Dual Port provides basic two-port functionality with a shared clock, and True Dual Port provides two independent ports with separate clocks for maximum flexibility and performance. This IP core is a versatile and high-performance solution for embedded systems and integrated circuits with memory requirements. The figure 2 shows the top level diagram of On Chip Memory.

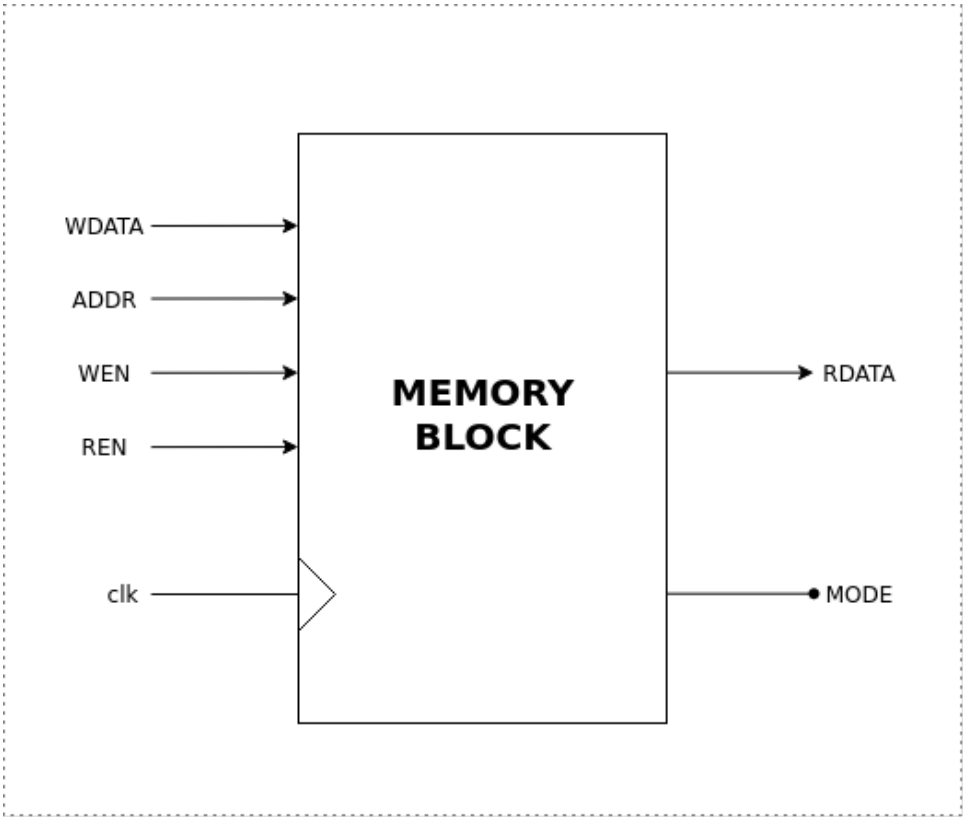

Figure 2. Top Module

IP Support Details

The Table 1 gives the support details for On Chip Memory.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	Non-Standard	Verilog	SDC	Verilog	brams_sim	Raptor	Raptor	Raptor

Table 1. Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	MEMORY_TYPE	SP	BRAMS	1
	DATA_WIDTH	32	LUTS	0
	WRITE_DEPTH	1024	CELLS	1
	-	-	REGISTERS	0
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	MEMORY_TYPE	TDP	BRAMS	128
	DATA_WIDTH	128	LUTS	3024
	WRITE_DEPTH	32768	CELLS	3152
	COMMON_CLK	TRUE	REGISTERS	0

Table 2. Resource Utilization

Ports

Table 3 lists the top interface ports of the On Chip Memory.

Signal Name	I/O	Description
Global Signals		
clk	I	Clock for Synchronization of two Ports
Port A		
clk_A	I	Clock for Port A of RAM
addr_A	I	Address Width of Port A
din_A	I	Input Data Port for RAM
wen_A	I	Write Enable to Port A
ren_A	I	Read Enable to Port A
dout_A	O	Output Data Port from RAM
Port B		
clk_B	I	Clock for Port B of RAM
addr_B	I	Address Width of Port B
din_B	I	Input Data Port for RAM
wen_B	I	Write Enable to Port B
ren_B	I	Read Enable to Port B
dout_B	O	Output Data Port from RAM

Table 3. On Chip Memory Interface

Parameters

Table 4 lists the parameters of the On Chip Memory Generator.

Parameter	Values	Default Value	Description
MEMORY_TYPE	SP, SDP, TDP	SP	Desired Memory Type
DATA_WIDTH	32, 64, 96, 128	32	Data Width of Memory
WRITE_DEPTH	2-32768	1024	Depth of Memory
COMMON_CLK	True/False	False	Common Clock for both Ports

Table 4. Parameters

Features Description

1. **Single Port RAM (SP)**

   A Single-Port RAM is a type of Random Access Memory that has only one port for reading and writing data. It allows only one operation (read or write) at a time, thus making it less flexible compared to a dual-port RAM which has two ports allowing for both read and write operations to occur simultaneously. Single-port RAM is commonly used in applications where cost and/or chip area are a concern, as they are simpler to implement and consume less resources compared to a dual-port RAM. It is shown in figure 3.

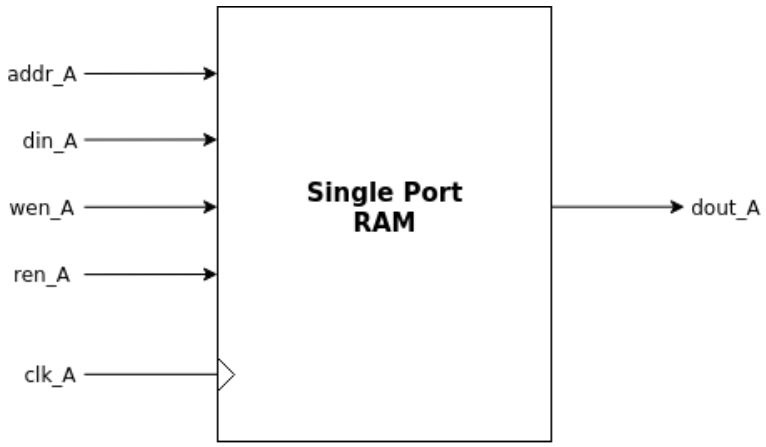

Figure 3. Single Port RAM

2. **Simple Dual Port RAM (SDP)**

   A Simple Dual-Port RAM is a type of Random Access Memory that has two independent ports, allowing for simultaneous read and write operations. This makes it more flexible compared to a single-port RAM, as it can handle multiple access requests at the same time. It is commonly used in applications where multiple processors or systems need to access shared memory simultaneously. It is shown in figure 4.

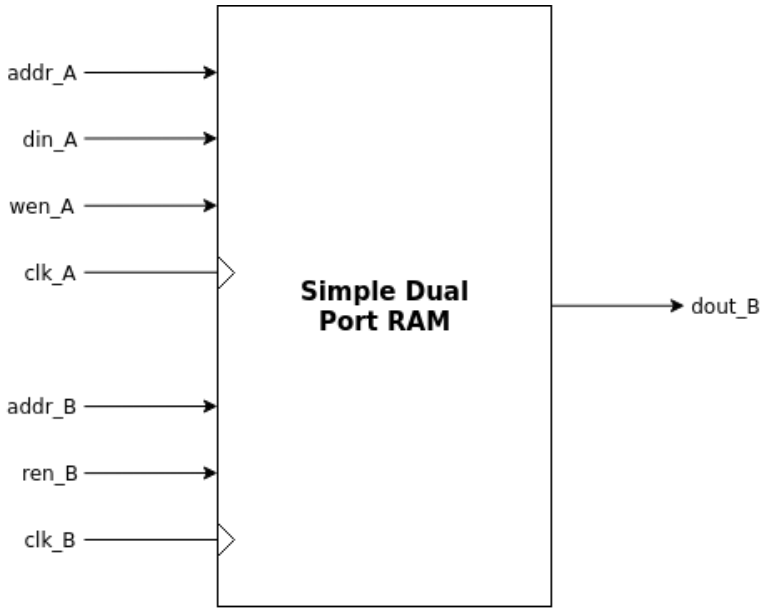

Figure 4. Sinple Dual Port RAM

Features Description

3. **True Dual Port RAM (TDP)**

   A True Dual-Port RAM is a type of Random Access Memory that has two completely independent ports, allowing for truly simultaneous and non-interfering read and write operations. Unlike a simple dual-port RAM, which may share certain elements such as data buses or address decoders, a true dual-port RAM has completely separate components for each port, allowing for truly independent and parallel access to the memory. True dual-port RAMs are commonly used in applications where the highest level of parallelism is required, such as in high-speed communication systems, real-time video processing, and other high-performance applications. It is shown in figure 5.

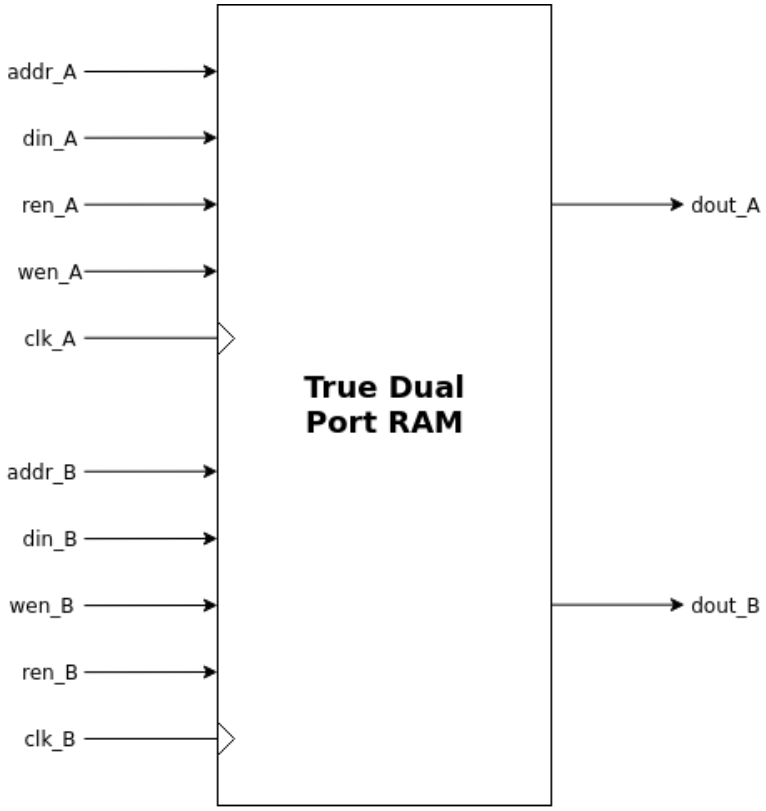

Figure 5. True Dual Port RAM

Design Flow

IP Customization and Generation

On Chip Memory IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configurator window as shown in figure 6.

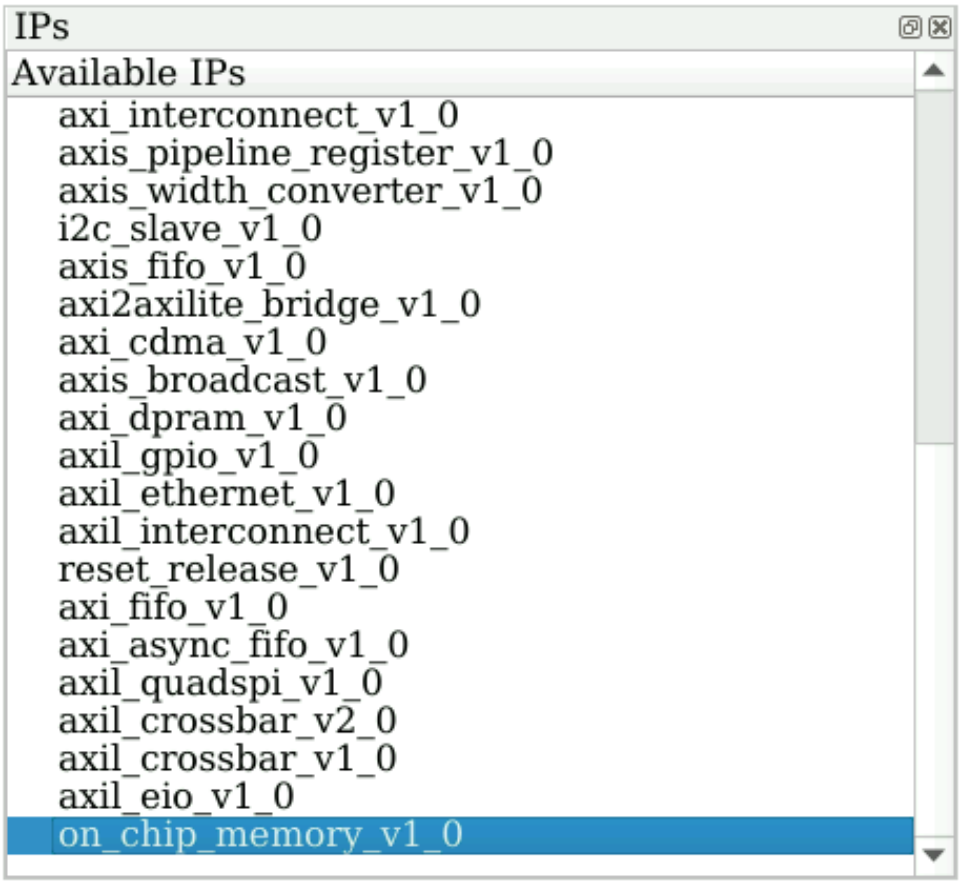

Figure 6. IP list

Parameters Customization: From the IP configuration window, the parameters of the On Chip Memory can be configured and it's features can be enabled for generating a customized On Chip Memory IP core that suits the user application requirements. All parameters are shown in figure 7.

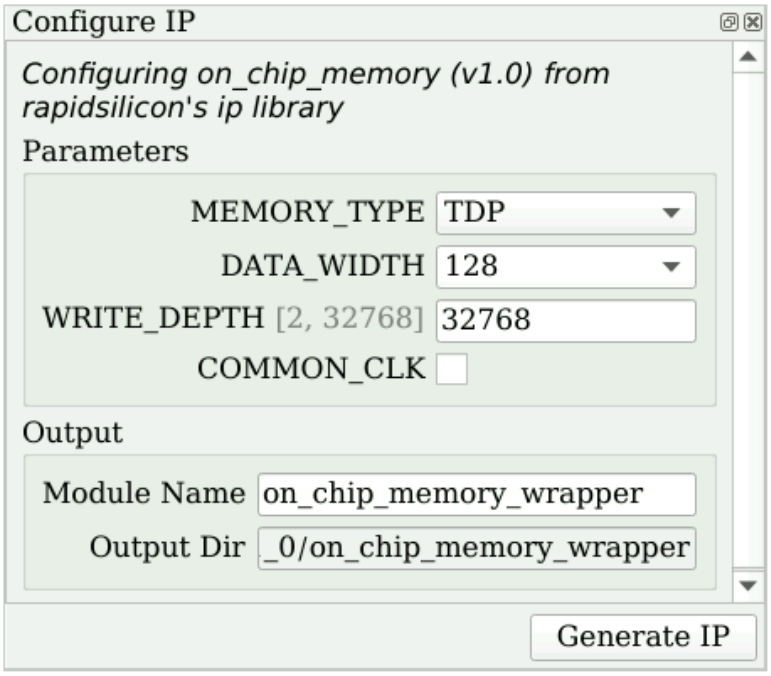

Figure 7. IP Configuration

Test Bench

The testbench attached with On Chip Memory Generator is Single Port RAM 32x1024. It is basically a comparison between the behavioural RTL and the generated RTL. This test provides 1024 random inputs to addr_A and din_A of both the RTLs and in the end, it compares all the outputs. If all the outputs match, then test will be passed otherwise it'll be failed.
The results of this test are attached below in figure 8.

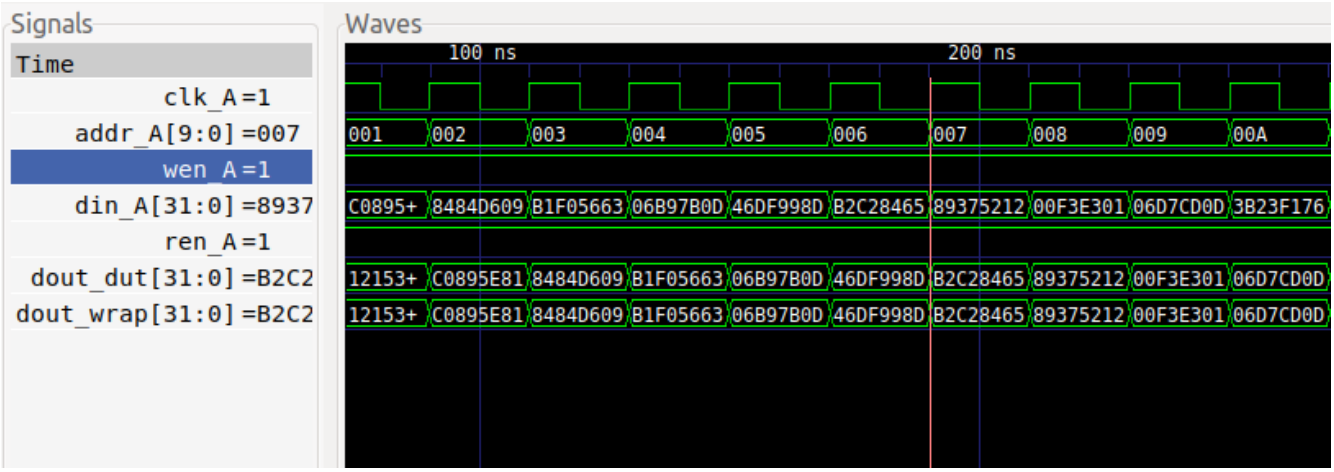

Figure 8. Test Result

Revision History

Date	Version	Revisions
January 31, 2023	0.01	Initial version On Chip Memory Generator User Guide Document