AXI4 FIFO v1.0

IP User Guide (Alpha Release)

January 25, 2023

RapidSilicon

Contents

IP Summary

Introduction

A FIFO is a type of memory buffer that is designed to organize and manipulate the data in such a manner that the oldest element is processed first. In a FIFO queue, the first item added to the queue is the first one to be removed. This is an AXI4 compliant FIFO IP for easy integration with other AXI based systems. A macro block diagram for the top level of this AXI4 FIFO is shown in Figure 1.

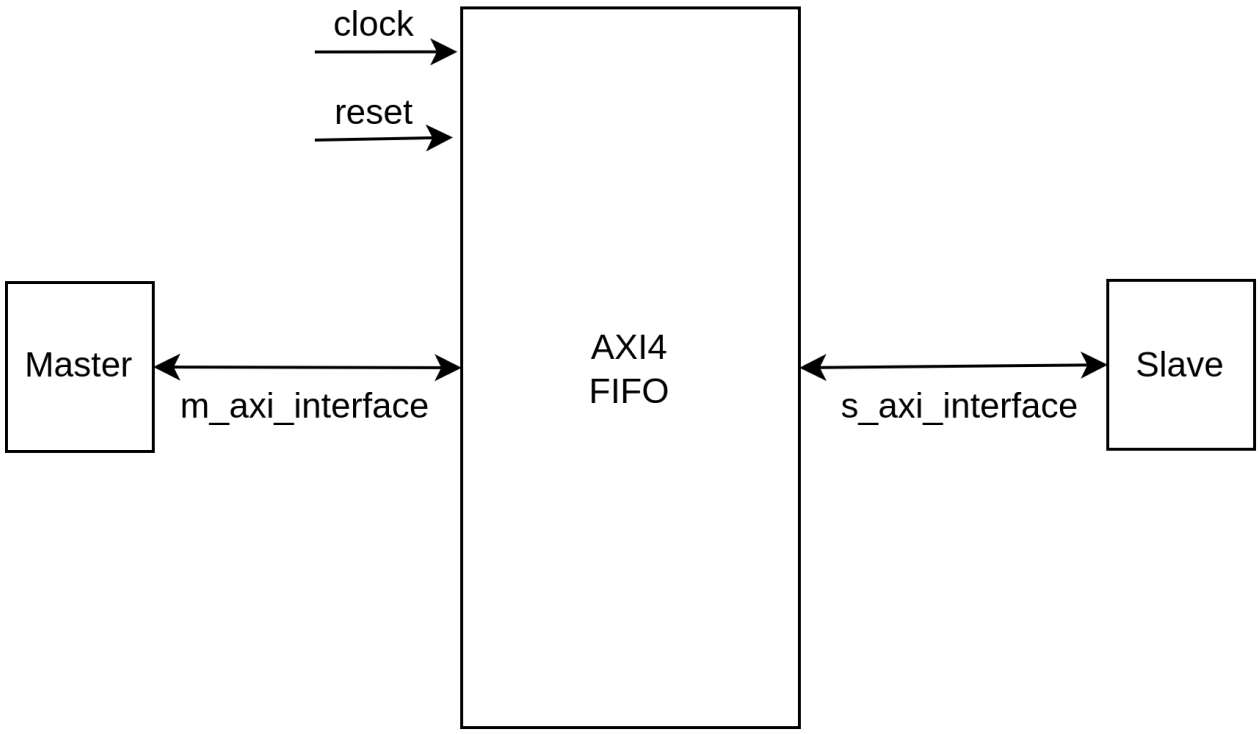

Figure 1. AXI4 FIFO Block Diagram

Revision History

Date	Version	Revisions
January 25, 2023	0.01	Initial version AXI4 FIFO User Guide Document