On-Chip Logic Analyzer v1.0

***IP User Guide** (Beta Release)*

May 29, 2024

RapidSilicon

Contents

IP Summary

Introduction

The On Chip Logic Analyzer (OCLA) core is a customizable logic analyzer that allow the user to debug a design. The internal signal of the design mapped on to the FPGA can be monitored using ocla. The user can set a trigger condition. The OCLA will capture the waveform of the signal of interest when trigger condition is met. The waveform can be analyzed for the user to determine the behavior of the design.

The OCLA core boasts a variety of features commonly found in modern logic analyzers, such as edge transition triggering, multi-trigger options, and configurable parameters such as the number of probes and trace memory depth.

Additionally, the OCLA offers several modes for data capturing operations during debugging, including continuous, pre-trigger, post-trigger, and center-trigger options.

Features

- Multiple Probe Ports
- Single and Multiple Sampling Clock support
- Emulated Input/Output (EIO) support
- Configurable trigger condition
- Configurable trigger mode
- Configurable data depth
- Cross Triggering support
- AXI probes on OCLA IP core to debug AXI IP cores in a system

Overview

On-Chip Logic Analyzer

The OCLA is an IP core that can be used to monitor and capture the behavior of signals that are connected to its "probe port." The OCLA IP communicate through the JTAG interface with the software running on a PC. The software will allow the user to set OCLA mode and controls as well as dumped the waveform and allow the user to view the waveform.

The signals, attached to the probe inputs, are sampled at design speeds and stored using on-chip block RAM (BRAM). The core parameters specify the number of probes, sample memory depth,debug mode and the width for each probe input. Communication with the OCLA core is conducted using JTAG interface of the FPGA.

The figure 1 shows the top-level interface diagram of the OCLA IP core.

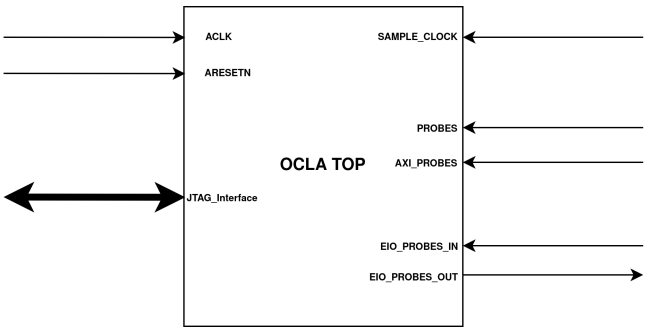


Figure 1. OCLA Top

After the design is loaded into the FPGA, use the OCLA tcl commands to set up a trigger event for the OCLA measurement. After the trigger occurs, the sample buffer is filled. You can view this data using the GTK waveform.

TCL commands can be found in OCLA Debug Guide.

Licensing

IP Specification

Overview

The OCLA IP is characterized by a modular design, comprising various modules such as the JTAG Interface, Trigger Control Unit, Sampler Buffer, Controller, and On-Chip Trace Memory modules. Furthermore, it is designed as a multi-clock system, with a sampling clock and an AXI clock.

The sampling clock is synchronized with the clock of the System/Design under test (S/DUT) and is used to sample data on the rising edge of this clock, based on the configured sampling mode of the OCLA. OCLA can be configured through the JTAG interface using tcl commands and the collected data can be subsequently read via the JTAG.

The On-Chip trace memory controller is implemented as a circular buffer based on a modified asynchronous FIFO. This design handles the clock domain crossing of the trace memory data and configuration data, ensuring efficient and accurate data transfer between the different modules.

The figure 2 presents an overview of the Debug Core in a practical use case.

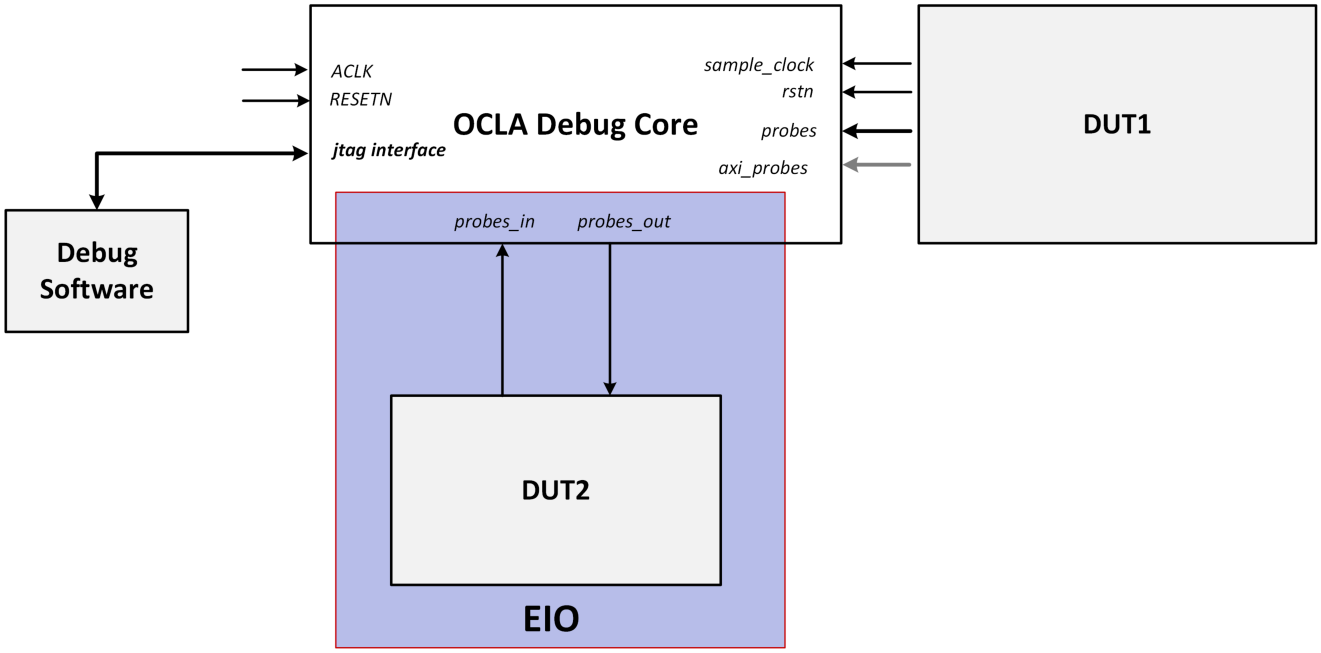


Figure 2. OCLA System Level Block Diagram

Probes

A probe is conssist of one or more signals selected by the user to represent a bus. The IP supports 15 native probes, allowing users to connect signals for debugging purposes. The size of each native probe can be configured within the range of 1 to 1024. The OCLA UI also allow user to select AXI mode interface which will add AXI bus signals automatically with compliant with AXI protocol. If the IP is configured in AXI Lite or AXI Full mode, users will have access to AXI probes. These AXI probes enable users to connect to the AXI bus for debugging purposes, providing a convenient way to debug AXI bus-related issues.

EIO Capability

The Emulate Input/Output (EIO) IP is a feature where the internal design nodes can act like a virtual input and output ports. Using this debugging core feature, users can both monitor and actively control internal FPGA signals in real time. The number and width of the input and output ports are customizable to interface with the FPGA design. The core facilitates input and output probes, enabling the virtual driving of logic blocks and verification of their functionality.

To drive any signal within the design, the user must connect it to the probes_out port of the IP core. Similarly, to monitor any signal in real time from the Design Under Test (DUT), it needs to be connected to the probes_in port of the IP core.

MODE

The OCLA IP core can be configuered in the following three modes.

- **NATIVE** In this mode the the user will be allowed to set number of probes that can be varry from 1 to 15 if sampling frequency is set to MULTIPLE. In case user want to use single sampling frequency then maximum allowed probes are 2. User can set the width of each probes that range from 1 to 1024. Once the IP is generated, the signals that user want to debug can be connected to these probes.
- **AXI** In this mode the user can select AXI Lite or AXI Full interface. The mode can be used if user wants to debug an AXI bus. The IP will be genrated having AXI probes where user can probes their AXI bus signals that he wants to debug.
- **NATIVE_AXI** This is dual mode where user can connect custom signals as well as AXI bus. In this mode the user is allowed to select number of probes and AXI type.

Trigger

The OCLA IP core utilizes a trigger mechanism to initiate the capture of probe data samples. The trigger signal can be selected from a variety of sources, including probe input signals or axi probe signal.
OCLA also allows for the configuration of various trigger conditions on the trigger signal, such as level, edge, and value compare. The OCLA continually monitors the trigger signal, and data sampling begins when all of the trigger conditions in the active trigger pattern are satisfied.
Additionally, the OCLA features a user-configurable trigger mode setting, which determines the amount of data that should be acquired by the system prior to and following the trigger event. The acquired data is stored in a circular buffer for further analysis, which enables the system to efficiently handle large data sets and continuously update the data being captured.

OCLA supports four triggers per probe. For example if MODE is set to NATIVE and sampling frequency is set to SINGLE. In that case maximum number of probes are 2 and total supported trigger will be 8.

Cross Triggering Support

The core sampling clock can be set to SINGLE or MULTIPLE. In case of SINGLE there will be single sampling clock and maximum two probes can be added where each probe size can varry from 1 to 1024 to support upto 2048 probes. The OCLA core support cross trigger means that user can put triggers on either probe because OCLA core will look into trigger condition of both probes. In case of MULTIPLE clock domain there will be seperate sampling clock for each probe and user can put triggers within a probe only that can varry from 1 to 1024

Trigger Conditions

Multiple options for trigger conditions are available for probe and input triggers signals. Following lists the trigger conditions:

Trigger Condition	Description
Don't Care	Default trigger condition. This is immidiate trigger. As soon as the OCLA start sampling, it will not wait for any event
Low level	OCLA triggers when the probe channel is low.
High level	OCLA triggers when the probe channel is high.
Falling Edge	OCLA triggers on the falling edge the probe channel.
Rising Egde	OCLA triggers on the rising edge the probe channel.
Either Edge	OCLA triggers on either edge of the probe channel.
Value Comparison	OCLA triggers when the value of a probe channel is equal /less than / greator than some user specified value.
Boolean Trigger equations	Advance Trigger Conditions AND, OR, <, >, == etc

Table 1. Trigger Conditions

Trigger Modes

The common trigger modes are post trig, pre trig, center and countinous.

- **Pre triggered** In Pre Trigger the OCLA will start sampling once the trigger condition met and will store the samples in buffer.
- **Post triggered** is the opposite and in this mode the logic analyzer stops the sampling immediately when the trigger is raised thus only storing data from before the triggering event.
- **Center triggered** is a combination putting the triggering event in the middle of the sampled data set. In center trigger the 50% samples will be count before trigger and 50% samples after trigger.
- **No trigger** mode OCLA sample data without waiting for any trigger event.

Fix number of samples

The OCLA IP core can be configured to dynamically sample a specified number of probe samples, rather than utilizing the default trace memory depth, at runtime. This allows for greater flexibility in the debuging process, as the number of probe samples can be adjusted to suit the specific requirements of runtimme debuging.

Standards

The OCLA can be configured and samples can be read via standarad JTAG interface.

IP Support Details

The table 2 presents the specifics of IP support for the OCLA IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
VIRGO	JTAG	SV	SDC	SV	-	-	Raptor	Third Party	Raptor

Table 2. IP Information

Resource Utilization

The table 3 presents the resources utilization of OCLA IP for the Virgo device within the Raptor Design Suite, specifically detailing the statistics of resource utilization for both the minimum and maximum configurations of the OCLA.

Configuration		Resource Utillization		
Minimum Resource	Options	Configuration	Resources	Utillized
	Number of Probe	1	LUT	263
	Trace Memory Depth	32	FLOPS	138
	EIO Enable	OFF	BRAM	1
	Mode	NATIVE	DSP	0
Maximum Resource	Options	Configuration	Resources	Utillized
	Number of Probe	1024	LUT	1068
	Trace Memory Depth	1024	FLOPS	5466
	EIO Enable	ON	BRAM	29
	Mode	NATIVE	DSP	0

Table 3. Resource Utillization

Ports

Table 5 lists the top interface ports of the OCLA.

Signal Name	I/O	Size	Description
Sampling Clock and Reset			
native_sampling_clk	I	1	Clock to Sample the Probe Data. It must be same as the Design under test
axi_sampling_clk_clk	I	1	Clock to Sample the AXI Bus data. It must be same as the Design under test
RESETn	I	1	Reset port of OCLA and it must be same as design under test
AXI Clock			
ACLK	I	1	AXI main clock
JTAG Interface			
JTAG_TCK	I	1	JTAG clock signal
JTAG_TMS	I	1	JTAG standard TMS
JTAG_TDI	I	1	JTAG standard TDI
JTAG_TDO	O	1	JTAG standard TDO
JTAG_TRST	I	1	JTAG reset signal
Emulated Input_Ouput (EIO) Ports			
eio_ip_clk	I	1	EIO input port clock
eio_op_clk	I	1	EIO output port clock
probes_in	I	1-512	EIO Input probes
probes_out	O	1-512	EIO output probes
OCLA Probes			
probe<n>	I	1-1024	OCLA Probes port in NATIVE mode. <n> can varry from 1 to 15
axi4_probes<n>	I	250 - 500	OCLA Probes port in AXI Full mode. This port name just reflects all signals of AXI4. <n> can varry from 1 to 2
axiLite_probes<n>	I	152-304	OCLA Probes port in AXI Lite mode. This port just reflects all signals of AXI4 Lite. <n> can varry from 1 to 2

Table 5. OCLA Interface

Parameters

Table 5 lists the parameters of the OCLA.

Parameters	Values	Default Value	Description
IP_TYPE	"ocla"	"ocla"	Define IP Type
IP_VERSION	32'h00000001	32'h00000001	Define IP Version.
IP_ID	Auto Generated	Auto Generated	Define IP ID which will be generated by the IP generator at run time
MODE	"NATIVE", "AXI", "NATIVE_AXI"	"NATIVE"	Define mode of OCLA
AXI_TYPE	"AXI4", "AXILite"	"AXILite"	Select AXI Type. Valid only if AXI or NATIVE_AXI mode is set
EIO_Enable	0 - 1	0	Enable EIO capability.
SAMPLING_CLK	"SINGLE", "MULTIPLE"	"SINGLE"	Set sampling clock type
NO_PROBES	1-15	1	Total Number of Probes. Valid in NATIVE and NATIVE_AXI mode only
MEM_DEPTH	32, 64, 128, 256, 512,1024	32	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
Probe<n>_Width	1-1024	1	Define size of each probe. <n> range from 1 to 15.
INPUT_PROBE_WIDTH	1- 512	1	Input probe size for EIO IP
OUTPUT_PROBE_WIDTH	1- 512	1	Output probe size for EIO IP

Table 5. Parameters

Design Flow

IP Customization and Generation

OCLA IP core is a part of the Raptor Design Suite Software. A customized ocla can be generated from the Raptor's IP configurator window.

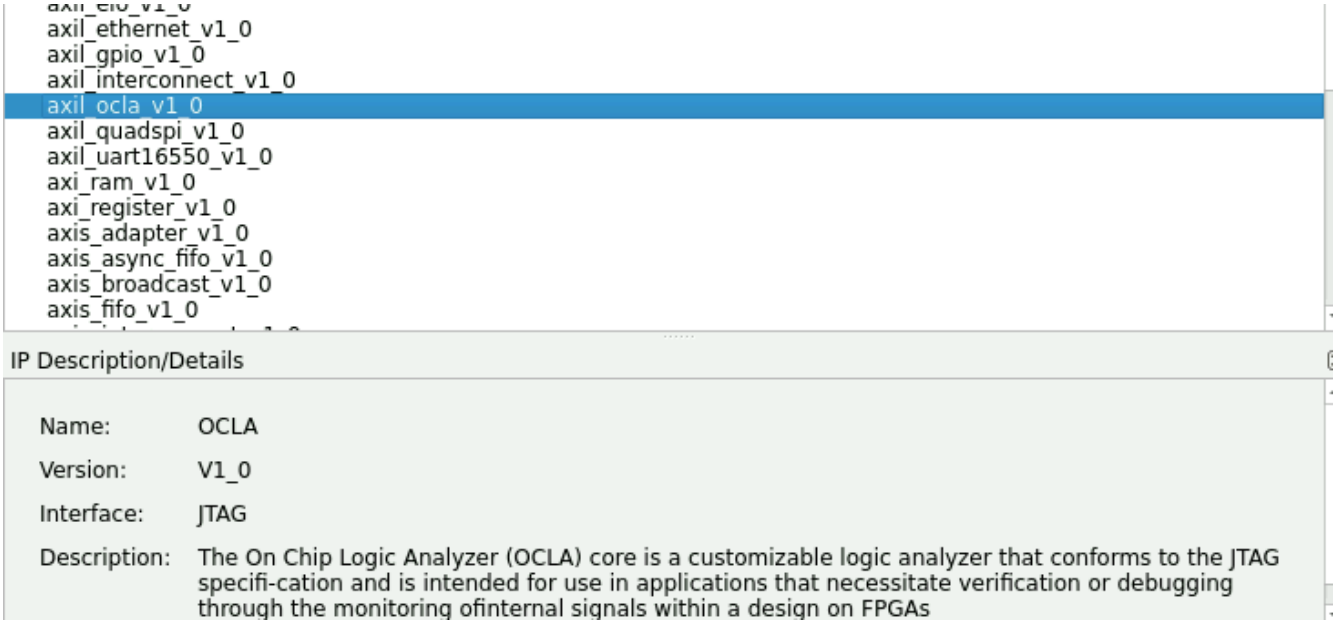


Figure 3. IP list

Parameters Customization: From the IP configuration window, the parameters of the OCLA can be configured and OCLA features can be enabled for generating a customized OCLA IP core that suits the user application requirment.

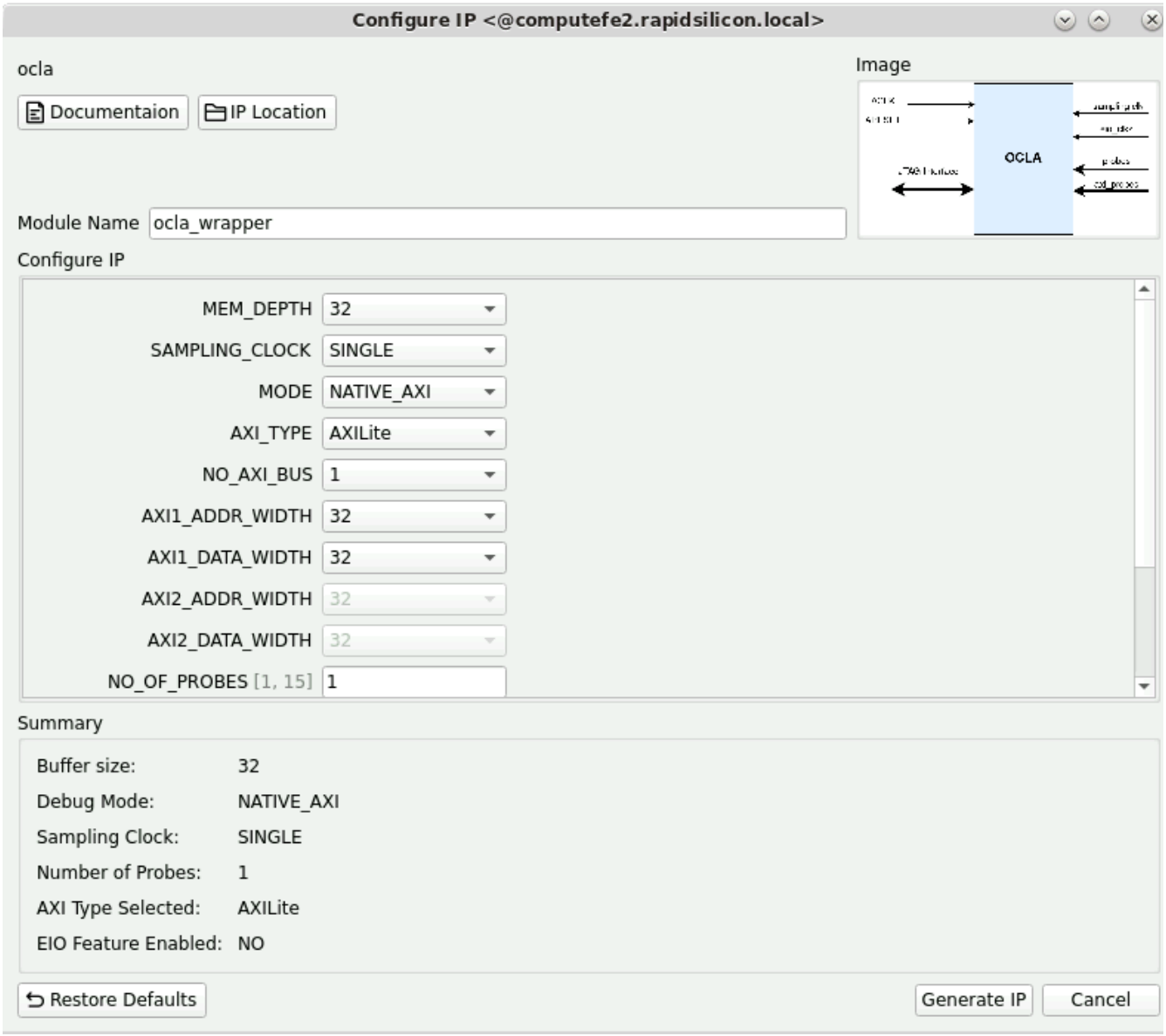


Figure 4. IP Configuration

OCLA Debug Subsystem

The Generated OCLA IP Wrapper

The IP customization and generation step is followed by the availability of a top wrapper and all source files for the user. The generated top wrapper file for the OCLA comprises of two distinct clock domains, namely the sample clock and the AXI clock.

It is crucial to note that the sample clock of the OCLA should be connected to the design being monitored, while the AXI clock should be connected to the main clock if clocks are different.

The signals of the design that are intended to be sampled are connected to the probes port of the OCLA. If the OCLA is configured in AXI mode then axi ports will be available at the top wrapper of the IP core where user can connect their AXI bus that he wants to debug.

For configuring the OCLA and reading the sampled data from the system, the JTAG interface must be connected to an GPIO through which IP will communicate with the software.

OCLA Debug Subsystem

The OCLA IP core, can be instantiated within a subsystem. The debug subsystem, as depicted in Figure 5, integrates the OLCA IP core within the design being monitored. The purpose of this integration is to allow for the runtime configurations of OCLA configurations through the use of the JTAG interface.

This interface serves as the primary means of controlling and configuring the OCLA IP core within the subsystem, enabling the debugging process to proceed efficiently.

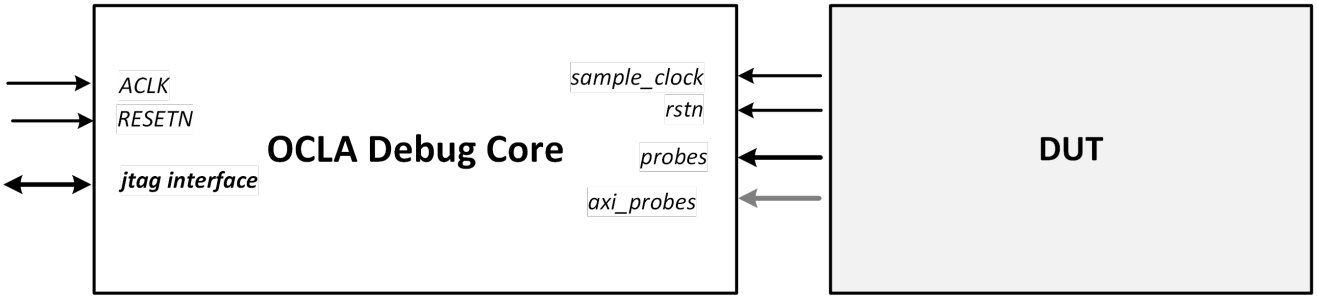


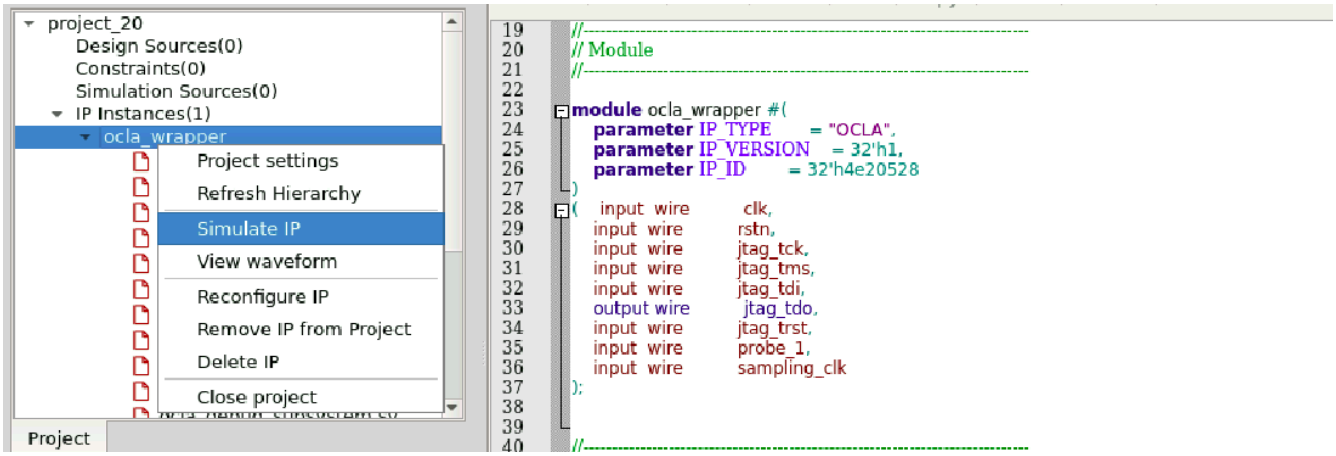
Figure 5. OCLA Debug Subsystem

Test Bench

To check the behavior of the IP Core, a verilog test-bench with basics configuration is available for simulation. Once the IP is generated then test-bench file can be found in the IP directory under sim folder.

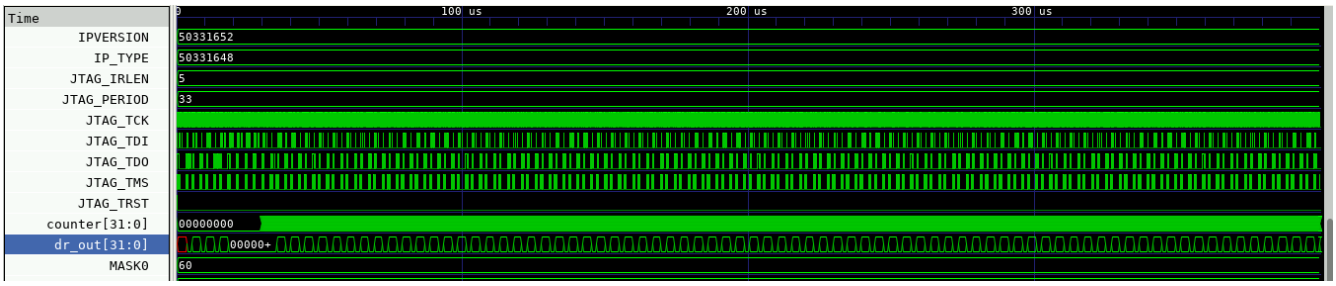
Running Simulation

1. Right click on the IP name within source tab and select Simulate IP as shown in figure below. ONce the simulation starts, first the IP Type, IP ID and IP Version registers will be read. After that OCLA will be configuered in rising edge and pre trigger mode. The OCLA probes are connected to a counter. Once the trigger condition met, the OCLA will samples the counter value and can be analyze using GTK waveform.



Running Simulation

2.This will run the simulation and result will dumped into vcd file.To see the waveform, again right click on the IP and select View waveform. The GTKWave will open showing the IP simulation result as shown in figure below.



Simulation Result

References

A comprehensive guide explaining how to use OCLA to debug a design can be found here.

Revision History

Date	Version	Revisions
May 29, 2024	0.01	Initial version OCLA User Guide Document