JTAG to AXI v1.0

***IP User Guide** (Beta Release)*

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Contents

IP Summary

Introduction

The JTAG-to-AXI IP is an AXI4 compliant IP that can be used to initiate AXI4 transactions inside the FPGA. The IP provides an AXI4 master interface on one side and a JTAG interface on the other side. The IP is most suited for use in debugging of AXI4 compliant IP cores and can send test vectors to AXI4 memory mapped slaves in order to verify their functionality.

Features

- AXI4 master interface for integration with logic modules.
- Configurable data width of AXI4 bus (32/64 bits).
- Dedicated 68 or 100 bits wide AXI data-in register containing address, 32 or 64 bits data and other control signals.
- Dedicated 34 or 66 bits wide AXI data-out register containing 32 or 64 bits read data from AXI4 slaves.
- Continuous AXI4 read transactions in fixed and incremental address mode.

Overview

JTAG to AXI

The JTAG-to-AXI IP is an AXI4 compliant IP that can be used to initiate AXI4 transactions inside the FPGA. The IP provides an AXI4 master interface on one side and a JTAG interface on the other side. The IP is most suited for use in debugging of AXI4 compliant IP cores and can send test vectors to AXI4 memory mapped slaves in order to verify their functionality. The IP implements standard 1-bit bypass register, 32-bit ID register and 5-bit instruction registers. Other than the standard registers, the IP also provides two user registers which can be used to send and receive data from AXI4 slaves. Figure 1 shows a high level block diagram of the JTAG-to-AXI IP.

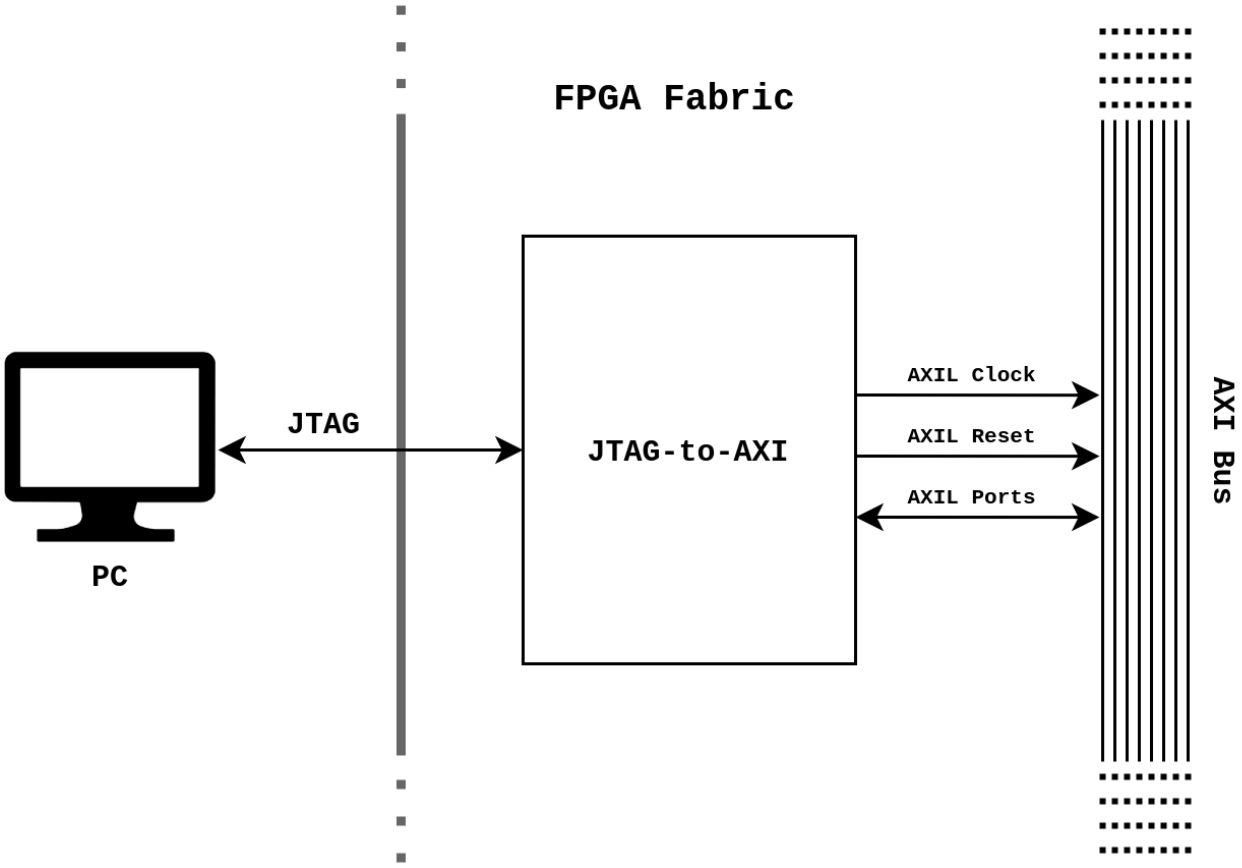

Figure 1. JTAG-to-AXI core use case.

Licensing

IP Specification

Overview

The figure 2 shows the high level block diagram of JTAG to AXI IP core. This section explain the specification of JTAG to AXI IP core. The IP has two clock domains. One clock domain which operates at a frequency of 30 MHz is the JTAG clock domain and the other is the AXI clock domain which operates at frequencies of up to 100 MHz. All signals in the JTAG logic are sampled on the rising edge of TCK and shifted out on the falling edge of TCK clock. Whereas, the AXI interface signals are sampled on the positive edge of the input clock ACLK. For the JTAG logic, the input signal TRST is used for reset. TRST is an asynchronous active-low reset signal. For the AXI logic, the input signal aresetn is used. This is also an asynchronous active-low reset.

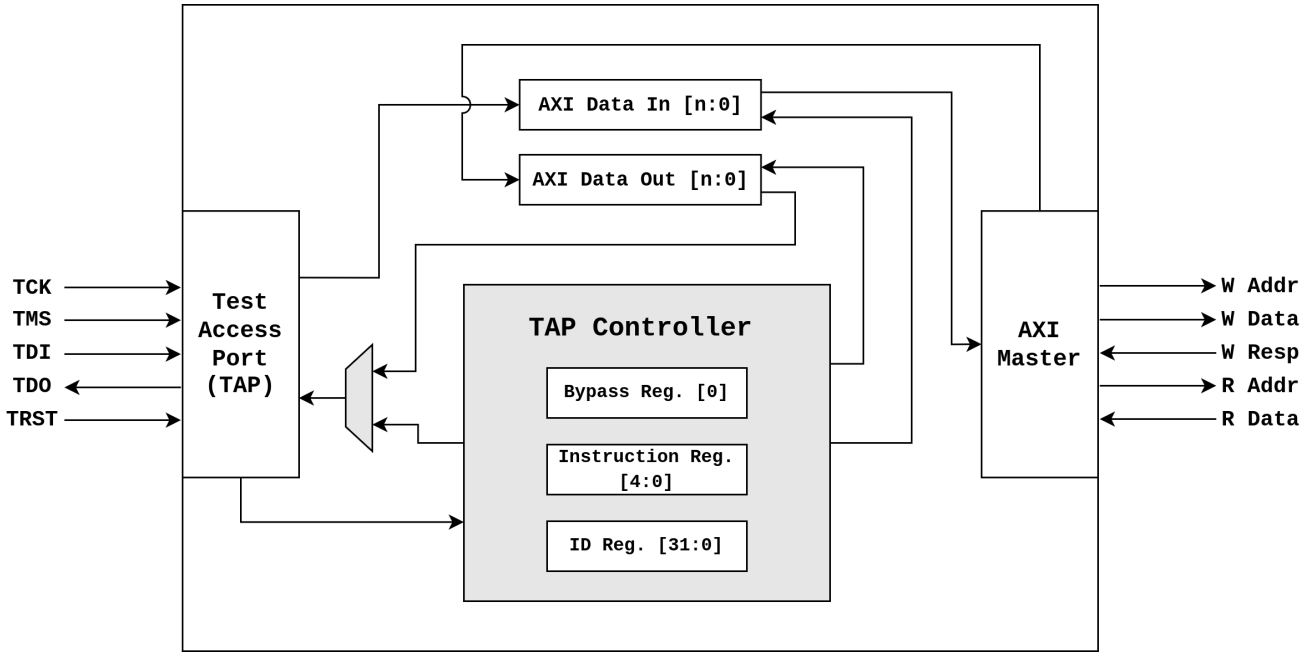

Figure 2. Top Module

Standards

The AXI4 interfaces is compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The table below presents the specifics of IP support for the JTAG-to-AXI IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources			Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Analysis and Elaboration**	**Simulation**	**Synthesis**
Gemini	AXI4-Lite	Verilog	SDC	Systemverilog	Raptor	Raptor	Raptor

Table 1. JTAG-to-AXI support details.

Resource Utilization

Tool	Raptor Design Suite			
FPGA Device	Gemini			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	AXI data bus width	32	LUT	331
			DFF	395
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	AXI data bus width	64	LUT	427
			DFF	585

Table 2. JTAG-to-AXI resource utilization.

Ports

Table-4 lists AXI Master I/O signals.

Signal Name	I/O	Description
AXI Clock and Reset		
ACLK	I	AXI4 Source Clock
ARESET	I	AXI4 Active High RESET
AXI WRITE ADDRESS CHANNEL		
m_axi_id	O	ID for for Write Address channel.
m_axi_awaddr	O	Address bus for Write Address channel.
m_axi_awlock	O	Not supported in AXI4.
m_axi_awcache	O	Cache for Write Address channel.
m_axi_awprot	O	Write Address channel Protection.
m_axi_awregion	O	No implementation, set to 4'b0000.
m_axi_awuser	O	No implementation, set to 4'b0000.
m_axi_awqos	O	No participation in QoS scheme so set to 4'b0000.
m_axi_awvalid	O	Address Valid for Write Address channel.
m_axi_awready	I	Address Ready for Write Address channel.
m_axi_awburst	O	Write Address channel Burst type.
m_axi_awlen	O	Burst Length for Write Address channel.
m_axi_awsize	O	Burst Size for Write Address channel.
AXI WRITE DATA CHANNEL		
m_axi_wdata	O	Write Data bus for Write Data channel
m_axi_wstrb	O	Write Data strobe for Write Data channel.
m_axi_wlast	O	Last signal for Write Data channel.
m_axi_wuser	O	No implementation, set to 4'b0000.
m_axi_wvalid	O	Data Valid for Write Data channel.
m_axi_wready	I	Data Ready for Write Data channel.
AXI WRITE RESPONSE CHANNEL		
m_axi_bresp	I	Response for Write Response channel.
m_axi_bvalid	I	Valid for Write Response channel
m_axi_bready	O	Ready for Write Response channel..
m_axi_buser	O	No implementation, set to 4'b0000.
AXI READ ADDRESS CHANNEL		
m_axi_arid	O	ID for for Read Address channel.
m_axi_araddr	O	Address bus for Read Address channel.
m_axi_arlock	O	Not supported in AXI4.
m_axi_arcache	O	Cache for Read Address channel.
m_axi_arprot	O	Read Address channel Protection.
m_axi_arregion	O	No implementation, set to 4'b0000.
m_axi_aruser	O	No implementation, set to 4'b0000.
m_axi_arwos	O	No participation in QoS scheme so set to 4'b0000.
m_axi_arvalid	O	Address Valid for Read Address channel.
m_axi_arready	I	Address Ready for Read Address channel.
m_axi_arburst	O	Read Address channel Burst type.
m_axi_arlen	O	Burst Length for Read Address channel.
m_axi_arsize	O	Burst Size for Read Address channel.

AXI READ DATA CHANNEL		
m_axi_rdata	I	Read Data bus for Read Data channel.
m_axi_rlast	I	Last signal for Read Data channel.
m_axi_rvalid	I	Data Valid for Read Data channel.
m_axi_rresp	I	Response for Read Data channel.
m_axi_rready	O	Ready for Read Data channel.
m_axi_ruser	O	No implementation, set to 4'b0000.
JTAG INTERFACE		
JTAG_TCK	I	Test Clock.
JTAG_TMS	I	Test Mode Select.
JTAG_TDI	I	Test Data Input.
JTAG_TDO	O	Test Data Output.
JTAG_TRST	I	Test Reset.

Table 4: AXI Master I/O signal description.

Parameters

Table 5 lists the parameters of the JTAG-to-AXI core.

Parameter	Values	Default Value	Description
AXI DATA WIDTH	32/64	32	Sets the width of AXI bus.

Table 5. JTAG-to-AXI configurable parameters.

Registers Address Space

Table 6 lists the configuration registers of the JTAG-to-AXI.

Name	Register ID	Bits	Access	Offset	Default Value	Description
ID Register	ID	32	RO	-	0x10000000	JTAG ID register
Instruction Register	INSTR	5	RW	-	0x02	JTAG instruction register
Bypass Register	BYPS	1	RW	0x04/0x08	-	JTAG bypass register
AXI Data-In	AXI_DAT_IN	68/ 100	WO	0x04/0x08	0x0	Write data with write/read address with additional and control signals
AXI Data-Out	AXI_DAT_ OUT	34/66	RO	0x04/0x08	0x0	Read data with write/read response

Table 6. JTAG-to-AXI register space.

Register Bank

ID Register

Table-7 lists the parameters of the JTAG-to-AXI core.

Bits	Description
31:0	32-bit ID value.

Table 7: Breakdown of ID register.

Instruction Register

Table-8 lists the parameters of the JTAG-to-AXI core.

Bits	Description
4:0	5-bit instruction code value.

Table 8: Breakdown of Instruction register.

Table-9 below indicate valid values for the instruction register.

Value	Selected register
5'b00010	ID register
5'b00100	AXI-Data In register
5'b01000	AXI-Data Out register
5'b11111	Bypass register

Table 9: Valid values for ID register.

Bypass Register

Table-10 lists the parameters of the JTAG-to-AXI core.

Bits	Description
0	1-bit bypass value.

Table 10: Breakdown of Bypass register.

AXI Data-Out Register

Table-11 lists the parameters of the JTAG-to-AXI core.

Bits	Description
33:32 *or 65:64*	2-bit write/read response channel data from slave
31:0 *or 63:0*	64-bit read data from AXI slave

Table 11: Breakdown of AXI Data-Out register.

AXI Data-In Register

Table-12 lists the parameters of the JTAG-to-AXI core.

Bits	Description
67:66 *or 99:98*	2-bit read mode signal
65:34 *or 97:34*	32 or 64-bit write data
33:2	32-bit write/read address
1	Write/$\overline{Read}$ operation
0	Set this bit to indicate a valid transaction data

Table 12: Breakdown of AXI Data-In register.

Table-13 below indicate valid values for the 2-bit read mode signal.

Value	Selected register
2'b00	Single read mode, only one location is read once
2'b01	Continuous fixed read mode, one specified location is read multiple times
2'b10	Continuous incremental read mode, subsequent locations are read once starting from the specified address
2'b11	Reserved, defaults to single read mode

Table 13: Valid values for ID register.

Design Flow

IP Customization and Generation

JTAG to AXI IP is a part of the Raptor Design Suite Software. A customized IP can be generated from the Raptor's IP configurator window. First enable IP Configurator and then select the jtag_to_axi IP from the IP list.

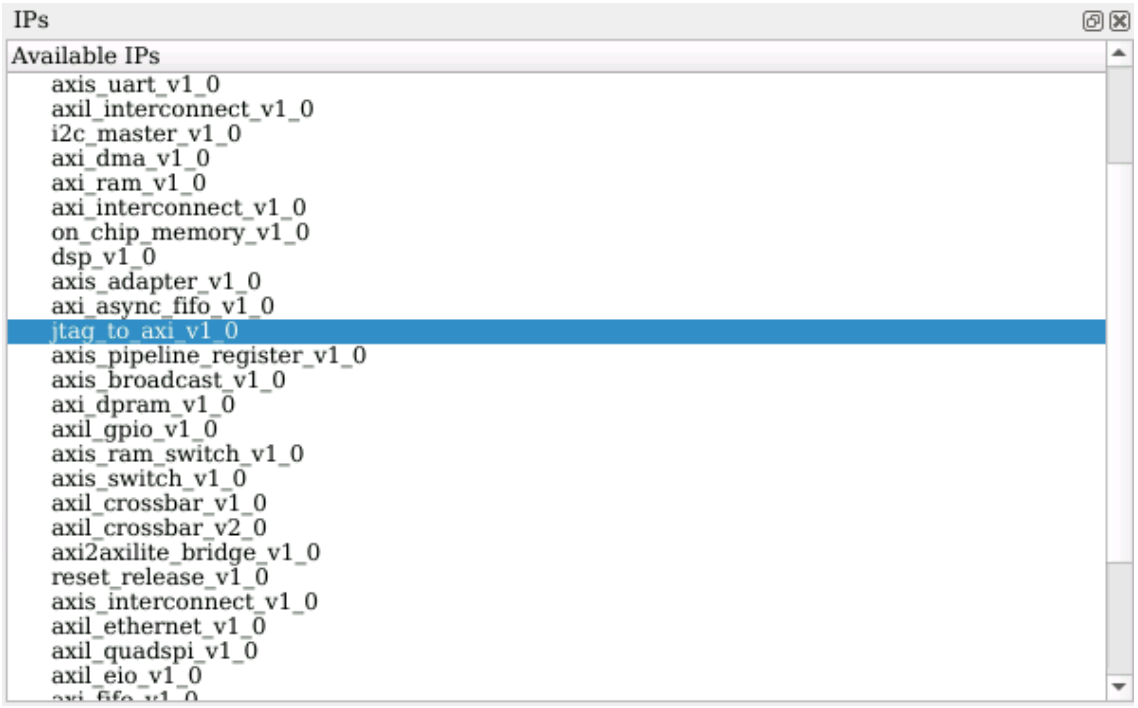

Figure 3: JTAG-to-AXI IP in Raptor IP suite.

Parameters Customization: From the IP configuration window, the parameters of the IP can be configured and jtag_to_axi features can be enabled for generating a customized IP core that suits the user application requirment.

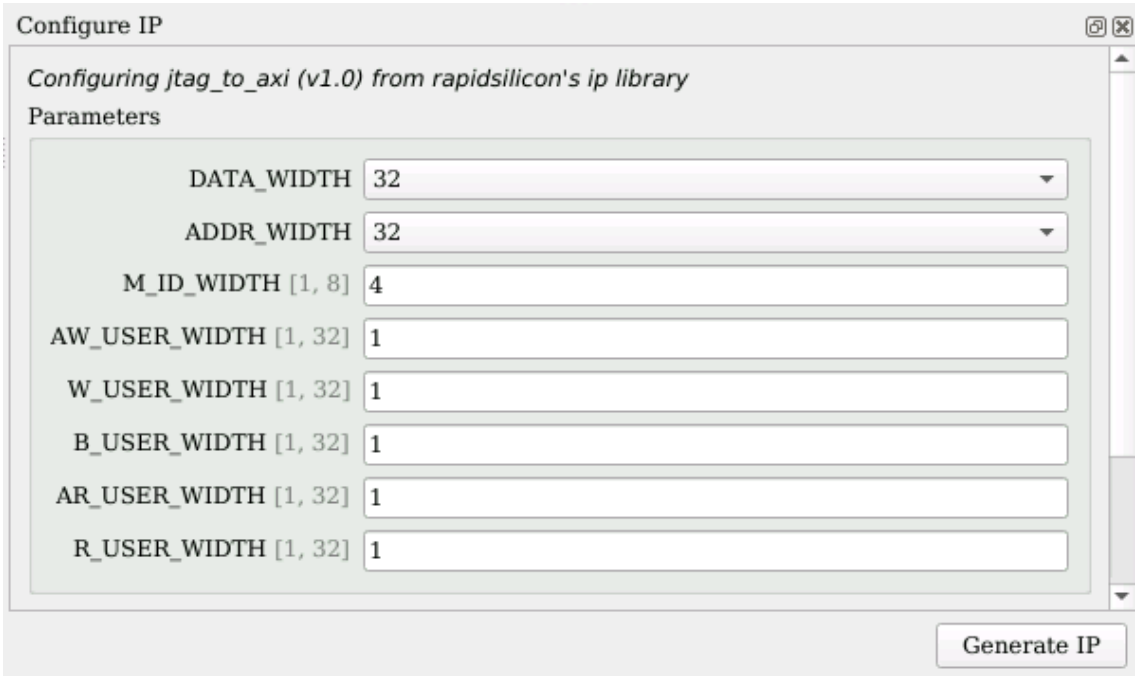

Figure 4: Configurable parameters for JTAG-to-AXI core.

JTAG-to-AXI Debug Subsystem

The Generated JTAG-to-AXI Core Wrapper

The IP customization and generation step is followed by the availability of a top wrapper and all source files for the user. The generated top wrapper file for the JTAG-to-AXI core (see figure 5) comprises of two distinct clock domains: JTAG clock and AXI clock.

The AXI4 master interface connects to AXI4 interface of slaves that need to be debugged. The JTAG interface is controlled by a JTAG compatible external device.

For reading/driving data, the AXI4 master interface must be connected to an AXI bus.

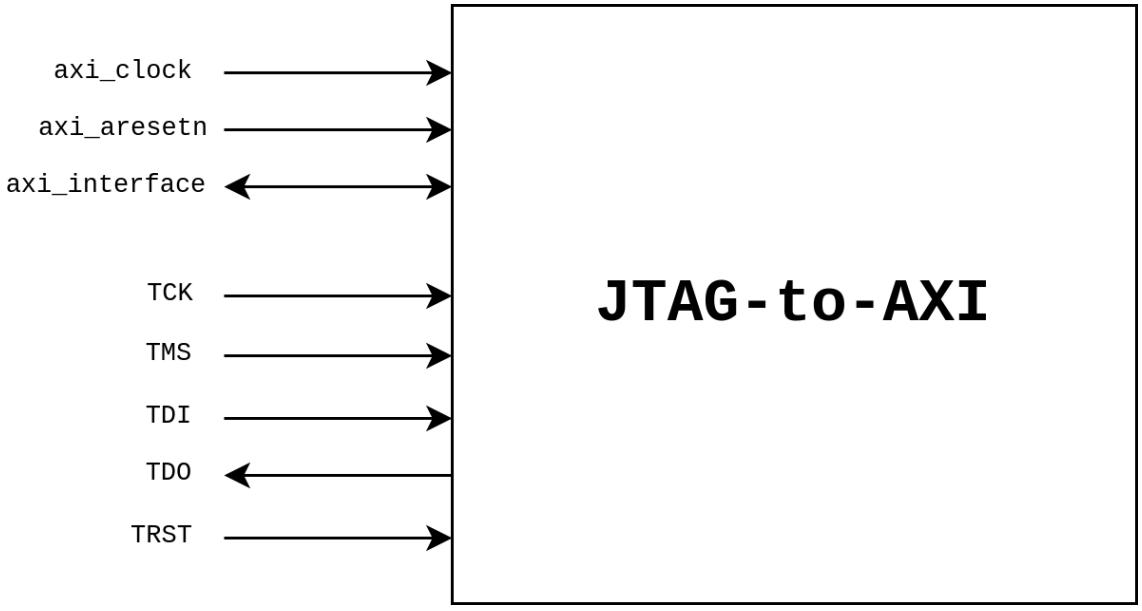

Figure 5. JTAG-to-AXI top wrapper.

JTAG-to-AXI Debug Subsystem

The JTAG-to-AXI core is primarily used to communicate with a design under test that is compliant with the AXI4 protocol. This allows access to internal registers of the DUT through external devices like computers etc.

Example Design

This IP has no example design.

Test Bench

This IP has no test bench.

Revision History

Date	Version	Revisions
February 3, 2023	0.01	Initial version of JTAG to AXI User Guide Document