AXILite UART v1.0

IP User Guide (Alpha Release)

January 25, 2023

RapidSilicon

Contents

IP Summary

Introduction

The AXIL UART is designed to be used with the AXIL bus, which provides a high-speed, low-latency data path between the UART and other components in the system. The AXIL UART is often used to interface with other peripherals such as memory or other processors, or to provide a serial communication link to external devices such as a PC or another microcontroller. UARTs typically include a transmitter and receiver and can be used for a wide range of applications. This is an AXILite compliant UART IP that can be integrated in a number of AXI based systems. A macro block diagram of this AXILite UART is shown in Figure 1.

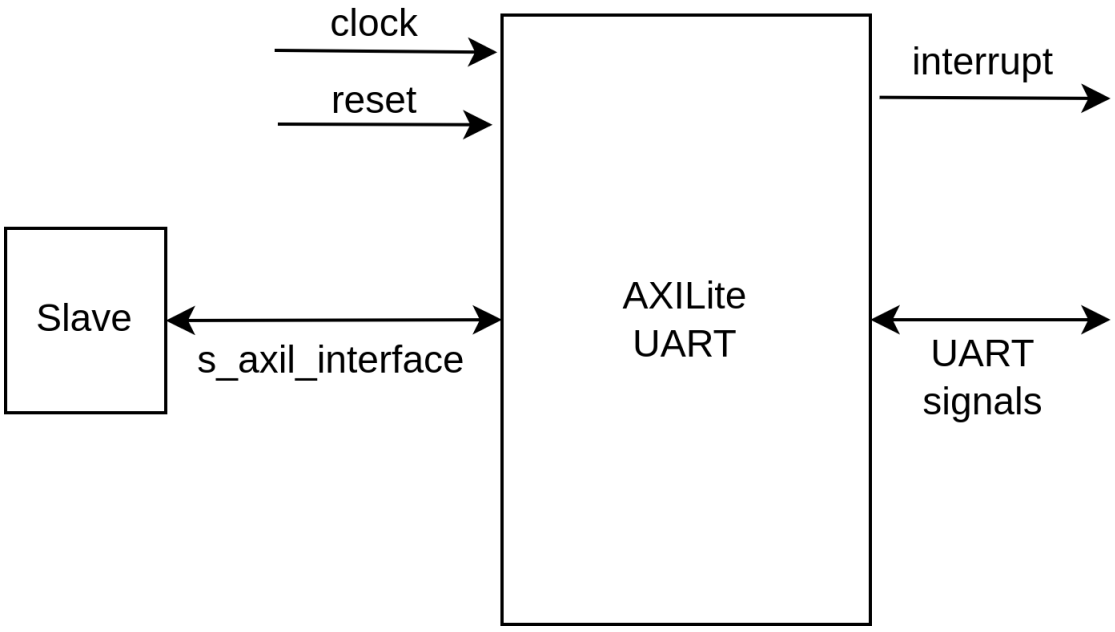

Figure 1. AXILite UART Block Diagram

Revision History

Date	Version	Revisions
January 25, 2023	0.01	Initial version AXILite UART User Guide Document