AXI Register

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IP Summary

Introduction

An AXI Register IP Core is a hardware module that provides a simple interface to read and write registers in a system-on-chip (SoC) design. The AXI protocol is a widely-used, industry-standard bus interface that enables high-speed communication between different modules in a SoC. This IP Core acts as a bridge between the AXI bus and the registers in the design. It can be customized to include any number of registers, each with a specific address and width. The IP core supports both read and write operations, allowing software running on a processor or other modules in the SoC to access the registers. The benefits of it include reduced design time, increased reliability, and improved system performance.

Features

- AXI4 (memory mapped) one master and one slave interface
- Configurable data width 8, 16, 32, 64, 128, 256, 512 and 1024 bits
- Configurable address width up to 64 bits
- Support ID width up to 32 bits
- Register options i.e. bypass, simple buffer or skid buffer for each channel
- Compatible with AXI4 Interconnect

Overview

AXI Register

The AXI Register IP Core is a part of Raptor Design Suite that provides a standard interface for reading and writing registers in a system-on-chip (SoC) design. It uses the AXI protocol, which is an industry-standard communication protocol that enables fast and efficient data transfer between different modules in the SoC. It supports both reading from and writing to the registers, which allows software running on a processor or other modules in the SoC to access. It can be customized to include a specific number of registers, each with its unique address and width. It simplifies the SoC design process, reduces design time, and ensures compatibility with other AXI-compliant modules in the SoC. It is typically used to configure and control modules like GPIO controllers, serial ports, or other peripheral devices.

Figure 1: AXI Register Block Diagram

IP Specification

Overview

The AXI Register is a IP core based on AMBA AXI Protocol which is a widely used, industry-standard bus interface that enables high-speed communication between different modules in an SoC. It has configurable register width and the width of the registers may range from 8 bits to 1024 bits, depending on the specific requirements of the SoC design. It support both read and write operations, allowing software running on a processor or other modules in the SoC to access the registers. It also supports up to 1024 bits for user signals. The IP core is comply with the AXI protocol and be compatible with other AXI-compliant modules in the SoC.

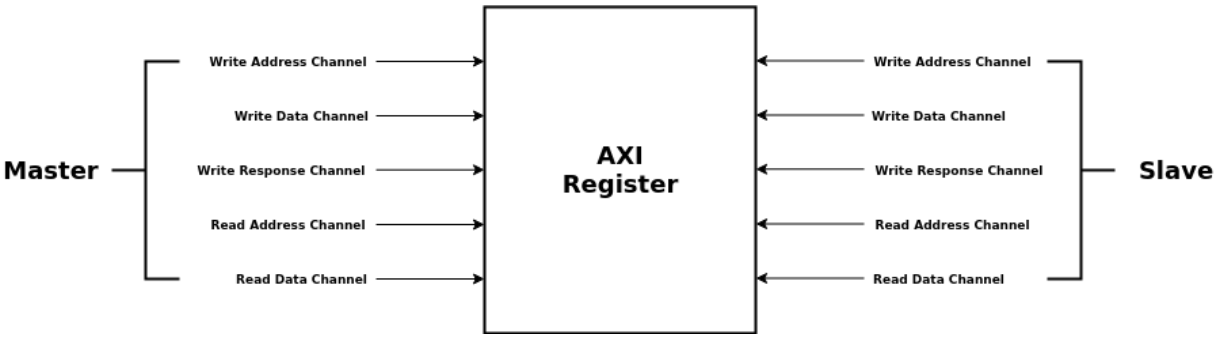

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI Register.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Verilog	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2. Other parameters are kept on their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	8	RAM36K	16
	ADDR_WIDTH	1	REGISTERS	161
	ID_WIDTH	1	-	-
	AW_REG_TYPE	1	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	1024	RAM36K	16
	ADDR_WIDTH	64	REGISTERS	4854
	ID_WIDTH	32	-	-
	AW_REG_TYPE	2	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI Register.

Signal Name	Input/Output	Description
clk	Input	Clock Signal for Synchronization
rst	Input	Active Low Reset Signal
Write Address Channel		
awid	Input	Write address ID
awaddr	Input	Write address
awlen	Input	Burst length
awsize	Input	Burst size
awburst	Input	Burst type
awlock	Input	Lock type
awcache	Input	Memory type
awprot	Input	Protection type
awvalid	Input	Write address valid
awready	Output	Write address ready
Write Data Channel		
wdata	Input	Write data
wstrb	Input	Write strobe
wlast	Input	Write last
wvalid	Input	Write valid
wready	Output	Write ready
Write Response Channel		
bid	Output	Response ID tag
bresp	Output	Write response
bvalid	Output	Write response valid
bready	Input	Write response ready
Read Address Channel		
arid	Input	Read address ID
araddr	Input	Read address

Signal Name	Input/Output	Description
arlen	Input	Burst length
arsize	Input	Burst size
arburst	Input	Burst type
arlock	Input	Lock type
arcache	Input	Memory type
arprot	Input	Protection type
arvalid	Input	Read address valid
arready	Output	Read address ready
Read Data Channel		
rid	Output	Read ID tag
rdata	Output	Read data
rresp	Output	Read response
rlast	Output	Read last
rvalid	Output	Read valid
rready	Input	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI Register.

Parameter	Values	Default Value	Description
DATA_WIDTH	8, 16, 32, 64, 128, 256, 512, 1024	32	Data Width of Register
ADDR_WIDTH	1 - 64	32	Address Width of Register
ID_WIDTH	1 - 32	32	ID field of Register
AW_USER_WIDTH	1 - 1024	1	User Field for AW Channel
W_USER_WIDTH	1 - 1024	1	User Field for W Channel
B_USER_WIDTH	1 - 1024	1	User Field for B Channel
AR_USER_WIDTH	1 - 1024	1	User Field for AR Channel
R_USER_WIDTH	1 - 1024	1	User Field for R Channel
AW_REG_TYPE	0, 1, 2	1	Register Type for AW Channel
W_REG_TYPE	0, 1, 2	2	Register Type for W Channel
B_REG_TYPE	0, 1, 2	1	Register Type for B Channel
AR_REG_TYPE	0, 1, 2	1	Register Type for AR Channel
R_REG_TYPE	0, 1, 2	2	Register Type for R Channel

Table 4: Parameters

Feature Description

The "'CHANNEL'_REG_TYPE" parameter in an AXI Register IP Core specifies how the register behaves when data is written to it. There are three types of registers that can be selected: Bypass, Simple Buffer, and Skid Buffer.

- **Bypass Register**

  A Bypass register is the simplest type of register. When data is written to it, the register immediately transfers the data to the output without storing it. This type of register is useful when there is no need to store the data and it can be directly passed on to the next module. The bypass register provides the fastest and most efficient data transfer but does not store the data.

- **Simple Buffer**

  A Simple Buffer register stores the data temporarily and releases it when requested. When data is written to a simple buffer register, it is stored in the register and is available for reading until it is overwritten. This type of register is useful when the data needs to be processed before being passed on to the next module. For example, a simple buffer register could be used to store data that needs to be processed by a CPU or a DSP core.

- **Skid Buffer**

  A Skid Buffer register is similar to a Simple Buffer register, but it has an additional feature called "skidding." Skidding means that if new data is written to the register before the old data is read, the new data overwrites the old data. This behavior can be useful when only the most recent data needs to be kept. Skid buffer registers are often used in real-time applications, such as video or audio processing, where it is important to have the most recent data.

Design Flow

IP Customization and Generation

AXI Register IP core is a part of the Raptor Design Suite Software. A customized register can be generated from the Raptor's IP configuration window as shown in figure 3.

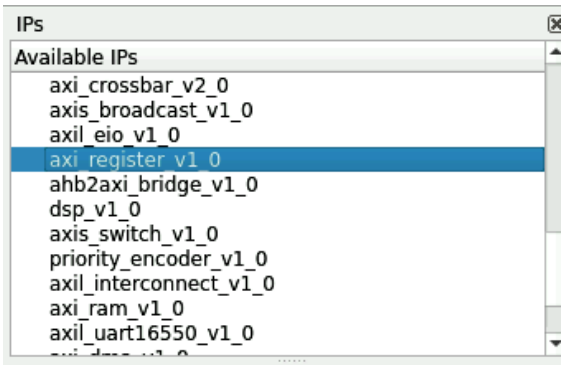

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI Register can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

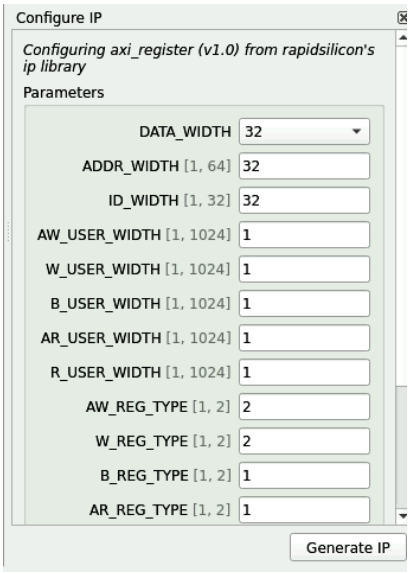

Figure 4: IP Configuration

Test Bench

Test for AXI Register

The testbench attached with AXI Register is CocoTB based verification environment. In this test, slave interface is connected to AXI Master and master interface is connected with AXI RAM. Master start writing and reading data to AXI RAM through AXI Register IP. The stimulus is generated by environment and test vectors are applied to the design. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
April 27, 2023	1.0	Initial version AXI Register User Guide