FIR Generator (Beta Release)

Version 0.1

December 22, 2023

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IP Summary

Introduction

The FIR Generator IP stands as a versatile tool for crafting Finite Impulse Response (FIR) Filters, offering adaptability in the number of filter taps and coefficients. With a customizable input data width, it effortlessly accommodates a wide spectrum of signal widths. This generator is meticulously optimized for speed, enabling parallel computations and ensuring efficient signal processing across diverse applications. Its flexible design empowers users to tailor FIR filters precisely to their specifications, fostering a high level of customization for advanced signal processing tasks.

Features

- Configurable Input Data Width from 1 - 18.
- Support for up to 120 Coefficients and filter Stages.
- Supports loading coefficients from either a source file in .txt or .hex format, or enter manually in the IP Configurator Window.

Overview

FIR Generator

The FIR Generator IP (Finite Impulse Response Generator Intellectual Property) is a versatile and high-performance hardware module designed for implementing Finite Impulse Response (FIR) filters in digital signal processing applications. FIR filters are widely used in various fields, including communications, audio processing, image processing, and more, to perform filtering and convolution operations on digital signals. A block diagram for a top level FIR Filter generated from the FIR Generator IP is shown in Figure 1.

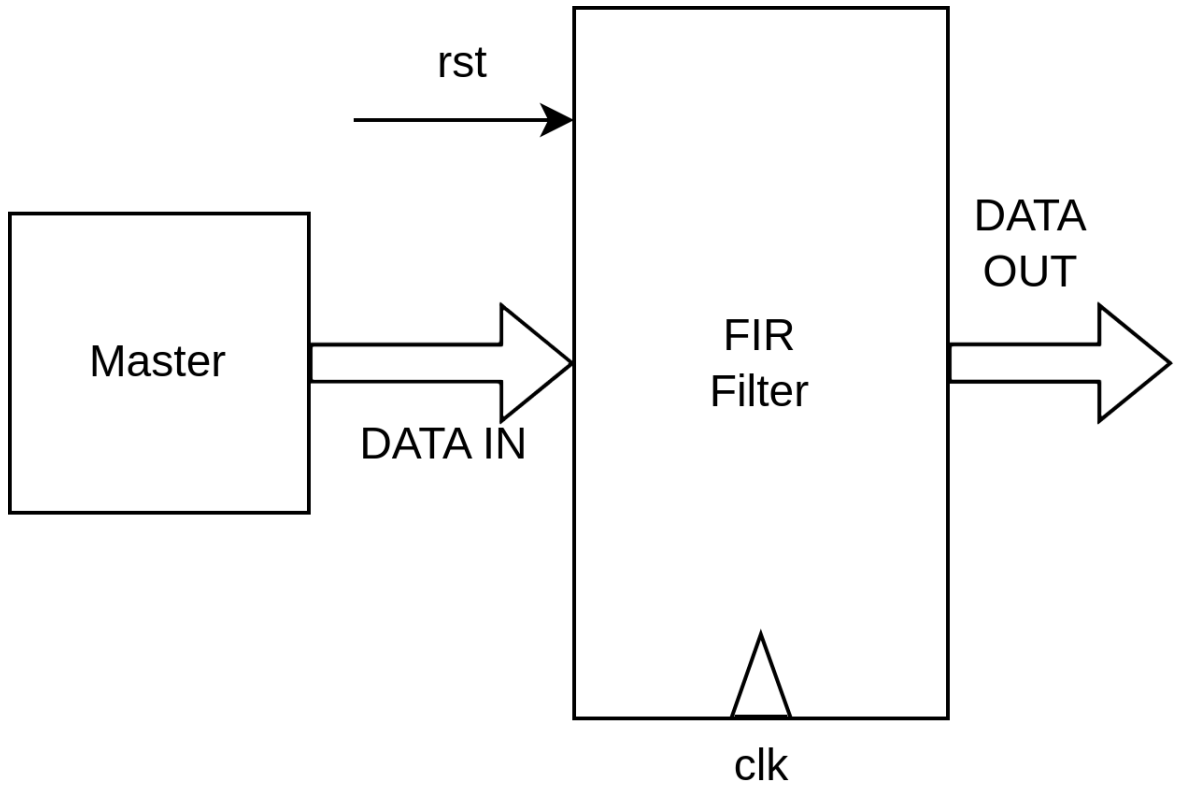

Figure 1: FIR Block Diagram

IP Specification

Standards

The FIR Generator soft IP supports the native interface with the standard DATA_IN and DATA_OUT ports along with the supporting clocks and reset signals in the port list.

IP Support Details

The Table 1 gives the support details for FIR Generator.

Compliance		IP Resources					Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Software Driver	Analyze and Elaboration	Simulation	Synthesis
GEMINI	Native	Verilog	-	Verilog	VVP	Iverilog	Raptor (Surelog)	Raptor (Icarus)	Raptor

Table 1: IP Details

Parameters

Table 2 lists the parameters of the FIR Generator.

Parameter	Values	Default Value	Description
INPUT WIDTH	1 - 18	18	Input Data Width
COEFFICIENTS	Up to 120 coefficients	-	Coefficients for the filter taps
COEFFICIENTS FILE	0 / 1	0	Grab coefficients from a .txt or .hex file or enter manually
FILE PATH	<path to the coefficients file>	0	Absolute Path of the .txt / .hex is located with coefficients
IP TYPE	-	FIRGEN	Type of Peripheral
IP VERSION	-	<ip_version>	Version of Peripheral
IP ID	-	<date_and_time>	Date and Time of the generated Peripheral

Table 2: Parameters

Note:

- *FILE PATH is only available when COEFFICIENTS FILE is selected.*
- *COEFFICIENTS is only available when COEFFICIENTS FILE is not selected.*

Port List

Table 3 lists the top interface ports of the FIR Generator.

Signal Name	I / O	Description
data_in {INPUT_WIDTH}	I	Data Input
data_out	O	Data Output
rst	I	Reset
clk	I	Common Clock for Synchronous Operation

Table 3: FIR Generator Interface

Resource Utilization

The parameters for computing the maximum and minimum resource utilization are given in Table 4, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	INPUT WIDTH	1	DSPs	1
	COEFFICIENTS	1		
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	INPUT WIDTH	18	DSPs	120
	COEFFICIENTS	120		

Table 4: Resource Utilization

Design Flow

IP Customization and Generation

FIR Generator IP core is a part of the Raptor Design Suite Software. A customized FIR IP can be generated from the Raptor's IP configurator window as shown in Figure 2.

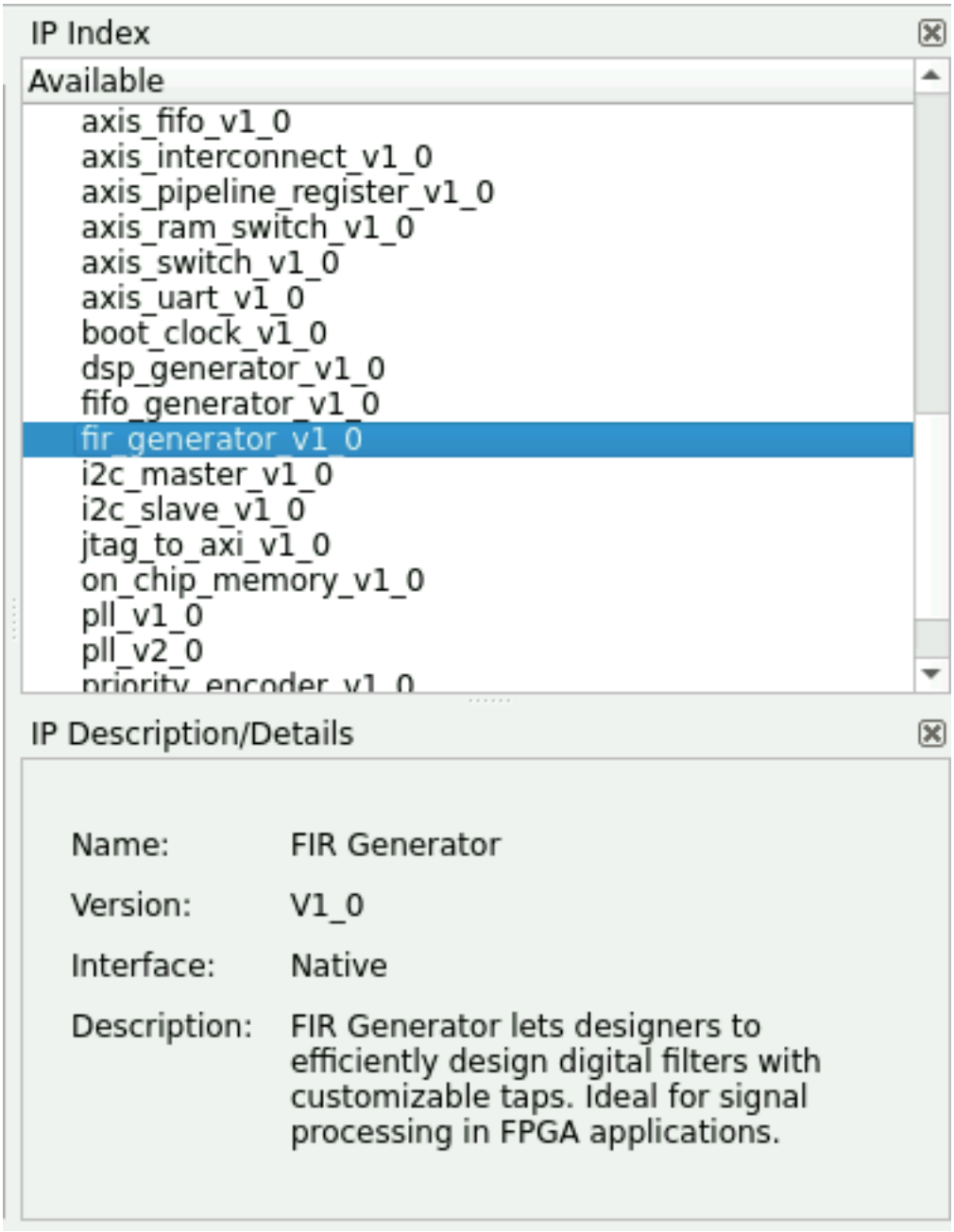

Figure 2: IP list

Parameters Customization

From the IP configuration window, the parameters of FIR Generator can be configured and IP features can be enabled for generating a FIR IP core that suits the user application requirement as shown in Figure 3. After IP Customization, the generated IP is made available to the user to be used in applications.

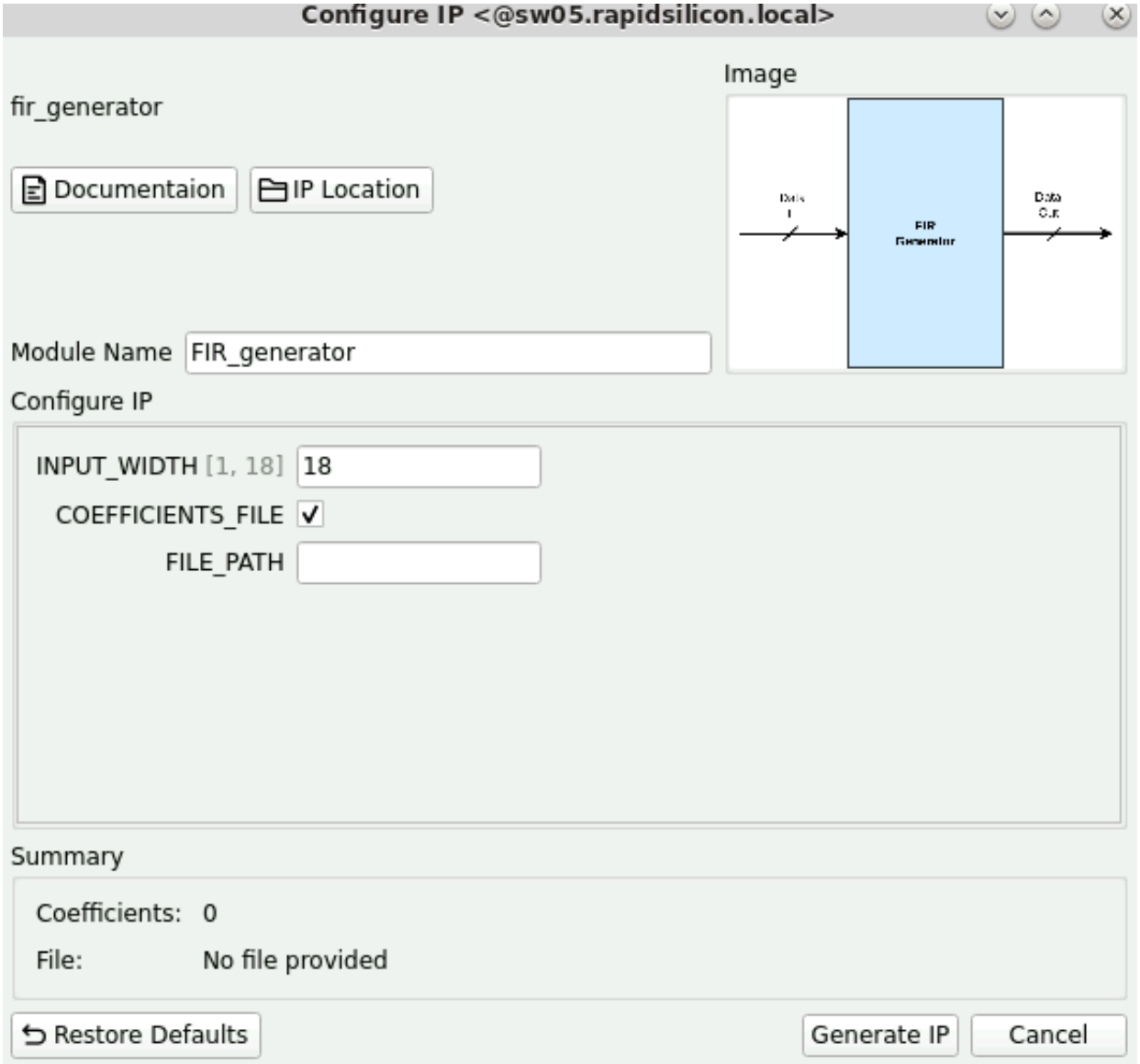

Figure 3: IP Configuration

Synthesis and PR

Raptor Suite is armed with tools for Synthesis and the generated post-synthesis net-lists can be viewed and analyzed from within the Raptor. The generated bit-stream can then be

uploaded on an FPGA device to be utilized in hardware applications.

Test Bench

The FIR Generator IP is tested and verified by utilizing unit level tests providing random data as the input and then the output from the FIR Generator IP is compared to a golden behavioral netlist.

Release

Release History

Date	Version	Revisions
December 22, 2023	0.1	Initial version FIR Generator User Guide Document