AXI Lite Interconnect

Version 1.0

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IP Summary

Introduction

The AXI Lite Interconnect IP core is a module which enables communication between different AXI Lite master and slave devices in a system-on-chip (SoC) design. AXI Lite is a simplified version of the full AXI (Advanced eXtensible Interface) protocol, with a reduced number of signals and a more limited feature set, which makes it suitable for low-complexity, low-bandwidth applications. The AXI Lite Interconnect IP core acts as a central hub for the AXI Lite bus, providing connectivity and arbitration for AXI Lite master devices and AXI Lite slave devices. It supports multi-master and multi-slave configurations, allowing multiple devices to access the same memory or peripheral resources in the system.

Features

- Low latency and high bandwidth communication: AXI Lite Interconnect IP core allows multiple AXI Lite masters to communicate with multiple AXI Lite slaves through a high-bandwidth and low-latency interconnect.
- Support for multiple masters and slaves: The IP core can connect up to 16 AXI Lite masters and 16 AXI Lite slaves. This allows for a highly configurable system-on-chip design.
- Low resource utilization: The AXI Lite Interconnect IP core has low resource utilization, making it suitable for use in resource-constrained designs.
- Configurability: AXI Lite interconnect is highly configurable, allowing designers to optimize the interconnect for their specific SoC design.
- Data Width: 32, 64 bits
- Address Width: 32, 64, 128, 256 bits

Overview

AXI Lite Interconnect

The AXI Lite Interconnect IP Core is a component of the Raptor Design Suite that provides a simple, low-latency interconnect between multiple AXI Lite master and slave peripherals. The AXI Lite protocol is a simplified version of the full AXI protocol, which is used in more complex systems. The AXI Lite Interconnect IP Core provides a way to connect multiple AXI Lite interfaces together without the need for a full AXI protocol implementation. It is often used in small embedded systems, where a limited number of peripherals need to be connected together. It is designed to be lightweight and efficient, with minimal overhead and low latency. It can be used with a variety of AXI Lite-compatible peripherals, including memory controllers, UARTs, SPI controllers, and GPIO controllers.

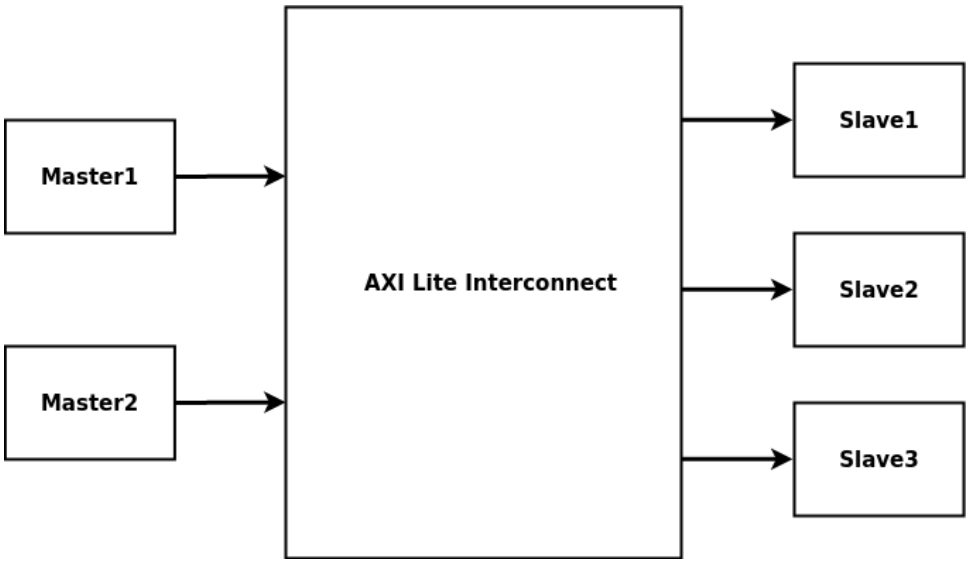

Figure 1: AXI Lite Interconnect Block Diagram

IP Specification

Overview

The AXI Lite Interconnect IP is a configurable and scalable IP block that provides connectivity between AXI Lite slave devices and AXI memory-mapped master devices. It supports the AXI4-Lite protocol, which is a simplified version of the AXI4 protocol. The AXI4-Lite protocol provides a simple, low-latency, and low-complexity interface for peripheral devices. It supports up to 16 AXI4-Lite slave devices and up to 16 AXI4-Lite master devices. It is highly configurable, allowing users to customize various parameters such as the number of ports. The figure 2 shows the top level diagram of AXI Lite Interconnect.

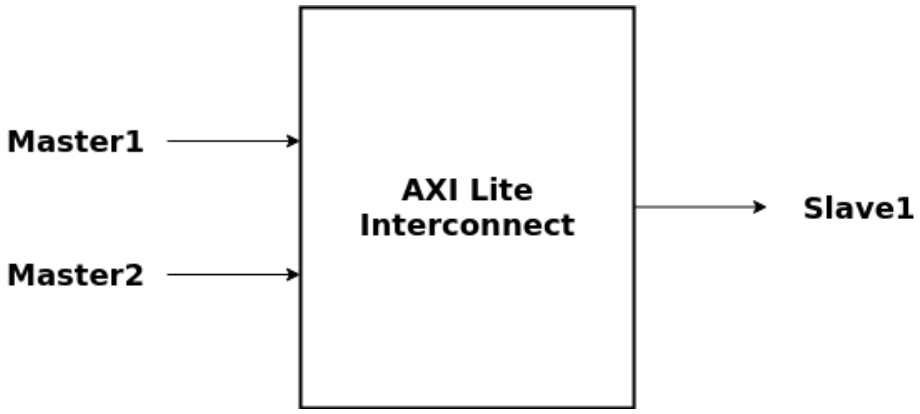

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI Lite Interconnect.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI-Lite	Verilog	-	Verilog	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	4	RAM36K	16
	M_COUNT	4	REGISTERS	138
	DATA_WIDTH	32	-	-
	ADDR_WIDTH	32	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	16	RAM36K	16
	M_COUNT	16	REGISTERS	570
	DATA_WIDTH	256	-	-
	ADDR_WIDTH	32	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI Lite Interconnect.

Signal Name	Input/Output	Description
clk	Input	Clock Signal for synchronization
rst	Input	Active Low Reset Signal
Write Address Channel		
awaddr	Input	Write address
awprot	Input	Protection type
awvalid	Input	Write address valid
awready	Output	Write address ready
Write Data Channel		
wdata	Input	Write data
wstrb	Input	Write strobe
wvalid	Input	Write valid
wready	Output	Write ready
Write Response Channel		
bresp	Output	Write response
bvalid	Output	Write response valid
bready	Input	Write response ready
Read Address Channel		
araddr	Input	Read address
arprot	Input	Protection type
arvalid	Input	Read address valid
arready	Output	Read address ready
Read Data Channel		
rdata	Output	Read data
rresp	Output	Read response
rvalid	Output	Read valid
rready	Input	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI Lite Interconnect.

Parameter	Values	Default Value	Description
S_COUNT	1-16	4	No. of Slave Interfaces
M_COUNT	1-16	4	No. of Master Interfaces
DATA_WIDTH	32, 64	32	Data Width of Interconnect
ADDR_WIDTH	32, 64, 128, 256	32	Address Width of Interconnect

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI Lite Interconnect IP core is a part of the Raptor Design Suite Software. A customized interconnect can be generated from the Raptor's IP configuration window as shown in figure 3.

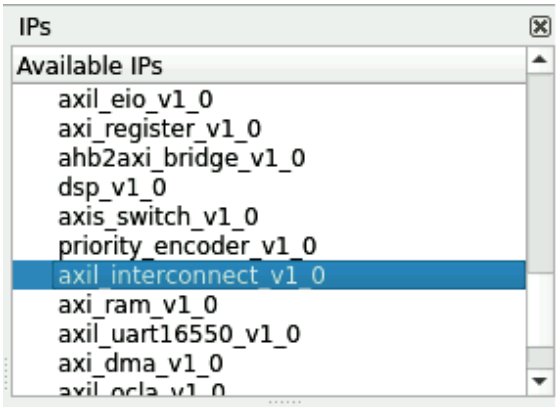

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI Lite Interconnect can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

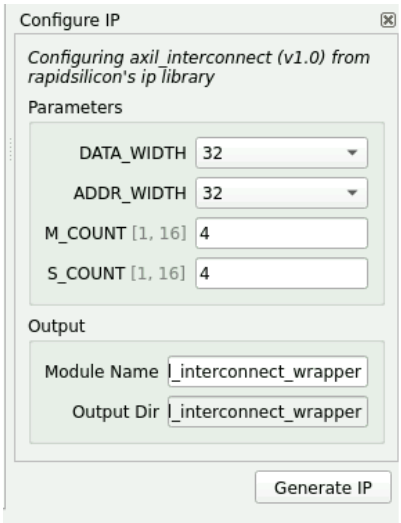

Figure 4: IP Configuration

Test Bench

Test for AXI Lite Interconnect 4x4

The testbench attached with AXI Lite Interconnect is CocoTB based verification environment. In this test, four masters ad four slaves are connected to interconnect. Interconnect assigns address space to each slave. Each master communicate with each slave. The stimulus is generated by environment and test vectors are applied to the design. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
April 26, 2023	1.0	Initial version AXI Lite Interconnect User Guide