AXI Central DMA v2.0

***IP User Guide** (Beta Release)*

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RapidSilicon

Contents

IP Summary

Introduction

The AXI Central Direct Memory Access (AXI CDMA) is a highly flexible and scalable soft IP core that is designed to provide a direct memory access (DMA) capability to System-on-Chip (SoC) designs. The AXI CDMA is optimized for memory-mapped source and destination addresses, enabling direct communication between different memory regions without the need for involvement from the processor.

Built on the widely adopted Advanced extensible Interface (AXI) bus protocol, the AXI CDMA offers a standardized interconnect architecture for on-chip and off-chip communication. By enabling fast and efficient data transfers between memory regions, the AXI CDMA reduces the load on the processor and improves the overall performance and efficiency of the system, especially for data-intensive applications. With its ease of integration, reliability, and high-performance capabilities, the AXI CDMA is an essential component of modern SoC designs and plays a critical role in enabling efficient communication between different components of the system.

Features

- Data Transfer via AXI4 Interface
- Register Access via AXI4-Lite Slave Interface
- Configurable address widths and data widths
- Register Direct Mode
- Optional realignment FIFO for unaligned transfers
- Interrupts for CDMA completion and errors

Overview

AXI Central DMA

The AXI CDMA is designed to be part of the custom embedded setup via the AXI4 Interconnect, providing convenient access to the system processor via the AXI4-Lite interface. To perform simple CDMA operations, the core can be controlled through the register interface. The core is responsible for transferring data between the designated source and destination addresses. Upon completion, the interrupt output from the AXI CDMA will trigger an interrupt in the system Interrupt Controller, freeing up the processor for other tasks shown figure 1. The CDMA is optimized for efficient data transfer between memory locations in the custom embedded setup.

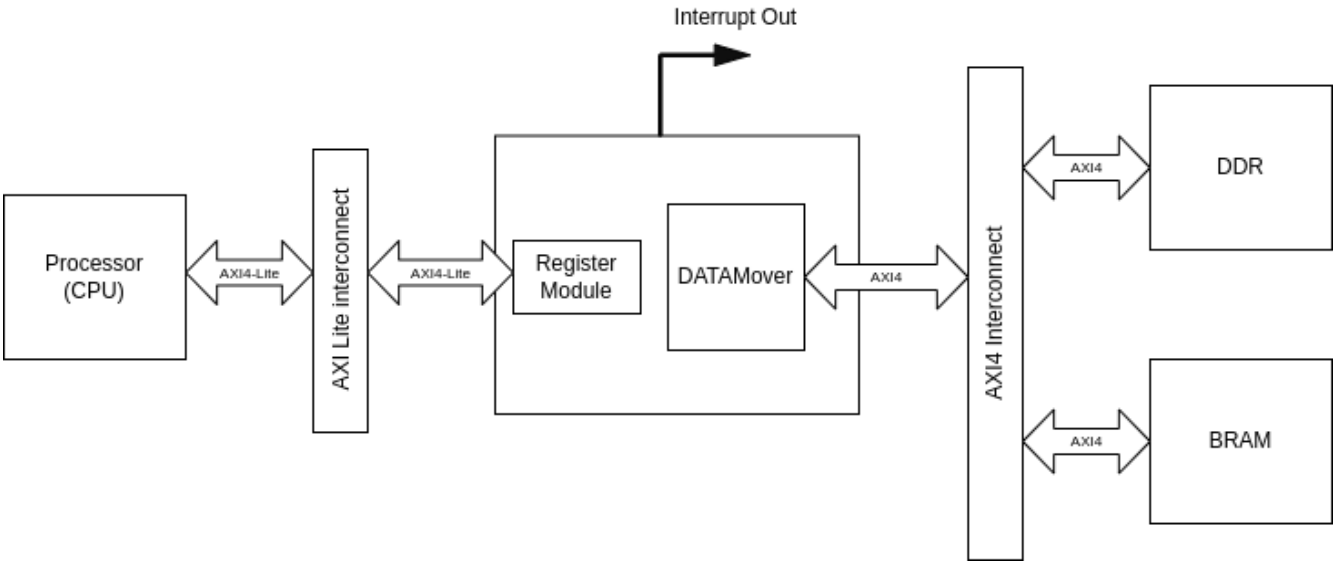

Figure 1. AXICDMA Typical configuration

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IP Specification

Overview

The figure 2 shows the detailed internal block diagram of the AXICDMA (AXI Central DMA). The AXI CDMA is a component designed to provide high-speed data transfer capabilities in an embedded processing system utilizing the AXI4 system interfaces.The core consists of multiple functional blocks, including an AXI4 Master interface for memory-mapped to memory-mapped (MM2M) transfer operations, an AXI4-Lite Slave interface for register access, and an AXI DataMover helper core for high-throughput data transfer.

The skid buffer is a component of the AXI CDMA IP core works by temporarily storing data, allowing for more time to process and transfer the information. The primary purpose of the skid buffer is to provide pipeline support, ensuring efficient and effective data transfer. The Register Module houses the control register for the AXI CDMA, which are accessible via the AXI4-Lite Slave interface. These registers provide control and monitoring for all CDMA operations and transfer requests.The AXI DataMover is responsible for the primary data transport function and offers various features, such as address boundary protection, automatic burst partitioning, and byte-level data realignment. This allows the AXI CDMA to read and write data from/to any byte offset combination, ensuring efficient and effective data transfer.

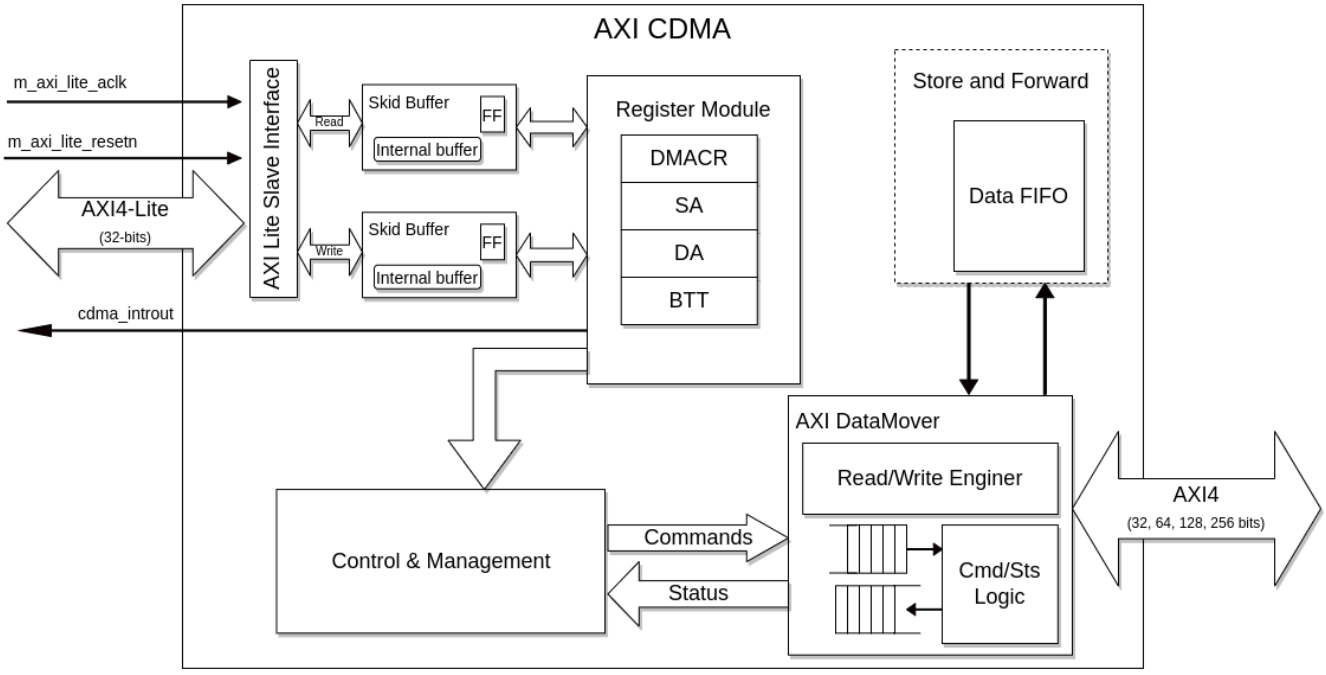

Figure 2. Top Module

The store and forward block with data FIFO is a component of the AXI CDMA IP core. It is connected with the AXI DataMover and its purpose is to temporarily store and buffer incoming data, allowing it to be processed in an efficient manner. The data FIFO serves as a buffer for the transfer of data between the DataMover and the store and forward mechanism helps to ensure a smooth and error-free flow of data within the system.

Revision History

Date	Version	Revisions
February 14, 2023	2.0	AXICDMA User Guide Document