AXI4 Interconnect

Version 1.0

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IP Summary

Introduction

The AXI4 (Advanced eXtensible Interface 4) interconnect is a widely-used, industry-standard protocol for connecting intellectual property (IP) blocks in a system-on-chip (SoC) design. The AXI4 interconnect supports high-bandwidth, low-latency communication between IP blocks, and provides a range of features and functionality to optimize system performance and reduce design complexity. It includes separate read and write channels for data and control information, support for burst transfers and out-of-order transaction processing, and features to support cache coherency and multi-master configurations. The AXI4 interconnect is widely used in a range of applications, including mobile devices, networking equipment, and high-performance computing systems. It provides a standardized interface that allows IP blocks from different vendors to be easily integrated into a single SoC design, reducing development time and cost.

Features

- High performance: AXI4 interconnect is designed for high performance with a high-bandwidth, low-latency interface that can handle large amounts of data.
- Scalability: The AXI4 interconnect is highly scalable, supporting a large number of masters and slaves. This makes it suitable for complex SoC designs.
- Multiple data channels: The AXI4 interconnect supports multiple data channels, allowing for simultaneous transfers of data between different components.
- Burst transfers: The AXI4 interconnect supports burst transfers, which allows for more efficient data transfer by reducing the number of transactions required.
- Configurability: AXI4 interconnect is highly configurable, allowing designers to optimize the interconnect for their specific SoC design.
- Address and data interleaving: AXI4 interconnect supports address and data interleaving, which allows for faster data transfers by overlapping address and data phases.
- Master Count: 16
- Slave Count: 16
- Data Width: 8, 16, 32, 64, 128, 256 bits
- Address Width: 32, 64, 128 bits
- User Width (per channel): Up to 1024 bits
- ID Width: Up to 8 bits

Overview

AXI4 Interconnect

AXI4 (Advanced eXtensible Interface 4) is a widely used interconnect protocol for system-on-chip (SoC) designs, which facilitates communication between different components of an SoC. Documentation of the AXI4 interconnect involves several aspects, including the specification of the protocol, the architecture and design of the interconnect, and the implementation details. The AXI4 specification document provides a detailed description of the protocol and its various features, including the different types of signals, transactions, and burst transfers. This document serves as a reference for SoC designers and system integrators who are implementing the AXI4 interface in their designs. The interconnect architecture and design documentation typically includes a description of the AXI4 master and slave interfaces, the arbitration and buffering mechanisms, and the routing of signals between different components. This documentation also covers the power and clocking requirements of the interconnect and any design constraints that need to be considered. Implementation documentation may include detailed design specifications, hardware and software documentation, and testing procedures. It may also include information on how to integrate the interconnect with other components of the SoC, such as memory controllers, peripherals, and processor cores.

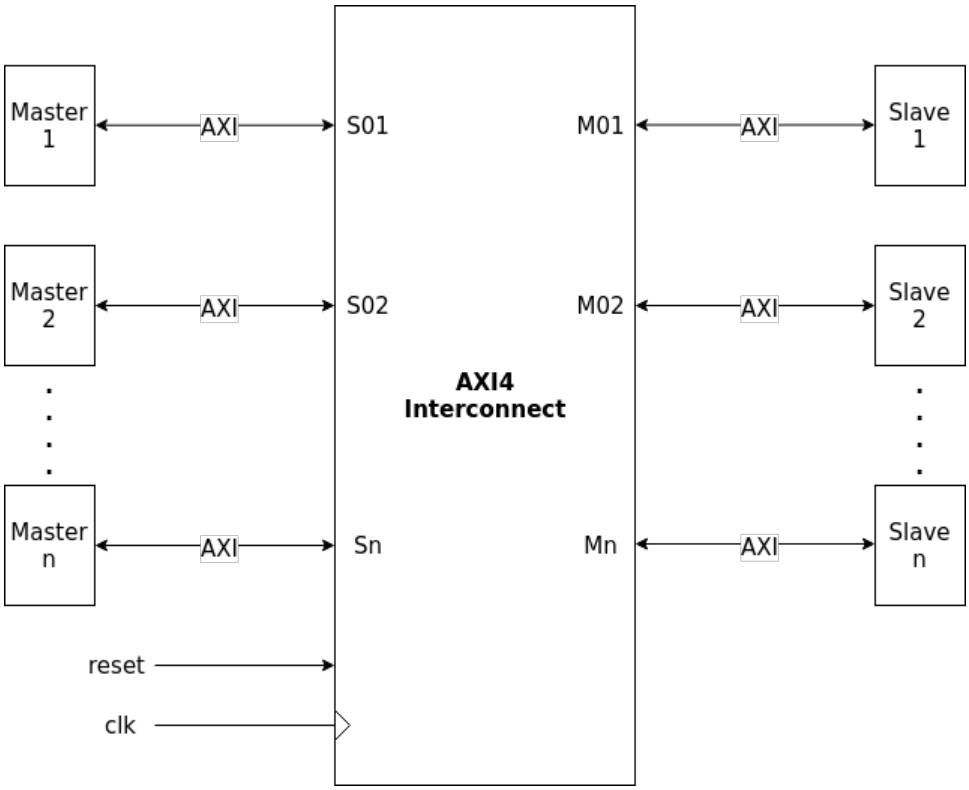

Figure 1: AXI4 Interconnect Block Diagram

IP Specification

Overview

The AXI4 Interconnect IP specification provides a standardized approach for connecting different components of a system-on-chip, such as processors, memories, DMA controllers, and other IP blocks, through a common bus architecture. It provides a set of rules and protocols for data transfer, flow control, arbitration, and other aspects of communication between the components. It supports multiple masters and multiple slaves, and can be configured to support different data widths, burst sizes, and transfer modes. It also supports various QoS (Quality of Service) levels and power management features to optimize system performance and energy efficiency. The figure 2 shows the top level diagram of AXI4 Interconnect.

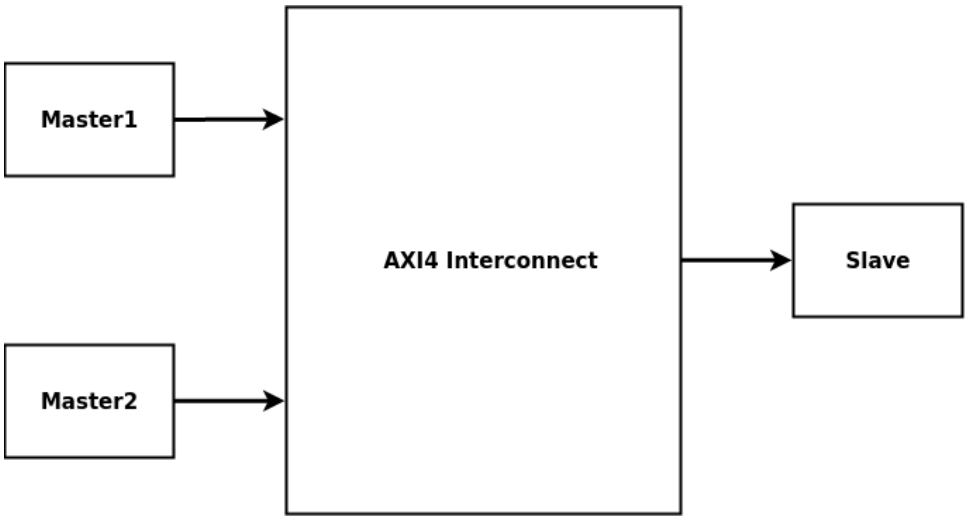

Figure 2: Top Module

IP Support Details

The Table 1 gives the support details for AXI4 Interconnect.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Verilog	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2, remaining parameters have been kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	1	REGISTERS	254
	M_COUNT	1	-	-
	DATA_WIDTH	32	-	-
	ADDR_WIDTH	32	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	S_COUNT	16	REGISTERS	1521
	M_COUNT	16	-	-
	DATA_WIDTH	256	-	-
	ADDR_WIDTH	32	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI4 Interconnect.

Signal Name	Input/Output	Description
clk	Input	Clock Signal for synchronization
rst	Input	Active Low Reset Signal
Write Address Channel		
awid	Input	Write address ID
awaddr	Input	Write address
awlen	Input	Burst length
awsize	Input	Burst size
awburst	Input	Burst type
awlock	Input	Lock type
awcache	Input	Memory type
awprot	Input	Protection type
awqos	Input	Quality of service
awuser	Input	User signal
awvalid	Input	Write address valid
awready	Output	Write address ready
Write Data Channel		
wdata	Input	Write data
wstrb	Input	Write strobe
wlast	Input	Write last
wvalid	Input	Write valid
wready	Output	Write ready
Write Response Channel		
bid	Output	Response ID tag
bresp	Output	Write response
bvalid	Output	Write response valid
bready	Input	Write response ready
Read Address Channel		

Signal Name	Input/Output	Description
arid	Input	Read address ID
araddr	Input	Read address
arlen	Input	Burst length
arsize	Input	Burst size
arburst	Input	Burst type
arlock	Input	Lock type
arcache	Input	Memory type
arprot	Input	Protection type
arqos	Input	Quality of service
aruser	Input	User signal
arvalid	Input	Read address valid
arready	Output	Read address ready
Read Data Channel		
rid	Output	Read ID tag
rdata	Output	Read data
rresp	Output	Read response
rlast	Output	Read last
rvalid	Output	Read valid
rready	Input	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI4 Interconnect.

Parameter	Values	Default Value	Description
S_COUNT	1-16	4	No. of Slaves connected to Interconnect
M_COUNT	1-16	4	No. of Masters connected to Interconnect
DATA_WIDTH	8, 16, 32, 64, 128, 256	32	Data Width of Interconnect
ADDR_WIDTH	32, 64, 128	32	Address Width of Interconnect
ID_WIDTH	1-1024	1	ID field of Interconnect
AW_USER_EN	True/False	True	User Enable Field for AW Channel
W_USER_EN	True/False	True	User Enable Field for W Channel
B_USER_EN	True/False	True	User Enable Field for B Channel
AR_USER_EN	True/False	True	User Enable Field for AR Channel
R_USER_EN	True/False	True	User Enable Field for R Channel
AW_USER_WIDTH	1-1024	1	User Field for AW Channel
W_USER_WIDTH	1-1024	1	User Field for W Channel
B_USER_WIDTH	1-1024	1	User Field for B Channel
AR_USER_WIDTH	1-1024	1	User Field for AR Channel
R_USER_WIDTH	1-1024	1	User Field for R Channel

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI4 Interconnect IP core is a part of the Raptor Design Suite Software. A customized interconnect can be generated from the Raptor's IP configuration window as shown in figure 3.

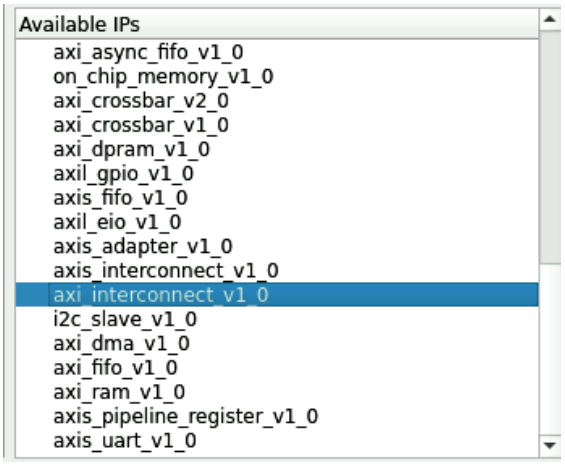

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI4 Interconnect can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in figure 4.

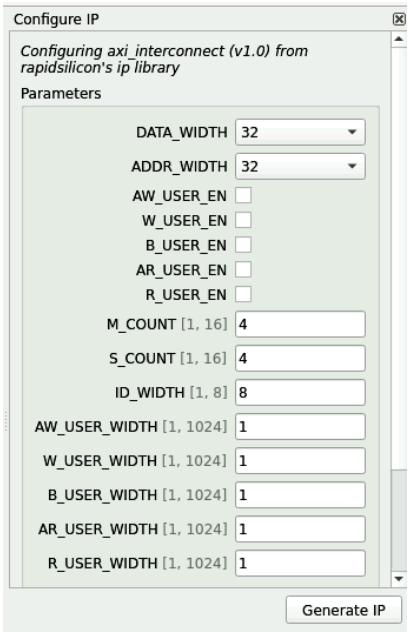

Figure 4: IP Configuration

Test Bench

Test for AXI4 Interconnect 4x4

The testbench attached with AXI4 Interconnect is CocoTB based verification environment. In this test, four masters ad four slaves are connected to interconnect. Interconnect assigns address space to each slave. Each master communicate with each slave. The stimulus is generated by environment and test vectors are applied to the design. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
April 26, 2023	1.0	Initial version AXI4 Interconnect User Guide