On-Chip Logic Analyzer v1.0

***IP User Guide** (Beta Release)*

December 7, 2023

RapidSilicon

Contents

IP Summary

Introduction

The On Chip Logic Analyzer (OCLA) core is a customizable logic analyzer that conforms to the AXI4-Lite specification and is intended for use in applications that necessitate verification or debugging through the monitoring of internal signals within a design on field-programmable gate arrays (FPGAs).

The OCLA core boasts a variety of features commonly found in modern logic analyzers, such as edge transition triggering, multi-trigger options, and configurable parameters such as the number of probes and trace memory depth.

Additionally, the OCLA offers several modes for data capturing operations during debugging, including continuous, pre-trigger, post-trigger, and center-trigger options.

Features

- Configurable number of probes
- Configurable trigger condition
- Configurable trigger mode
- Configurable number of input triggers
- Configurable data depth
- Configurable data sampling mode

Overview

On-Chip Logic Analyzer

The OCLA is an IP core that can be used to monitor and capture the behavior of signals that are connected to its "probe port." The OCLA is configured through an AXI-lite slave interface, which allows the user to set up the OCLA's modes and controls.

The OCLA captures the behavior of the signals by performing a synchronous sampling operation. This means that the OCLA samples the signals at the clock of edge that is as the design that is being monitored, ensuring that the captured data is accurate and in sync with the behavior of the design.

The figure 1 shows the top-level interface diagram of the OCLA IP core, which is a customizable building block that can be integrated into a debug system.

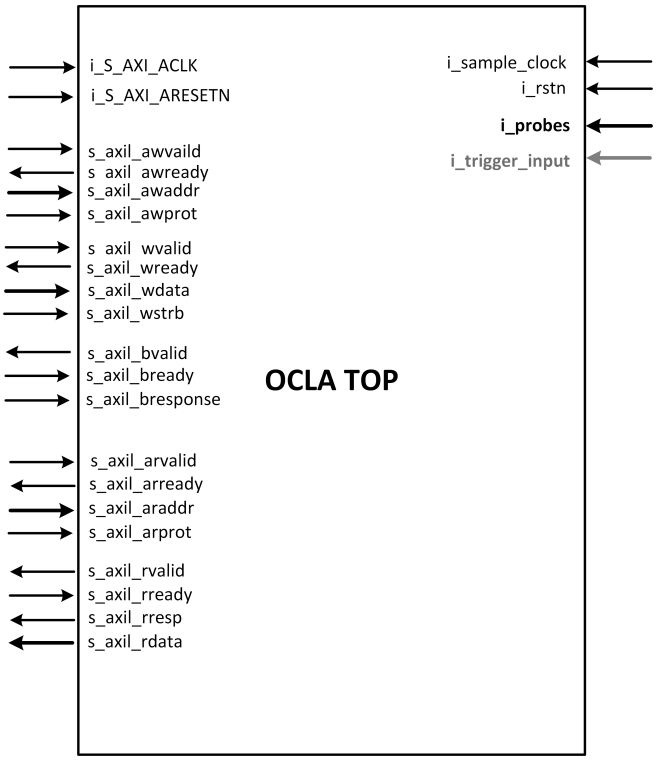


Figure 1. OCLA Top

Licensing

IP Specification

Overview

The figure 2 presents a detailed internal block diagram of the OCLA (On-Chip Logic Analyzer). It is characterized by a modular design, comprising various modules such as the OCLA AXI-lite Slave interface, Trigger Control Unit, Sampler Buffer, OCLA Controller, and OCLA On-Chip Trace Memory modules. Furthermore, it is designed as a multi-clock system, with a sampling clock and an AXI bus clock.

The sampling clock is synchronized with the clock of the System/Design under test (S/DUT) and is used to sample data on the rising edge of this clock, based on the configured sampling mode of the OCLA.

The OCLA can be configured through the AXI interface on the rising edge of the AXI bus clock. The collected data can be read via the AXI interface, also running on the AXI clock.

The modules that control the sampling operation of the OCLA, such as the Sampler Buffer and the OCLA Controller, operate on the sampling clock. In contrast, the AXI Slave and the Stream Out Buffer modules operate on the AXI clock and are used to configure or read the acquired data from the trace memory.

The On-Chip trace memory controller is implemented as a circular buffer based on a modified asynchronous FIFO. This design handles the clock domain crossing of the trace memory data and configuration data, ensuring efficient and accurate data transfer between the different modules.

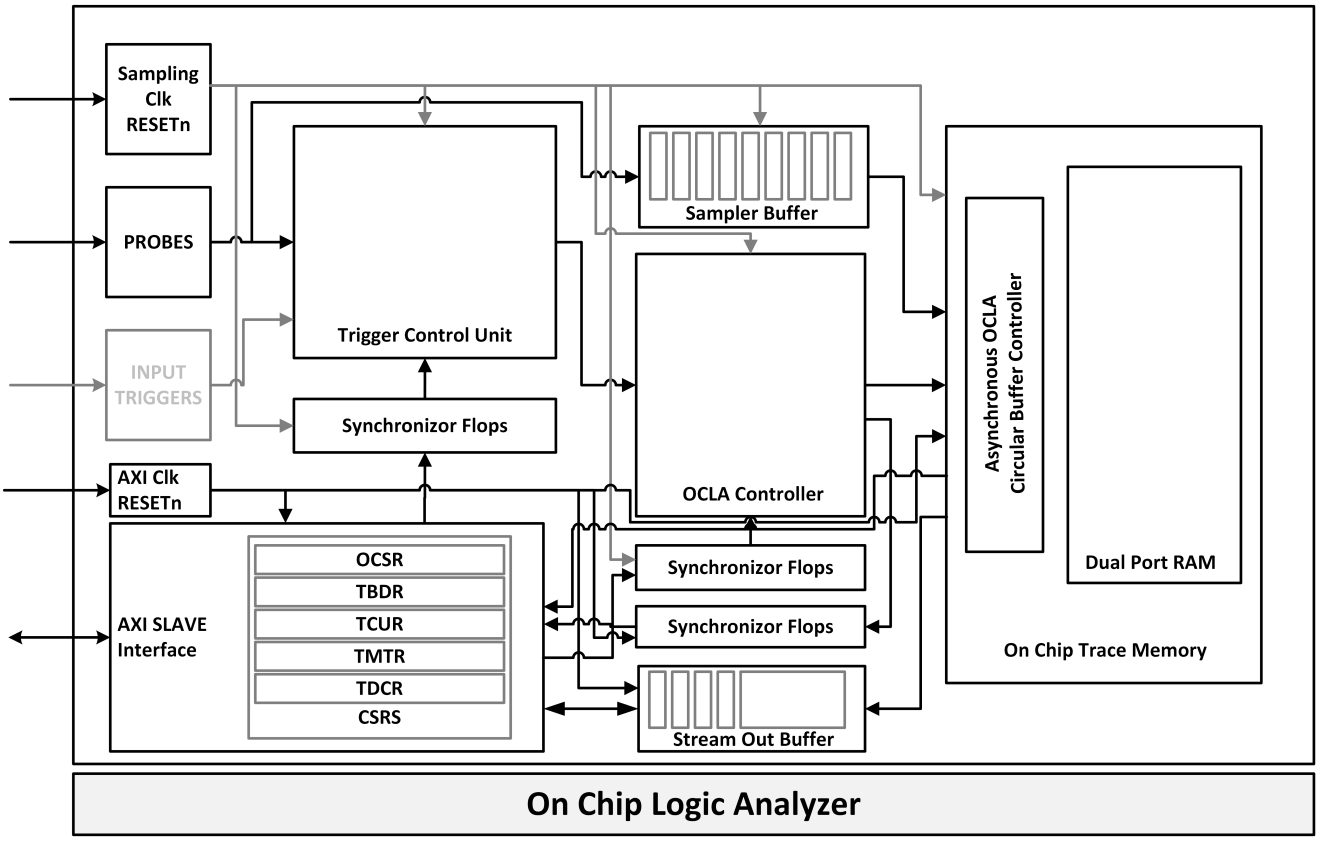


Figure 2. Top Module

Trigger

The OCLA IP core utilizes a trigger mechanism to initiate the capture of probe data samples. The trigger signal can be selected from a variety of sources, including probe input signals or trigger input signals.
OCLA also allows for the configuration of various trigger conditions on the trigger signal, such as level, edge, and value compare. The OCLA continually monitors the trigger signal, and data sampling begins when all of the trigger conditions in the active trigger pattern are satisfied.
Additionally, the OCLA features a user-configurable trigger mode setting, which determines the amount of data that should be acquired by the system prior to and following the trigger event. The acquired data is stored in a circular buffer for further analysis, which enables the system to efficiently handle large data sets and continuously update the data being captured.

OCLA supports four triggers. User can set upto 4 triggers at a time.

Trigger Conditions

Multiple options for trigger conditions are available for probe and input triggers signals. Following lists the trigger conditions:

Trigger Condition	Description
Don't Care	Default trigger condition. The channel is not used to determine the trigger event.
Low level	OCLA triggers when the probe channel is low.
High level	OCLA triggers when the probe channel is high.
Falling Edge	OCLA triggers on the falling edge the probe channel.
Rising Egde	OCLA triggers on the falling edge the probe channel.
Either Edge	OCLA triggers on either edge of the probe channel.
Value Comparison	OCLA triggers when the value of a probe channel is equal /less than / greator than some user specified value.
Boolean Trigger equations	Advance Trigger Conditions AND, OR, <, >, == etc

Table 1. Trigger Conditions

Trigger Modes

The common trigger modes are post trig, pre trig, center and countinous.

- **Pre triggered** the stored data set will consist of data sampled after the trigger.
- **Post triggered** is the opposite and in this mode the logic analyzer stops the sampling immediately when the trigger is raised thus only storing data from before the triggering event.
- **Center triggered** is a combination putting the triggering event in the middle of the sampled data set
- **Continous trigger** mode continounsly samples data.

Fix number of samples

The OCLA IP core can be configured to dynamically sample a specified number of probe samples, rather than utilizing the default trace memory depth, at runtime. This allows for greater flexibility in the debuging process, as the number of probe samples can be adjusted to suit the specific requirements of runtimme debuging.

Standards

The AXI4-Lite Slave interface is compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The table 2 presents the specifics of IP support for the OCLA IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources					Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Software Driver**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4-lite	Systemverilog	SDC	-	-	-	Raptor	Third Party	Raptor

Table 2. IP Information

Resource Utilization

The table 3 presents the resources utilization of OCLA IP for the Gemini device within the Raptor Design Suite, specifically detailing the statistics of resource utilization for both the minimum and maximum configurations of the OCLA.

Configuration		Resource Utillization		
Minimum Resource	Options	Configuration	Resources	Utillized
	Number of Probe	1	LUT	263
	Trace Memory Depth	32	FLOPS	138
	Value Compare Feature	OFF	BRAM	1
	Input Triggers	0	DSP	0
Maximum Resource	Options	Configuration	Resources	Utillized
	Number of Probe	1024	LUT	1068
	Trace Memory Depth	1024	FLOPS	5466
	Value Compare Feature	ON	BRAM	29
	Input Triggers	32	DSP	0

Table 3. Resource Utillization

Ports

Table 5 lists the top interface ports of the OCLA.

Signal Name	I/O	Description
Sampling Clock and Reset		
i_sample_clk	I	Clock to Sample the Probe Data. It must be same as the Design under test
i_rstn	I	Reset port of OCLA and it must be same as design under test
AXI Clock and Reset		
i_S_AXI_ACLK	I	AXI4-Lite Clock
i_S_AXI_ARESETN	I	AXI4-Lite RESET
AXI WRITE ADDRESS CHANNEL		
s_axil_awvalid	I	AXI4-Lite Write address valid
s_axil_awready	O	AXI4-Lite Write address ready
s_axil_awaddr	I	AXI4-Lite Write address
s_axil_awprot	I	AXI4-Lite Protection type
AXI WRITE DATA CHANNEL		
s_axil_wvalid	I	AXI4-Lite Write valid
s_axil_wready	O	AXI4-Lite Write ready.
s_axil_wdata	I	AXI4-Lite Write data
s_axil_wstrb	I	AXI4-Lite Write strobes
AXI WRITE RESPONSE CHANNEL		
s_axil_bvalid	O	AXI4-Lite Write response valid
s_axil_bready	I	AXI4-Lite Response ready
s_axil_bresp	O	AXI4-Lite Write response
AXI READ ADDRESS CHANNEL		
s_axil_arvalid	I	AXI4-Lite Read address valid
s_axil_arready	O	AXI4-Lite Read address ready
s_axil_araddr	I	AXI4-Lite Read address
s_axil_arprot	I	AXI4-Lite Protection type
AXI READ DATA CHANNEL		
s_axil_rvalid	I	AXI4-Lite Read valid
s_axil_rready	O	AXI4-Lite Read ready
s_axil_rresp	I	AXI4-Lite Read data
s_axil_rdata	O	AXI4-Lite Read response
OCLA PORTS		
i_probes	I	OCLA Probes port
i_trigger_input	I	OCLA Trigger input port. It is an optional port

Table 5. OCLA Interface

Parameters

Table 5 lists the parameters of the OCLA.

Parameters	Values	Default Value	Description
NO_OF_PROBES	1-1024	1	Number of OCLA probe ports.
MEM_DEPTH	32, 64, 128, 256, 512,1024	32	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
VALUE_COMPARE	TRUE/FALSE	FALSE	To enable Value Compare feature
VALUE_COMPARE_PROBE_WIDTH	1-31	1	Probe width in case of value compare mode
TRIGGER_INPUTS_EN	TRUE/FALSE	FALSE	To enable Trigger inputs
NO_OF_TRIGGERS_INPUT	1-31	1	Number of trigger input ports.
S_AXI_DATA_WIDTH	32	32	AXI data width
S_AXI_ADDR_WIDTH	8, 16, 32	32	AXI address width

Table 5. Parameters

Registers Address Space

Table 7 lists the configuration registers of the OCLA.

Name	Register ID	Bits	Type	Off sets	Default Value	Description
OCLA Status Register	OCSR	32	RO	0x00	0xC0000000	Bitfields of this OCSR contains configuration status of OCLA
Trace Buffer Data Register	TBDR	32	RO	0x04	0x00000000	TBDR can be read to stream the whole acquisition data to some output interface
Trigger Control Register	TCUR	32	RW	0x08	0x00000000	TCUR is used to control the trigger control unit (2 Triggers)
Trigger Control Register	TCUR1	32	RW	0x14	0x00000000	TCUR1 is used to control the trigger control unit (2 Triggers)
Trigger Mode Type Register	TMTR	32	RW	0x0C	0x00000000	TMCR is used configure trigger Modes
Trigger Data Compare Register	TDCR	32	RW	0x10	0x00000000	Trigger Data to compare with the probe port
IP Type Register	IP TYPE	32	RO	0x18	"ocla"	This register hold the IP Type "ocla"
IP Verison Register	IP VERSION	32	RO	0x1C	"0x00000001"	This register hold the IP Version
IP ID Register	IP ID	32	RO	0x20	"0x03881734"	This register hold the IP ID

Configuration Registers

Design Flow

IP Customization and Generation

OCLA IP core is a part of the Raptor Design Suite Software. A customized ocla can be generated from the Raptor's IP configurator window.

Figure 3. IP list

Parameters Customization: From the IP configuration window, the parameters of the OCLA can be configured and OCLA features can be enabled for generating a customized OCLA IP core that suits the user application requirment.

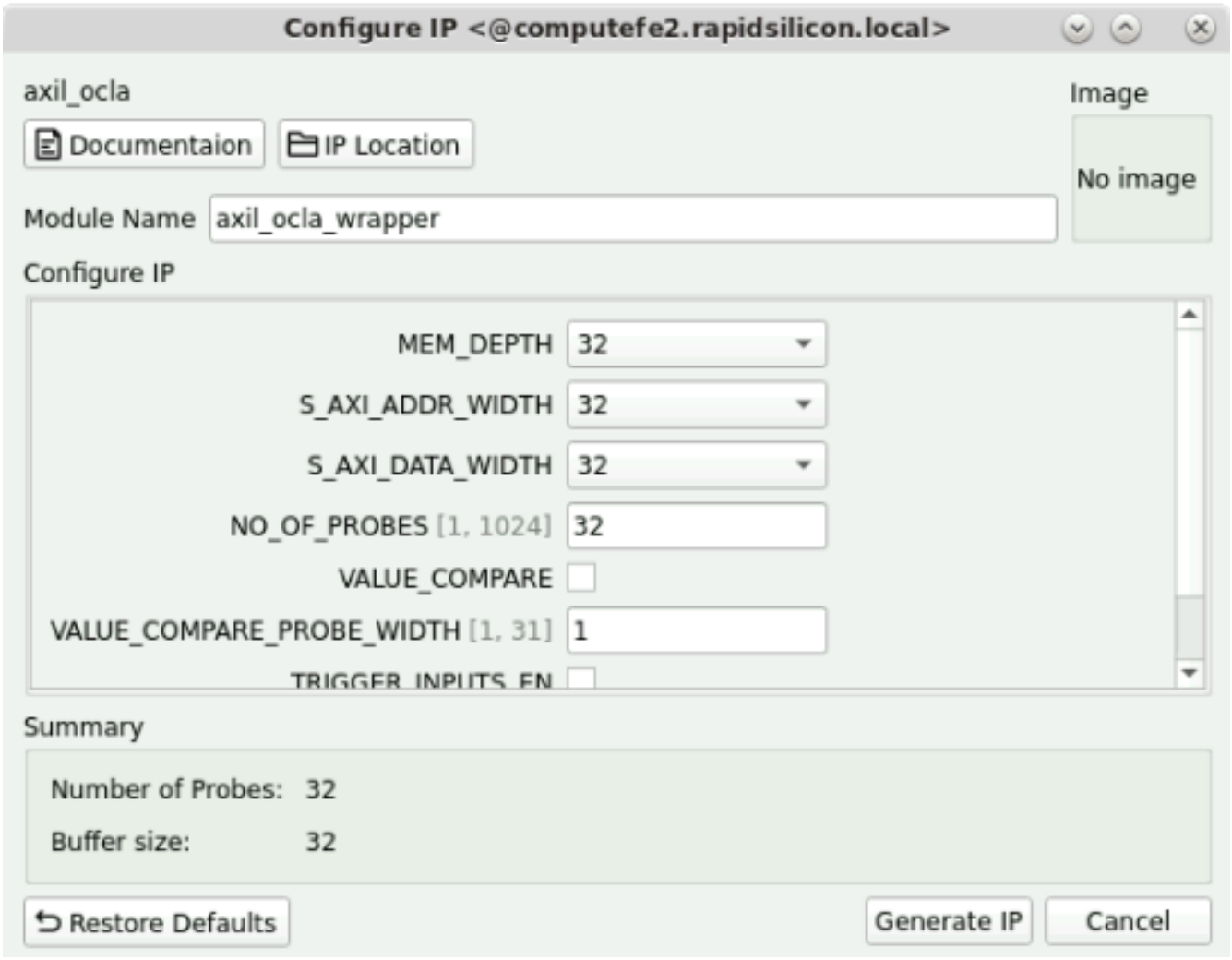


Figure 4. IP Configuration

OCLA Debug Subsystem

The Generated OCLA IP Wrapper

The IP customization and generation step is followed by the availability of a top wrapper and all source files for the user. The generated top wrapper file for the OCLA (see figure 1) comprises of two distinct clock domains, namely the sample clock and the AXI clock.

It is crucial to note that the sample clock of the OCLA should be connected to the design being monitored, while the AXI clock should be connected to the AXI bus clock.

The signals of the design that are intended to be sampled are connected to the probes port of the OCLA. In addition, the user-specified optional input triggers signals can be connected to the corresponding port in the top wrapper.

For configuring the OCLA and reading the sampled data from the system, the AXI-lite slave interface must be connected to an AXI bus.

OCLA Debug Subsystem

The OCLA IP core, a component used for debugging purposes, can be instantiated within a subsystem. The debug subsystem, as depicted in Figure 5, integrates the OLCA IP core within the AXI bus and the design being monitored. The purpose of this integration is to allow for the runtime configurations of OCLA configurations through the use of the JTAG interface.

This interface serves as the primary means of controlling and configuring the OCLA IP core within the subsystem, enabling the debugging process to proceed efficiently.

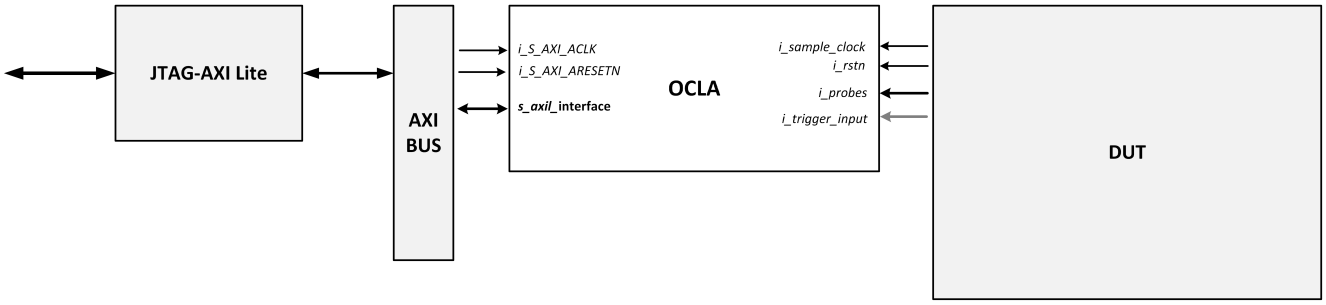


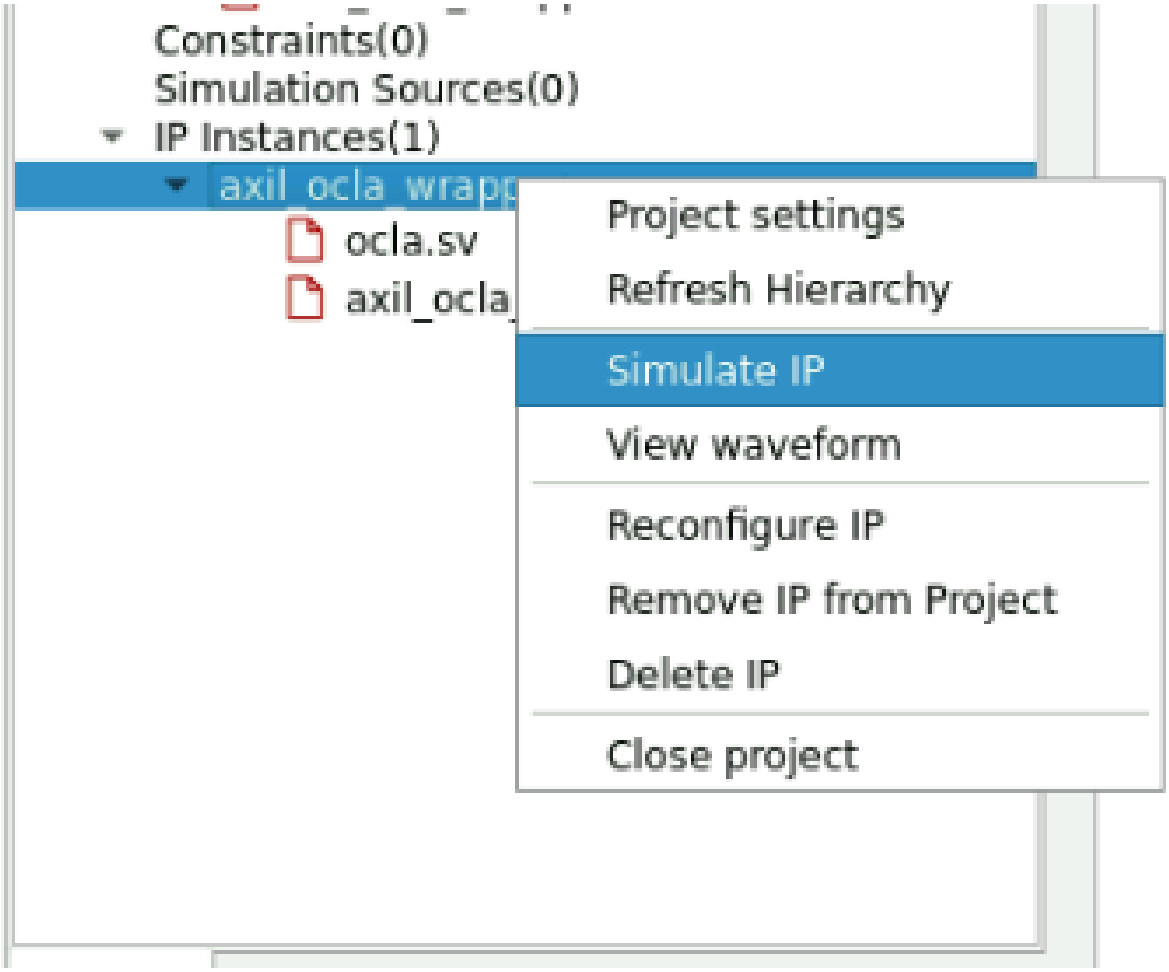
Figure 5. OCLA Debug Subsystem

Test Bench

To check the behavior of the IP Core, a verilog test-bench with basics configuration is available for simulation. Once the IP is generated then test-bench file can be found in the IP directory under sim folder.

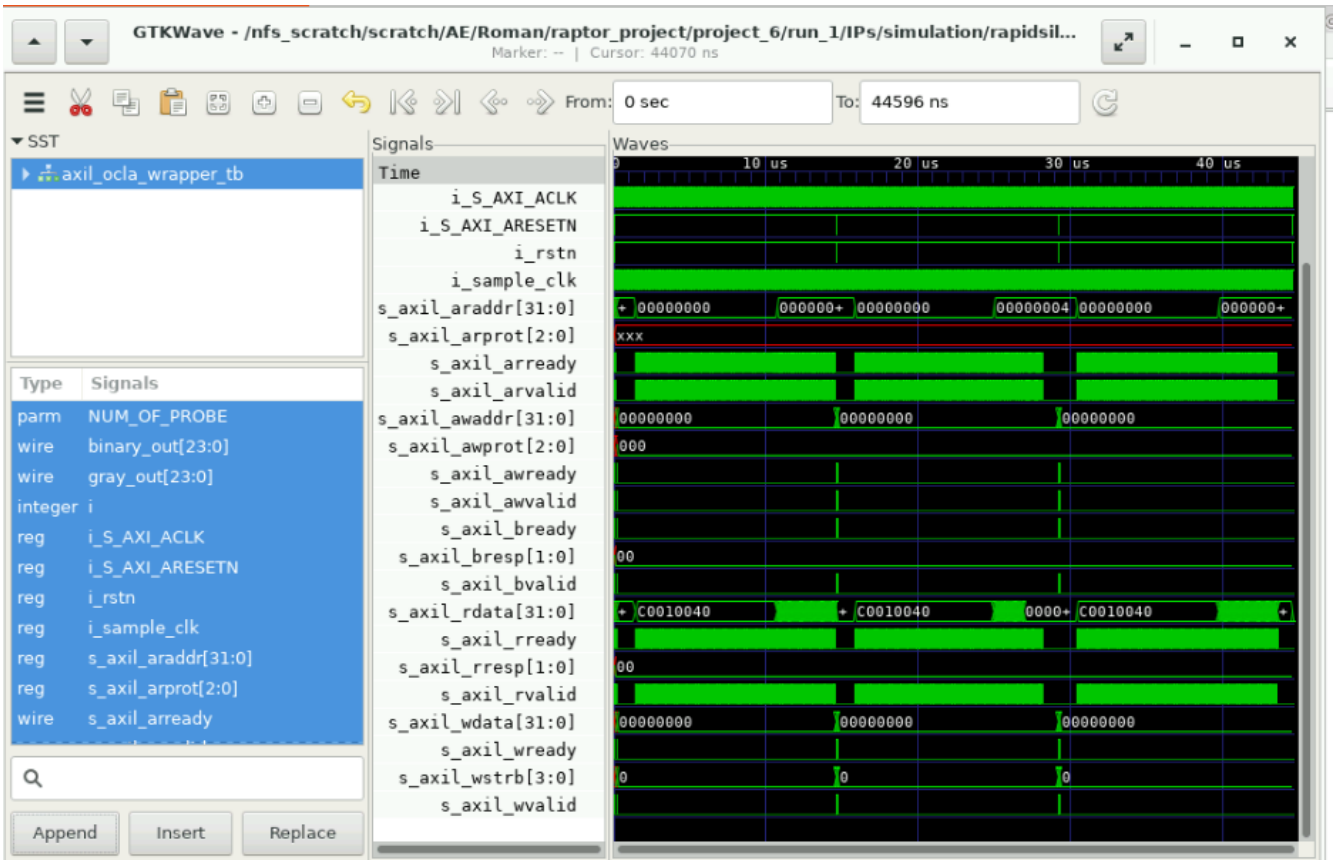
Running Simulation

1. Right click on the IP name within source tab and select Simulate IP as shown in figure below.



Running Simulation

2.This will run the simulation and result will dumped into vcd file.To see the waveform, again right click on the IP and select View waveform. The GTKWave will open showing the IP simulation result as shown in figure below.



Simulation Result

References

A comprehensive guide explaining how to use OCLA to debug a design can be found here.

Revision History

Date	Version	Revisions
December 7, 2023	0.01	Initial version OCLA User Guide Document