AXI DPRAM
(Beta Release)

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IP Summary

Introduction

AXI DPRAM (Dual-Port RAM) is a type of memory block that uses the AXI (Advanced eXtensible Interface) protocol for data communication. The AXI protocol is a widely used interface standard for high-speed digital circuits, providing a high-bandwidth, low-latency communication link between hardware components. It is specialized type of RAM that has two independent ports for simultaneous read and write operations from two different sources. This feature allows for greater flexibility and efficiency in data transfer between different hardware components in a digital system. It is particularly useful in applications where multiple components need to access the memory block at the same time, without causing delays or conflicts. One of the key advantages of the AXI DPRAM is its ability to operate at high speeds. This makes it ideal for use in high-performance applications where fast data transfer is critical.

Features

- AXI4 (memory mapped) one master and one slave interface
- Configurable data width 8, 16, 32, 64, 128, 256 bits
- Configurable address width 8 to 16 bits
- Support ID width up to 32 bits
- Extra pipeline register for each port.
- Interleaving write and read burst cycles option for each port
- Compatible with AXI4 Interconnect

Overview

AXI DPRAM

The AXI DPRAM IP Core is a part of Raptor Design Suite which is designed to be used in digital systems and is compatible with the AMBA AXI4 (Advanced eXtensible Interface 4) standard. It is a high-performance memory that features two independent data ports, allowing simultaneous read and write access from two different sources. It is commonly used in applications where high-speed data transfer is required, such as in graphics processing, video processing, and networking. It provides efficient data transfer between the memory and other components in the system. It includes features such as burst transfer support, configurable address width and data width.

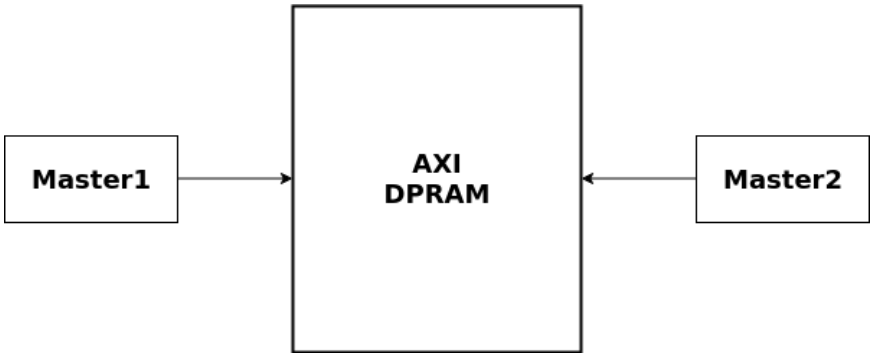

Figure 1: AXI DPRAM Block Diagram

IP Specification

The AXI DP RAM IP core is a high-performance, dual-port RAM memory block designed for use in FPGAs. It is based on the Advanced Microcontroller Bus Architecture (AMBA) AXI4 protocol and features two independent read/write ports, allowing for simultaneous access by multiple processors or peripherals. It supports a wide range of data widths, from 8 bits to 256 bits, and can be configured for different memory sizes up to a maximum of 16 terabytes. It also includes extra pipeline registers for each port and interleaving write and read burst cycles option for each port. This IP core is commonly used in a wide range of applications, including embedded systems, digital signal processing, network processing, and video processing. It is fully customizable and can be easily integrated into new or existing FPGA designs.

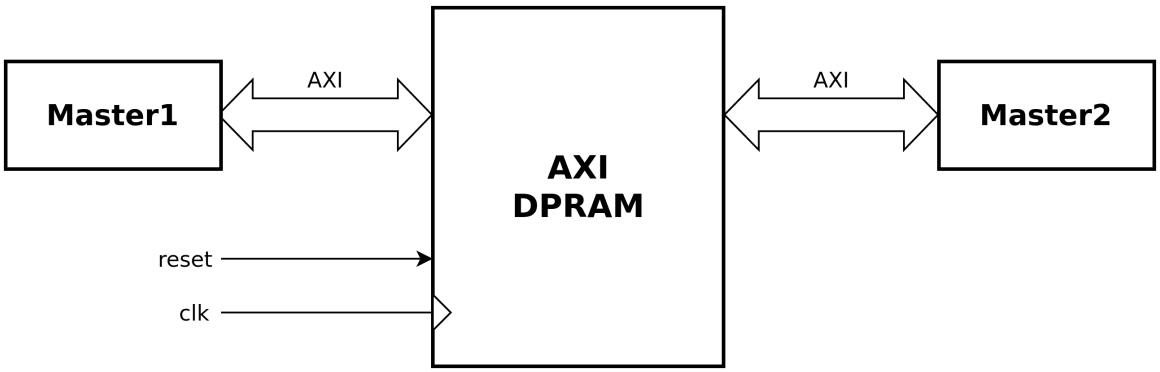

Figure 2: Top Module

Standards

The AXI4 Master and Slave interfaces are compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The Table 1 gives the support details for AXI DPRAM.

Compliance		IP Resources				Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Simulation Model**	**Analyze and Elaboration**	**Simulation**	**Synthesis**
GEMINI	AXI4	Verilog	-	Cocotb	-	Raptor	Raptor	Raptor

Table 1: Support Details

Resource Utilization

The parameters for computing the maximum and the minimum resource utilization are given in Table 2. Other parameters are kept at their default values.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
	Configuration		**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	8	BRAMS	1
	ADDR_WIDTH	8	REGISTERS	115
	ID_WIDTH	8	LUTS	195
	A_PIP_OUT	False	-	-
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	DATA_WIDTH	256	BRAMS	16
	ADDR_WIDTH	16	REGISTERS	976
	ID_WIDTH	32	LUTS	1287
	A_PIP_OUT	True	-	-

Table 2: Resource Utilization

Ports

Table 3 lists the top interface ports of the AXI DPRAM.

Signal Name	I/O	Description
a_clk	I	Clock Signal for Port A of RAM
a_rst	I	Active High Synchronous Reset Signal for Port A of RAM
b_clk	I	Clock Signal for Port B of RAM
b_rst	I	Active High Synchronous Reset Signal for Port B of RAM
Master Write Address Channel		
s_axi_awid	I	Write address ID
s_axi_awaddr	I	Write address
s_axi_awlen	I	Burst length
s_axi_awsize	I	Burst size
s_axi_awburst	I	Burst type
s_axi_awlock	I	Lock type
s_axi_awcache	I	Memory type
s_axi_awprot	I	Protection type
s_axi_awvalid	I	Write address valid
s_axi_awready	O	Write address ready
Master Write Data Channel		
s_axi_wdata	I	Write data
s_axi_wstrb	I	Write strobe
s_axi_wlast	I	Write last
s_axi_wvalid	I	Write valid
s_axi_wready	O	Write ready
Master Write Response Channel		
s_axi_bid	O	Response ID tag
s_axi_bresp	O	Write response
s_axi_bvalid	O	Write response valid
s_axi_bready	I	Write response ready
Master Read Address Channel		
s_axi_arid	I	Read address ID
s_axi_araddr	I	Read address
s_axi_arlen	I	Burst length
s_axi_arsize	I	Burst size
s_axi_arburst	I	Burst type
s_axi_arlock	I	Lock type
s_axi_arcache	I	Memory type
s_axi_arprot	I	Protection type
s_axi_arvalid	I	Read address valid
s_axi_arready	O	Read address ready
Master Read Data Channel		
s_axi_rid	O	Read ID tag

Signal Name	I/O	Description
s_axi_rdata	O	Read data
s_axi_rresp	O	Read response
s_axi_rlast	O	Read last
s_axi_rvalid	O	Read valid
s_axi_rready	I	Read ready
Slave Write Address Channel		
m_axi_awid	O	Write address ID
m_axi_awaddr	O	Write address
m_axi_awlen	O	Burst length
m_axi_awsize	O	Burst size
m_axi_awburst	O	Burst type
m_axi_awlock	O	Lock type
m_axi_awcache	O	Memory type
m_axi_awprot	O	Protection type
m_axi_awvalid	O	Write address valid
m_axi_awready	I	Write address ready
Slave Write Data Channel		
m_axi_wdata	O	Write data
m_axi_wstrb	O	Write strobe
m_axi_wlast	O	Write last
m_axi_wvalid	O	Write valid
m_axi_wready	I	Write ready
Slave Write Response Channel		
m_axi_bid	I	Response ID tag
m_axi_bresp	I	Write response
m_axi_bvalid	I	Write response valid
m_axi_bready	O	Write response ready
Slave Read Address Channel		
m_axi_arid	O	Read address ID
m_axi_araddr	O	Read address
m_axi_arlen	O	Burst length
m_axi_arsize	O	Burst size
m_axi_arburst	O	Burst type
m_axi_arlock	O	Lock type
m_axi_arcache	O	Memory type
m_axi_arprot	O	Protection type
m_axi_arvalid	O	Read address valid
m_axi_arready	I	Read address ready
Slave Read Data Channel		
m_axi_rid	I	Read ID tag
m_axi_rdata	I	Read data
m_axi_rresp	I	Read response

Signal Name	I/O	Description
m_axi_rlast	I	Read last
m_axi_rvalid	I	Read valid
m_axi_rready	O	Read ready

Table 3: Port List

Parameters

Table 4 lists the parameters of the AXI DPRAM.

Parameter	Values	Default Value	Description
DATA_WIDTH	8, 16, 32, 64, 128, 256	32	Data Width of RAM
ADDR_WIDTH	8 - 16	16	Address Width of RAM
ID_WIDTH	1 - 32	32	ID field of RAM
A_PIP_OUT	True/False	True	Piplelined Output for Port A
B_PIP_OUT	True/False	True	Piplelined Output for Port B
A_INTERLEAVE	True/False	True	Interleave write and read burst cycles on Port A
B_INTERLEAVE	True/False	True	Interleave write and read burst cycles on Port B

Table 4: Parameters

Design Flow

IP Customization and Generation

AXI DPRAM IP core is a part of the Raptor Design Suite Software. A customized memory can be generated from the Raptor's IP configuration window as shown in figure 3.

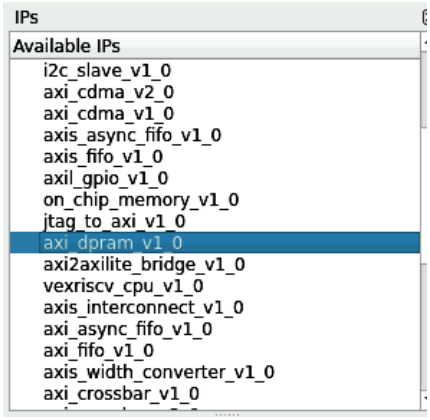

Figure 3: IP List

Parameters Customization

From the IP configuration window, the parameters of the AXI DPRAM can be configured and it's features can be enabled for generating a customized IP core that suits the user application requirements. All parameters are shown in Figure 4. In Figure 4, the module name specifies the name of both the Verilog file and the top-level IP name that will be generated based on above configured parameters. The Output Dir is a directory option that allows the user to specify where they want the generated IP to be saved.

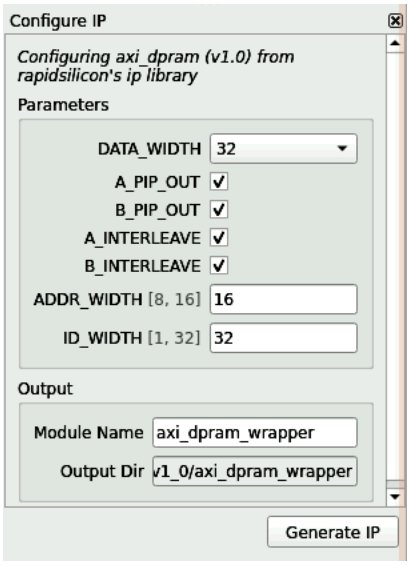

Figure 4: IP Configuration

Test Bench

The AXI DPRAM IP is provided with a testbench which is based upon Cocotb verification environment. In this test, multiple read/write transactions are performed by two masters. The input data is generated using a test data generator module. The output data is compared with the expected output data to verify the correctness of the IP core's operation. The dump file is generated to view the output of the test. In the end, there is status for passing or failure of the test.

Revision History

Date	Version	Revisions
May 11, 2023	0.1	Initial version AXI DPRAM User Guide