AXI DDR SDRAM V1.0

IP User Guide(Beta Release)

August 4, 2024

RapidSilicon

Contents

IP Summary

Introduction

This document provides a technical overview of the AXI DDR SDRAM controller IP core. This pre-verified module facilitates communication between an AXI bus and DDR SDRAM memory devices. It bridges the protocol gap between the processor-centric AXI interface and the specialized commands required by DDR memory.

It translates AXI transactions into the specific command, address, and data signals required by the DDR memory. This core can be configured via Raptor's IP Catalog GUI interface.

Features

- 32-bit AXI4 slave interface
- Supporting AXI read and write transactions
- Handling address translation between AXI and DDR memory space
- Generating the necessary control signals for DDR memory refresh and power management
- Providing error detection and correction capabilities (depending on specific IP implementation)

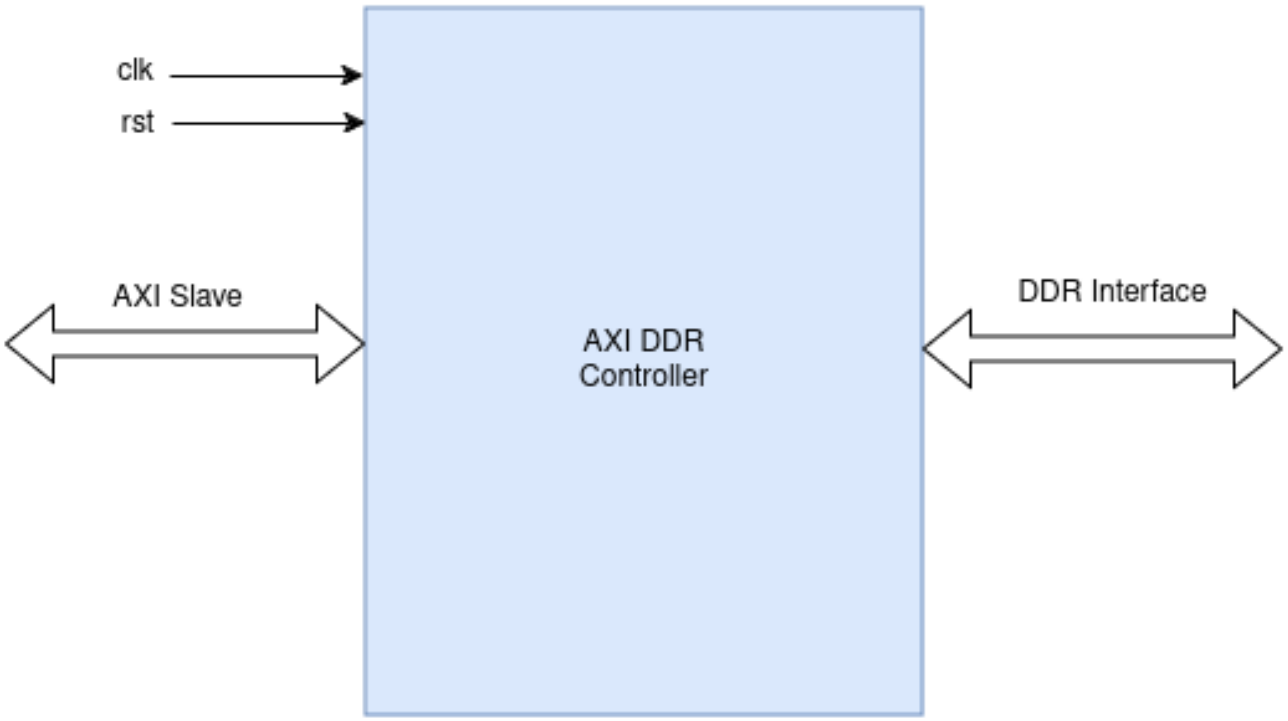

Figure 1. AXIblock level diagram

Licensing

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IP Specification

Overview

The AXI DDR SDRAM (Double Data Rate Synchronous Dynamic Random-Access Memory) controller is a sophisticated memory interface employed in high-performance digital systems, leveraging the Advanced eXtensible Interface (AXI) protocol for optimal data transfer efficiency. DDR SDRAM operates by synchronizing data transfers to both the rising and falling edges of the clock signal, effectively doubling the data throughput compared to single data rate (SDR) SDRAM. The integration of AXI with DDR SDRAM ensures efficient and reliable data transactions, making it ideal for applications requiring high bandwidth and fast memory access, such as high-performance computing, graphics processing, and complex embedded systems.

An AXI-based memory controller translates AXI transactions into appropriate DDR commands while managing the timing and complexity of DDR operations. For read transactions, the memory controller checks if the required row in the DDR SDRAM is active; if not, it issues an activate command followed by a read command. The fetched data is then sent back through the AXI read data channel. For write transactions, the controller similarly activates the necessary row if it isn't already active and then issues a write command to store the data from the AXI write data channel into the DDR memory. The controller intelligently schedules these commands to optimize performance, including interleaving commands to different banks, issuing precharges when needed, and ensuring timely refresh operations.

The key DDR SDRAM commands include ACTIVATE, READ, WRITE, PRECHARGE, REFRESH, and NO OPERATION (NOP). The ACTIVATE command makes a specific row within a memory bank accessible for read or write operations. The READ command retrieves data from the activated row, while the WRITE command stores data in the activated row. The PRECHARGE command closes the currently active row in a bank, preparing it for the next activate command. The REFRESH command periodically refreshes the data in the memory cells to prevent data loss due to charge leakage. NOP commands are used to introduce delays as required by timing constraints.

By combining the high-speed capabilities of DDR memory with the flexible and efficient AXI protocol, the AXI DDR SDRAM controller optimizes data transactions through burst mode, supports out-of-order transactions, and includes quality of service (QoS) levels for prioritizing critical data transfers. The memory controller also hides the latency of DDR operations by overlapping commands and transactions where possible. Error handling mechanisms ensure reliable communication, making the AXI DDR SDRAM controller a critical component in modern digital systems, essential for maintaining high performance and power efficiency in demanding applications.

IP Support Details

Compliance		IP Resources					Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Software Driver	Analyze and Elaboration	Simulation	Synthesis
GEMINI	AXI4	Systemverilog	SDC	Systemverilog	-	-	Raptor	Raptor	Raptor

Ports

Table 2 lists the top interface ports of the AXI Async FIFO.

Signal Name	I/O	Description
AXI Clock and Reset		
i_s_axi_clk	I	AXI4 Clock
i_s_axi_resetn	I	AXI4 RESET
i_m_axi_clk	I	AXI4 Clock
AXI WRITE ADDRESS CHANNEL		
s_axil_awvalid	I	AXI4 Write address valid
s_axil_awready	O	AXI4 Write address ready
s_axil_awaddr	I	AXI4 Write address
s_axil_awprot	I	AXI4 Protection type
AXI WRITE DATA CHANNEL		
s_axil_wvalid	I	AXI4 Write valid
s_axil_wready	O	AXI4 Write ready.
s_axil_wdata	I	AXI4 Write data
s_axil_wstrb	I	AXI4 Write strobes
AXI WRITE RESPONSE CHANNEL		
s_axil_bvalid	O	AXI4 Write response valid
s_axil_bready	I	AXI4 Response ready
s_axil_bresp	O	AXI4 Write response
AXI READ ADDRESS CHANNEL		
s_axil_arvalid	I	AXI4 Read address valid
s_axil_arready	O	AXI4 Read address ready
s_axil_araddr	I	AXI4 Read address
s_axil_arprot	I	AXI4 Protection type
AXI READ DATA CHANNEL		
s_axil_rvalid	I	AXI4 Read valid
s_axil_rready	O	AXI4 Read ready
s_axil_rresp	I	AXI4 Read data
s_axil_rdata	O	AXI4 Read response
DDR Interface		
ddr_ck_p	I	DDR clock positive
ddr_ck_n	O	DDR clock negative
ddr_cke	I	DDR Clock enable
ddr_cs_n	I	DDR chip select
ddr_ras_n	I	DDR Row address strobe
ddr_cas_n	O	DDR Column address strobe
ddr_we_n	I	DDR wriite enable

ddr_ba	I	DDR bank address
ddr_a	O	DDR Address
ddr_dm	I	DDR data mask
ddr_dqs	O	DDR data strobe
ddr_dq	I	DDR data

AXI Async FIFO Interface

Parameters

Table 3 lists the parameters of the AXI Async FFIFO.

Parameter	Values	Default Value	Description
READ_BUFFER	0-1	1	Data width of data being transferred.
BA_BITS	1-3	2	FIFO address width.
ROW_BITS	1-13	13	FIFO ID width.
COL_BITS	1-11	11	Depth of internal FIFO.
DQ_LEVEL	0-1	1	Data width of data being transferred.

Parameters

Resource Utilization

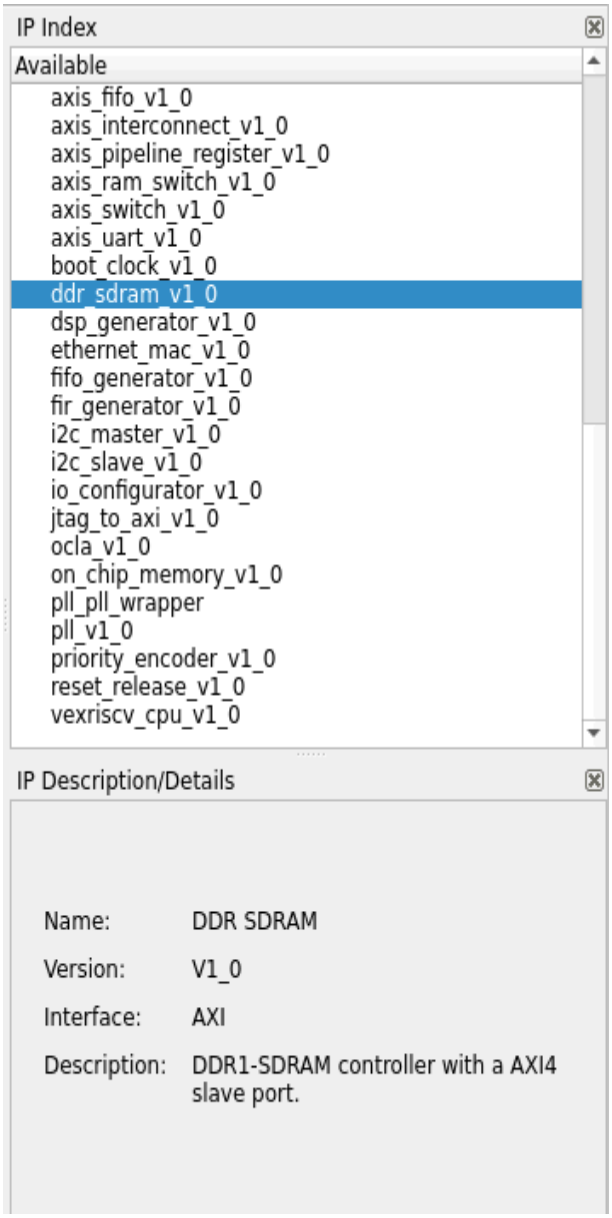
Please note that the utilization provided in this section for the AXI DDR SDRAM core should be considered as estimates, as they are based on its usage in conjunction with other design modules in the FPGA. Once integrated with other designs in the system, the FPGA resource utilization and core timing may differ from the reported results.

Tool	Raptor Design Suite			
FPGA Device	GEMINI			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	FIFO DEPTH	8	LUT	119
	DATA WIDTH	8	Registers	217
	ADDR WIDTH	8	BRAM	5
	ID WIDTH	8	DSP	0
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	FIFO DEPTH	8096	LUT	610
	DATA WIDTH	64	Registers	717
	ADDR WIDTH	32	BRAM	22
	ID WIDTH	8	DSP	0

Design Flow

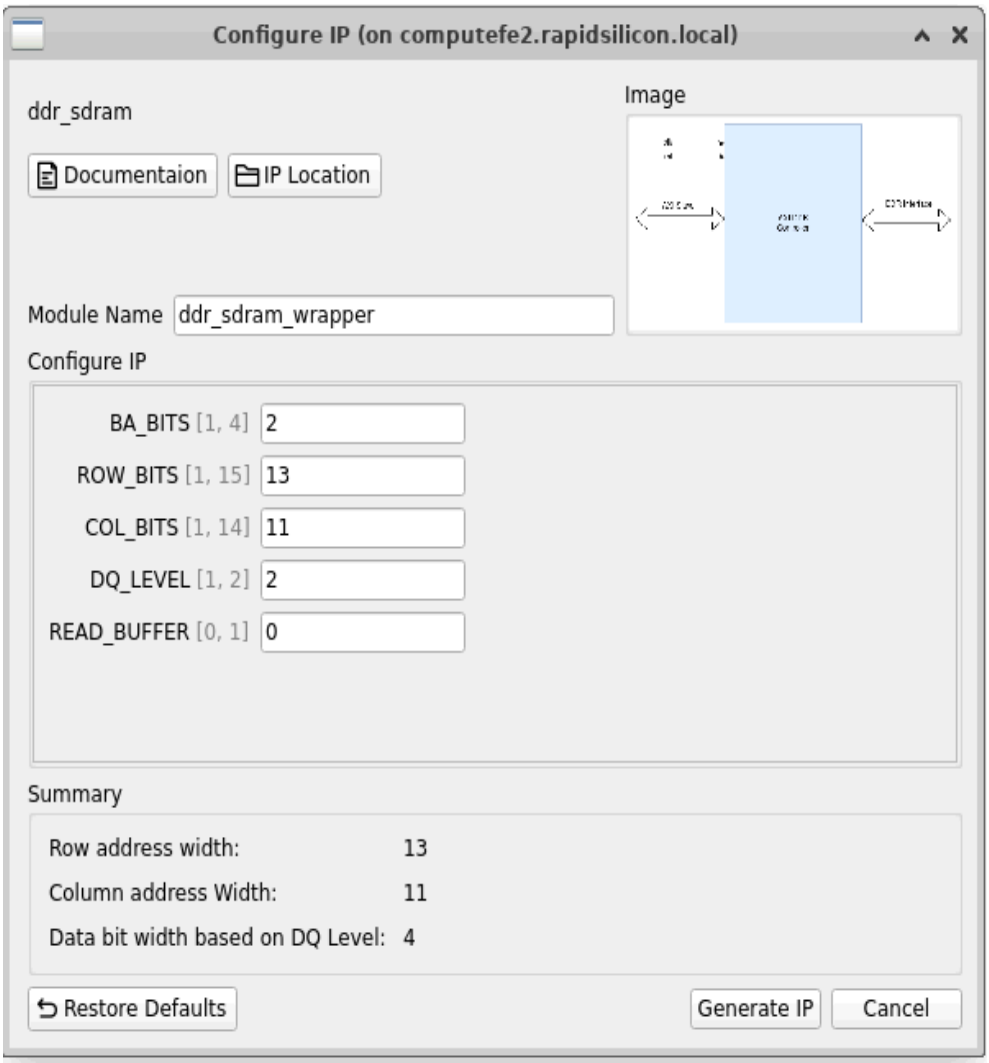
IP Customization and Generation

AXI DDR SDRAM IP core is a part of the Raptor Design Suite Software. A customized AXI DDR SDRAM can be generated from the Raptor's IP configurator window.



Selecting AXI DDR SDRAM from IP Catalog List

Parameters Customization: From the IP configuration window, the parameters of the AXI DDR SDRAM can be configured and AXI DDR SDRAM features can be enabled for generating a customized AXI DDR SDRAM IP core that suits the user application requirement.



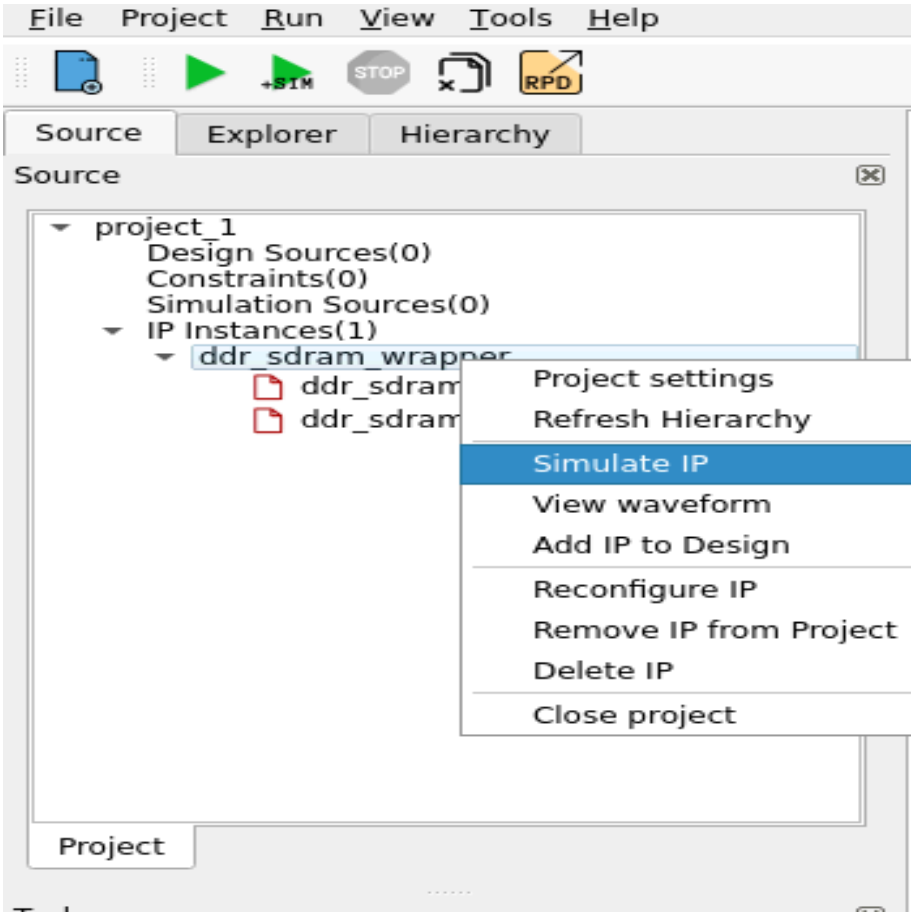
IP Configuration

Synthesis and PnR

Raptor Suite is armed with tools for Synthesis along with Post and Route capabilities and the generated post- synthesis and post-route and place netlists can be viewed and analyzed from within the Raptor. The generated bitstream can then be uploaded on an FPGA device to be utilized in hardware application

Test Bench

The IP package hosts a simple Verilog based test bench that validates design functionality. It can be simulated using Iverilog, Verilator or other simulators. The simulation can be easily run by clicking the "Simulate IP" button as shown in figure 4. The waveforms are also dumped for in-depth analysis of the whole operation which can be seen by clicking the "View Waveform" button.



Simulate IP Window

Revision History

Date	Version	Revisions
August 4, 2024	0.01	Initial version AXIUser Guide Document