Emulate-IO v1.0

***IP User Guide** (Beta Release)*

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RapidSilicon

Contents

IP Summary

Introduction

The Emulate-IO core is an AXI4-Lite compliant IP that offers input and output probes to sample and drive signals on FPGA fabric. The core provides an AXI4-slave interface that can be used to control the emulated IOs in real time. A total of 1024 probes are provided by the core, half of which can be set as inputs and the other half can be set as outputs.

Features

The EIO IP provides the following features to the user:

- AXI4-Lite slave interface for reading the sampled input probes and driving the output probes.
- Configurable data width of AXI4-Lite bus (32/64 bits).
- Up to sixteen 32-bit or eight 64-bit wide dedicated registers for storing sampled inputs.
- Up to sixteen 32-bit or eight 64-bit wide dedicated registers for storing output values to be driven on output probes.
- Separate input and output clocks for registering inputs and outputs.

Overview

Emulate-IO

The EIO core can be configured through its AXI-Lite slave interface. The core provides input and output probes to virtually drive logic blocks and verify their functionality. An overview of the IP in a practical use case is shown in figure-1.

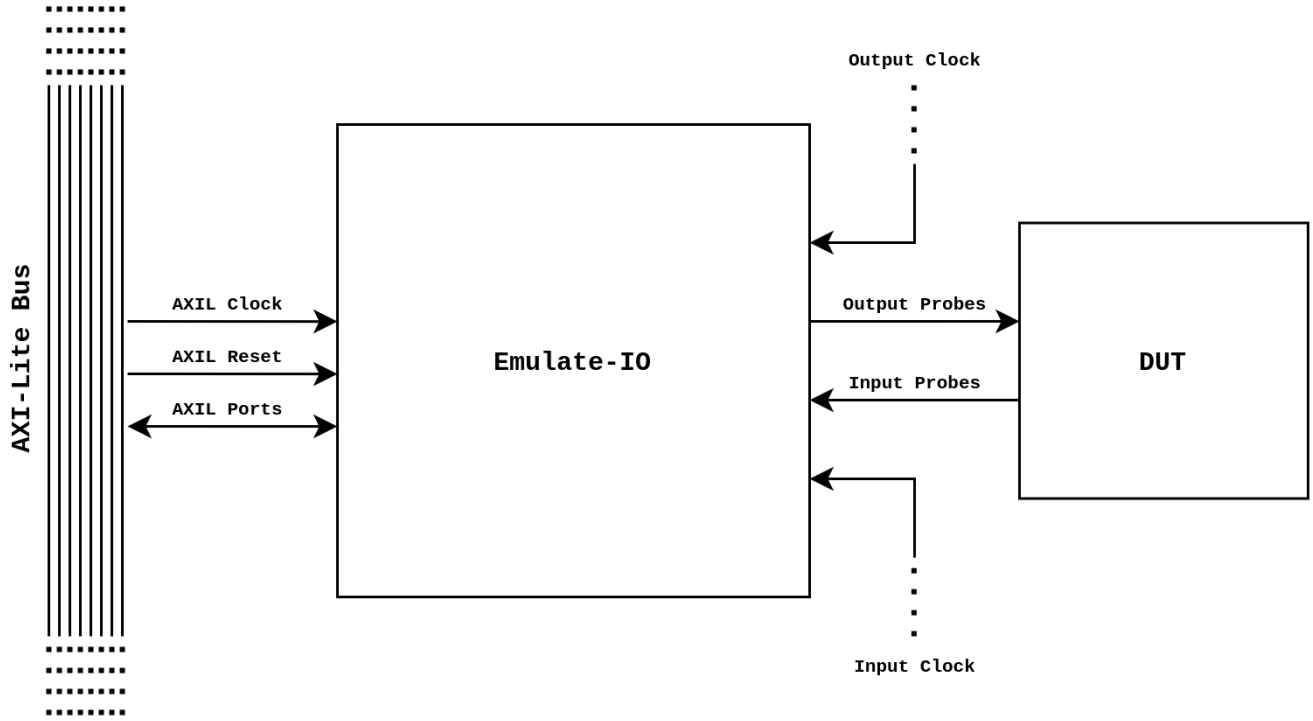

Figure 1. EIO core use case.

Licensing

IP Specification

Overview

The figure-2 shows the internal block diagram of EIO core. The core includes a control register which will is reserved and currently does not provide any functionality. The number of input and output probes can be varied between 1 and 512. The probe are named from the perspective of the core. This means that input probes refer to the probes that are fed to the inputs port of the core (outputs *of* the DUT). Similarly, output probes refer to the probes that originate from the output ports of the core (inputs *to* the DUT).

The core has three clock inputs: AXIL, input and output clock. The AXIL clock drives the AXI-Lite logic. All of the input probes are sampled on the rising edge of the input clock. Similarly all outputs are driven using the output clock as well. All three clocks can be synchronous or asynchronous but this information must be passed to Raptor while generating the IP.

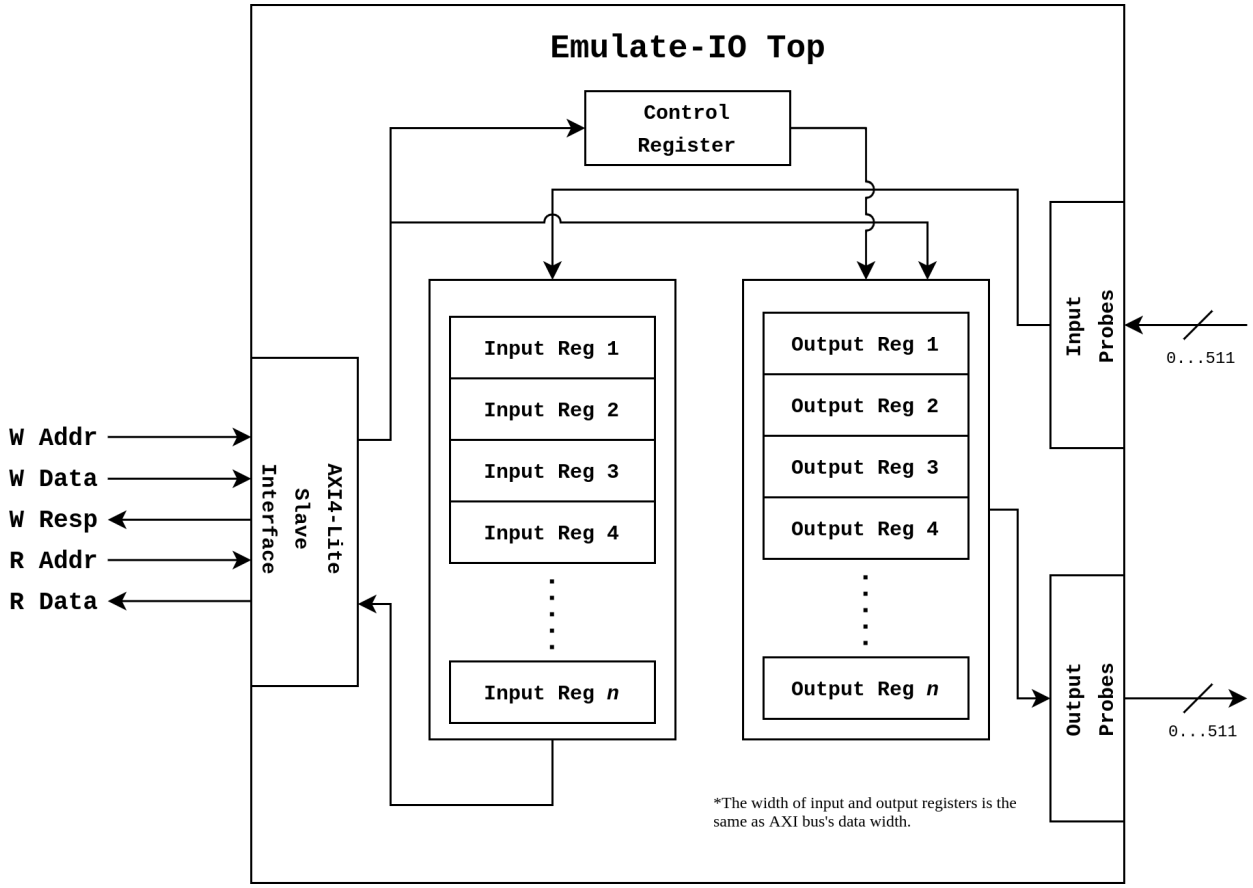

Figure 2. EIO core block diagram.

The state of IO probes, 1 or 0, is stored in internal registers that are accessible through the AXI-Lite interface. The width of these registers is the same as the configured AXIL data bus width. The number of these registers depends on the number of probes. For example, a single 32-bit bit input register is sufficient to store data from up to 32 input probes and same goes for output registers. It is also possible to partially fill a register, for example if the number of input probes is selected to be 90 with 64-bit AXIL data width then two input registers will be generated. The first register will store the least significant 64 bits and the second register will store the most significant 26 bits. The remaining 38 bits of the second register will be initialized with zeros and will always be read asr zero. The same

logic is followed for output registers as well. Further details about the register space can be found in the *'Register Space'* section.

Standards

The AXI4-Lite Slave interface is compliant with the AMBA® AXI Protocol Specification.

IP Support Details

The table below presents the specifics of IP support for the EIO IP Core, including pertinent information such as synthesis, simulation and source details.

Compliance		IP Resources			Tool Flow		
Device	**Interface**	**Source Files**	**Constraint File**	**Testbench**	**Analysis and Elaboration**	**Simulation**	**Synthesis**
Gemini	AXI4-Lite	Verilog	SDC	Systemverilog	Raptor	Raptor	Raptor

Table 1. EIO support details.

Resource Utilization

Tool	Raptor Design Suite			
FPGA Device	Gemini			
Configuration			**Resource Utilization**	
Minimum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	Number of input probes	1	LUT	32
	Number of output probes	1	DFF	73
	AXIL bus data width	32	BRAM	0
	AXIL and input clock sync	Yes	DSP	0
	AXIL and output clock sync	Yes		
Maximum Resource	**Options**	**Configuration**	**Resources**	**Utilized**
	Number of input probes	512	LUT	305
	Number of output probes	512	DFF	3718
	AXIL bus data width	64	BRAM	0
	AXIL and input clock sync	No	DSP	0
	AXIL and output clock sync	No		

Table 2. EIO resource utilization.

Ports

Table 4 lists the top interface ports of the EIO core.

Signal Name	I/O	Description
Clocks		
S_IP_CLK	I	Clock for sampling input probes
S_OP_CLK	I	Clock for updating output probes
AXI Clock and Reset		
S_AXI_ACLK	I	AXI4-Lite Clock
S_AXI_ARESETN	I	AXI4-Lite RESET
AXI WRITE ADDRESS CHANNEL		
s_axil_awvalid	I	AXI4-Lite write address valid
s_axil_awready	O	AXI4-Lite write address ready
s_axil_awaddr	I	AXI4-Lite write address
s_axil_awprot	I	AXI4-Lite protection type
AXI WRITE DATA CHANNEL		
s_axil_wvalid	I	AXI4-Lite write valid
s_axil_wready	O	AXI4-Lite write ready.
s_axil_wdata	I	AXI4-Lite write data
s_axil_wstrb	I	AXI4-Lite write strobes
AXI WRITE RESPONSE CHANNEL		
s_axil_bvalid	O	AXI4-Lite write response valid
s_axil_bready	I	AXI4-Lite response ready
s_axil_bresp	O	AXI4-Lite write response
AXI READ ADDRESS CHANNEL		
s_axil_arvalid	I	AXI4-Lite read address valid
s_axil_arready	O	AXI4-Lite read address ready
s_axil_araddr	I	AXI4-Lite read address
s_axil_arprot	I	AXI4-Lite protection type
AXI READ DATA CHANNEL		
s_axil_rvalid	I	AXI4-Lite read valid
s_axil_rready	O	AXI4-Lite read ready
s_axil_rresp	I	AXI4-Lite read data
s_axil_rdata	O	AXI4-Lite read response
EIO PORTS		
probe_in	I	EIO input probes (up to 512)
probe_out	I	EIO output probes (up to 512)

Table 4. EIO AXIL interface.

Parameters

Table 5 lists the parameters of the EIO core.

Parameter	Values	Default Value	Description
AXIL DATA WIDTH	32/64	32	Sets the width of AXIL bus.
NO. OF INPUT PROBES	1...512	8	Sets the number of input probes.
NO. OF OUTPUT PROBES	1...512	8	Sets the number of output probes.
AXI AND INPUT CLOCK SYNC	True or False	False	Sets whether the AXI and INPUT clock are synchronized or not.
AXI AND OUTPUT CLOCK SYNC	True or False	False	Sets whether the AXI and OUTPUT clock are synchronized or not.

Table 5. EIO configurable parameters.

Registers Address Space

Table 6 lists the configuration registers of the EIO.

Name	Register ID	Bits	Access	Offset	Default Value	Description
Control Register	CTRL	32	RW	0x00	0x00000000	Control register (Reserved)
Input Probe Register	AXI_DAT_IN	32/64	WO	0x04/0x08	0x00000000	Data at the input probes of EIO (received from the DUT)
Output Probe Register	AXI_DAT_OUT	32/64	RO	0x04/0x08	0x00000000	Data at the output probes of EIO (sent to the DUT)

Table 6. EIO register space.

Design Flow

IP Customization and Generation

The EIO IP core is a part of the Raptor Design Suite Software. A customized EIO core can be generated from the Raptor's IP configurator window.

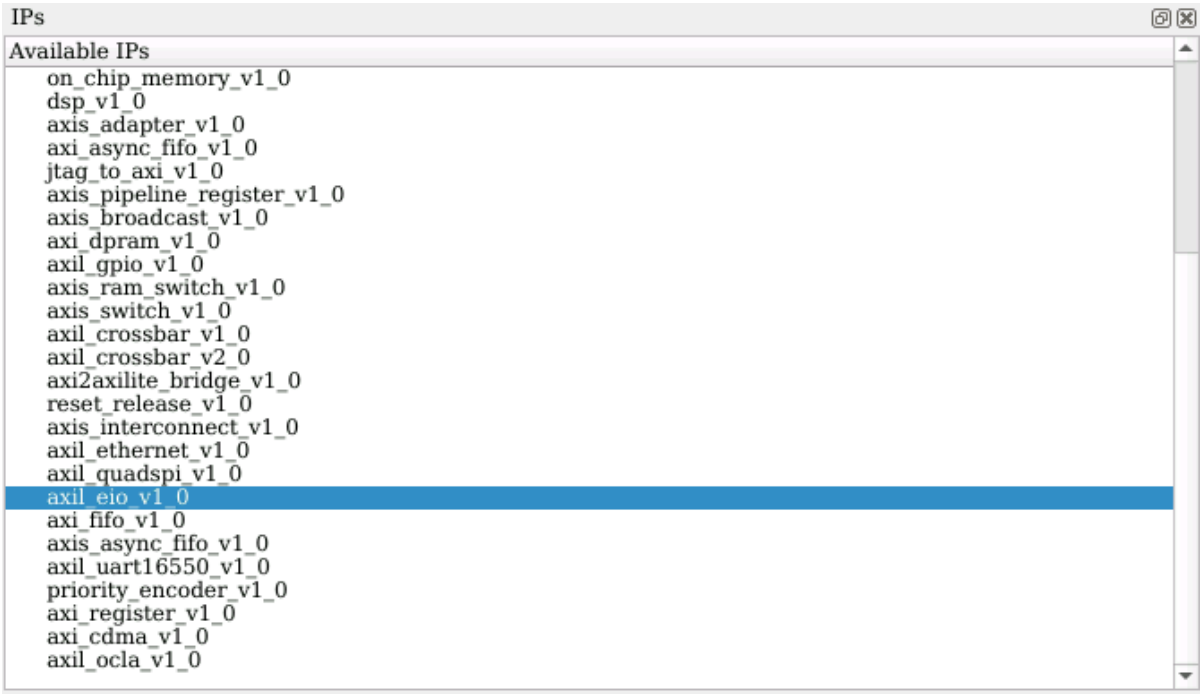

Figure 3. EIO core in Raptor IP Suite.

Parameters Customization: From the IP configuration window, the parameters of the EIO can be configured and EIO features can be enabled for generating a customized EIO IP core that suits the user application requirement.

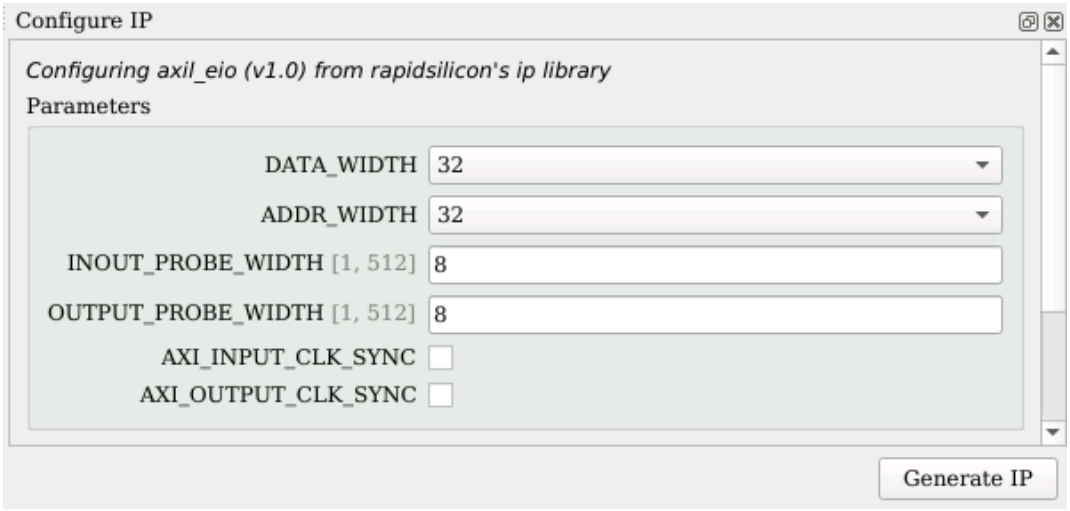

Figure 4. Configuration options for EIO.

EIO Debug Subsystem

The Generated EIO Core Wrapper

The IP customization and generation step is followed by the availability of a top wrapper and all source files for the user. The generated top wrapper file for the EIO (see figure 5) comprises of three distinct clock domains: input clock, output clock and AXI clock.

The signals of the design that are intended to be sampled are connected to the input probes of the EIO core. Similarly, the signals of the design that are intended to be driven are connected to the output probes of EIO core.

For configuring the EIO core and reading/driving data, the AXI-Lite slave interface must be connected to an AXI bus.

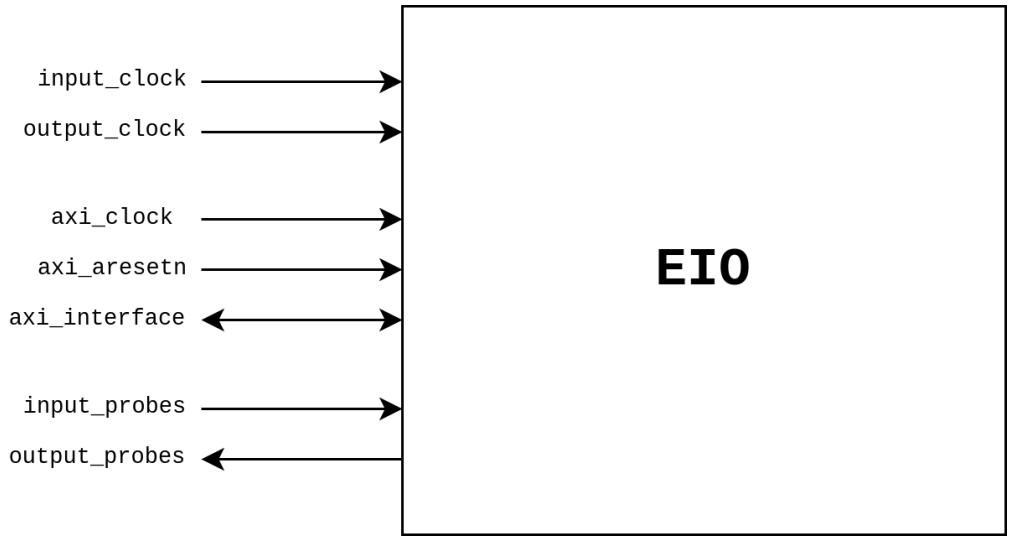

Figure 5. EIO top wrapper.

EIO Debug Subsystem

The EIO core is primarily used for providing inputs to a design under test while capturing its outputs as well. This mimics the behaviours of IOs without actually having to use dedicated IOs for the design. Since this IP is essentially used for debugging of a design, it can be integrated with the JTAG-to-AXI core for runtime configurations of EIO core through a JTAG host.

Example Design

This IP has no example design.

Test Bench

This IP has no test bench.

Revision History

Date	Version	Revisions
February 3, 2023	0.01	Initial version of EIO User Guide Document