**AHB2AXI4\_bridge IP**

AHB2AXI4 bridge is a protocol conversion IP. It converts incoming AHB (Advance High Performance Bus) protocol signals to AXI (Advanced Extensible Interface) protocol. Block diagram of AHB2AXI4 IP is shown in figure below:

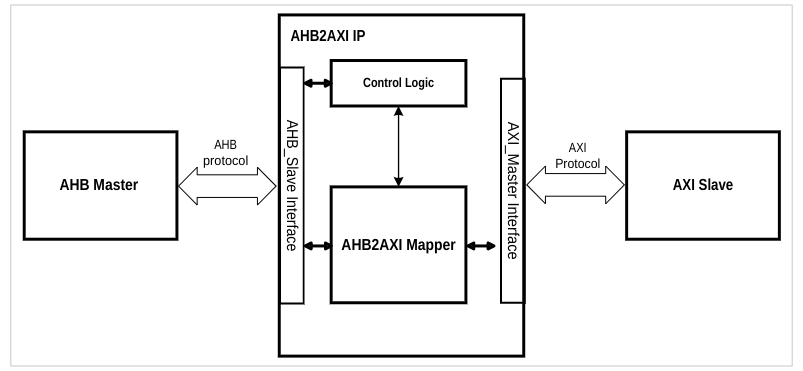


Figure1: Block Diagram

In AHB2AXI4 IP AHB\_Slave Interface is slave interface on AHB bus side. It accepts the control signals when a transfer is initiated by master side and generates ahb\_hreadyout based on the transfer progress on the AXI side.

The Control logic is the main controlling unit which generates the respective signals depending upon the transfer type and progress of that transfer. It detects the properties of a transfer on AHB side (Read/Write, Burst, Single, transfer type) and upon this information generate the AXI transfer signals appropriately. Below is the functional level flow diagram:

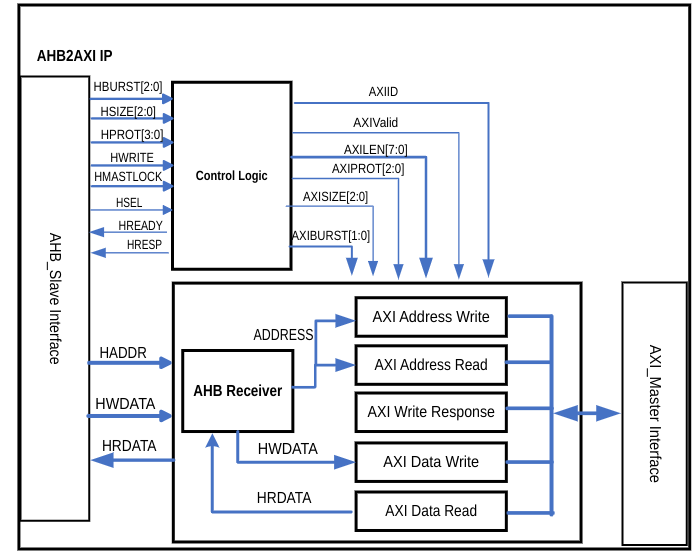


Figure2: Flow/Functional Diagram

**I/O signal Description**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S. No** | **Signal Name** | **Interface Type** | **I/O** | **Description** |
| 1 | s\_ahb\_aclk | AHB | I | AHB clock signal |
| 2 | s\_ahb\_areset | AHB | I | AHB reset signal active high (for entire design) |
| 3 | ahb\_hsel | AHB | I | Slave select signal of AHB interface |
| 4 | ahb\_haddr | AHB | I | AHB address bus |
| 5 | ahb\_hprot | AHB | I | Protection type. This signal indicates the normal, privileged level of the transaction and whether the transaction is a data access or an instruction access. |
| 6 | ahb\_htrans | AHB | I | AHB Transfer Type (NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY) |
| 7 | ahb\_hsize | AHB | I | Indicate the size of transfer. Tells how many bytes are in a AHB transfer |
| 8 | ahb\_hwrite | AHB | I | Transfer direction signal. This signal indicates AHB write access if HIGH and AHB read access if LOW. |
| 9 | ahb\_hburst | AHB | I | Burst type. Indicates if the transfer forms part of the burst. AHB supports Single, INCR, WRAP4, INCR4, WRAP8, INCR8, WRAP16, INCR16 burst type.  Note: The reference design doesn’t use this signal because it supports only single transfer type burst support is added by using this signal and generating the respective AXI signals for different burst types. |
| 10 | ahb\_hwdata | AHB | I | Write Data Bus is used to transfer the data from master to slave during write transactions. |
| 11 | ahb\_hreadyout | AHB | O | The AHB slave use this signal to indicate its ready to accept the transfer. |
| 12 | ahb\_hreadyin | AHB | I | HREADY input signal from interconnect if any |
| 13 | ahb\_hrdata | AHB | O | Read Data bus slave drives this bus to during read transfer when ahb\_hwrite is LOW. |
| 14 | ahb\_hresp | AHB | O | Provide information about the status of the transfer LOW means no error HIGH means error in transfer |
| 15 | ahb\_hnonsec | AHB | I | Indicates that the current transfer is either a Non-secure transfer or a Secure transfer. |
| **AXI Write Address Channel** | | | | |
| 16 | m\_axi\_awid[id\_width-1:0] | AXI | O | Write address ID. This signal is the identification tag for the write address group of signals |
| 17 | m\_axi\_awlen[7:0] | AXI | O | Burst length. The burst length gives the exact number of transfers in a burst |
| 18 | m\_axi\_awsize[2:0] | AXI | O | Burst size. This signal indicates the size of each transfer in the burst |
| 19 | m\_axi\_awburst[1:0] | AXI | O | Burst type. The burst type indicates the burst type AXI support FIXED, INCR, WRAP burst type this IP supports INCR and WRAP |
| 20 | m\_axi\_awaddr[addr\_width-1:0] | AXI | O | AXI Write address. The write address bus gives the address of the first transfer in a write burst transaction |
| 21 | m\_axi\_awprot | AXI | O | Protection type. This signal indicates the normal, privileged, or secure protection level of the write transaction and whether the transaction is a data access or an instruction access. |
| 22 | m\_axi\_awvalid | AXI | O | This signal indicates that valid write address and control information are available |
| 23 | m\_axi\_awready | AXI | I | This signal indicates that the slave is ready to accept an address and associated control signals |
| **AXI Write Data Channel** | | | | |
| 24 | m\_axi\_wdata[data\_width-1:0] | AXI | O | Write Data Bus. Master drives this bus to put data on this bus when performing a write transaction. |
| 25 | m\_axi\_wstrb[data\_width/8-1:0] | AXI | O | Write strobes. This signal indicates which byte lanes to update in memory. |
| 26 | m\_axi\_wlast | AXI | O | This signal indicates the last transfer of a burst  transaction. |
| 27 | m\_axi\_wvalid | AXI | O | This signal indicates that valid write data and  strobes are available. |
| 28 | m\_axi\_wready | AXI | I | This signal indicates that the slave can accept the write data. |
| **AXI Write Response Channel** | | | | |
| 29 | m\_axi\_bid[id\_width-1:0] | AXI | I | This signal is the identification tag for the write  response signals. |
| 30 | m\_axi\_bresp[1:0] | AXI | I | This signal indicates the status of the write  Transaction. |
| 31 | m\_axi\_bvalid | AXI | I | This signal indicates that a valid write  response is available. |
| 32 | m\_axi\_bready | AXI | O | This signal indicates that the master can  accept the response information. |
| **AXI Read Address Channel** | | | | |
| 33 | m\_axi\_arid[id\_width-1:0] | AXI | O | This signal is the identification tag for the read  address group of signals. |
| 34 | m\_axi\_araddr[addr\_width-1:0] | AXI | O | The read address bus gives the initial address  of a read burst transaction. |
| 35 | m\_axi\_arprot[2:0] | AXI | O | This signal provides protection unit information  for the read transaction. |
| 36 | m\_axi\_arvalid | AXI | O | When High, this signal indicates that the read address and control information is valid. |
| 37 | m\_axi\_arlen[7:0] | AXI | O | The burst length gives the exact number of transfers in a read burst. |
| 38 | m\_axi\_arsize[2:0] | AXI | O | This signal indicates the size of each transfer in the read burst. |
| 39 | m\_axi\_arburst[1:0] | AXI | O | Burst type. The burst type indicates the burst type AXI support FIXED, INCR, WRAP burst types. |
| 40 | m\_axi\_arready | AXI | I | This signal indicates that the slave is ready to accept an address and associated control signals for read transfer. |
| **AXI Read Data Channel** | | | | |
| 41 | m\_axi\_rid[d\_width-1:0] | AXI | I | This signal is the identification tag for the read data group of signals. |
| 42 | m\_axi\_rdata[data\_width-1:0] | AXI | I | Read Data Bus driven by AXI slave |
| 43 | m\_axi\_rresp[1:0] | AXI | I | his signal indicates the status of the read transfer. |
| 44 | m\_axi\_rvalid | AXI | I | This signal indicates that the required read data is available and the read transfer can be completed. |
| 45 | m\_axi\_rready | AXI | O | This signal indicates that the master can accept  the read data and response information. |

**Parameters Defined**

Below table defines the parameter defined in design their default values and range.

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No** | **Parameter Name** | **Allowable Values** | **Default Values** |
| 1 | Id\_width | Range (1-32) | 1 |
| 2 | addr\_width | Range (6-32) | 32 |
| 3 | data\_width | 32,64 | 32 |

**Notes:**

1. The same address and data width is used on both AHB and AXI interfaces.

2. The reference RTL don’t support burst transfers this is added in RTL by checking the ahb\_hburst and assigning appropriate values to m\_axi\_awburst, m\_axi\_arburst, m\_axi\_awlen, m\_axi\_arlen, m\_axi\_awvalid, m\_axi\_wvalid, m\_axi\_wlast, m\_axi\_arvalid.

**Clock**

The AHB2AXI IP uses s\_ahb\_aclk at both AHB and AXI interfaces.

**Data Width**

The IP supports the same data width on both AHB and AXI side. The data width selection (32 or 64) can be made using parameter “data\_width”.

No address/data translation/conversion from AHB to AXI takes place inside AHB2AXI4 Bridge. The write/read address from AHB is passed to AXI address. AHB write data is passed on to AXI and AXI read data is passed on to AHB read data.

**Transaction Type Mapping from AHB to AXI**

Different possible transaction types from AHB interface to AXI interface are mapped according to below table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AHB Transaction** | **BIT value** | **AXI Transaction** | | **Description** |
| **ahb\_burst** | **ahb\_burst[2:0]** | **m\_axi\_awburst/m\_axi\_arburst** | **m\_axi\_awlen/m\_axi\_arlen** |
| SINGLE | 0 | INCR | 0 | Single transfers on AHB are converted to INCR of length 0 |
| INCR | 1 | INCR | 0 | Indefinite length increment transfers on AHB are converted to INCR of length 0 |
| WRAP4 | 2 | WRAP | 3 | WRAP4 transfer on AHB is converted to WRAP transfer of length 3 on AXI side. |
| INCR4 | 3 | INCR | 3 | INCR4 transfer on AHB is converted to INCR transfer of length 3 on AXI side. |
| WRAP8 | 4 | WRAP | 7 | WRAP8 transfer on AHB is converted to WRAP transfer of length 7 on AXI side. |
| INCR8 | 5 | INCR | 7 | INCR8 transfer on AHB is converted to INCR transfer of length 7 on AXI side. |
| WRAP16 | 6 | WRAP | 15 | WRAP16 transfer on AHB is converted to WRAP transfer of length 15 on AXI side. |
| INCR16 | 7 | INCR | 15 | INCR16 transfer on AHB is converted to INCR transfer of length 15 on AXI side. |

ahb\_hprot (Protection) and ahb\_nonsec (Secure/nonsecure) mapping from AHB to AXI Interface is shown in below table:

|  |  |  |  |
| --- | --- | --- | --- |
| **AHB** | | **AXI** | |
| **Signal** | **value** | **Signal (AW and AR)** | **value** |
| ahb\_hprot[0] | 0 | Prot[2] | 1 |
| ahb\_hprot[0] | 1 | Prot[2] | 0 |
| ahb\_hprot[1] | 0 | Prot[0] | 0 |
| ahb\_hprot[1] | 1 | Prot[0] | 1 |
| ahb\_hnonsec | 0 | Prot[1] | 0 |
| ahb\_hnonsec | 1 | Prot[1] | 1 |