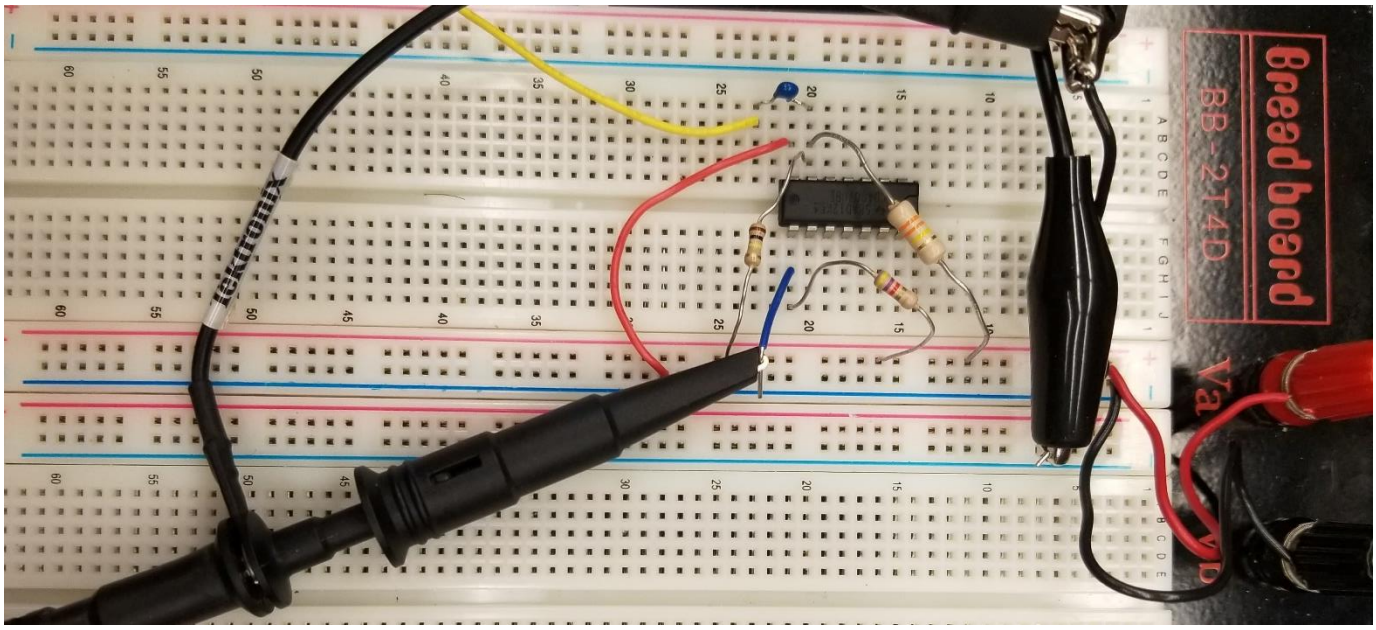
Lab 2 Report

Dr. Gregori

ENGG *3450 – Electrical Devices



Lab Group 42: Tuesday 3:30 Section:

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Special Thanks to the Teacher assistants in this course that helped us complete this experiment successfully during the lab. We would like to thank them for their patience and the time they invest into sharing their knowledge in Electronic Devices with the students at the University Of Guelph.

The following report outlines two experiments that made use of a CD4007 chip to better develop an understanding of characteristic transistor behaviours. The first experiment focused on the relationship between drain current and voltage in NMOS transistors while the second experiment was performed in the same manner with the NMOS switched out for a PMOS. Both experiments additionally sought to establish a trend in drain voltage and current for an increasing gate voltage. Functionality design of the CD4007 chip allowed it to be used as both the NMOS and PMOS transistor for the experiments, as it contains three transistors of each type. Connections to gain in the CD4007 chips were available at ports 3, 6 and 10, each providing voltage to one NMOS and one PMOS transistor however, for the following experiments NMOS and PMOS. transistors were exclusively tested and were never implemented simultaneously. For the common source amplifier circuits analysed in Experiment 2, the NMOS transistor showed for higher performance across all frequencies. As seen in the oscilloscope graphs, the circuit that implemented the NMOS transistor consistently produced an output waveform with a higher peak-peak voltage and therefore a superior gain. The NMOS and PMOS circuits were different in one small way. While both transistors require a resistance directly outside the drain voltage node, in the NMOS this voltage drop preceeds the drain node and follows the node in PMOS. Because the NMOS transistor flows from its drain node to the source, the DC supply must experience a voltage drop before drain current flows through the transistor. Comparatively, the PMOS transistor, which flows from source to drain, was followed by a resistor before being connected to ground, while the DC voltage was directly supplied to the transistor. This necessary difference in the circuit design as a result of opposite forward current direction could attribute to the difference in voltage output capacity and the tolerance to high frequencies observed by the NMOS common source amplifier circuit.

Experiment 1.1: NMOS I-V Characteristics

NMOS Experiment Values (Resistor: 1.784 KΩ):

V(GS)	V(D)	I(D)	V(DD)	V(DS)	I(D)	V(DD)	V(D)	I(D)
0.3712	11.99	0.0056	2.522	0.3687	1.207007	2.557	0.289	1.2713
0.6497	11.98	0.0112	3.024	0.452	1.441704	3.038	0.3591	1.501626
1.278	11.91	0.0504	4.093	0.646	1.932175	4.059	0.491	2.00000
1.586	11.86	0.0784	4.533	0.7342	2.129372	4.594	0.5632	2.259417
2.143	11.13	0.4876	5.589	0.9782	2.584529	5.565	0.7003	2.72685
2.44	10.54	0.8183	6.068	1.111	2.778587	6.02	0.768	2.943946
2.741	9.83	1.21633	6.528	1.26	2.952915	6.521	0.8447	3.181783
3.397	7.926	2.2836	7.592	1.766	3.265695	7.519	1.008	3.649664
3.707	6.888	2.8654	8.042	2.086	3.338565	8.022	1.095	3.882848
3.996	5.871	3.4355	8.592	2.543	3.390695	8.581	1.199	4.137892
4.29	4.783	4.0454	9.064	2.962	3.420404	9.11	1.304	4.375561
4.597	3.641	4.6855	9.565	3.423	3.442825	9.571	1.404	4.577915
4.868	2.707	5.2090	10.04	3.869	3.459081	10.09	1.517	4.805493
5.5	1.759	5.7404	11.06	4.84	3.486547	11.08	1.799	5.202354
5.791	1.601	5.8290	11.51	5.281	3.491592	11.61	1.982	5.396861
6.07	1.492	5.8901	12.05	5.788	3.51009	12.06	2.171	5.543161
Table 1 (V(DD) = 12V)			**Table 2 (V(DS) = 4V)**			**Table 3 (V(DS) = 5V)**		

NMOS Graph Analysis:

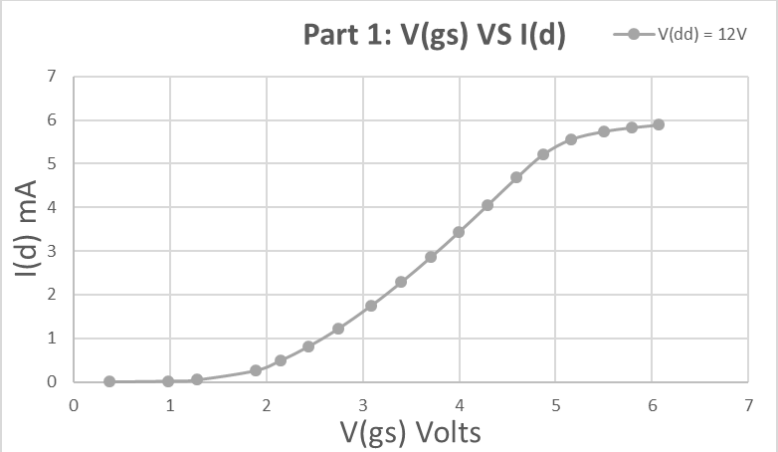

Figure 1: V(GS) Vs I(D)-NMOS

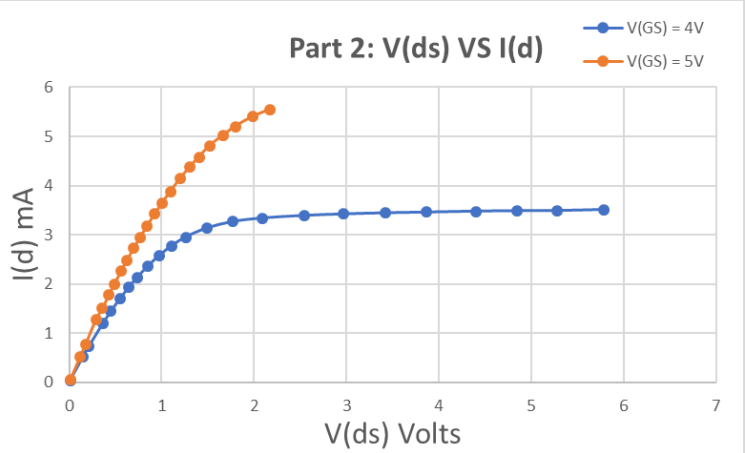

Figure 2: V(DS) Vs I(D)-NMOS

Experiment 1.2: PMOS I-V Characteristics

PMOS Experiment Values (Resistor: 1.774 KΩ):

V(GS)	V(D)	I(D)	V(DD)	V(DS)	I(D)	V(DD)	V(D)	I(D)
5.624	4.476	4.308906	1.408	0.316	0.615558	1.385	0.247	0.641488
5.312	5.101	3.956595	2.064	0.499	0.882187	2.116	0.405	0.964487
5.079	5.858	3.529876	2.795	0.708	1.176437	2.77	0.556	1.248027
4.797	6.581	3.122322	3.539	0.927	1.472379	3.47	0.712	1.554679
4.457	7.501	2.60372	4.014	1.105	1.639797	4.179	0.877	1.86133
4.133	8.18	2.22097	4.668	1.383	1.851747	5.007	1.095	2.205186
3.812	9.022	1.746336	5.391	1.728	2.064825	5.679	1.298	2.46956
3.524	9.658	1.387824	6.115	2.06	2.285795	6.419	1.486	2.780722
3.111	10.48	0.924464	6.81	2.529	2.413191	7.138	1.684	3.074408
2.819	10.99	0.636979	7.518	3.02	2.535513	7.814	1.964	3.297632
2.587	11.387	0.413191	8.235	3.572	2.628523	8.47	2.189	3.540586
2.14	11.8043	0.177959	8.891	4.094	2.704059	9.204	2.512	3.772266
1.775	11.992	0.072153	9.576	4.631	2.787486	9.868	2.801	3.983653
1.229	11.994	0.071026	10.257	5.139	2.885006	10.589	3.095	4.224352
1.002	11.994	0.071026	10.987	5.779	2.935738	11.299	3.569	4.357384
0.5001	11.994	0.071026	11.957	6.639	2.997745	12.029	3.949	4.554679
Table 4 (V(DD) = 12.12V)			**Table 5 (V(DS) = 4V)**			**Table 6 (V(DS) = 5V)**		

PMOS Graph Analysis:

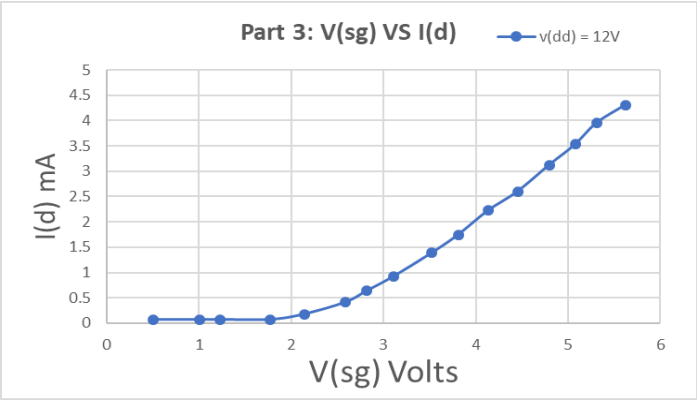

Figure 3: V(GS) Vs I(D)-PMOS

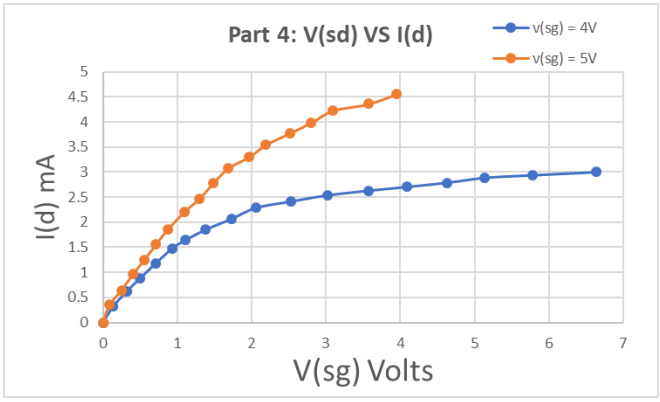

Figure 4: V(DS) Vs I(D)-PMOS

Experiment 2: Common Source Amplifier

The second experiment analyzed a common-source amplifier circuit. Resistors were found to be 4.78, 325.4 and 99.2 kΩ for theoretical values of 4.7, 330 and 100 kΩ respectively. After the circuit was constructed, the DC voltage supply was set to 10 V. Channel one of the oscilloscopes was connected to the sinusoidal voltage source VI and the function generator to produce a waveform with 300 mV peak-peak voltage, while channel two was connected to the drain voltage node of the transistor. Voltage waveforms were recorded at frequencies of 2.5, 25, 250 and 2500 kHz. The experiment was executed using the NMOS and PMOS transistors, exclusively.

N-MOS Oscilloscope Result Analysis:

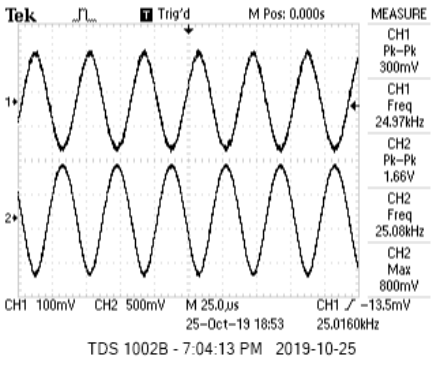

Figure 5: 25KHz N-MOS Result

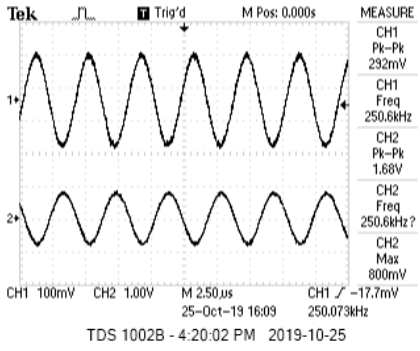

Figure 6: 250KHz N-MOS Result

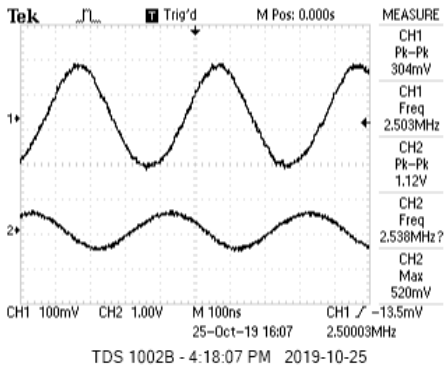

Figure 7: 2.5MHz N-MOS Result

The resistance of the capacitance lowers as frequency increases causing the shift seen in figure 7. This reduces the Gain supplied by the transistor. When analyzing the 25Khz and 250Khz results we can see that the peak to peak is almost constant until a large frequency is introduced into the system

P-MOS oscilloscope Result Analysis:

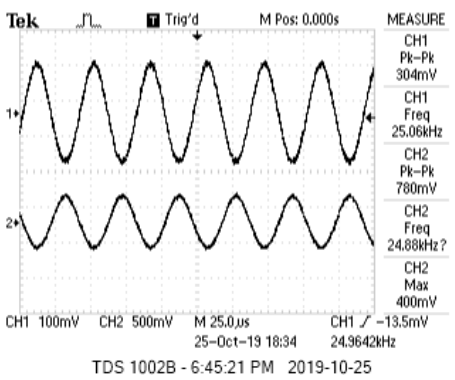

Figure 8: 25KHz P-MOS Result

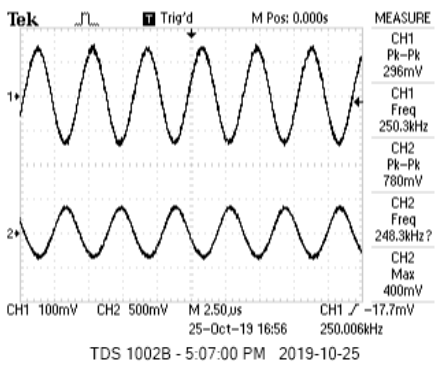

Figure 9: 250KHz P-MOS Result

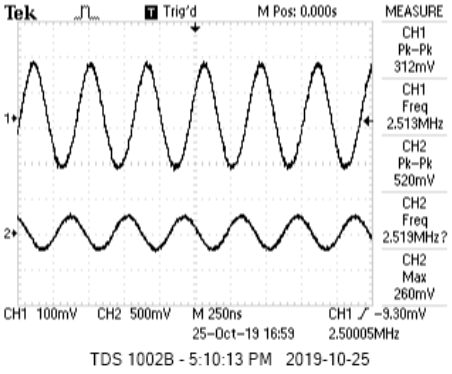

Figure 10: 2.5MHz P-MOS Result

N-MOS Vs P-MOS Result Summary:

Transistor	Frequency	Channel 1 PK-PK (mv)	Channel 2 PK-PK (mV)	Voltage Gain (Av)	Gm Value	Kn value	Vtn Value
NMOS	25 KHz	304 mV	1.66 V	5.461	-1.14	0.325059	0.05
	250 KHz	292 mV	1.68 V	5.53	-1.15	0.325059	0.05
	2.5 KHz	304 mV	1.12 V	3.6842105	-0.7705	0.325059	0.05
PMOS	25 KHz	304 mV	780 mV	2.5657894	-0.5366	0.325059	0.05
	250 KHz	296 mV	780 mV	2.6351351	-0.5511	0.325059	0.05
	2.5 KHz	312 mV	520 mV	1.6666667	-0.3486	0.325059	0.05

Table 7: Experiment 2 results summary

As voltage gain decreases, the Gm value decreases.

Result Interpretation

$$i_D = \frac{k_n}{2}(v_{GS} - V_{tn})^2.$$

Equation 1: Finding Kn

$$R_{on} = \frac{1}{k_n(v_{GS} - V_{tn})}.$$

Equation 2: Finding Ron

$$A_v = \frac{v_o}{v_i} = -g_m R.$$

Equation 3: Finding gain

sample Calculations:

Using formula 1, Kn was calculated to be 0.1863 in saturation mode, where Vtn = 0.05 as extracted from experiment's 1 NMOS graph, a Vgs of 6.05 was used to ensure that NMOS was in saturation mode, and an Id value of 3.354002 which was obtained from Experiment 1. The transistor resistance was calculated using the formula 2 resulting in a value of 28.65. To calculate the gain, formula 3 was used. In saturation mode, Vout was 1.492V and Vin was 6.07 resulting in a gain value of 0.25. The MOSFET's transconductance was calculated to be -0.1378. These sample calculations were used for experiment 1 and 2 to calculate the Gm, Kn, voltage gain, and the Vtn values.