Lab 5: Xilinx System Generator Designing a DSP Block

ENGG3050: Reconfigurable Computing Systems

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Group 42: Tuesday-3:30 Section

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1 Project Implementation

1.1 Problem Statement

The main objective of lab 5 was to compare different implementations of two math functions using the Xilinx System Generator software.

1.2 Assumptions and Constraints

Constraints includes using an FPGA board, the Xilinx System Generator, and MATLAB to integrate functions into the system generator.

1.3 System Overview Justification Of Design

1.3.1 Designed System Overview

The system created integrated two functions using system generator. (Were they displayed anywhere Bilal??) The two functions created were:

$$out = (4 * x) + (3.2 * y) - (2.1 * z)$$

$$f(x) = \begin{cases} x^3 + 0.5x & |x| \leq 1 \\ 2x - 0.5sgn(x) & |x| \geq 1 \end{cases}$$

1.3.2 System Functionality and Reasons Behind Design

The system was made using the block diagrams in system generator and MATLAB. The first function was made using 3 multipliers, 2 adders, and 1 subtractor to perform the operations on the constants and the variables.

The second function was implemented using a block called thresh hold for the sgn function and a multiplexer to select the right output for the value of x used. It also used multipliers, adders, and subtractors to obtain the correct output.

These designs were chosen due to their simplicity and efficiency. More complicated designs were not needed due to the simplicity of the functions being integrated.

2 Circuit Diagram

The schematic shown uses different functionalities of the system generator to implement the given functions. These include adders, multipliers, subtractors, multiplexers, and MATLAB code integrated into a block. There were 2 special blocks used; threshold for the sgn function and the absolute value block.

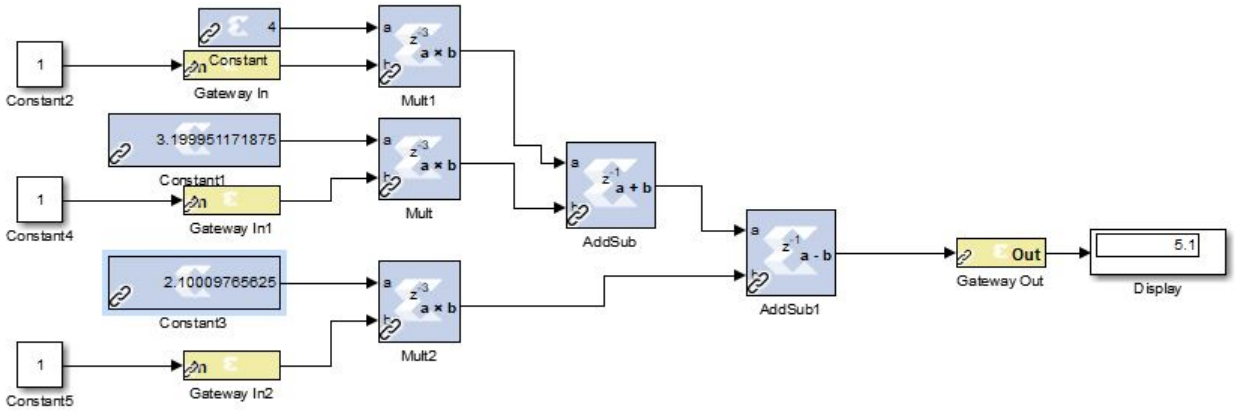

Figure 1: Equation 1 Diagram

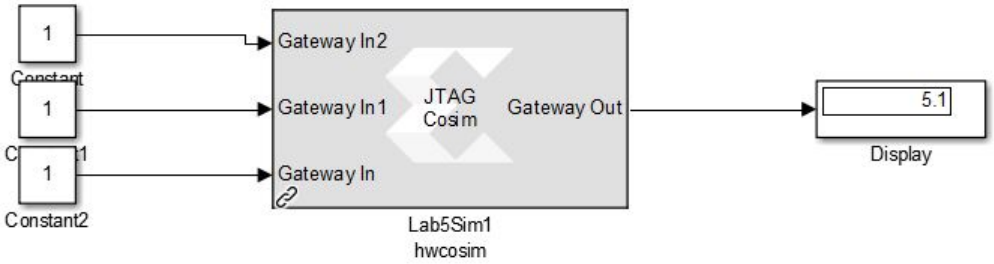

Figure 2: Equation 1 Simulation

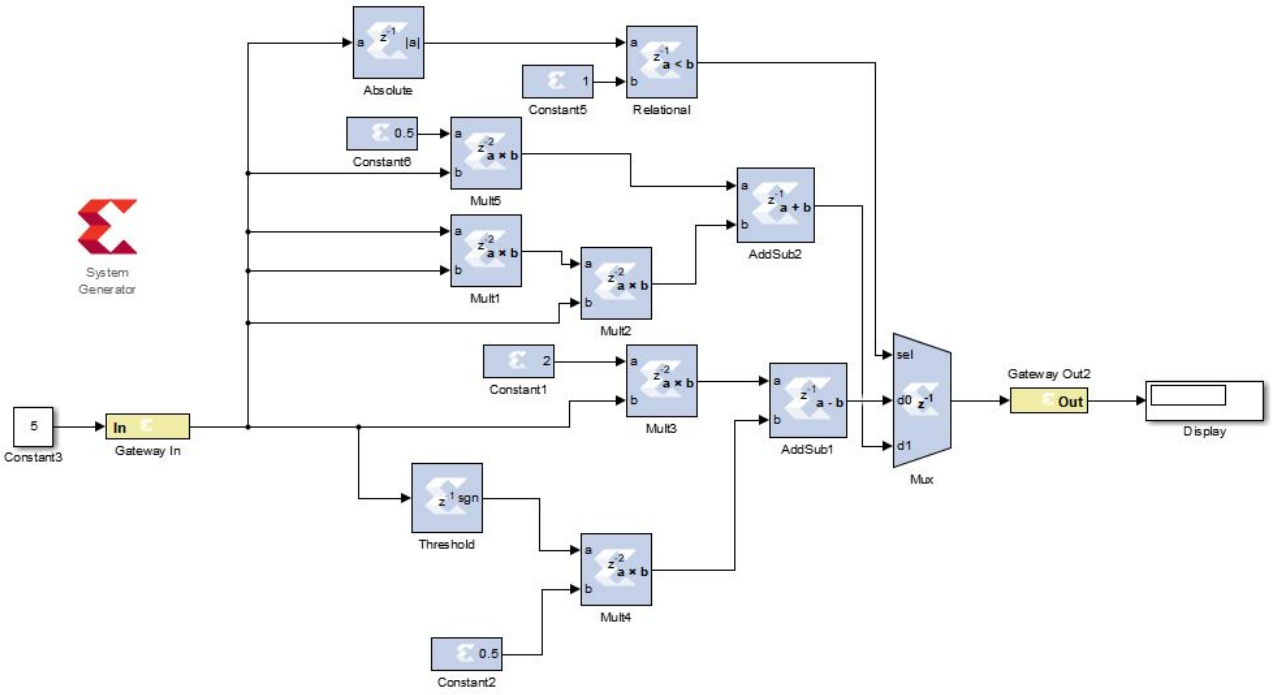

Figure 3: Equation 2 Diagram

Figure 4: Equation 2 Simulation

3 Error Analysis

There were no errors encountered in the synthesis of this lab. The outputs received were the expected outputs, therefore there were no errors in them either.

4 Resources used

The resources used are shown in the diagrams below. The piecewise function used more resources than the other equation. This was expected due it being more complex than the other equation.

Name	Slice LUTs (63400)	Slice Registers (126800)	DSPs (240)	Bonded IOB (210)	BUFGCTRL (32)
eq1	68	99	2	83	1

Figure 5: Equation 1 Resources

Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	LUT as Memory (19000)	LUT Flip Flop Pairs (63400)	DSPs (240)	Bonded IOB (210)	BUFGCTRL (32)
eq2	98	175	50	97	1	71	3	66	1

Figure 6: Equation 2 Resources