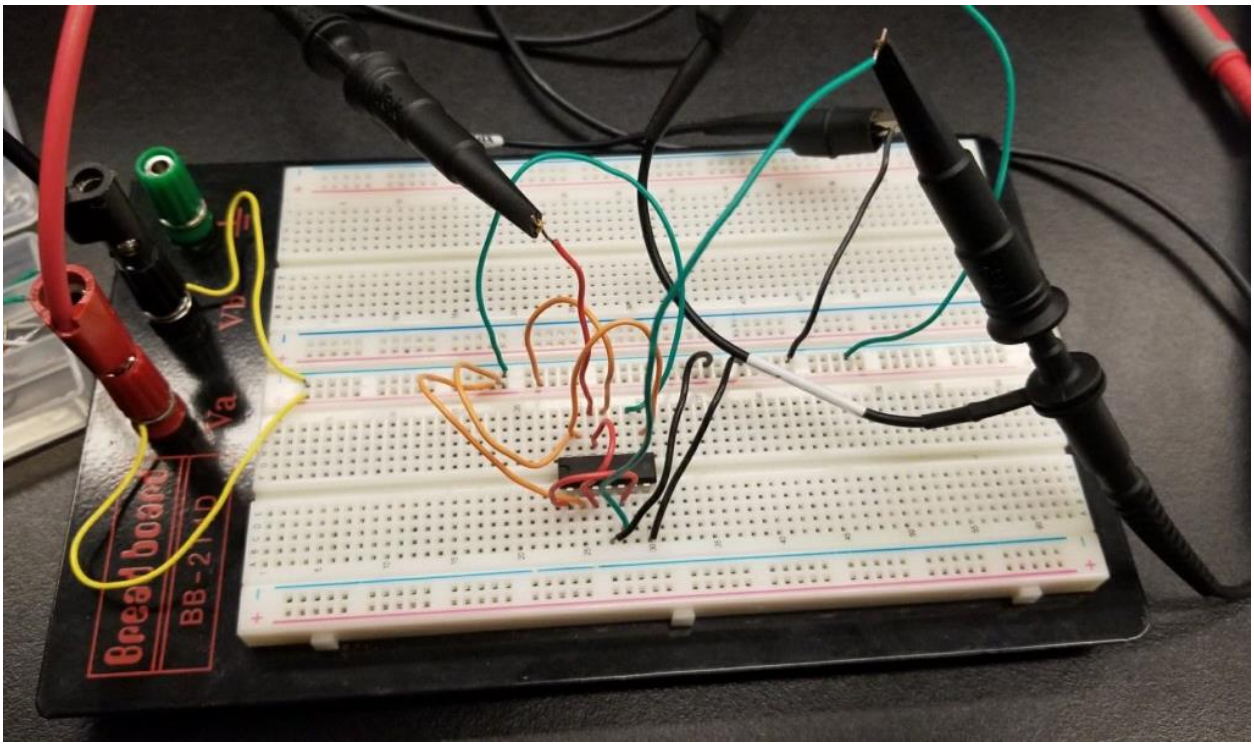
Lab 3 Report

Dr.Gregori ENGG *3450 – Electrical Devices



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Special Thanks to the Teacher assistants in this course that helped us complete this experiment successfully during the lab. We would like to thank them for their patience and the time they invest into sharing their knowledge in Electronic Devices with the students at the University Of Guelph.

Experiment 1 – CMOS Inverter VTC and Propagation Delay

1.1- CMOS Inverter VTC

The first part of this experiment aimed to characterize the CMOS inverter by means of its voltage transfer characteristic (VTC). The VTC is represented by the function relating Vi to Vo over the inverter. This graph details the three regions of operation which includes the voltage range that will produce a low output signal (logic 0), a high output signal (logic 1) and the transition region. The CMOS inverter using the CD4007 chip and schematic displayed in figure 1.1.2. A DC voltage of 5 V was supplied to the circuit at the PMOS terminal of the CMOS inverter while the NMOS terminal was set to ground. Output voltage recordings were made for gate voltage values between 0 and 5 V. Figure 1.1.1 (seen below) shows the VTC function produced from the dataset.

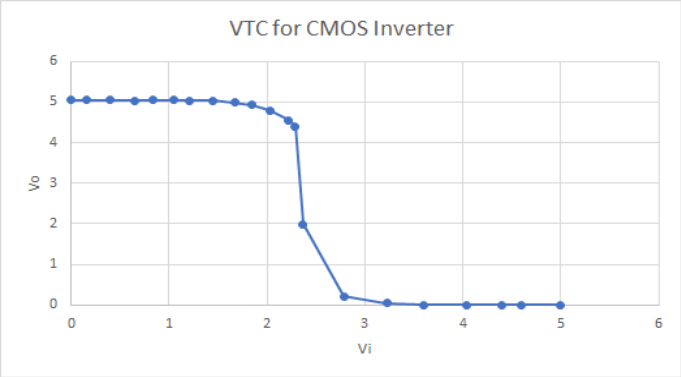

Figure 1.1.1 VTC graph for a CMOS inverter

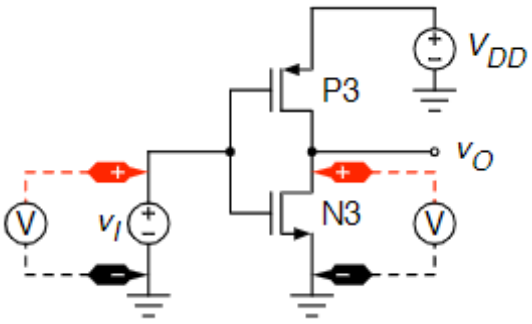

Figure 1.1.2 VTC circuit schematic

Graphical analysis of the VTC function determined a switching threshold (point where Vi = Vo) of 2.35 V from interpolation of Vi values 2.29 and 2.36 V.

VoL	VoH	ViL	ViH	NML	NMH
0.5	4.5	0.5	0.5	0	4

Table 1.1.1 Theoretical values for noise margins.

VoL	VoH	ViL	ViH	NML	NMH
0.5	4.85	1.94	2.72	1.44	2.13

Table 1.1.2 Experimental values for noise margins.

Table 1.1.1 presents the voltages characterizing the theoretical regions of operation for the CP4007 chip, from the component's datasheet. Theoretical values argue a transition region $0.5 \leq Vo \leq 4.5$ V. Comparatively, Table 1.1.2 established an experimentally proven transition region $0.5 \leq Vo \leq 4.85$ V.

1.2 Propagation Delay

The second part of this experiment proceeded to characterize the CMOS inverter, but this time, with respect to propagation delay. Propagation delay represents the average time it takes for the input voltage signal to pass through the inverter and like VTC, it is an intrinsic property of individual electronic components. The circuit constructed for the previous experiment was

used once again, the only difference being the gate voltage connection, which connected the function generator to the oscilloscope with the oscilloscope channel set to DC coupling.

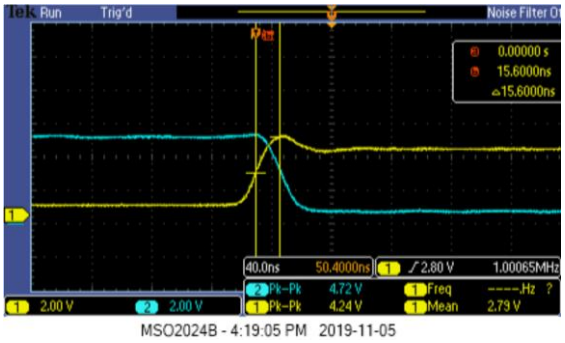

Figure 1.2.1 Propagation delay from high to low signal output (in blue).

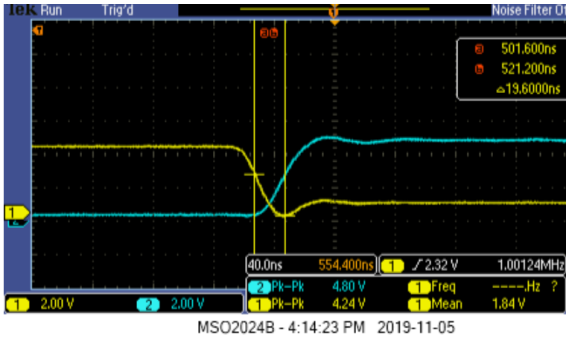

Figure 1.2.2 Propagation delay from low to high signal output (in blue).

Figure 1.2.1 (seen above to the left) displays the propagation delay for a falling-edge voltage output over the CMOS inverter, which was observed to be 15.6 ns. Similarly, Figure 1.2.2 (seen above to the right) displays the propagation delay for a rising-edge voltage output over the CMOS inverter, which was observed to be 19.6 ns.

Experiment 2 – Ring Oscillator

The second experiment sought to develop an understanding of the basic operations performed by a ring oscillator and the effect of frequency on the circuit's performance. Ring oscillator circuits are used to achieve a near-ideal, periodic waveform by connecting an odd number of inverters to form a loop to produce zero-time rise/fall edges. This experiment specifically made use of three inverters however, applications conventionally make use of at least five. The inverters function as delay stages as the signal propagates through them individually, only to return inverted (high to low or low to high) after a known period, before being inverted again, completing a full signal oscillation. The CD4007 chip provided the transistors needed to build the circuit. Three CMOS transistors were established and connected in a cascading manner to form a loop. This loop was supplied by a DC voltage of 5 V.

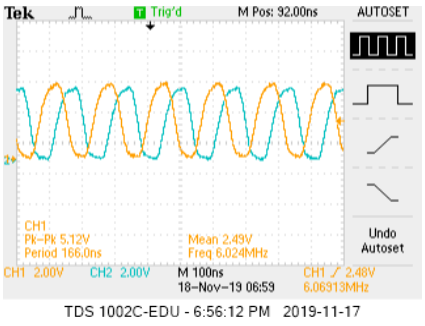

Figure 2.1 V2 in blue and Vo in yellow.

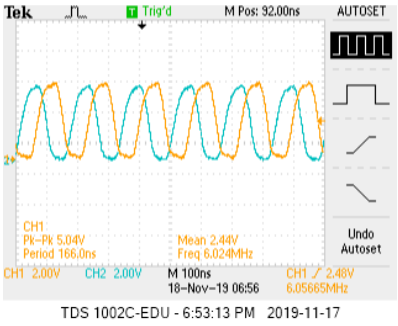

Figure 2.2 V1 in blue and Vo in yellow.

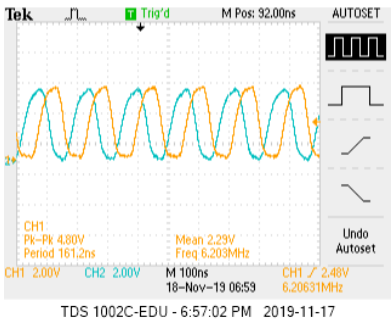

Figure 2.3 V2 in blue and V1 in yellow.

From Figures 2.1 through 2.3, frequencies were consistently observed to be around 6 MHz for peak-peak voltages of approximately 5 V (for all voltage signals). Point voltages V2

and V1 following the first and second inverters in the series, correspondingly, such that V2 was an inversion of the output signal and V1 was an inversion of the DC signal.

Experiment 3 – Logic Gates

3.1 NAND Gate

The first part of this experiment shared the same focus as that of experiment 1.1, substituting the CMOS inverter with a NAND gate. A NAND gate is a logical operator that produces a logic ‘0’ when all inputs are logic ‘1’ and produces a logic ‘0’ otherwise. A similar circuit to that used in experiment 1.1 was constructed using the CD4011 chip in place of the CD4007 chip, which provided NAND gates with connections A, B and J instead of gate, drain and supply seen by the transistors previously used. A DC supply of 5 V was assigned to signal B and the remaining channel was connected to signal A.

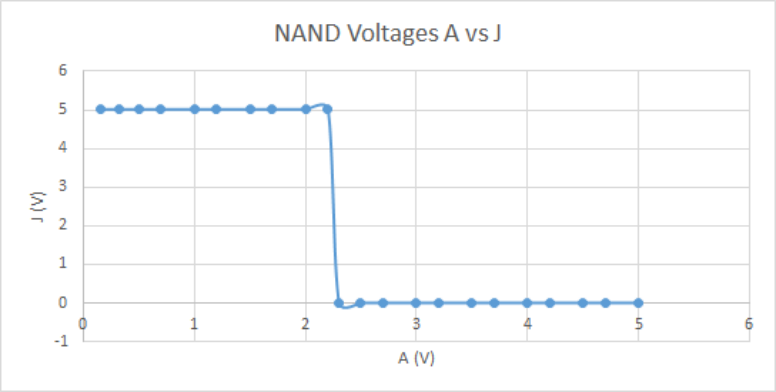

Figure 3.1.1 - Voltage at J against voltage at A for a NAND gate with voltage at B set to 5 V.

Figure 3.1.1 displays a high output voltage (signal J) for a low input voltage (signal A) and vice versa. This agrees with the logical conditions associated with the NAND gate since signal B was connected to the 5 V DC voltage supply, thus assigning it a logic ‘1’; only when A is given a sufficiently high voltage signal that constitutes a logic ‘1’ as well will the produced output voltage signal J be logic ‘0’. Additional cases for input signal combinations were assessed in experiment 3.1 to further describe output signal J. The experiment was repeated for input signal B equal to 0 V, reverse DC connections between inputs A and B and tied inputs, which all produced J outputs in agreement with the logical conditions for a NAND gate.

3.2 NAND, NOR & NOT Gates

The second part of this experiment set out to establish quantifiable ranges for high and low logic. To achieve this, the experiment made use of red and green LED lights, connected to the circuit in a way that would indicate a logic ‘0’ when the red light was on and logic ‘1’ when the green light was on. The experiment was performed twice, using the CD4011 chip to test a NAND circuit and again using the CD4001 chip to test a NOR circuit. Opposite to the NAND gate, a NOR gate is a logical operator than produces a logic ‘1’ when all inputs are logic ‘0’ and otherwise produces a logic ‘0’. A DC voltage equivalent to a high logic signal was supplied to the circuit and diodes were connected in series with 1 kΩ resistors.

NAND		
A	B	J
0	0	1
0	1	1
1	0	1
1	1	0

Table 3.2.1 NAND truth table.

NOR		
A	B	J
0	0	1
0	1	0
1	0	0
1	1	0

Table 3.2.2 NOR truth table.

NOR from AND

AND			NOR		
A	B	J	A	B	J
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	1	1	0

Table 3.2.3 Verification Of Results

As seen in experiment 3.1, Table 3.2.1 affirms the conditional logic for a NAND gate, such that a low output voltage signal (logic '0') is produced exclusively for the case where all inputs are high (logic '1') while Table 3.2.2 asserts the conditional logic for a NOR gate, such that a high output voltage signal is exclusively produced for the case that all inputs are low.

For experiment 1.1, the key difference between theoretical and experimental transition regions, lies in the continuity of the VTC function. The range ViL ≤ Vi ≤ ViH is considered the undefined region since noise is produced instead of an output signal. Values obtained from the datasheet produced a theoretical undefined region equivalent to a single point, such that ViL = ViH = 0.5 V. More realistically, experimental values produced an undefined region 1.94 ≤ Vi ≤ 2.72 V. The higher and lower voltage ranges that are exclusive to the transition region (not a part of the undefined region) are defined as the noise margins. Larger noise margins are desirable because their size is proportional to the components noise immunity. For experiment 1.2, average propagation delay was calculated to be 17.6 ns. This contradicts values for t_{PHL} and t_{PLH} found in the CD4007 chip datasheet, which gave 30 and 25 ns respectively. Not only were experimental values given significantly lower than the theoretical values, they weren't even scalable since $t_{PHL} < t_{PLH}$ for experimental values and $t_{PHL} > t_{PLH}$ for those found in the datasheet, leading to the belief that values were compromised by experimental error. Based on the comparison between propagation delay observed in experiment 1.2 and experiment 2, the influence of frequency on propagation delay was observed to be a proportional relationship such that in experiment 1.2 a frequency of 1 MHz resulted in a propagation delay of approximately 17.6 ns, whereas the frequency of 6 MHz used in experiment 2 corresponded to a frequency delay of approximately 100 ns between point voltage V1 and output voltage Vo. This is conceptually sound since frequency is an inverse measurement of time and delay is a time measurement; increasing frequency will increase propagation delay likely because the signal is being processed at a great rate.

Experiment 3 established the formative knowledge between digital and mathematical interpretation of logic operators, justifying the complement functions such that AND exclusively produces a high output signal for exclusively high inputs and OR produces an exclusively low signal for exclusively low input signals (the inverse was observed for NAND and NOR). Furthermore, NAND is a universal gate, meaning any other operator is a function of NAND, for example the NOT operation can be replicated using NAND by passing the input as two identical signals. NOR is represented by passing NAND inverted inputs through another NAND gate and finally a secondary NAND inverter. See figure 3.2.3 for experimental validation of logic (note that a NOT gate inverts a 0 to a 1 and a 1 to a 0 as extracted from experiment- Table of NOT Gate was not included to meet the 5 page limit).