

# Présentation du bureau d'étude Pilote d'une barre franche

Présenté par :

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- BERKI Amira

Encadré par :

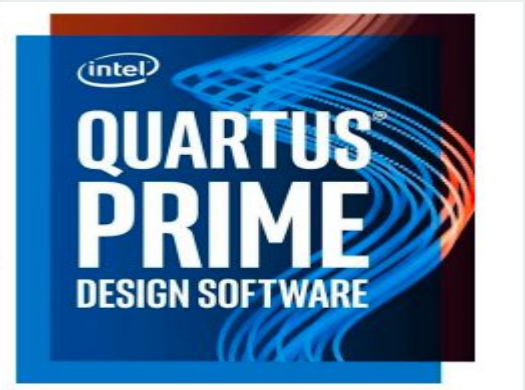
- PERISSE Thierry

# Plan

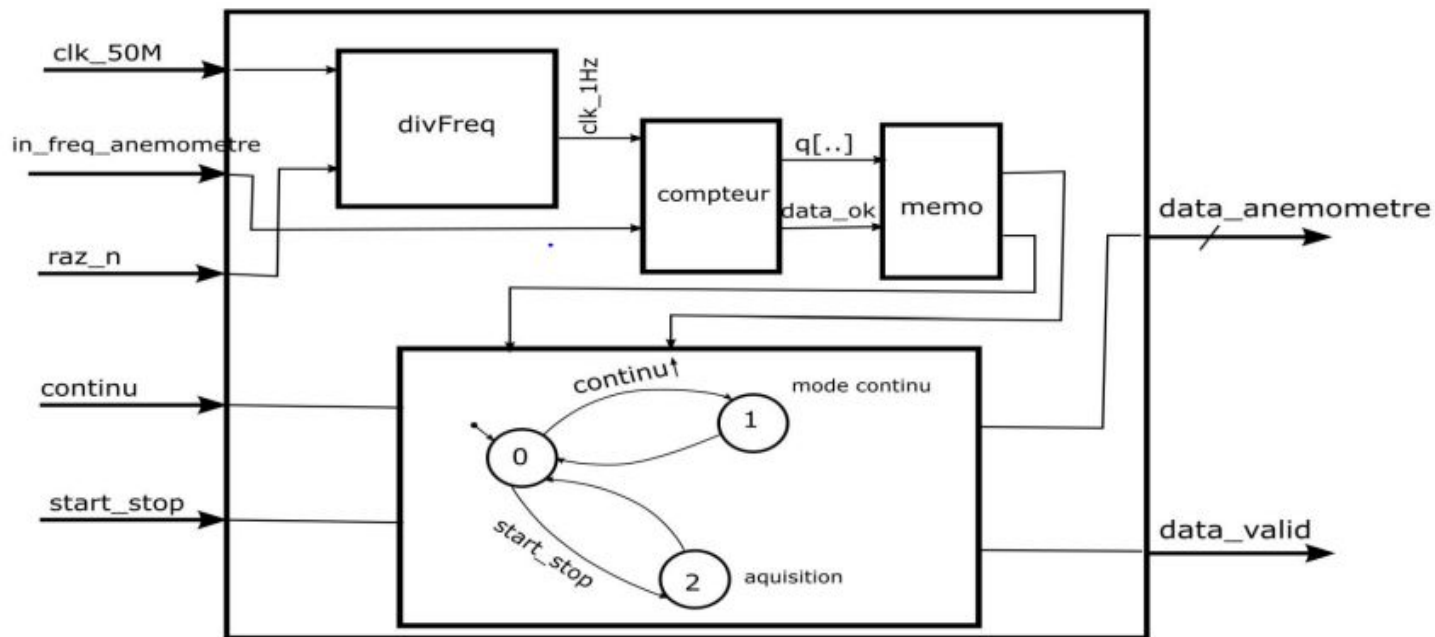


- Introduction
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- Conception du SOPC
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# Introduction



# Démarche de la conception de la fonction gestion anémomètre

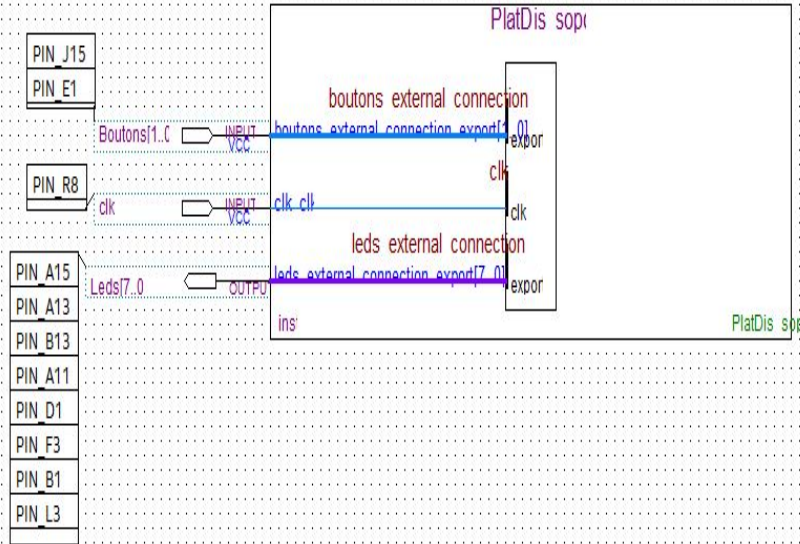


# Conception du SOPC



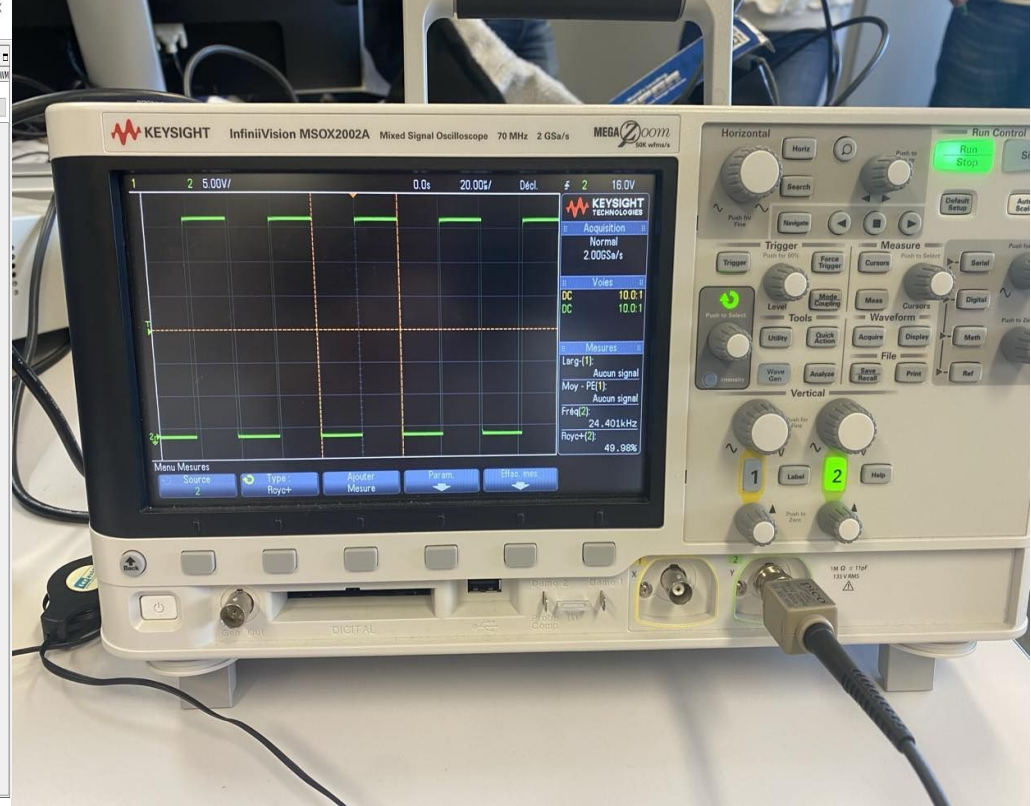
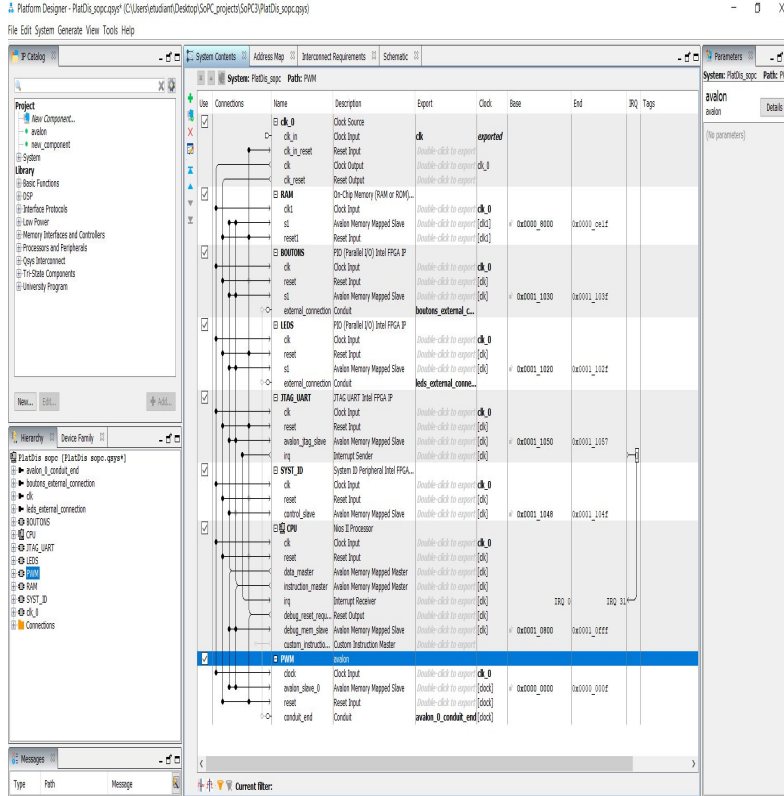
- Définition d'un SOPC
- Différents composant d'un SOPC
- But de la conception du SOPC

# Vérification du bon fonctionnement de notre SOPC



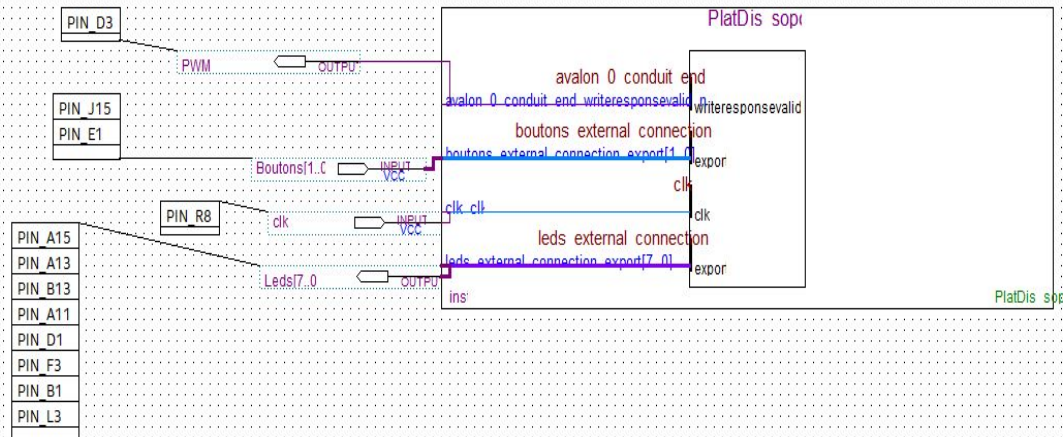
Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags
✓		<b>clk_0</b>	Clock Source						
		clk_in	Clock Input	clk	exported				
		clk_in_reset	Reset Input						
		clk	Clock Output						
		clk_reset	Reset Output						
✓		<b>RAM</b>	On-Chip Memory (RAM or ROM)...						
		clk1	Clock Input						
		s1	Avalon Memory Mapped Slave						
		reset1	Reset Input						
✓		<b>BOUTONS</b>	PIO (Parallel I/O) Intel FPGA IP						
		clk	Clock Input						
		reset	Reset Input						
		s1	Avalon Memory Mapped Slave						
		external_connection	Conduit	boutons_external_c...					
✓		<b>LEDS</b>	PIO (Parallel I/O) Intel FPGA IP						
		clk	Clock Input						
		reset	Reset Input						
		s1	Avalon Memory Mapped Slave						
		external_connection	Conduit	leds_external_conne...					
✓		<b>JTAG_UART</b>	JTAG UART Intel FPGA IP						
		clk	Clock Input						
		reset	Reset Input						
		avalon_jtag_slave	Avalon Memory Mapped Slave						
		irq	Interrupt Sender						
✓		<b>SYST_ID</b>	System ID Peripheral Intel FPGA...						
		clk	Clock Input						
		reset	Reset Input						
		control_slave	Avalon Memory Mapped Slave						
✓		<b>CPU</b>	Nios II Processor						
		clk	Clock Input						
		reset	Reset Input						
		data_master	Avalon Memory Mapped Master						
		instruction_master	Avalon Memory Mapped Master						
		irq	Interrupt Receiver						
		debug_reset_requ...	Reset Output						
		debug_mem_slave	Avalon Memory Mapped Slave						
		custom_instructio...	Custom Instruction Master						

## Intégration de la fonction PWM dans notre SOPC





# Intégration de la fonction PWM dans notre SOPC



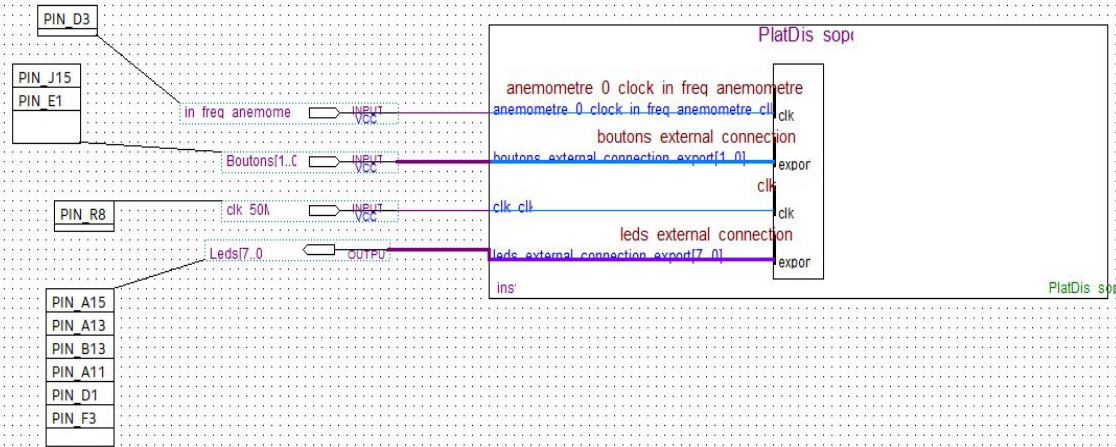


# Intégration de la fonction PWM dans notre SOPC



Quel est le but exact de  
l'intégration de la fonction PWM  
dans notre SOPC ?

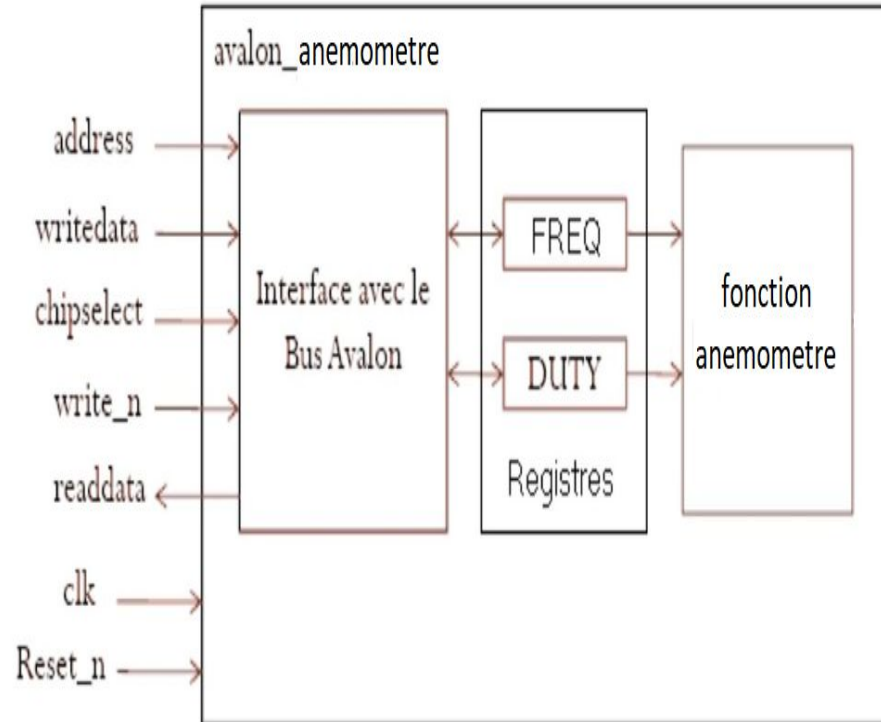
# Intégration de la fonction gestion anémomètre dans le SOPC



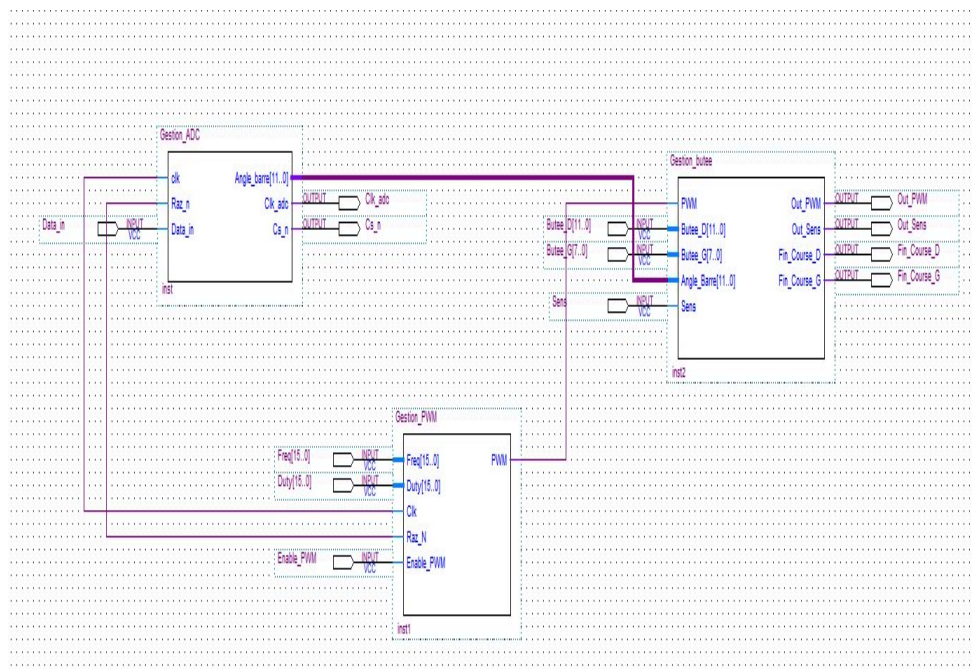
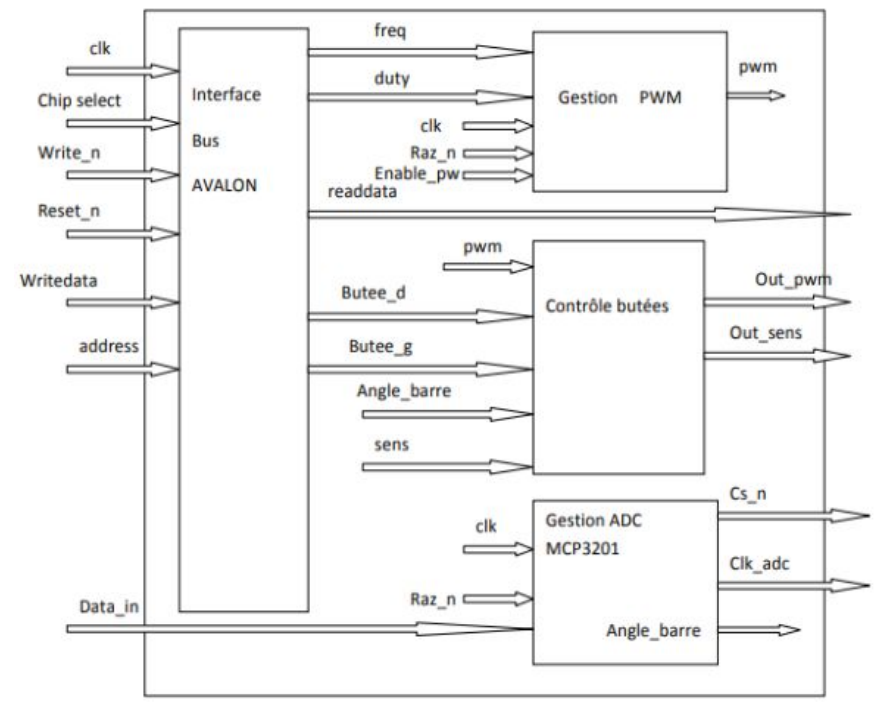
System Contents	Address Map	Interconnect Requirements	Schematic				
<b>System:</b> FlatDis_socp <b>Path:</b> clk_0							
Use	Connections	Name	Description	Export	Clock	Base	End
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>clk_0</b> clk_in clk_in_reset clk clk_reset	<b>Clock Source</b> Clock Input Reset Input Clock Output Reset Output	<b>clk</b> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>exported</b>		
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>RAM</b> clk1 s1 reset1	On-Chip Memory (RAM or ROM)... Clock Input Avalon Memory Mapped Slave Reset Input	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk1]	# 0x0000_8000	0x0000
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>BOUTONS</b> clk reset s1 external_connection	PIO (Parallel I/O) Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave Conduit	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk]	# 0x0001_1030	0x0000
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>LEDs</b> clk reset s1 external_connection	PIO (Parallel I/O) Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave Conduit	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk]	# 0x0001_1020	0x0000
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>JTAG_UART</b> clk reset avalon_jtag_slave irq	JTAG UART Intel FPGA IP Clock Input Reset Input Avalon Memory Mapped Slave Interrupt Sender	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk]	# 0x0001_1050	0x0000
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>SYST_ID</b> clk reset control_slave	System ID Peripheral Intel FPGA... Clock Input Reset Input Avalon Memory Mapped Slave	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk]	# 0x0001_1048	0x0000
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>CPU</b> clk reset data_master instruction_master irq debug_reset_req... debug_mem_slave custom_instructio...	Nios II Processor Clock Input Reset Input Avalon Memory Mapped Master Avalon Memory Mapped Master Interrupt Receiver Reset Output Avalon Memory Mapped Slave Custom Instruction Master	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>clk_0</b> [clk] [clk] [clk] [clk]		IRQ 0
<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/> <b>anemometre_0</b> reset avalon_anemometre clock_in_freq_ane... clock_1	Reset Input Avalon Memory Mapped Slave Clock Input Clock Input	<i>Double-click to export</i> <i>Double-click to export</i> <i>Double-click to export</i>	<b>anemometre_0_cloc...</b> <b>exported</b> <b>clk_0</b>	# 0x0000_0000	0x0000

ETHIOPIAN PROS 11.1 FOR CRYSTAL CONTAINER GROUP: 100000, 1000000, 10000000, 100000000

```
-----  
Freq d'entr e :  
InFreq = 250 Hz  
-----  
vitesse de sortie :  
data Vitesse mesur e = 250 Km/h  
-----  
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InFreq = 250 Hz  
-----  
vitesse de sortie :  
data Vitesse mesur e = 250 Km/h  
-----  
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InFreq = 250 Hz  
-----  
vitesse de sortie :  
data Vitesse mesur e = 250 Km/h  
-----  
Freq d'entr e :  
InFreq = 250 Hz  
-----  
vitesse de sortie :  
data Vitesse mesur e = 250 Km/h  
-----
```



# Démarche de la conception de la fonction gestion vérin



# Intégration de la fonction vérin dans le SOPC

Use	Connections	Name	Description	Export
<input checked="" type="checkbox"/>		<input type="checkbox"/> <b>clk_0</b>	Clock Source	<b>clk</b>
		clk_in	Clock Input	<b>reset</b>
		clk_in_reset	Reset Input	<i>Double-click to export</i>
		clk	Clock Output	<i>Double-click to export</i>
		clk_reset	Reset Output	
<input checked="" type="checkbox"/>		<input type="checkbox"/> <b>onchip_memory2_0</b>	On-Chip Memory (RAM or ROM) Intel ...	
		dk1	Clock Input	<i>Double-click to export</i>
		s1	Avalon Memory Mapped Slave	<i>Double-click to export</i>
		reset1	Reset Input	<i>Double-click to export</i>
<input checked="" type="checkbox"/>		<input type="checkbox"/> <b>nios2_gen2_0</b>	Nios II Processor	
		clk	Clock Input	<i>Double-click to export</i>
		reset	Reset Input	<i>Double-click to export</i>
		data_master	Avalon Memory Mapped Master	<i>Double-click to export</i>
		instruction_master	Avalon Memory Mapped Master	<i>Double-click to export</i>
		irq	Interrupt Receiver	<i>Double-click to export</i>
		debug_reset_request	Reset Output	<i>Double-click to export</i>
		debug_mem_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>
		custom_instruction_m...	Custom Instruction Master	<i>Double-click to export</i>
<input checked="" type="checkbox"/>		<input type="checkbox"/> <b>jtag_uart_0</b>	JTAG UART Intel FPGA IP	
		clk	Clock Input	<i>Double-click to export</i>
		reset	Reset Input	<i>Double-click to export</i>
		avalon_jtag_slave	Avalon Memory Mapped Slave	<i>Double-click to export</i>
		irq	Interrupt Sender	<i>Double-click to export</i>
<input checked="" type="checkbox"/>		<input type="checkbox"/> <b>avalon_verin</b>	new_component	
		clock	Clock Input	<i>Double-click to export</i>
		reset	Reset Input	<i>Double-click to export</i>
		avalon_slave_0	Avalon Memory Mapped Slave	<i>Double-click to export</i>
		conduit_end	Conduit	<b>new_component_0_con...</b>

# Conclusion



Bilans :

- Compréhension de la conception avec du VHDL
- Prise en main Platform Designer pour la conception d'un SOPC
- Une expérience assez complète sur la conception d'un système électronique numérique





# Merci pour votre attention