Inputs, Outputs & States of the FSM

Inputs	Description	Meaning of ‘1’
PS	Password setup button	Button pressed
AR	Arm mode button	Button pressed
DO	Door open mode button	Button pressed
CP	Confirm password button	Button pressed
PV	Password valid flag	Given password is valid
PM	Password match flag	Input matches password
TU	Time is up flag	Time is up (30 s)
CLK_1HZ	1 Hz clock	Input is high
RESET	Reset	Input is high
BCD_input	Password input as 12-bit BCD	

Outputs	Description	Meaning of ‘1’
SL	Status LED	LED open
DL	Door open LED	LED open
PL1	Attempt LED 1	LED open
PL2	Attempt LED 2	LED open
PL3	AttemptLED 3	LED open
ALM	Alarm	ALM is activated
PASS	12-bit BCD password	

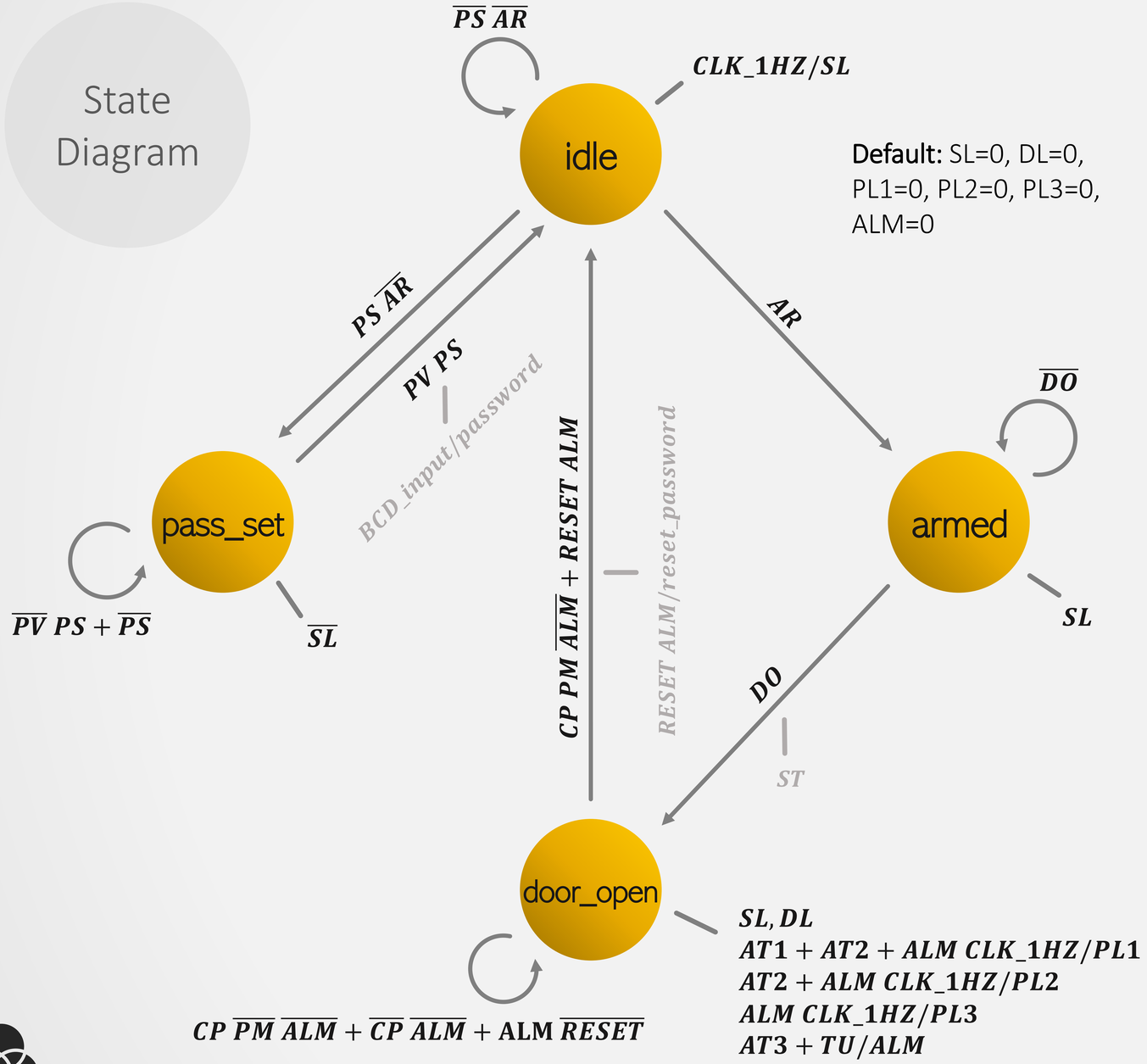
States	Description
idle	Idle mode
pass_set	Password setup mode
armed	Arm mode
door_open	Door open mode

IMPORTANT NOTES

For the demonstration purposes, blinking of LEDs represented by X. The actual code was SL <= clk_1hz

The global clock and 1 Hz clock are equal to each other for simulation purposes.

State Diagram



NOTES

Even if the given password is greater than 999, system accepts it as an attempt in the door open mode.

AT1, AT2, AT3, reset_password and ST are hypothetical signals. When the alarm goes off and RESET button is pressed, password is set to its default value which is all zero and the system goes to idle mode. The hypothetical reset_password signal expresses this. ST shows timer starts counting.

The actual system has **attempt** signal which is an integer that can have values between 0 and 3. AT1, AT2 and AT3 are hypothetical signals representing these four states of the attempt signal. This is found more convenient to express output equation in the state diagram.

	AT1	AT2	AT3
attempt = 0	0	0	0
attempt = 1	1	0	0
attempt = 2	0	1	0
attempt = 3	0	0	1