National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

Computer Architecture and Organization

Course Code:	EE-321	**Semester:**	Spring 2020
Credit Hours:	3+1	**Prerequisite Codes:**	Digital Logic Design
Instructor:	Taufique-ur-Rehman	**Discipline:**	Electrical Engineering
Office:	Room A-206, Faculty Block	**Telephone:**	
Lecture: **Labs:**	Tuesday , Wednesday and Friday Thursday	**E-mail:**	Taufique.rehman@seecs.edu.pk
Class Room:	CR-19/20 (IAEC)	**Consulting Hours:**	Wednesday 3:00 to 5:00
Knowledge Group:	DSSP	**Updates on LMS:**	End of every week

Course Description:

This course will focus on the principles, current practices, and issues in computer architecture and organization. Students will be introduced to the understanding of computer organization: roles of processors, main memory, and input/output devices. Understanding data path and control designs for processors. Understanding memory organization, including cache structures and virtual memory schemes. Understanding parallel processing and multi-core computers.

Course Objectives:

- A complete understanding of program execution.
- Understanding of computer functional components, their characteristics, their performance and their interactions.
- Understanding of computer architecture so to run programs more efficiently.
- Understanding parallelism in processor systems.

Books:

Text Books:
1. *Computer Architecture : A Quantitative approach* Fourth Edition By Hennessy, Patterson
2. William Stallings, Computer Organization and Architecture, Eighth/Ninth Edition, Prentice Hall.

Reference Books:
3. *Computer System Architecture* Third edition By M. Morris Mano
4. *The Intel Microprocessors* Sixth Edition By Barry B. Brey
5. *Computer Organization and Design The Hardware/Software interface* Fourth edition By Hennessy, Patterson

Main Topics to be Covered:

- Introduction to Computer Evolution/ Performance
- Computer Memories, Cache Memory, Internal Memory, External Memory
- Instruction Sets: Addressing modes, Formats, Functions
- Processor Structure &Function : Instruction cycle, pipelining
- Design a RISC micro-processor
- Instruction Level Parallelism and Superscalar Processors & Multicore Computers

Course Learning Outcomes (CLO)

	Upon successful completion of this course the students will be able to demonstrate the following: -	PLO	BT LEVEL*
1	**Understand** the function of major components of computer systems.	1	C-2
2	**Analyze** the internal architecture and organization of the processor.	2	C-4
3	**Validate** the underlying theoretical concepts of computer architecture and organization through simulation	5	P-3
* BT=Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A=Affective domain			

Mapping of CLOs TO Program Learning Outcomes

PLOs/ CLOs	CLO-1	CLO-2	CLO-3
PLO1 (Engineering Knowledge)	√		
PLO2(Problem Analysis)		√	
PLO3(Designing/Development of Solutions)			
PLO4(Investigation)			
PLO5(Modern tool usage)			√
PLO6(The Engineer and Society)			
PLO7(Environment and Sustainability)			
PLO8(Ethics)			
PLO9(Individual and Team Work)			
PLO10(Communication)			
PLO11(Project Management)			
PLO:12(Lifelong Learning)			

Mapping of CLOs to Assessment Modules and Weight ages (in accordance with NUST statutes)

To be filled in at the end of the course

CLOs\PLOs	CLO-1	CLO-2	CLO-3
Quizzes: (7.5%)	√	√	
Assignments: (7.5%)	√	√	
OHT-1: (11.25%)	√		
OHT-2: (11.25%)		√	
Labs: (15%)		√	√
Lab Test: (10%)			√
End Semester Exam: (37.5%)	√	√	
Total: 100%			

Lecture Breakdown:

Week No	Lecture	Topics
1.	**1.**	Course Contents, grading policies and review of basic components of a computer system.
	2.	Introduction and motivation to Computer Architecture and Micro-Architecture
	3.	Evolution of Processor Technologies
	Lab 01	LabVolt Trainer Familiarization
2.	4.	Data Addressing Modes (Generic) and review of Intel's data addressing Modes
	5.	Instruction Cycle and execution sequence of a simple program in a processor system
	6.	Designing and Writing Machine Codes for a simple processor system
	Lab 02	LabVolt Trainer Familiarization
3.	**7.**	Writing Machine Codes for Intel processor systems and Instruction Set Encodings
	8.	Designing a RISC processor
	9.	Designing a RISC processor
	Lab 03	Bus Operations
4.	10	Design Metrics (Throughput , Latency , Timing)
	11	Design Metrics (Throughput , Latency , Timing) and understanding the tradeoffs in Speed , Cost and Area
	12.	Memory types , technologies and Composing Memory
	Lab 04	Read and Write Cycles
5.	13.	Cache Memory Design
	14.	Cache Memory Design
	15.	Cache Memory Performance
	Lab 05	Declaration and Manipulation of Variables in Assembly Language

6.	**OHT-1**	
7.	16.	Cache Memory Performance and Levels of Cache Memory
	17.	Internal Memory Organization
	18.	Correction Codes, Advanced Memory Architectures
	Lab 06	Flag and Jump Commands in Assembly Language
8.	19.	External Memory
	20.	RAID System
	21.	SSD, Optical drives and Tapes
	Lab 07	Write a program for searching a data within an array
9.	22.	I/O Modules, Programmed I/O
	23.	Interrupt Driven I/O
	24.	Direct Memory Access
	Lab 08	Write a program to make a simple calculator program
10.	25.	Instruction Level Parallelism, Pipelining a MIPS Processor
	26.	Instruction Level Parallelism, Pipelining a MIPS Processor
	27.	Pipelining Hazards (Structural Hazards)
	Lab 09	Write a program to display the input number on the standard display without using the library integer display procedure
11.	28.	Pipelining Hazards (Data Hazards)
	29.	Pipelining Hazards (Control Hazards) Jumps
	30.	Pipelining Hazards (Control Hazards) Branches
	Lab 10	Floating Point Numbers

12.	**OHT-2**	
13.	31.	Introduction and Motivation to Superscalar Processors
	32.	Basic 2-Way In-order Superscalar Processor
	33.	Interrupts and Exception Handling in Processors
	Lab 11	Array sorting of Floating Point Numbers
14.	34.	Vector Processors Introduction And working principles
	35.	Examples of Vector Micro-Architecture
	36.	Introduction to SIMD processors and GPU's
	Lab 12	Write a program for 8051 microcontroller that turns on LEDs
15.	37.	Introduction to SIMD processors and GPU's
	38.	Motivation for Multithreading
	39.	Course-grained multithreading
	Lab 13	Write a program for 8051 microcontroller that turns on an LEDs using interrupt
16.	40.	Multiple Processor Organizations
	41.	Cache Coherence Protocols
	42.	Hardware and Software Issues
17.		Multicore Organization
		Multicore Organization
		Revision
	Lab 14	Lab Test
18.		ESE

Lab Experiments:
Lab 1 : LabVolt Trainer Familiarization
Lab 2 : Bus Operations
Lab 3 : Read Cycles
Lab 4 : Write cycles
Lab 5 : Declaration and Manipulation of Variables in Assembly Language
Lab 6 : Declaration and Manipulation of Variables in Assembly Language
Lab 7 : Write a program for searching a data within an array
Lab 8 : Write a program for searching a data within an array
Lab 9 : Write a program to display the input number on the standard display without using the library integer display procedure
Lab 10 : Floating Point Numbers
Lab 11 : Array sorting of Floating Point Numbers
Lab 12 : Write a program for 8051 microcontroller that turns on LEDs
Lab 13 : Write a program for 8051 microcontroller that turns on an LEDs using interrupt
Lab 14 : Lab Tests

Grading Policy:	
Quizzes Policy	The quizzes are a mandatory component of the overall assessment. The purpose of quizzes is to keep the students up-to-date with the lecture material and test basic understanding of the course concepts. There will be at least **6** unannounced quizzes conducted in the class any time during the lecture. Each quiz will consist of questions that target specific topics from the most recent as well as previous week lectures.
Assignments	To give sufficient practice and comprehensive understanding of the subject assignments will be given, on submitting you must declare that which questions you attempted yourself. The evaluated assignment is an individual effort and no hints will be posted on forum. Only declared questions by individual student will be evaluated. If the declared question done by you is found a copy of other then you may loose all the marks in assignments and get zero in assignments category. The questions in assignments will be challenging to give students the confidence and enable them to prepare for the exams well. Home works will be submitted at the beginning of class on the due date. The students are advised to do the assignment themselves. Copying of assignment is highly discouraged, taken as cheating case and dealt accordingly. Late submissions will also loose marks.

Conduct of Labs	The labs will be conducted for three hours each week. For the conduct of lab, the students will be divided into groups with 2 students per group. A lab handout comprising pre-lab, in-lab, and post-lab report parts will be provided to students for study and analysis during the week preceding each lab session. The students are expected to complete pre-lab work before lab starts and come prepared for the lab. Any student failing to complete pre-lab will not be allowed to attend lab session. The students will be evaluated during each lab based on demonstration, oral viva, and lab report submitted by them individually on completion of lab work. The students are required to be punctual in the lab; latecomers will not be allowed in the lab. No make-up provisions for the missed labs. Each lab is evaluated by Lab Engineer by taking a Lab Quiz and lab report. A comprehensive lab test will be arranged during closing weeks of semester and students will be individually evaluated accordingly.
Other Matters **Academic Honesty and Plagiarism**	Plagiarism is the unacknowledged use of other's work, including the copying of Assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.
Classroom Etiquettes	It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of class room behavior will be observed: - 1. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time. 2. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended. 3. All the cell phones must be switched OFF prior to entering the class room.
Tools / Software Requirement:	
	1. The Microsoft Macro Assembler (MASM) is used for programming in assembly language. Microcontroller 8051 is used for implementation.