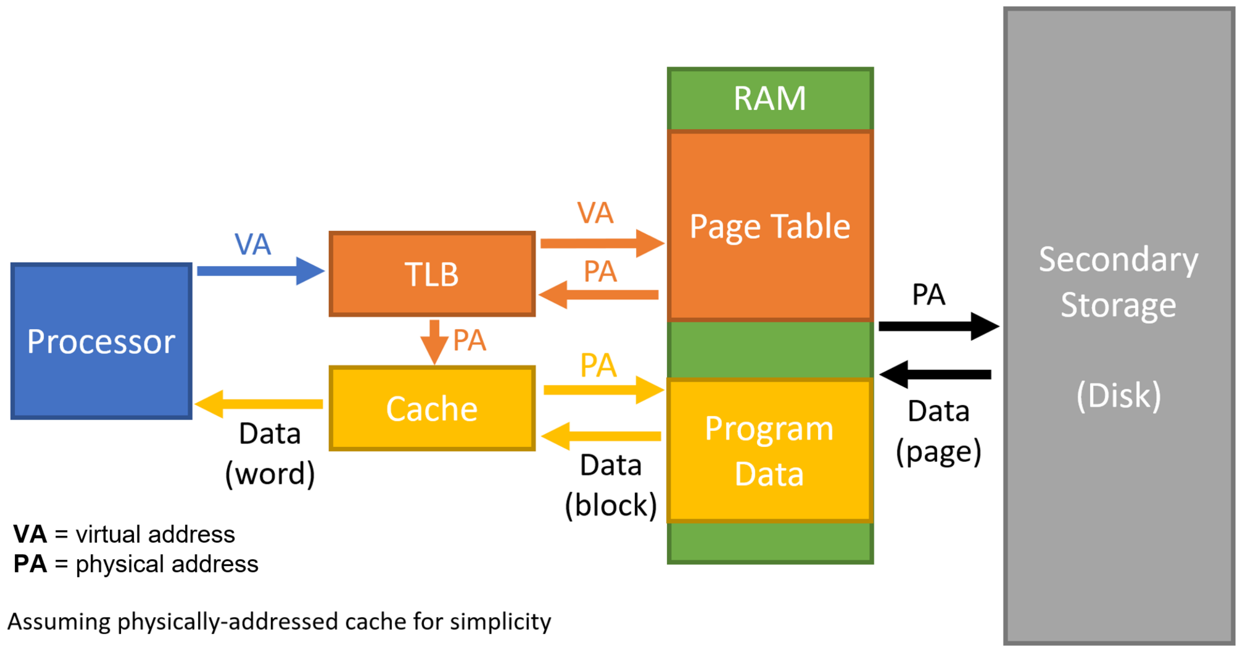
HW9.5. Resolving a Page Fault

A page fault occurs when the data that the program requests is not present in the main memory. For this question, we will try to enumerate the steps (in order) when resolving a page fault.

As a recap, the memory hierarchy would look like the following:



Arrange the following steps <u>in the correct order.</u>

Follow the arrows shown in the figure. We start from the processor side.

Drag from here:

Construct your solution here: ?

Given the virtual address, we access the TLB to look for the physical address translation. No translation exists for that address. TLB misses.

Since the TLB misses, we access the page table in the main memory (RAM) for the translation. Valid bit is 0. Data is on the secondary storage (Disk). Page fault.

We load a page of data from the secondary storage (Disk) to the main memory (RAM).

Page table is updated in the main memory (RAM) to point to the loaded page from the secondary storage (Disk). There's a valid physical address translation now.

The virtual address to physical address translation is loaded to the TLB. We now have the physical address of the data we need.

Given the physical address, we access the data cache. Since the page was just loaded earlier, it does not exist in the cache. Cache misses.

Since the cache misses, we

Homework 9

Assessment overview

Total points: 80/100

Score: 80%

Question

Value: 15

History: 15

Awarded points: 15/15

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

load the block of data from the main memory (RAM).

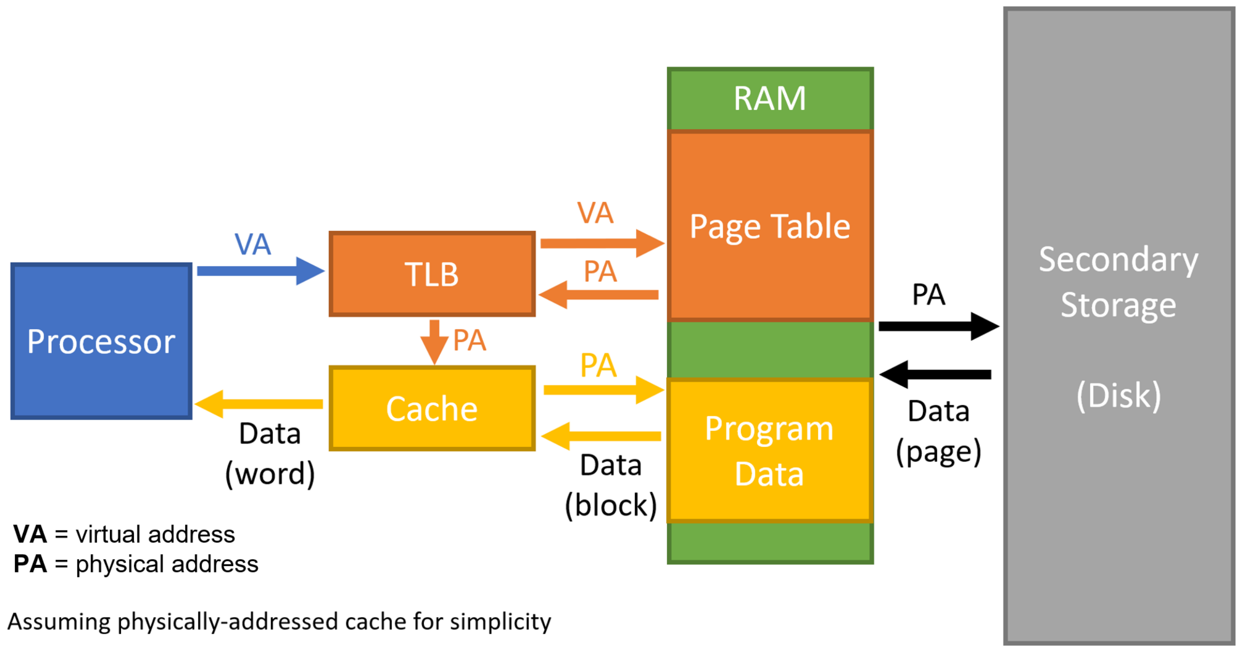
The cache can now return the corresponding data word to the processor.

Try a new variant

Correct answer

A page fault occurs when the data that the program requests is not present in the main memory. For this question, we will try to enumerate the steps (in order) when resolving a page fault.

As a recap, the memory hierarchy would look like the following:



Assuming physically-addressed cache for simplicity

Arrange the following steps <u>in the correct order.</u>

Follow the arrows shown in the figure. We start from the processor side.

Correct answer (in the specified order):

Given the virtual address, we access the TLB to look for the physical address translation. No translation exists for that address. TLB misses.

Since the TLB misses, we access the page table in the main memory (RAM) for the translation. Valid bit is 0. Data is on the secondary storage (Disk). Page fault.

We load a page of data from the secondary storage (Disk) to the main memory (RAM).

Page table is updated in the main memory (RAM) to point to the loaded page from the secondary storage (Disk). There's a valid physical address translation now.

The virtual address to physical address translation is loaded to the TLB. We now have the physical address of the data we need.

Given the physical address, we access the data cache. Since the page was just loaded earlier, it does not exist in the cache. Cache misses.

Since the cache misses, we load the block of data from the main memory (RAM).

The cache can now return the corresponding data word to the processor.

Submitted answer correct: 100%

Submitted at 2022-11-20 04:54:08 (PST)

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