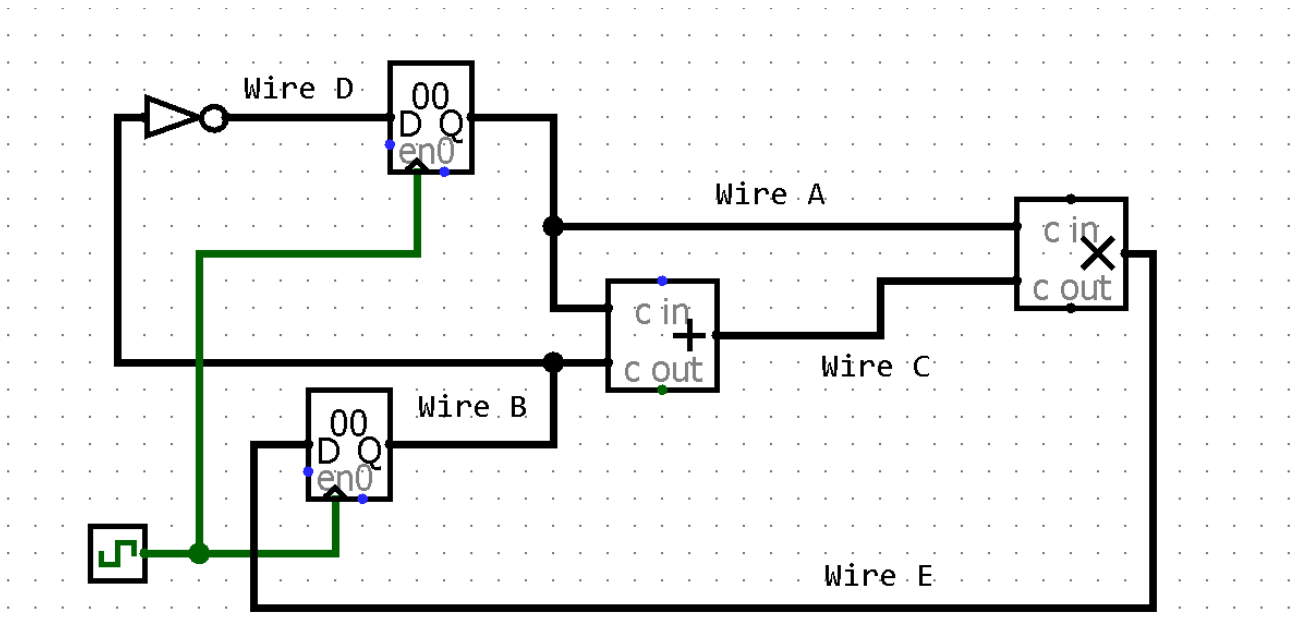
HW5.5. Critical Path

Feel free to check out the guide that we have prepared to help you in this problem.

Consider the following circuit:



Assume the following:

The `not` gate has a delay of 1 ns.

The adder block has a delay of 10 ns.

The multiplier block has a delay of 15 ns.

The registers have `clk-to-q` delays of 2 ns each, a setup time of 5 ns. Both registers have the same hold time.

At time 0, we trigger a positive edge of the clock (For now, assume no setup or hold time violations occur).

For each wire, determine the following delays relative to the positive edge of the clock: (input only the number, don't include the units)

Q1.1: Delay seen at Wire A: integer

Q1.2: Delay seen at Wire B: integer

Q1.3: Delay seen at Wire C: integer

Q1.4: Delay seen at Wire D: integer

Q1.5: Shortest delay seen at Wire E: integer

Q1.6: Longest delay seen at Wire E: integer

As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Q1.7: What is the maximum hold time for our registers in order for the circuit to have well-defined behavior?
Hint: All paths (between flipflops) must satisfy the hold time inequality for the entire system to work properly.

integer

Homework 5

Assessment overview

Total points: 45/100

Score: 45%

Question

Value: 20

History:

Awarded points: 0/20

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

Q1.8: What is the largest combinational logic delay of this circuit? Note that register `clk-to-q` isn't considered part of the combinational logic delay
Hint: Consider all valid paths (between flipflops) in the entire system then pick the longest one.

integer

Q1.9: What is the shortest possible clock period that we could use in order for the circuit to have well-defined behavior? Note that we need to ensure that the inputs to both registers are stable within the register setup time window before the next positive edge of the clock happens.
Hint: Your answer in the previous question will be relevant for this one.

integer

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