HW7.2. Cache Hits and Miss Types

For this question, assume that we are working with 16-bit memory addresses.

For the following cache types:

a: Determine the number of bits for tag, index and offset.

b: Analyze how each cache behaves for the given access patterns.

For each memory access, determine if the result is a hit, a compulsory miss, a capacity miss, or a conflict miss.

For this problem, we can use the following simplified convention when classifying miss types:

***Conflict miss**: If the address was in the cache, but isn't anymore (got evicted) and the cache is still not full.*

***Capacity miss**: If the address was in the cache, but isn't anymore (got evicted) and the cache is full.*

***Compulsory miss**: If the address was never in the cache (cold start).*

Q1: A fully associative cache with 16 B blocks, 64 B capacity, and FIFO (First In-First Out) eviction policy

Q1.1: Tag: 12 ✓100%

Q1.2: Index: 0 ✓100%

Q1.3: Offset: 4 ✓100%

Q1.4: 0x1000: Compulsory Miss ✓100%

Q1.5: 0x1010: Compulsory Miss ✓100%

Q1.6: 0x1000: Hit ✓100%

Q1.7: 0x1020: Compulsory Miss ✓100%

Q1.8: 0x1004: Hit ✓100%

Q1.9: 0x1030: Compulsory Miss ✓100%

Q1.10: 0x1008: Hit ✓100%

Q1.11: 0x1040: Compulsory Miss ✓100%

Q1.12: 0x1000: Capacity Miss ✓100%

Q2: A direct-mapped cache with 8 B blocks, and 1 KiB capacity

Q2.1: Tag: 6 ✓100%

Q2.2: Index: 7 ✓100%

Q2.3: Offset: 3 ✓100%

Q2.4: 0x1000: Compulsory Miss ✓100%

Homework 7

Assessment overview

Total points: 50/100

Score: 50%

Question

Value: 20

History: 20

Awarded points: 20/20

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Previous question

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Attached files

No attached files

Attach a file

Attach text

Q2.5: 0x1001: Hit ✓100%

Q2.6: 0x2000: Compulsory Miss ✓100%

Q2.7: 0x1002: Conflict Miss ✓100%

Q2.8: 0x1003: Hit ✓100%

Q2.9: 0x2001: Conflict Miss ✓100%

Q2.10: 0x1004: Conflict Miss ✓100%

Q2.11: 0x1005: Hit ✓100%

Q2.12: 0x2002: Conflict Miss ✓100%

Q3: A 2-way set associative cache with 4 B blocks, 16 B capacity, and LRU (Least Recently Used) eviction policy

Q3.1: Tag: 13 ? ✓100%

Q3.2: Index: 1 ? ✓100%

Q3.3: Offset: 2 ? ✓100%

Q3.4: 0x1000: Compulsory Miss ✓100%

Q3.5: 0x2000: Compulsory Miss ✓100%

Q3.6: 0x1000: Hit ✓100%

Q3.7: 0x3000: Compulsory Miss ✓100%

Q3.8: 0x1002: Hit ✓100%

Q3.9: 0x2002: Conflict Miss ✓100%

Q3.10: 0x1004: Compulsory Miss ✓100%

Q3.11: 0x2004: Compulsory Miss ✓100%

Q3.12: 0x3000: Capacity Miss ✓100%

Try a new variant

Correct answer

Q1: A fully associative cache with 16 B blocks, 64 B capacity, and FIFO (First In-First Out) eviction policy

Q1.1: Tag: 12

Q1.2: Index: `0`

Q1.3: Offset: 4

Q1.4: 0x1000: `Compulsory Miss`
Q1.5: 0x1010: `Compulsory Miss`
Q1.6: 0x1000: `Hit`
Q1.7: 0x1020: `Compulsory Miss`
Q1.8: 0x1004: `Hit`
Q1.9: 0x1030: `Compulsory Miss`
Q1.10: 0x1008: `Hit`
Q1.11: 0x1040: `Compulsory Miss`
Q1.12: 0x1000: `Capacity Miss`
Q2: A direct-mapped cache with 8 B blocks, and 1 KiB capacity

Q2.1: Tag: 6

Q2.2: Index: 7

Q2.3: Offset: 3

Q2.4: 0x1000: `Compulsory Miss`

Q2.5: 0x1001: `Hit`

Q2.6: 0x2000: `Compulsory Miss`

Q2.7: 0x1002: `Conflict Miss`

Q2.8: 0x1003: `Hit`

Q2.9: 0x2001: `Conflict Miss`

Q2.10: 0x1004: `Conflict Miss`

Q2.11: 0x1005: `Hit`

Q2.12: 0x2002: `Conflict Miss`

Q3: A 2-way set associative cache with 4 B blocks, 16 B capacity, and LRU (Least Recently Used) eviction policy

Q3.1: Tag: 13

Q3.2: Index: 1

Q3.3: Offset: 2

Q3.4: 0x1000: `Compulsory Miss`

Q3.5: 0x2000: `Compulsory Miss`

Q3.6: 0x1000: `Hit`

Q3.7: 0x3000: `Compulsory Miss`

Q3.8: 0x1002: `Hit`

Q3.9: 0x2002: `Conflict Miss`

Q3.10: 0x1004: `Compulsory Miss`

Q3.11: 0x2004: `Compulsory Miss`

Q3.12: 0x3000: `Capacity Miss`

A few quick tips: Note that the offset corresponds to the block size, and the index corresponds to the number of sets. Tag is simply the rest of the bits.

When determining hits/misses, it is often useful to write out what's stored where. You may notice that FIFO is fairly easy to compute, while LRU requires moving around blocks. LRU is often preferred, though, because it leads to better hit rate. Try out the other policy on questions 1 and 3, and you will find that LRU tends to outperform FIFO.

Compulsory misses always occur when we first access a block, since we absolutely must add that block, regardless of cache properties. Capacity misses relate to the fact that we eventually need to evict blocks, and occur when our cache is full. Conflict misses occur when we still have empty spots in our cache, but we had to evict the block anyway because we ran out of space in the particular set. Generally, a higher assiciativity reduces conflict misses, while a higher size reduces capacity misses. Generally, increases in capacity or associativity also slow the cache down, so there's always a tradeoff when choosing cache size.

Submitted answer 4 **correct: 100%**
Submitted at 2022-10-29 06:00:15 (PDT)
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Submitted answer 3 **partially correct: 97%**
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Submitted answer 2 **partially correct: 91%**
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