HW5.4. Common SDS Pitfalls

Feel free to check out the guide that we have prepared to help you in this problem.

As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

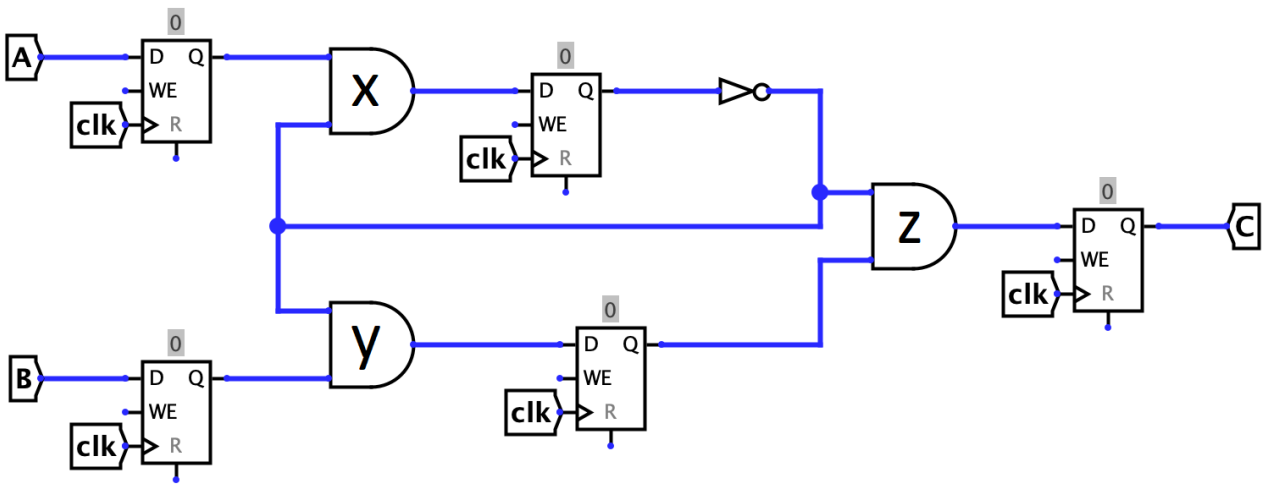
Also, once you have correctly answered the following questions, spend some time reading the provided explanations to understand the common misconceptions and why they are wrong.

Which of the following statements are true?

- ☐ (a) The digital circuit can still work reliably even if the hold time requirement is not satisfied.
- ☐ (b) We can increase the operating clock frequency of the system if we can make the maximum logic delay smaller.
- ☐ (c) Increasing the clock period always solves setup time violations.
- ☐ (d) Setup time is the time needed for the input to be stable before the positive edge of the clock.
- ☐ (e) The clk-to-q delay of the flipflop changes by changing the clock period.
- ☐ (f) Keeping everything else constant, increasing combinational logic complexity (hence, increasing the delay) can make the entire system fail to work properly.
- ☐ (g) Hold time is the delay of the flipflop after the positive edge of the clock.
- ☐ (h) Increasing the clock period can solve hold time violations.

Select all possible options that apply.

Suppose we have the following digital circuit:



Assume the following:

You can safely ignore inputs A and B, and output C for this problem.

You can ignore the R and WE ports in the flipflops. Those are not relevant to this problem.

The delays of the AND gates (x, y, z) are identical.

The delay of the NOT gate is the same as the AND gate delay.

All flipflops are connected to the same clock.

All flipflops are identical to each other (i.e. they have the same clock-to-q delays, setup times, and hold times).

Select all valid inequalities that can be used if we want to calculate for the minimum clock period for the system.

Homework 5

Assessment overview

Total points: 40/100

Score: 40%

Question

Value: 5

History:

Awarded points: 0/5

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

You want to consider the longest combinational path delay to get the minimum clock period.

Hint: Try tracing out the path that is being described by the delay summation and see if those paths makes sense.

☐ (a) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (b) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (c) $t_{\text{clk-to-q}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (d) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (e) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (f) $t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (g) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (h) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☐ (i) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{setup}} + t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} + t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

Select all possible options that apply.

Save & Grade *20 attempts left* | Save only | *Additional attempts available with new variants*