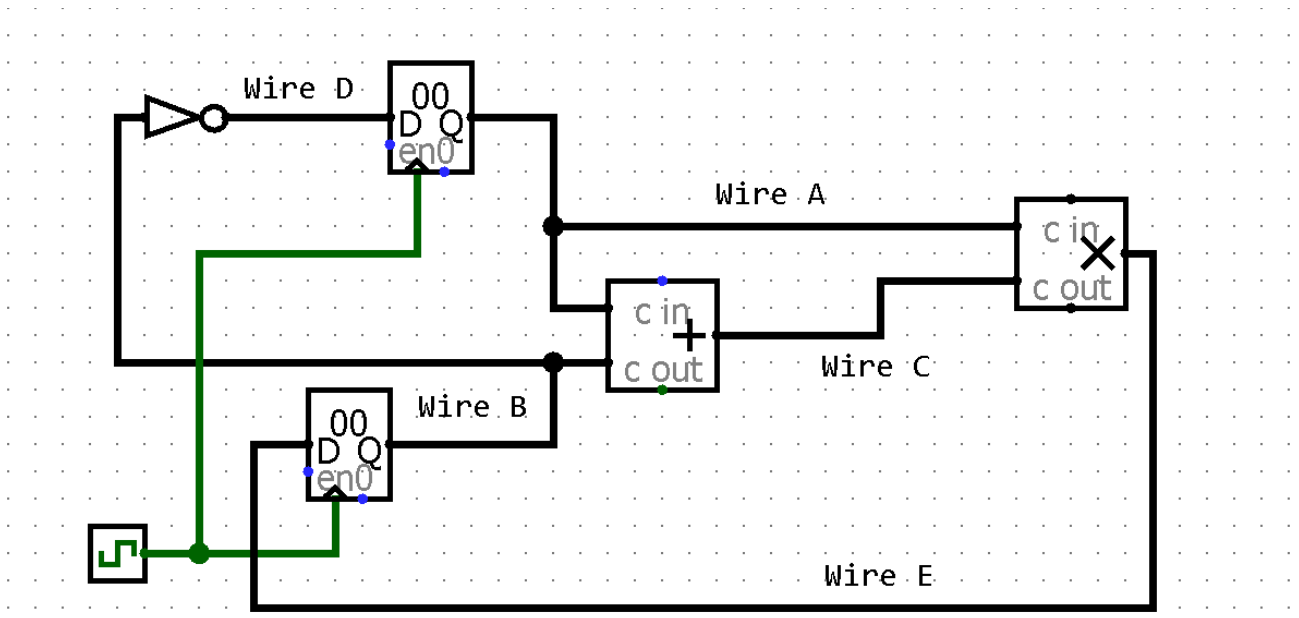
HW5.5. Critical Path

Feel free to check out the guide that we have prepared to help you in this problem.

Consider the following circuit:



Assume the following:

The `not` gate has a delay of 1 ns.

The adder block has a delay of 10 ns.

The multiplier block has a delay of 15 ns.

The registers have `clk-to-q` delays of 2 ns each, a setup time of 5 ns. Both registers have the same hold time.

At time 0, we trigger a positive edge of the clock (For now, assume no setup or hold time violations occur).

For each wire, determine the following delays relative to the positive edge of the clock: (input only the number, don't include the units)

Q1.1: Delay seen at Wire A: 1 ✕ 0%

Q1.2: Delay seen at Wire B: 1 ✕ 0%

Q1.3: Delay seen at Wire C: 1 ✕ 0%

Q1.4: Delay seen at Wire D: 1 ✕ 0%

Q1.5:

Shortest delay seen at Wire E: 1 ✕ 0%

Q1.6:

Longest delay seen at Wire E: 1 ✕ 0%

As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Q1.7: What is the maximum hold time for our registers in order for the circuit to have well-defined behavior?
Hint: All paths (between flipflops) must satisfy the hold time inequality for the entire system to work properly.

Homework 5

Assessment overview

Total points: 100/100

Score: 100%

Question

Value: 20

History: 20

Awarded points: 20/20

Report an error in this question

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1 ? × 0%

Q1.8: What is the largest combinational logic delay of this circuit? Note that register `clk-to-q` isn't considered part of the combinational logic delay
Hint: Consider all valid paths (between flipflops) in the entire system then pick the longest one.

11 ? × 0%

Q1.9: What is the shortest possible clock period that we could use in order for the circuit to have well-defined behavior? Note that we need to ensure that the inputs to both registers are stable within the register setup time window before the next positive edge of the clock happens.
Hint: Your answer in the previous question will be relevant for this one.

1 ? × 0%

Try a new variant

Correct answer

Feel free to check out the guide that we have prepared to help you in this problem.

Q1.1: Delay seen at Wire A: 2

Q1.2: Delay seen at Wire B: 2

Q1.1 and 1.2: At time 0, the clock ticks. At time 2, Wires A and B update as a result of the registers changing value. This is purely due to the clk-to-q delay of the registers.

Q1.3: Delay seen at Wire C: 12

Q1.3: Wire C is the output of the adder. The adder's inputs both change at time 2, so Wire C changes at time 2+10 = 12.

Q1.4: Delay seen at Wire D: 3

Q1.4: Wire D is the output of the not gate. The not gate's input changes at time 2, so Wire D changes at time 2+1 = 3.

Q1.5: Shortest delay seen at Wire E: 17

Q1.6: Longest delay seen at Wire E: 27

Q1.5 and Q1.6: Wire E is the output of the multiplier. The multiplier's inputs first change at time 2, and last change at time 12, so Wire E first changes at 2+15 = 17, and last changes at 12+15=27.

As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Q1.7: What is the maximum hold time for our registers in order for the circuit to have well-defined behavior?
Hint: All paths (between flipflops) must satisfy the hold time inequality for the entire system to work properly.

3

Q1.7: The input to the top register first changes at time 3, so our maximum hold time is 3 ns. Note that the input to the bottom register first changes at time 17, so a hold time of 3 ns is fulfilled for the bottom register.

Q1.8: What is the largest combinational logic delay of this circuit? Note that register `clk-to-q` isn't considered part of the combinational logic delay
Hint: Consider all valid paths (between flipflops) in the entire system then pick the longest one.

25

Q1.8: The last changes happen at time 27. Subtracting the clk-to-q delay of 2 ns gives our combinational logic delay of 25 ns.

Q1.9: What is the shortest possible clock period that we could use in order for the circuit to have well-defined behavior? Note that we need to ensure that the inputs to both registers are stable within the register setup time window before the next positive edge of the clock happens.
Hint: Your answer in the previous question will be relevant for this one.

32

Q1.9: At time 27, the bottom register's input stabilizes. After that, we need to wait another 5 ns to fulfill the setup time requirement. Thus, our circuit is stable and ready for another clock tick at time 32. Thus, our fastest clock cycle is 32 ns. Note that the upper register has its input stabilize at 3 ns, so its setup time is fulfilled by time 32.

Submitted answer 20 **incorrect: 0%**
Submitted at 2022-10-21 00:09:56 (PDT)

Submitted answer 19 **incorrect: 0%**
Submitted at 2022-10-21 00:09:51 (PDT)

Submitted answer 18 **incorrect: 0%**
Submitted at 2022-10-21 00:09:48 (PDT)

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