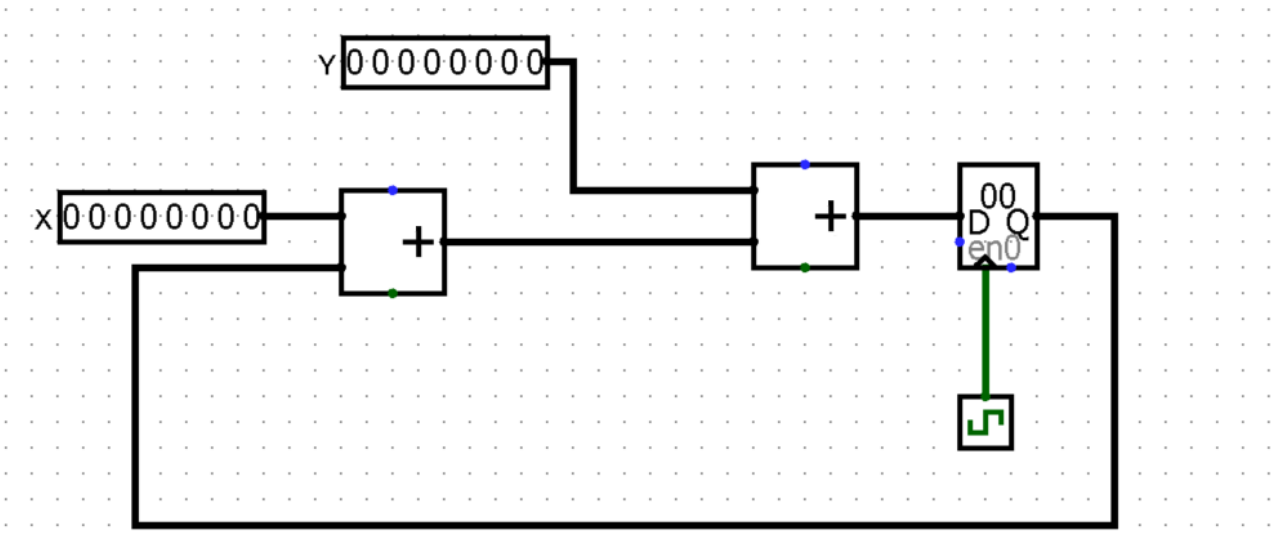
## HW5.6. Adder Circuit

Feel free to check out the guide that we have prepared to help you in this problem.

Consider the following circuit:




X and Y update at each rising edge of the clock. You are given the following: the adder propagation delay is 2 ns, the register setup time is 2 ns, the register hold time is 4 ns, the register `clk-to-q delay` is 3 ns, and the clock frequency is 100 MHz.

*Hint: If an input updates at each rising edge of the clock, you can think of it as an output from a register with 0 `clk-to-q delay`.*

As a reminder, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Q1.1: After the rising edge of the clock, how many nanoseconds elapse before the input to the register changes?
*Hint: Consider all the paths going into the register, the shortest one will induce the first input change to the register.*

integer

Q1.2: Is the hold time requirement of the register met?
*Hint: Your answer to the previous question will be relevant for this one.*

- (a) Yes
- (b) No

Q1.3: Will the circuit work properly?
*Hint: Recall that both setup and hold time inequalities should be satisfied for the circuit to work properly.*

- (a) Yes
- (b) No

**Now assume that X and Y update 2 ns after each clock trigger**

*Hint: Now we can think of the inputs as coming from registers with `clk-to-q` delay of 2 ns.*

Q2.1: What is the the minimum clock period needed to ensure that the system works correctly?
*Hint: You would need to identify the longest combinational path delay for this one. Consider all paths that leads to the register input.*

integer

Q2.2: What is the maximum clock frequency at which the circuit will work properly? Express your answer in MHz.
*Hint: Maximum clock frequency = 1/(minimum clock period).*

number (rtol=0.01, atol=1e-08)

Now we want to rearrange the components of this accumulator.

For each of the following suggestions, state how it will affect the max clock frequency.

Q3.1: Swap X and Y

- (a) Increases max clock frequency
- (b) Doesn't affect max clock frequency
- (c) Decreases max clock frequency

Q3.2: Add X and Y first, then add the result with the output of the register
*Note that the current setup has input X added to the register output first before being added to Y.*

- (a) Increases max clock frequency
- (b) Doesn't affect max clock frequency
- (c) Decreases max clock frequency

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