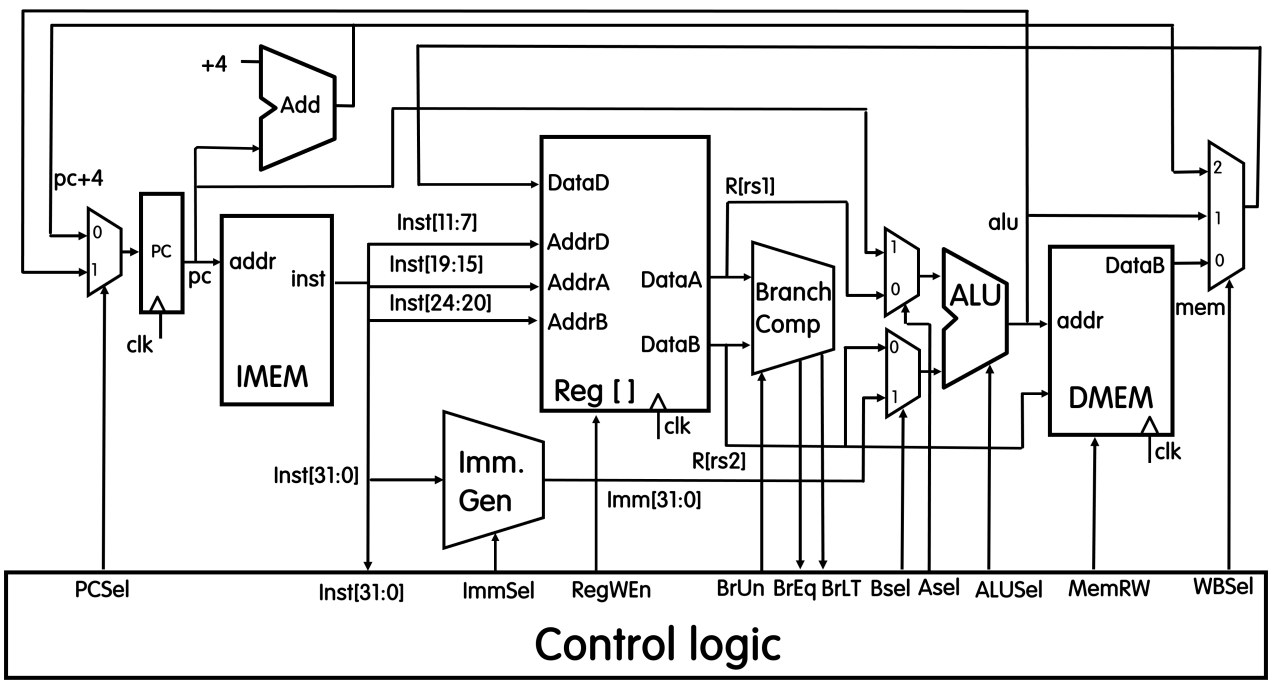
HW6.5. Supporting new instructions

The datapath below implements the RV32I instruction set.



Specify whether the following proposed instructions can be implemented using this datapath **without modifications** (That is, you can only change the control signals, but the datapath connections remain the same). If the instruction can be implemented, specify what the control signal should be (either 0 or 1). If the control signal corresponds to a multiplexer select signal, check the datapath provided earlier to see which data the multiplexer will be selecting (note the data going into the 0 and 1 inputs of the mux). If the instruction is not implementable, write "No" in the implementable column and "N/A" in the Control Signals column.

Example:

Instruction	Description	Implementable?	Control Signals
Add `add rd, r1, rs2`	`rd = rs1 + rs2`	**Yes**	**PCSel = 0** **WBSel = 1**

Instruction	Description	Implementable?	Control Signals
Register offset load `lwreg rd, rs1, rs2`	`rd = 4 bytes of memory starting at address (rs1 + rs2)`	Yes ✓100%	**ASel =** 0 ✓100% **BSel =** 0 ✓100%

beq with writeback
`beq rd, rs1, rs2, label`
	`rd = rs1 + rs2`
	`if (rs1 == rs2){`
	`PC = PC + offset}`
		No ✓100%	**WBSel =** N/A ✓100%
			PCSel = N/A ✓100%

PC-relative load `lwpc rd, imm`	`rd = 4 bytes of memory starting at address (PC + imm)`	Yes ✓100%	**ASel =** 1 ✓100% **BSel =** 1 ✓100%

Homework 6

Assessment overview

Total points: 93.82/100

Score: 93%

Question

Value: 15

History: 15

Awarded points: 15/15

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

Load word with add `lwadd rd, rs1, rs2, imm`	`rd = (4 bytes at memory address (rs1 + imm)) + rs2. M[rs1 + imm] + rs2`	No ? ✓100%	**RegWEn =** N/A ? ✓100% **WBSel =** N/A ? ✓100%

Try a new variant

Correct answer

Specify whether the following proposed instructions can be implemented using this datapath **without modifications** (That is, you can only change the control signals, but the datapath connections remain the same). If the instruction can be implemented, specify what the control signal should be (either 0 or 1). If the control signal corresponds to a multiplexer select signal, check the datapath provided earlier to see which data the multiplexer will be selecting (note the data going into the 0 and 1 inputs of the mux). If the instruction is not implementable, write "No" in the implementable column and "N/A" in the Control Signals column.

Example:

Instruction	Description	Implementable?	Control Signals
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Instruction	Description	Implementable?	Control Signals
Register offset load `lwreg rd, rs1, rs2`	`rd = 4 bytes of memory starting at address (rs1 + rs2)`	`Yes`	**ASel =** `0` **BSel =** `0`
beq with writeback `beq rd, rs1, rs2, label`	`rd = rs1 + rs2 if (rs1 == rs2){ PC = PC + offset}`	`No`	**WBSel =** `N/A` **PCSel =** `N/A`
PC-relative load `lwpc rd, imm`	`rd = 4 bytes of memory starting at address (PC + imm)`	`Yes`	**ASel =** `1` **BSel =** `1`
Load word with add `lwadd rd, rs1, rs2, imm`	`rd = (4 bytes at memory address (rs1 + imm)) + rs2. M[rs1 + imm] + rs2`	`No`	**RegWEn =** `N/A` **WBSel =** `N/A`

`lwreg rd, rs1, rs2` can be implemented somewhat similarly to a typical load instruction, but using different operands going into the ALU.

`beq rd, rs1, rs2, label` cannot be implemented, however, because it requires two different additions (adding rs1 and rs2, and pc + offset) which cannot be done with a single ALU.

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`lwadd rd, rs1, rs2, imm` cannot be implemented, however, because it requires two different additions (adding rs1 and imm, and memory data + rs2) which cannot be done with a single ALU.

Submitted answer 3 **correct: 100%**
Submitted at 2022-10-23 08:31:41 (PDT)

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Submitted answer 2 **partially correct: 50%**
Submitted at 2022-10-23 08:31:22 (PDT)

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Submitted answer 1 **partially correct: 16%**
Submitted at 2022-10-23 08:30:44 (PDT)

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