HW7.2. Cache Hits and Miss Types

For this question, assume that we are working with 16-bit memory addresses.

For the following cache types:

a: Determine the number of bits for tag, index and offset.

b: Analyze how each cache behaves for the given access patterns.

For each memory access, determine if the result is a hit, a compulsory miss, a capacity miss, or a conflict miss.

For this problem, we can use the following simplified convention when classifying miss types:

***Conflict miss**: If the address was in the cache, but isn't anymore (got evicted) and the cache is still not full.*

***Capacity miss**: If the address was in the cache, but isn't anymore (got evicted) and the cache is full.*

***Compulsory miss**: If the address was never in the cache (cold start).*

Q1: A fully associative cache with 16 B blocks, 64 B capacity, and FIFO (First In-First Out) eviction policy

Q1.1: Tag: integer

Q1.2: Index: integer

Q1.3: Offset: integer

Q1.4: 0x1000:

Q1.5: 0x1010:

Q1.6: 0x1000:

Q1.7: 0x1020:

Q1.8: 0x1004:

Q1.9: 0x1030:

Q1.10: 0x1008:

Q1.11: 0x1040:

Q1.12: 0x1000:

Q2: A direct-mapped cache with 8 B blocks, and 1 KiB capacity

Q2.1: Tag: integer

Q2.2: Index: integer

Q2.3: Offset: integer

Q2.4: 0x1000:

Homework 7

Assessment overview

Total points: 0/100

Score: 0%

Question

Value: 20

History:

Awarded points: 0/20

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

Q2.5: 0x1001:

Q2.6: 0x2000:

Q2.7: 0x1002:

Q2.8: 0x1003:

Q2.9: 0x2001:

Q2.10: 0x1004:

Q2.11: 0x1005:

Q2.12: 0x2002:

Q3: A 2-way set associative cache with 4 B blocks, 16 B capacity, and LRU (Least Recently Used) eviction policy

Q3.1: Tag: integer

Q3.2: Index: integer

Q3.3: Offset: integer

Q3.4: 0x1000:

Q3.5: 0x2000:

Q3.6: 0x1000:

Q3.7: 0x3000:

Q3.8: 0x1002:

Q3.9: 0x2002:

Q3.10: 0x1004:

Q3.11: 0x2004:

Q3.12: 0x3000:

Save & Grade *20 attempts left* | Save only | *Additional attempts available with new variants*