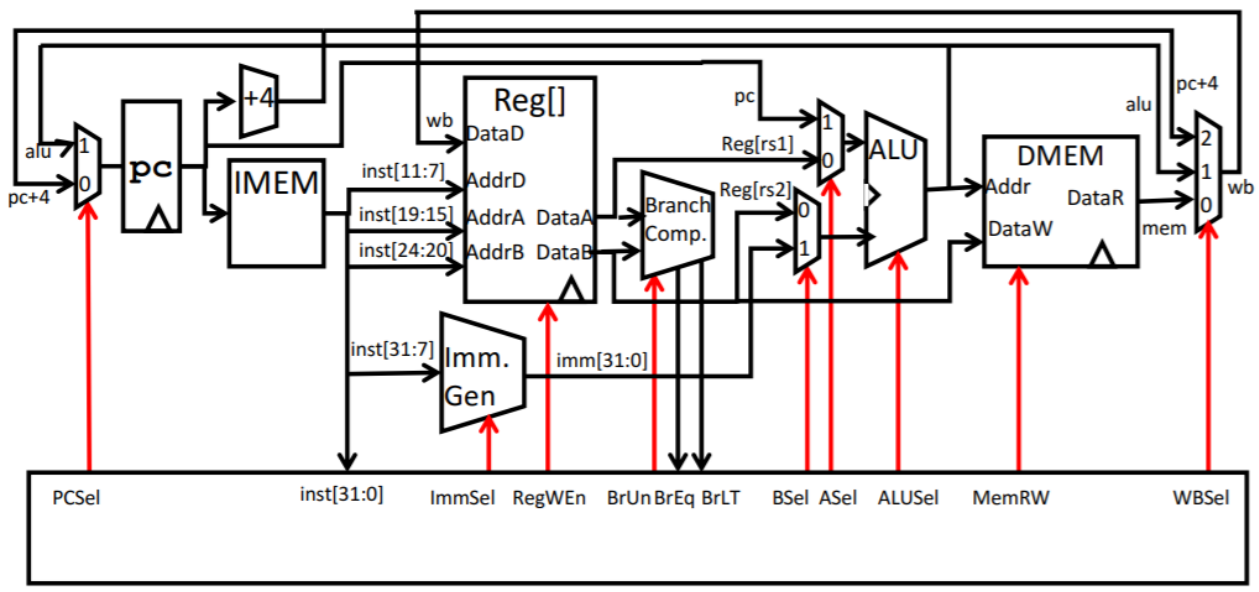
HW6.2. Datapath Design Part 1: Single Cycle

Feel free to check out the guide that we have prepared to help you in this problem.

Below is a copy of the RISC-V datapath presented in lecture:



Assume the following delays for components. Any component not listed is assumed to have a negligible delay.

Element	Reg clk-to-q	Reg setup	MUX	ALU	MemRead	MemWrite	RegFile Read	RegFile Setup	BranchComp
Parameter	$t_{clk-to-q}$	t_{setup}	t_{mux}	t_{alu}	$t_{mem-read}$	$t_{mem-write}$	$t_{rf-read}$	$t_{rf-setup}$	$t_{branch-comp}$
Delay (ps)	30	20	50	200	250	250	150	20	75

1.1: What instruction type takes the longest to execute in this datapath (i.e. the instruction type that dictates the critical path of the datapath)?

- (a) Load Instructions: lb, lw, ... ✓
- (b) Branches: beq, bne, ...
- (c) jal
- (d) I-type ALU Instructions: addi, xori, ...
- (e) Store Instructions: sw, sbu, ...
- (f) R-type ALU Instructions: add, xor, ...
- (g) jalr
- (h) lui
- (i) auipc

✓ 100%

1.2: For the instruction that takes longest to execute in this datapath, which components would be relevant to the critical path calculation? (Do not include components that are still used by the instruction but are not on the critical path for the given delays)

- (a) PC-MUX
- (b) PC register ✓
- (c) IMEM ✓
- (d) Imm-Gen
- (e) RegFile read ✓
- (f) Branch Comparator
- (g) A-MUX ✓
- (h) B-MUX
- (i) ALU ✓
- (j) DMEM ✓
- (k) WB-MUX ✓
- (l) RegFile Write ✓

Select all possible options that apply.

✓ 100%

Homework 6

Assessment overview

Total points: 30/100

Score: 30%

Question

Value: 20

History: 20

Awarded points: 20/20

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

1.3: What is the critical path delay (or the minimum operating clock period) of this circuit, in ps?

1000 ? ✓ 100%

1.4: What is the fastest clock frequency that can be used with this datapath? Express your answer in GHz.
Take note of the time units

1 ? ✓ 100%

Recall that latency refers to how long any given instruction takes to finish, while throughput is defined as the number of instructions finished per unit time.

1.5: What is the minimum latency of a single instruction, in cycles?
Hint: How many clock cycles does it take to finish 1 instruction?

1 ? ✓ 100%

1.6: What is the minimum latency of a single instruction, in picoseconds?
Hint: The clock period you calculated earlier is the number of seconds per clock cycle.

1000 ? ✓ 100%

1.7: What is the maximum throughput, in instructions/cycle?
Hint: How many instructions finish in 1 clock cycle?

1.00 ? ✓ 100%

1.8: What is the maximum throughput, in instructions/second?
Hint: Take note of the time units, count the zeroes properly.

1.00e9 ? ✓ 100%

Take note of your all your answers in this problem (write them down if ever). We'll be drawing some conclusions based on the numbers you calculated here in Part 2: Pipelined datapath.

Try a new variant

Correct answer

1.1: What instruction type takes the longest to execute in this datapath (i.e. the instruction type that dictates the critical path of the datapath)?
(a) Load Instructions: lb, lw, ...

1.2: For the instruction that takes longest to execute in this datapath, which components would be relevant to the critical path calculation? (Do not include components that are still used by the instruction but are not on the critical path for the given delays)
(b) PC register
(c) IMEM
(e) RegFile read
(g) A-MUX
(i) ALU
(j) DMEM
(k) WB-MUX
(l) RegFile Write

1.3: What is the critical path delay (or the minimum operating clock period) of this circuit, in ps?
`1000`

1.1 - 1.3: We go from PC Register to Instruction Memory, which is Register clk-to-q (30 ps).

Then we read Instruction Memory, which is Mem Read (250 ps).

Then we READ regfile, RegFile Read (150 ps). Note that the register read is purely combinational (we just sample the output wire of the register), so it doesn't require a clock tick to continue.

Then we go through a MUX before the ALU, which is (50 ps). Note that both A-Mux and B-Mux selections are executed in parallel and only contributes one mux delay.

Then we go through the ALU, which is (200 ps).

Then we read from DMEM (Note that we can't write DMEM, since that would result in writeback not doing anything, so we don't need to wait for later steps) (250 ps)

Then we go through the WB mux (50 ps)

Then we write back to our regfile, so we need to wait for the setup time (20 ps) of the register file.

Our total is thus 1000 ps.

The instruction that traces IMEM -> Register read -> A/B MUX -> ALU -> DMEM (read) -> Register Write is loads.

1.4: What is the fastest clock frequency that can be used with this datapath? Express your answer in GHz.
Take note of the time units

`1.00`

1.4: Frequency = 1/period = 1/(1000 ps) = 1 GHz

Recall that latency refers to how long any given instruction takes to finish, while throughput is defined as the number of instructions finished per unit time.

1.5: What is the minimum latency of a single instruction, in cycles?
Hint: How many clock cycles does it take to finish 1 instruction?

`1`

1.6: What is the minimum latency of a single instruction, in picoseconds?
Hint: The clock period you calculated earlier is the number of seconds per clock cycle.

`1000`

1.7: What is the maximum throughput, in instructions/cycle?
Hint: How many instructions finish in 1 clock cycle?

`1.00`

1.8: What is the maximum throughput, in instructions/second?
Hint: Take note of the time units, count the zeroes properly.

`1.00e9`

1.5 through 1.8: Each instruction takes one cycle to go through the entire datapath, and one instruction finishes per cycle. Assuming we use our fastest clock cycle of 1 GHz, we get a latency of 1 ns and 1 billion ops/second, respectively.

Take note of your all your answers in this problem (write them down if ever). We'll be drawing some conclusions based on the numbers you calculated here in Part 2: Pipelined datapath.

Submitted answer **correct: 100%**
Submitted at 2022-10-23 05:40:42 (PDT)

hide

1.1: What instruction type takes the longest to execute in this datapath (i.e. the instruction type that dictates the critical path of the datapath)?
(a) Load Instructions: lb, lw, ... ✓ 100%

1.2: For the instruction that takes longest to execute in this datapath, which components would be relevant to the critical path calculation? (Do not include components that are still used by the instruction but are not on the critical path for the given delays)

(b) PC register ✅
(c) IMEM ✅
(e) RegFile read ✅
(g) A-MUX ✅
(i) ALU ✅
(j) DMEM ✅
(k) WB-MUX ✅
(l) RegFile Write ✅
✓ 100%

1.3: What is the critical path delay (or the minimum operating clock period) of this circuit, in ps?
`1000` ✓ 100%

1.4: What is the fastest clock frequency that can be used with this datapath? Express your answer in GHz.
Take note of the time units

1 ? ✓ 100%

Recall that latency refers to how long any given instruction takes to finish, while throughput is defined as the number of instructions finished per unit time.

1.5: What is the minimum latency of a single instruction, in cycles?
Hint: How many clock cycles does it take to finish 1 instruction?

1 ✓ 100%

1.6: What is the minimum latency of a single instruction, in picoseconds?
Hint: The clock period you calculated earlier is the number of seconds per clock cycle.

`1000` ✓ 100%

1.7: What is the maximum throughput, in instructions/cycle?
Hint: How many instructions finish in 1 clock cycle?

1 ? ✓ 100%

1.8: What is the maximum throughput, in instructions/second?
Hint: Take note of the time units, count the zeroes properly.

`1000000000` ? ✓ 100%

Take note of your all your answers in this problem (write them down if ever). We'll be drawing some conclusions based on the numbers you calculated here in Part 2: Pipelined datapath.