HW6.3. Datapath Design Part 2: Pipelined

Feel free to check out the guide that we have prepared to help you in this problem.

This question is supposed to be answered after Datapath Design Part 1: Single Cycle

We decide to improve the performance of our CPU by splitting it into 3 stages: Instruction Fetch (IF), Execution (X), and Memory Access (M). Note that this is different from the 5-stage pipeline shown in lecture. The pipelined datapath is shown below. **The blue lines indicate where we decide to make the split, meaning any necessary pipeline registers will be added to the datapath at these locations.**

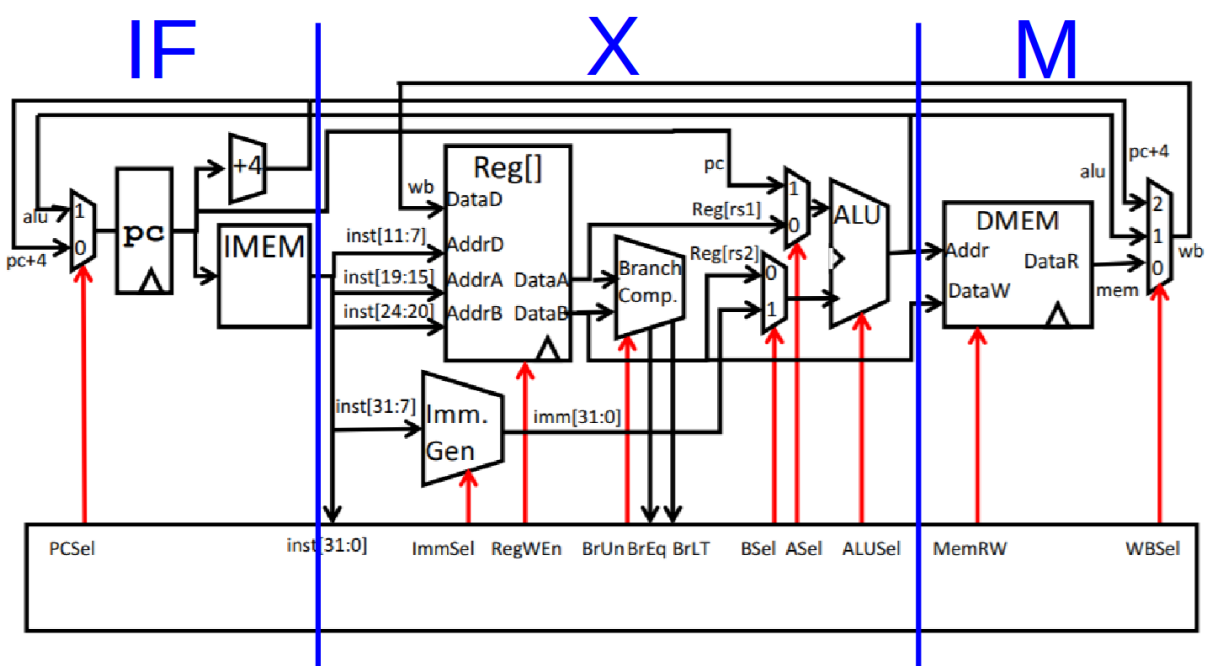
A more detailed description of each stage (Read the descriptions carefully):

IF: the PC is input into the instruction memory and the output is saved in a pipeline register.

X: the instruction is decoded, we read data from the regfile, perform some computation with the ALU, and save any necessary data in pipeline registers. **Note that writing back the ALU output to the PC mux is considered part of the X stage, but there are no pipeline registers separating the ALU output and the PC mux.**

M: data is read/written to memory, and data is potentially written back into the registers. **Note that writing back data from the WB mux output to the Reg File is considered part of the M stage, but there are no pipeline registers separating the WB mux output and the Reg File.**

For this problem, you may assume any control signal is properly handled for all pipeline stages. You can also assume that hazards will not occur.



Assume the following delays for components. Any component not listed is assumed to have a negligible delay. *These are the same numbers from Part 1: Single Cycle.*

Element	Reg clk-to-q	Reg setup	MUX	ALU	MemRead	MemWrite	RegFile Read	RegFile Setup	BranchComp
Parameter	$t_{clk-to-q}$	t_{setup}	t_{mux}	t_{alu}	$t_{mem-read}$	$t_{mem-write}$	$t_{rf-read}$	$t_{rf-setup}$	$t_{branch-comp}$
Delay (ps)	30	20	50	200	250	250	150	20	75

1.1: What instruction type takes the longest to execute given the pipeline stages (i.e. the instruction type that dictates the critical path of the pipelined datapath)?
Hint: Try to find the path with the longest combinational delay in the datapath (you can try to answer 1.2 first), then check which of the instructions listed below utilize that path. The Reference Card might be able to help when identifying the specific instruction traversing a specific path.

- ○ (a) auipc
- ○ (b) R-type ALU Instructions: add, xor, ...
- ○ (c) Branches: beq, bne, ...
- ○ (d) jalr
- ○ (e) jal
- ○ (f) lui
- ○ (g) I-type ALU Instructions: addi, xori, ...

Homework 6

Assessment overview

Total points: 0/100

Score: 0%

Question

Value: 20

History:

Awarded points: 0/20

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

○ (h) Store Instructions: sw, sbu, ...

○ (i) Load Instructions: lb, lw, ...

1.2: For the instruction described in question , which components would be relevant to the critical path calculation?

☐ (a) Pipeline registers between IF and X

☐ (b) Pipeline registers between X and M

☐ (c) PC-MUX

☐ (d) PC register

☐ (e) IMEM

☐ (f) Imm-Gen

☐ (g) RegFile read

☐ (h) Branch Comparator

☐ (i) A-MUX

☐ (j) B-MUX

☐ (k) ALU

☐ (l) DMEM

☐ (m) WB-MUX

☐ (n) RegFile Write

Select all possible options that apply.

1.3: What is the critical path delay (or the minimum operating clock period) of this circuit, in ps?

integer

1.4: What is the fastest clock frequency that can be used with this datapath? Express your answer in GHz.
Take note of the time units

number (3 significant figures)

Recall that latency refers to how long any given instruction takes to finish, while throughput is defined as the number of operations finished per unit time.

1.5: What is the minimum latency of a single instruction, in cycles?
Hint: How many clock cycles does it take to finish 1 instruction?

integer

1.6: What is the minimum latency of a single instruction, in picoseconds?
Hint: The clock period you calculated earlier is the number of seconds per clock cycle.

integer

1.7: What is the maximum throughput, in instructions/cycle?
Hint: Assuming the processor has been executing instructions for a while, how many instructions finish every clock cycle?

number (3 significant figures)

1.8: What is the maximum throughput, in instructions/second?
Hint: Take note of the time units, count the zeroes properly.

number (3 significant figures)

1.9: Based on the above and your answers in Part 1: Single Cycle, what can reasonably be concluded about the advantages of pipelining?

☐ (a) We can increase the clock frequency

☐ (b) We can handle more than one instruction at a time

☐ (c) A single instruction passes through the datapath faster

- [ ] (d) We can finish executing more instructions per cycle

Select all possible options that apply.

Save & Grade *20 attempts left* | Save only | *Additional attempts available with new variants*