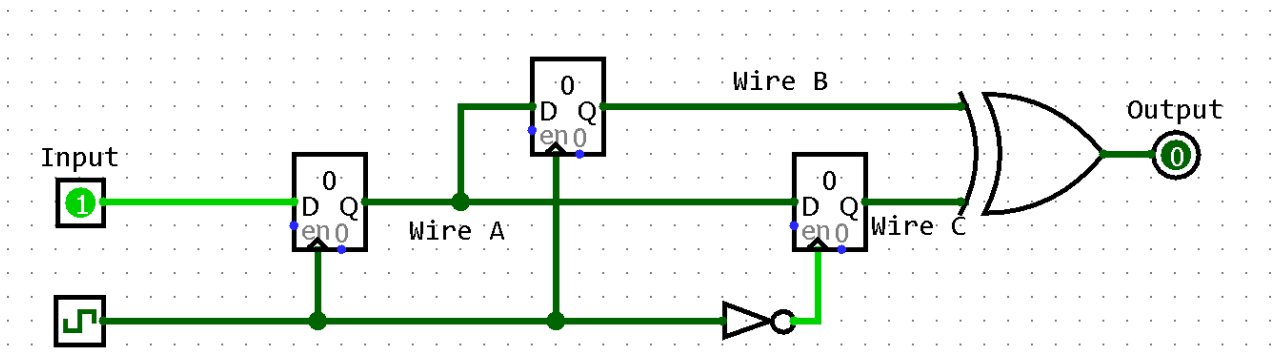
HW5.3. Flipflop Basics and Waveform Diagrams

Feel free to check out the guide that we have prepared to help you in this problem.

Consider the following circuit:



Assume the following:

All register outputs are 0 at time 0.

The clock period is 6 ns. At time 0, the clock changes from 1 to 0 (so the first positive edge is at time 3).

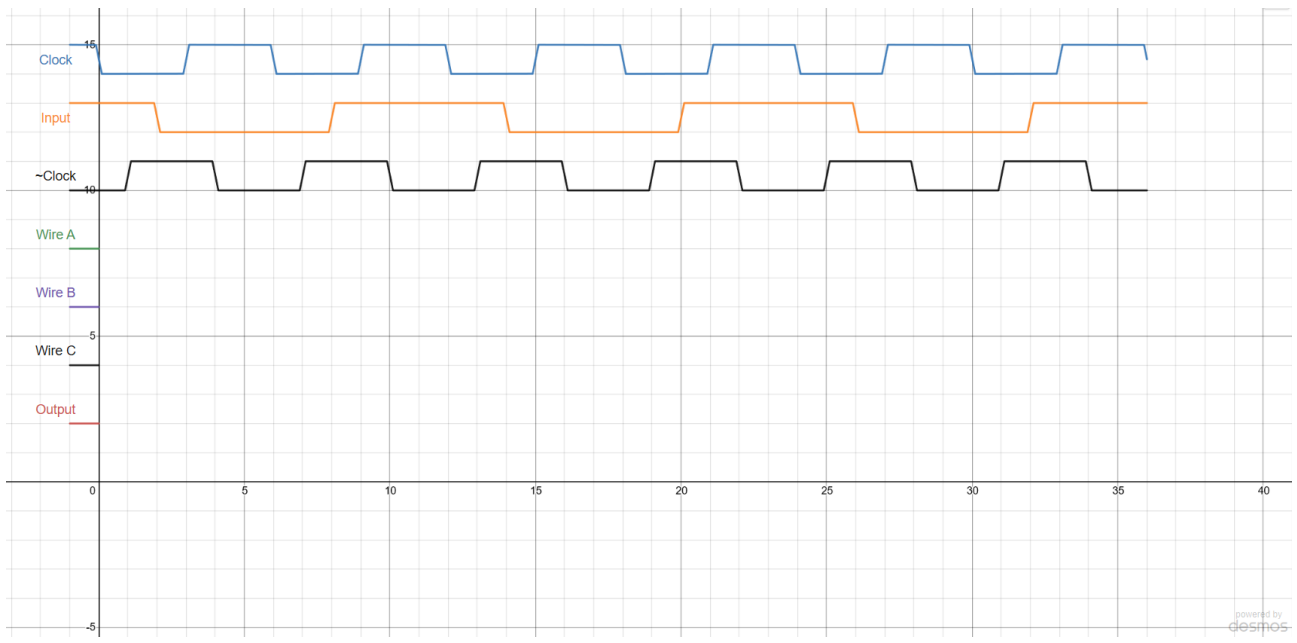
The input toggles (switches back and forth between 0 and 1) every 6 ns, exactly 1 ns before each positive edge.

Each register stores 1 bit. The clk-to-q delay is 2 ns. The setup and hold times are negligible (<1 ns).

The `NOT` and `XOR` gates have propagation delays of 1 ns.

All other components (ex. wires) have negligible delay.

For this problem, we will examine how the circuit behaves within the time range [0,36].



The above is a waveform diagram of the circuit. Complete the waveform diagram. Note that all wires start with a value of 0, as shown in the diagram.

The row for ~Clock is filled in for you. Explanation: At time 0, Clock changes from 1 to 0. Due to the not gate propagation delay, it takes 1 ns for ~Clock to change. Thus, at time 1, ~Clock changes from 0 to 1. Similarly, at time 3, Clock changes from 0 to 1, and thus, at time 4, ~Clock changes from 1 to 0.

Hint: ~Clock is relevant because it is the clock for the rightmost flipflop in the diagram.

As a reminder, registers store a value in "memory", which is continuously outputted at the output port Q. When the clock changes from 0 to 1 (i.e. a positive edge), the register samples the value seen at its input D, and updates the value stored in memory. The clk-to-q delay is the time between the clock positive edge and the time that the Q output gets updated to a new value.

Hint: the flipflop definition above is relevant because combinational logic does not rely on the clock. The combinational logic output changes as its input changes (after some logic delay).

Write all times that the wires toggle (or transition between 0 to 1 or 1 to 0), in order, separated by commas, with no spaces. For example, the answer for ~Clock would be `1,4,7,10,13,16,19,22,25,28,31,34`. Consider only changes that happen between time 0 and time 36 (including toggles that happen at exactly time 36).

Q1.1: Wire A: 1 ? ✕ 0%

Q1.2: Wire B: 1 ? ✕ 0%

Q1.3: Wire C: 1 ? ✕ 0%

Q1.4: Output: 1 ? ✕ 0%

Try a new variant

Correct answer

Feel free to check out the guide that we have prepared to help you in this problem.

Q1.1: Wire A: `11,17,23,29,35`

Q1.2: Wire B: `17,23,29,35`

Q1.3: Wire C: `15,21,27,33`

Q1.4: Output: `16,18,22,24,28,30,34,36`

The full waveform diagram can be found here. Credit to Desmos for making clean waveform diagrams. Note that the transition from 0 to 1 and vice versa is not instantaneous in our diagrams. This is true in real circuits too (it takes some time to transition from high to low voltage), but as in the diagram, the transition time is generally considered negligible.

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