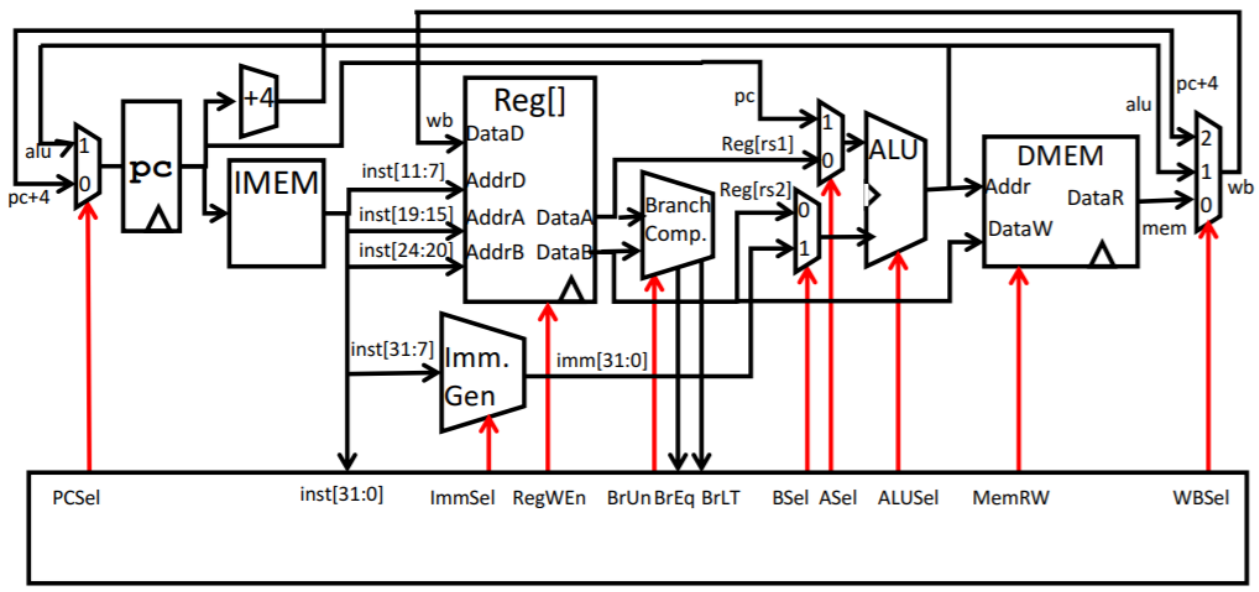
HW6.2. Datapath Design Part 1: Single Cycle

Feel free to check out the guide that we have prepared to help you in this problem.

Below is a copy of the RISC-V datapath presented in lecture:



Assume the following delays for components. Any component not listed is assumed to have a negligible delay.

Element	Reg clk-to-q	Reg setup	MUX	ALU	MemRead	MemWrite	RegFile Read	RegFile Setup	BranchComp
Parameter	$t_{clk-to-q}$	t_{setup}	t_{mux}	t_{alu}	$t_{mem-read}$	$t_{mem-write}$	$t_{rf-read}$	$t_{rf-setup}$	$t_{branch-comp}$
Delay (ps)	30	20	50	200	250	250	150	20	75

1.1: What instruction type takes the longest to execute in this datapath (i.e. the instruction type that dictates the critical path of the datapath)?

- ○ (a) lui
- ○ (b) jalr
- ○ (c) jal
- ○ (d) I-type ALU Instructions: addi, xori, ...
- ○ (e) Load Instructions: lb, lw, ...
- ○ (f) Store Instructions: sw, sbu, ...
- ○ (g) Branches: beq, bne, ...
- ○ (h) R-type ALU Instructions: add, xor, ...
- ○ (i) auipc

1.2: For the instruction that takes longest to execute in this datapath, which components would be relevant to the critical path calculation? (Do not include components that are still used by the instruction but are not on the critical path for the given delays)

- ☐ (a) PC-MUX
- ☐ (b) PC register
- ☐ (c) IMEM
- ☐ (d) Imm-Gen
- ☐ (e) RegFile read
- ☐ (f) Branch Comparator
- ☐ (g) A-MUX
- ☐ (h) B-MUX
- ☐ (i) ALU
- ☐ (j) DMEM
- ☐ (k) WB-MUX
- ☐ (l) RegFile Write

Select all possible options that apply.

1.3: What is the critical path delay (or the minimum operating clock period) of this circuit, in ps?

Homework 6

Assessment overview

Total points: 0/100

Score: 0%

Question

Value: 20

History:

Awarded points: 0/20

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

integer

1.4: What is the fastest clock frequency that can be used with this datapath? Express your answer in GHz.
Take note of the time units

number (3 significant figures)

Recall that latency refers to how long any given instruction takes to finish, while throughput is defined as the number of instructions finished per unit time.

1.5: What is the minimum latency of a single instruction, in cycles?
Hint: How many clock cycles does it take to finish 1 instruction?

integer

1.6: What is the minimum latency of a single instruction, in picoseconds?
Hint: The clock period you calculated earlier is the number of seconds per clock cycle.

integer

1.7: What is the maximum throughput, in instructions/cycle?
Hint: How many instructions finish in 1 clock cycle?

number (3 significant figures)

1.8: What is the maximum throughput, in instructions/second?
Hint: Take note of the time units, count the zeroes properly.

number (3 significant figures)

Take note of your all your answers in this problem (write them down if ever). We'll be drawing some conclusions based on the numbers you calculated here in Part 2: Pipelined datapath.

Save & Grade *20 attempts left* | Save only | *Additional attempts available with new variants*