HW5.4. Common SDS Pitfalls

Feel free to check out the guide that we have prepared to help you in this problem.

As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Also, once you have correctly answered the following questions, spend some time reading the provided explanations to understand the common misconceptions and why they are wrong.

Which of the following statements are true?

☐ (a) The clk-to-q delay of the flipflop changes by changing the clock period.

☑ (b) We can increase the operating clock frequency of the system if we can make the maximum logic delay smaller. ✓

☐ (c) Hold time is the delay of the flipflop after the positive edge of the clock.

☑ (d) Increasing the clock period always solves setup time violations. ✓

☐ (e) The digital circuit can still work reliably even if the hold time requirement is not satisfied.

☐ (f) Increasing the clock period can solve hold time violations.

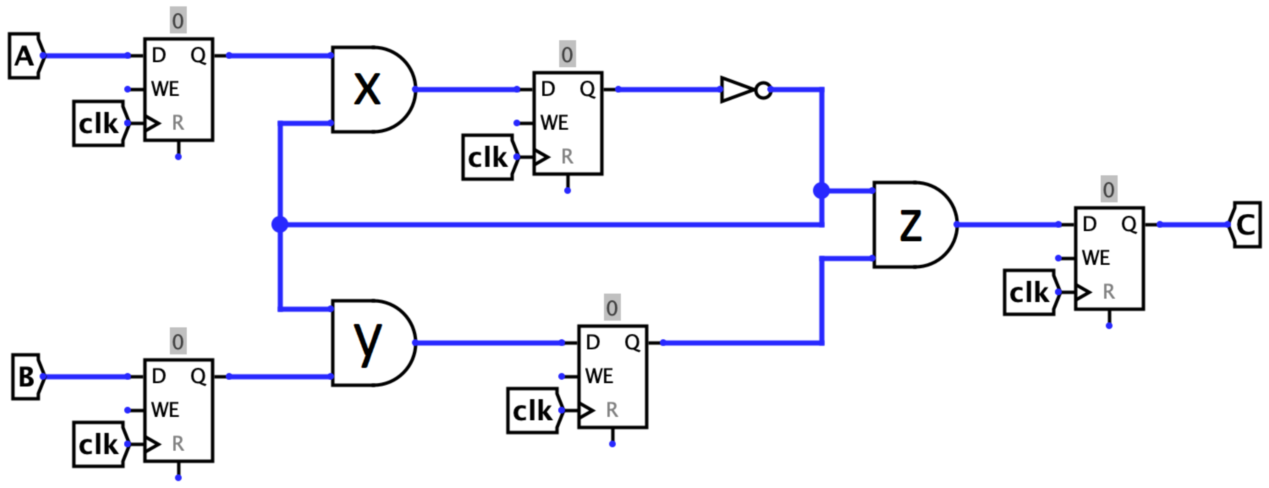
☑ (g) Keeping everything else constant, increasing combinational logic complexity (hence, increasing the delay) can make the entire system fail to work properly. ✓

☑ (h) Setup time is the time needed for the input to be stable before the positive edge of the clock. ✓

Select all possible options that apply. ?

✓ 100%

Suppose we have the following digital circuit:



Assume the following:

You can safely ignore inputs A and B, and output C for this problem.

You can ignore the R and WE ports in the flipflops. Those are not relevant to this problem.

The delays of the AND gates (x, y, z) are identical.

The delay of the NOT gate is the same as the AND gate delay.

All flipflops are connected to the same clock.

All flipflops are identical to each other (i.e. they have the same clock-to-q delays, setup times, and hold times).

Homework 5

Assessment overview

Total points:	100/100
Score:	100%

Question

Value:	5
History:	5 5
Awarded points:	5/5

Report an error in this question

Previous question

Next question

Attached files

No attached files

Attach a file

Attach text

Select <u>all valid inequalities</u> that can be used if we want to calculate for the minimum clock period for the system.

You want to consider the <u>longest combinational path delay</u> to get the minimum clock period.

Hint: Try tracing out the path that is being described by the delay summation and see if those paths makes sense.

□ (a) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☑ (b) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

□ (c) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{setup}} + t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} + t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☑ (d) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

□ (e) $t_{\text{clk-to-q}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

□ (f) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

□ (g) $t_{\text{clk-to-q}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

□ (h) $t_{\text{clk-to-q}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$

☑ (i) $t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

Select all possible options that apply. ?

✓ 100%

Try a new variant

Correct answer

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As a reminder for the following questions, a circuit must fulfill the following conditions in order to exhibit consistently correct behavior:

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Also, once you have correctly answered the following questions, spend some time reading the provided explanations to understand the common misconceptions and why they are wrong.

Which of the following statements are true?

(b) We can increase the operating clock frequency of the system if we can make the maximum logic delay smaller.
(d) Increasing the clock period always solves setup time violations.
(g) Keeping everything else constant, increasing combinational logic complexity (hence, increasing the delay) can make the entire system fail to work properly.
(h) Setup time is the time needed for the input to be stable before the positive edge of the clock.

Increasing the clock period always solves setup time violations. This is true. increasing the clock period gives more margin for the setup time to be satisfied.

We can increase the operating clock frequency of the system if we can make the maximum logic delay smaller. This is true. Decreasing the maximum logic delay allows us to decrease the clock period without violating setup time, thus increasing the clock frequency.

Setup time is the time needed for the input to be stable before the positive edge of the clock. This is true. This is the exact definition of setup time.

Keeping everything else constant, increasing combinational logic complexity (hence, increasing the delay) can make the entire system fail to work properly. This is true. If the maximum logic delay increases, then we might end up violating the setup time if the clock period is fixed.

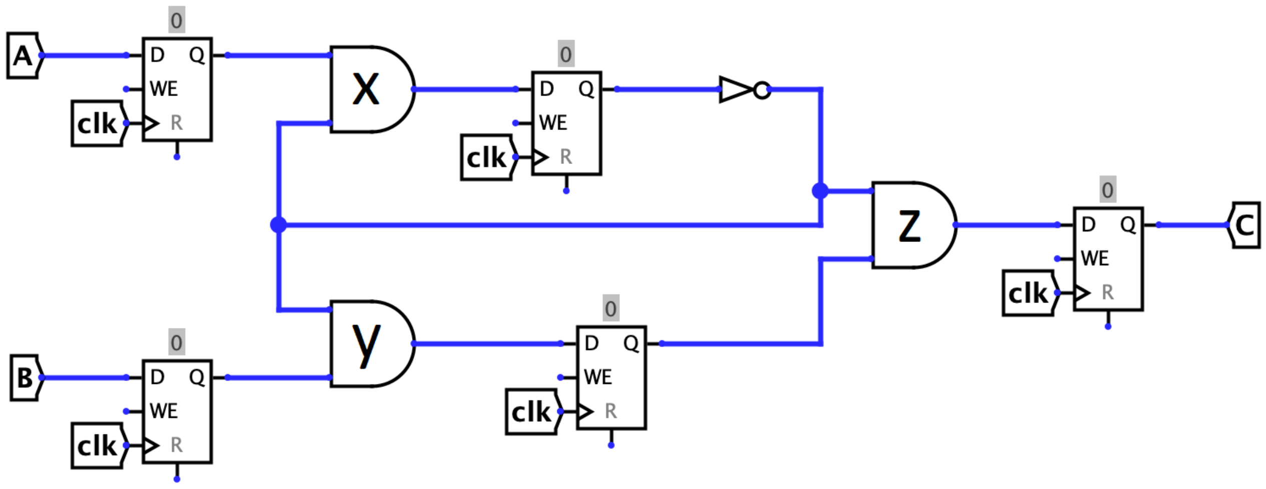
Hold time is the delay of the flipflop after the positive edge of the clock. This is false. Hold time is not a delay, it is a timing requirement. The flipflop propagation delay is called the clock-to-q delay.

Increasing the clock period can solve hold time violations. This is false. If you look at the inequalities given above, the clock period does not have any relation whatsoever with the hold time. Those are two different inequalities.

The digital circuit can still work reliably even if the hold time requirement is not satisfied. This is false. The two inequalities must both be satisfied for a digital circuit to exhibit consistently correct behavior.

The clk-to-q delay of the flipflop changes by changing the clock period. This is false. The clk-to-q delay of a flipflop is an inherent property of the flipflop itself. External inputs, such as the clock, will not change any inherent flipflop property (setup and hold time included).

Suppose we have the following digital circuit:



Assume the following:

You can safely ignore inputs A and B, and output C for this problem.

You can ignore the R and WE ports in the flipflops. Those are not relevant to this problem.

The delays of the AND gates (x, y, z) are identical.

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All flipflops are connected to the same clock.

All flipflops are identical to each other (i.e. they have the same clock-to-q delays, setup times, and hold times).

Select all valid inequalities that can be used if we want to calculate for the minimum clock period for the system.

You want to consider the longest combinational path delay to get the minimum clock period.

Hint: Try tracing out the path that is being described by the delay summation and see if those paths makes sense.

(b)

$$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

(d)

$$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

(i)

$$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

The longest combinational delay is almost always the path that passes through as many logic gates as possible between two flipflops. Sometimes, there will be explicit inputs to the system, such as the inputs A and B for this problem, but they are usually described as synchronous to the clock (meaning, you can actually treat them as flipflops as well). Take care when identifying the longest paths though, as some logic gates might have significantly larger delay than others, which makes it the path with the longest delay, even if that path does not go through many logic gates.

A common misconception when calculating for the minimum clock period is to consider the paths that *go through* the flipflops. These are not valid paths. Remember that flipflops require the positive edge of the clock to transfer the input to its output, that's why the flipflop propagation delay is called "clock to q". Delay calculations always start from the output of a flipflop (or an input that is synchronized to the clock) and ends at the input of a flipflop (or an output that is synchronized to the clock). Therefore, the delay summation should always start with the clk-to-q delay + any combinational logic path + setup time of the receiving flipflop. The clk-to-q delay should only appear once in the sum (at the start). Same goes for the setup time (at the end of the sum). **Delay calculations should not go through a flipflop**; the flipflop is technically blocking the delay propagation as it waits for the next positive edge of the clock.

Submitted answer 2 correct: 100%

Submitted at 2022-10-21 00:05:02 (PDT)

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✓ 100%

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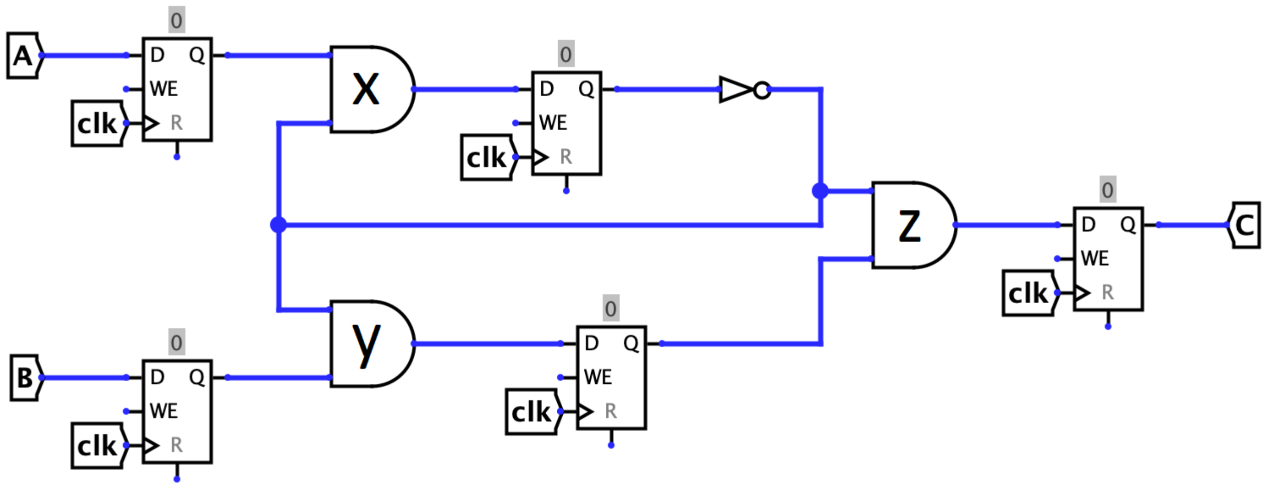

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(b)

$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-z}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

(d)

$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-x}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

(i)

$t_{\text{clk-to-q}} + t_{\text{NOT}} + t_{\text{AND-y}} + t_{\text{setup}} \leq t_{\text{clk-period}}$ ✓

✓ 100%

Submitted answer 1 incorrect: 0%

Submitted at 2022-10-21 00:04:45 (PDT)

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