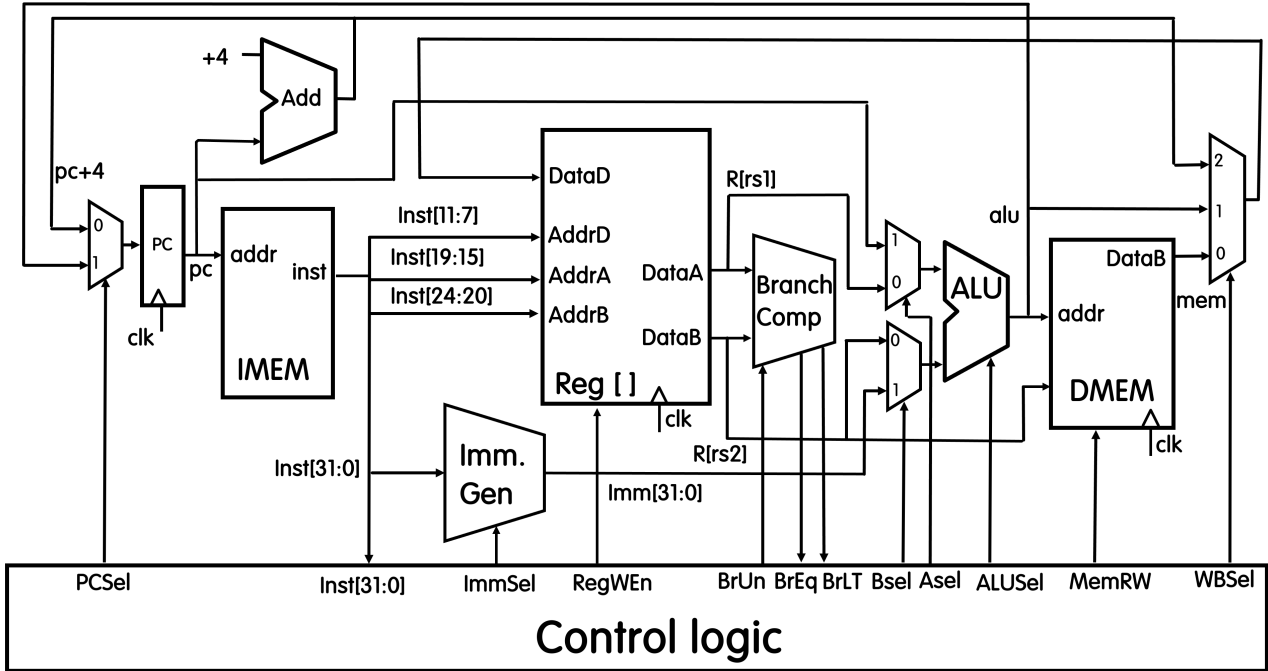## HW6.5. Supporting new instructions

The datapath below implements the RV32I instruction set.

Specify whether the following proposed instructions can be implemented using this datapath **without modifications** (That is, you can only change the control signals, but the datapath connections remain the same). If the instruction can be implemented, specify what the control signal should be (either 0 or 1). If the control signal corresponds to a multiplexer select signal, check the datapath provided earlier to see which data the multiplexer will be selecting (note the data going into the 0 and 1 inputs of the mux). If the instruction is not implementable, write "No" in the implementable column and "N/A" in the Control Signals column.

Example:

Instruction	Description	Implementable?	Control Signals
Add `add rd, r1, rs2`	`rd = rs1 + rs2`	Yes	PCSel = 0 WBSel = 1

Instruction	Description	Implementable?	Control Signals
Register offset load `lwreg rd, rs1, rs2`	`rd = 4 bytes of memory starting at address (rs1 + rs2)`	⬜ ❓	ASel = ⬜ ❓ BSel = ⬜ ❓
beq with writeback `beq rd, rs1, rs2, label`	`rd = rs1 + rs2 if (rs1 == rs2){ PC = PC + offset}`	⬜ ❓	WBSel = ⬜ ❓ PCSel = ⬜ ❓
PC-relative load `lwpc rd, imm`	`rd = 4 bytes of memory starting at address (PC + imm)`	⬜ ❓	ASel = ⬜ ❓ BSel = ⬜ ❓

Homework 6

Assessment overview

Total points: 0/100

Score: 0%

Question

Value: 15

History:

Awarded points: 0/15

Report an error in this question ▾

Attached files

No attached files

Attach a file ▾

Attach text ▾

| Load word with add

`lwadd rd, rs1, rs2, imm` | rd = (4 bytes at memory address (rs1 + imm)) + rs2. M[rs1 + imm] + rs2 | [input] ? | RegWEn =
 [input] ?

 WBSel =
 [input] ? |