

Realization of a Wireless Transmission System

Abstract—This report goes over the designing and building process of a wireless transmission system working at 400MHz. More specifically, the design includes a Colpitts oscillator, class C amplifiers and a Yagi-Uda antenna. Although, the design works in simulations, due to a poor realization of the circuitry, the expected functionality and performance of the design was not achieved in practice.

I. INTRODUCTION

Wireless transmission systems are among the important foundations of modern technology. While the transmission circuit converts data into a signal, the antenna propagates it in radio waves, with the effectiveness reliant on the particular design choices.

In this report, the electronics and electrodynamics theory is applied in practice to design and build a wireless transmission system. It poses the question as to what design choices fit the best for both the antenna and electronics circuit, alongside the ability to manufacture such a system for it to operate in its desired functionality.

Section II will explain the overarching design goals, section III will look into the Electronics stage of the system, Section IV is about the Antenna, while Section V will illustrate the functionality of the system when combined. For each of the sections, the theory involved, simulations, realization and results will be examined and discussed.

II. OVERALL DESIGN

A. Stage Block diagrams

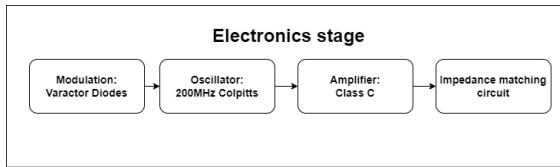


Fig. 1. Block diagram of Electronics stage.

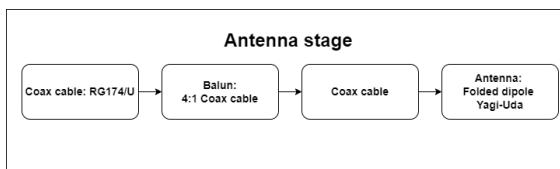


Fig. 2. Block diagram of Antenna stage.

B. Design Goals

Aside from the project requirements, there are specifications that we are aiming for:

- 1) 400MHz frequency.
- 2) Maximize power transfer efficiency: $RL(dB) < -20dB$ at 400MHz.
- 3) $\approx 200\Omega$ antenna input impedance.

For 400MHz, a Colpitts oscillator can be used for the electronics and the lengths of the antenna elements will determine its resonant frequency

III. ELECTRONICS

A. Theory

The electronics design consists of two core components of the overall wireless transmission system. The oscillator is responsible in creating a carrier frequency in the desired frequency for the information signal modulation, and a power amplifier alongside impedance matching circuits to deliver as much power as possible for the transmission.

a) *Oscillator*: The chosen mode of modulation is Frequency Modulation (FM), in which the voltage (amplitude) of the input signal will control a frequency offset in the output signal. This offset is targeted to be ± 150 KHz, as shown (in an exaggerated manner) in figure 3. The mode is chosen due to its capability to provide a better signal quality and a resistance towards noise interference [1].

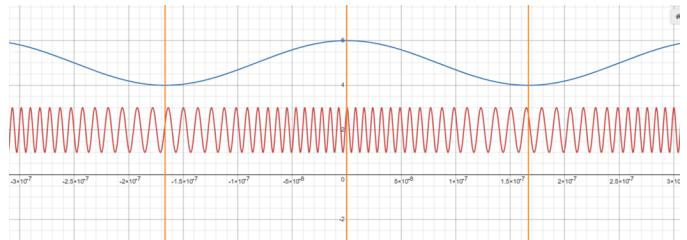


Fig. 3. Frequency Modulation (FM)

The complete oscillator circuit is shown in figure 4. The circuit can be separated into two core components for it to operate at the desire frequency, the main Colpitts oscillator, operating at 200 MHz and the class C amplifier, amplifying the first 400 MHz harmonic.

The design used a tuned LC-tank circuit and a capacitive voltage divider as the feedback source. One of the main advantages of this design is that it minimize the self and mutual inductance effect within the tank circuit, this further improves the frequency output stability [2].

However, when we take a closer look at the oscillator circuit on its own in Fig. 5, $+V$ of the output is connected to the LC-tank of the oscillator circuit creating an additional

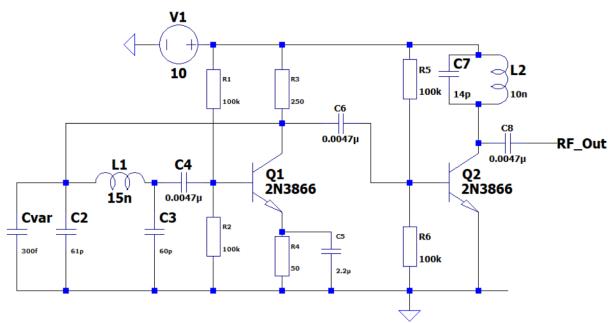


Fig. 4. Complete Oscillator Circuit with Class C Amplifier

node at the LC-tank. This makes the large signal analyses impractical be used to directly determine oscillation frequency. Therefore, small signal analysis has to be attempted in order to determine the oscillation frequency.

Unlike the large signal analysis, small signal analysis can not analyse the behavior of the circuit during a full oscillation when it is stable. However it can still give us an insight on the initialization of the oscillation at the very beginning.

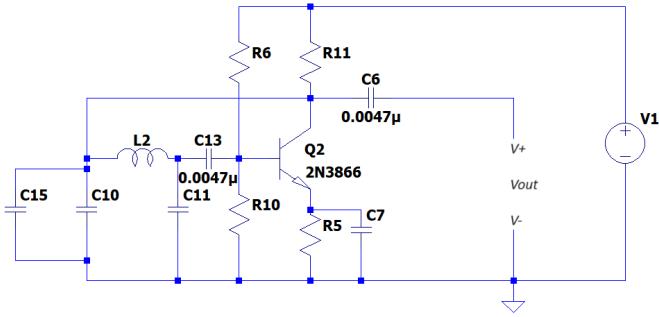


Fig. 5. Oscillator Circuit

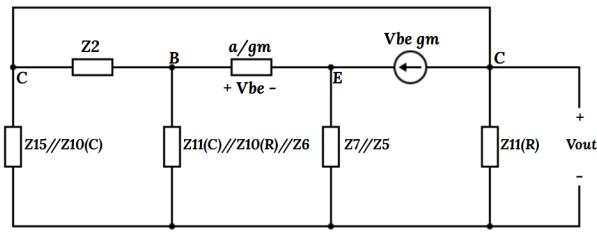


Fig. 6. SSEC of the Oscillator Circuit

As can be seen in the SSEC design of the Oscillator circuit (Fig. 6), the far left node is also labeled the same as the collector and that's because there is a short at the very top of the circuit that connects and merges them together. Also the two identical coupling capacitors are shorted. (Fig. 5)

The circuit (Fig. 6) is virtually cut at V_{be} in order to get a response at V_{be} from the initial voltage across V_{be} . Thus, the loop gain equation of the SSEC is going to be

$$A_{loop} = \frac{V_B - V_E}{V_{be}} \quad (1)$$

By applying Kirchhoff's Current Law at every node of the circuit, the node voltage theorem is correctly applied to determine the loop gain of SSEC.

$$Z_K = Z_{11(R)} // Z_{10(C)} // Z_{15} \quad (2)$$

$$Z_L = Z_{11(C)} // Z_{10(R)} // Z_6 \quad (3)$$

$$Z_M = Z_5 // Z_7 \quad (4)$$

KCL at Node C:

$$I_c + \frac{V_C}{Z_K} + \frac{V_C - V_B}{Z_2} = 0 \quad (5)$$

KCL at Node B:

$$\frac{V_B - V_C}{Z_2} + \frac{V_B}{Z_L} + I_b = 0 \quad (6)$$

KCL at Node E:

$$-I_b + \frac{V_E}{Z_M} - I_c = 0 \quad (7)$$

where $I_c = g_m \cdot V_{be}$ and $I_c = a \cdot I_b$

After solving for nodes V_B and V_E and substituting them into the loop gain equation, the loop gain is obtained as:

$$A_{loop} = -g_m \left(\frac{1 + \frac{1}{a} + \frac{Z_2}{a \cdot Z_K}}{\frac{2}{Z_L} + \frac{Z_2}{Z_L \cdot Z_K}} - \left(1 + \frac{1}{a} \right) Z_M \right) \quad (8)$$

where the impedance's are defined as:

$$Z_2 = jwL_2 \quad Z_5 = R_5$$

$$Z_6 = R_6 \quad Z_7 = \frac{1}{jwC_7}$$

$$Z_{10(R)} = R_{10} \quad Z_{10(C)} = \frac{1}{jwC_{10}}$$

$$Z_{11(R)} = R_{11} \quad Z_{11(C)} = \frac{1}{jwC_{11}}$$

$$Z_{15} = \frac{1}{jwC_{15}}$$

By substituting the impedance's into the loop gain equation, simplifying the resultant loop gain equation and canceling out the imaginary parts of the final version of the loop gain along with further rigorous algebraic manipulations, the oscillation frequency is obtained as given below in Fig. 7

$$\omega = \sqrt{\frac{2C_{11} + \left(\frac{1}{a} + 1\right) \frac{R_5^2 C_7}{1 + (\omega R_5 C_7)^2}}{\frac{L_2 C_{10}(C_{15} R_{11} + C_{10} R_{11})}{a R_{11}} - \frac{L_2 C_{10}(C_{15} R_{11} + C_{10} R_{11})}{R_{10} R_6 R_{11}}}}$$

$$f = \frac{\omega}{2\pi}$$

Fig. 7. Oscillation Frequency of Oscillator Circuit

In the LTSpice design shown in Figure 4 C_{var} shown as another capacitor, in truth the variable capacitor consists of two varactor diodes that change its capacitance value dependent on its voltage input. The variable capacitor circuit design is shown in further detail in Figure 8. The input to this varactor configuration comes from a tuned audio (or other information) source, like the AD2. This will cause a difference

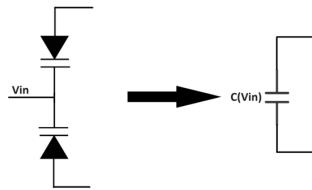


Fig. 8. Circuit design of the variable capacitor

in capacitance in the loop, causing a frequency shift depending on input amplitude: FM.

The oscillation frequency equation from Fig. 7 shows that the main oscillator component can only have an oscillation frequency of 236 MHz while staying within reasonable component values, in which it is way below the system desired operating frequency. Despite the change of value in C10 and C11 (from Fig. 5) to satisfy the equation, the maximum achievable simulated oscillation frequency can only go up to 337 MHz. After rigorous design consideration and analysis, the circuit's Fast Fourier Transform (FFT) in figure 9 shows that a higher harmonic occurs at the system's desired frequency of 400 MHz.

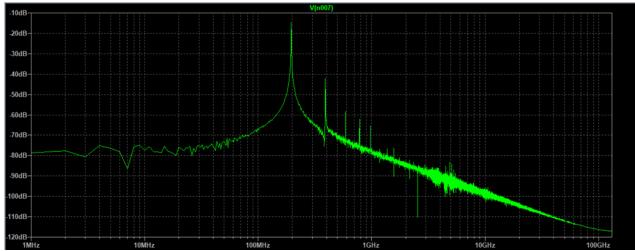


Fig. 9. FFT of the Colpitts oscillator circuit

The general idea is to isolate and amplify the circuit's first harmonic at the system's desired frequency of 400 MHz. This can be achieved with the help of an amplifier that can operate in high frequency and has a very narrow bandwidth of operation. Research shows that out of all types of amplifier, Class C amplifiers have a very narrow bandwidth that only allows the current to flow when its frequency is equal to the resonance frequency of the tank[3].

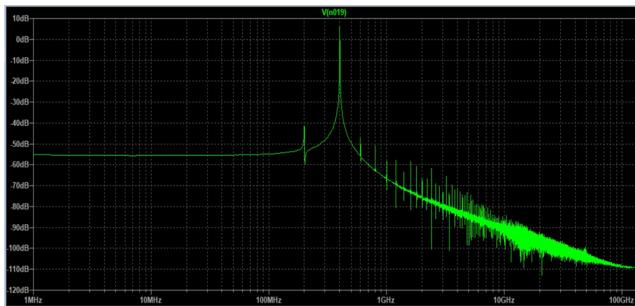


Fig. 10. FFT of the complete oscillator circuit

Figure 10 shows the success of the prior theory. The complete oscillator now operates at the desired frequency of 400 MHz. The additional class C amplifier stage plays a

crucial part in both attaining the desired frequency, but also to dampen any unwanted harmonics, before the output of the oscillator circuit is connected to the power amplifier.

b) Power Amplifier: The output of the oscillator circuit is acting as the input for the power amplifier. The main function is to amplify the power with the highest possible gain and deliver maximum power output for the antenna to reach its peak transmission distance. Whilst the design took into consideration the creativity to create a unique amplifier design, the main concern is to deliver as much power as possible. Therefore, the final design chosen is the one that has the highest power gain compared to other amplifier designs that have been discontinued and that will not be mentioned. The final proposed design of the amplifier can be seen in figure 11

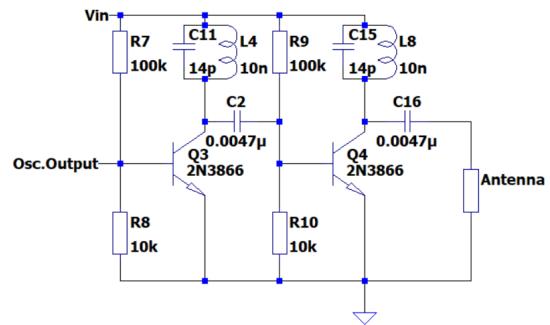


Fig. 11. The power amplifier design

The final amplifier design consists of two class C amplifiers. An advantage of the class C amplifier is its easy scalability, as stacking class C amplifiers in series is commonly used in a few other applications.[4] It allows the team to compare the results based on the total amplifier stages used. Thus, it is possible to choose the total amplifier stages used. Other than performance, the issue of the additional cost for another stage of the amplifier is taken into consideration. After three amplifier stages, it is concluded that the gain provided with another stage was not worth the additional cost and parasitic effect. Another reason is that the class C amplifier is mentioned to be one of the best choices in terms of efficiency and its suitability to operate in high frequency. Class C amplifiers have a practical efficiency as high as 85%, and it is mentioned to have a considerably low power loss in the power transistors [5].

The resonance frequency of the tank can be calculated with equation 9. Other than its function as a narrow harmonic filter, the LC tank stores magnetic energy within the inductor and electric energy within the capacitor. This stored energy contributes to increasing the efficiency of the overall class C amplifier by reducing the power dissipated by the transistor and maintaining the oscillation and providing a better output signal.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad (9)$$

To achieve maximum power delivered into the antenna, it is necessary for the impedance of the oscillator's output to be the complex conjugate of the power amplifier's input. As the power output calculation shown in equation 10, with R_s the input impedance and R_L as output impedance. In the case of $R_s = R_L^*$, the equation reduces to equation 11 as the imaginary components in the denominator cancels out. With these theorems in mind, it is necessary to implement a circuit to match these impedances to prevent big power losses between the stages.

$$P_L = \frac{V^2 R_L}{(R_s + R_L)^2} \quad (10)$$

$$P_{max} = \frac{V^2}{4R_L} \quad (11)$$

The circuit design shown in figure 12 is intended to match the source impedance to the load impedance. In comparison to other matching circuits such as the L-type circuit, the π -type and T-type are deemed the most suitable for operating in a narrow bandwidth and with a high Q component [6].

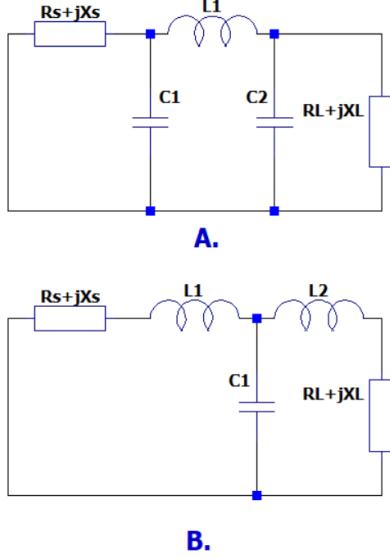


Fig. 12. Impedance matching circuits A. π -type circuit, B. T-type circuit

The input impedance $R_s + jX_s$ will be tempered by the impedances of the capacitors and inductors to match the load impedance $R_L + jX_L$. The calculations are as shown in equation 12 for the π -type circuit, and equation 13 for T-type circuit.

$$Z_{In} = \left\{ \left[(R_L + jX_L) // \frac{1}{j\omega C_2} \right] + j\omega L_1 \right\} // j\omega C_1 \quad (12)$$

$$Z_{In} = \left[(R_L + jX_L + j\omega L_2) // \frac{1}{j\omega C_1} \right] + j\omega L_1 \quad (13)$$

LTspice is used to simulate each of the input and output impedances for every stage, to provide more exact measurements, as shown in figure 14 in section III-B. The simulated

value is then used in the calculation to create the necessary circuit for maximizing power delivery. The final amplifier circuit alongside its impedance matching system is shown in figure 13

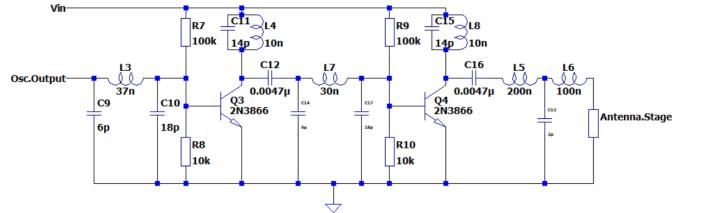


Fig. 13. Complete power amplifier circuit

The choices of determining between π -type and T-type is based on the load that is intended to match. In the case of matching to a high ohmic load ($R_L > 100\Omega$), it is recommended to utilize π -type circuit and the T-type is recommended in the case of matching to a low ohmic load ($R_L < 100\Omega$). [6]

B. Simulation

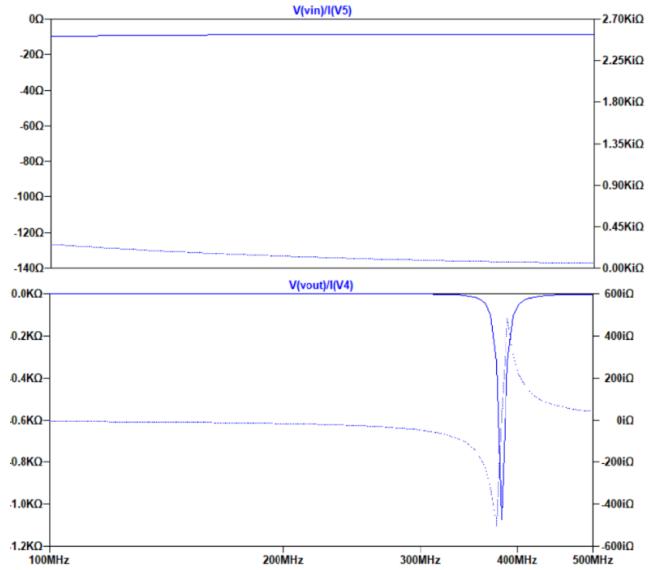


Fig. 14. LTspice simulation of output and input impedances

The final circuit is shown in figure 15 with the oscillator's output signal operating as the power amplifier's input signal alongside the impedance matching circuit in between each stage to maximize power transmission. The output load is a 50Ω resistor to simulate the desired connector impedance to the antenna. The results of each simulation shown in this section took the parasitic effects at high frequency into consideration for capacitors, inductors, resistors and transistors.

The output voltage and current are shown in figure 16 alongside the power input to the amplifier stage and the expected power output on the 50Ω load. The simulations show a smooth sine wave of 2 V and a 40 mA current peak-to-peak, the simulated power input shows an average power of 6.75 mW, and the expected power output of the whole

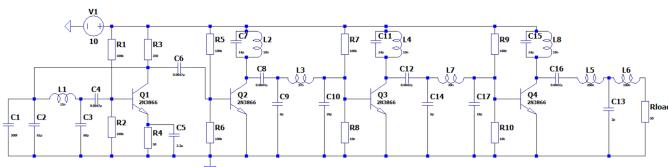


Fig. 15. Finalized electronic circuit

electronics circuit shows an average of 39.431 mW. Based on the simulation results, the amplifier stage is capable of amplifying the power input with an amplification factor of 5.84.

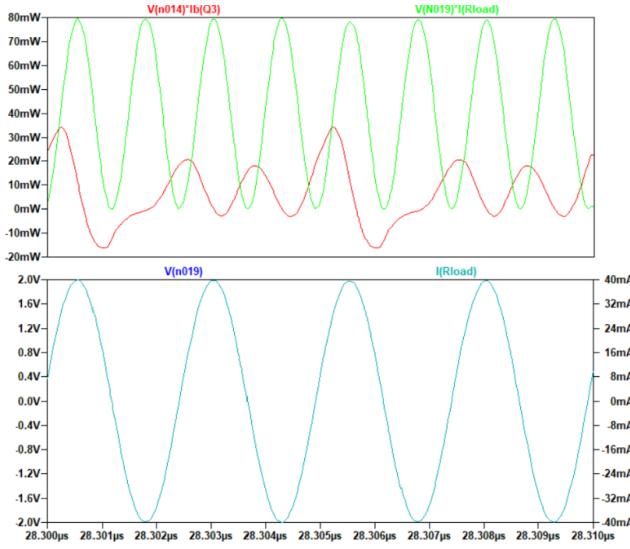


Fig. 16. Power prior to the amplifier stage (red), power delivered to a $50\ \Omega$ load (green), the output voltage and output current of the electronics circuit.

C. Realization

The electronics circuit creation involves the use of the KiCAD software tool to design the PCB layout. The final design utilizes the 2N3866 for all the BJTs and a variable capacitance diode BB857. Other components are chosen with the capability and impedance provided in high frequency alongside the overall price of the manufacturing process. The final circuit produced is shown in figure 17.

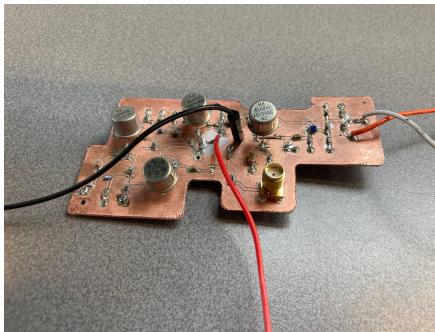


Fig. 17. Realization of the electronics circuit

D. Results and Discussion

Figure 18 represents the output of the manufactured circuit. The circuit's output is a long way from the theoretically expected output, as the manufacturing process suffers from many mistakes that will be further discussed.



Fig. 18. Output of the manufactured circuit

Early on in the realization, many easy-to-avoid mistakes were made, such as exaggerated use of solder and causing tear damage to the pads. Due to only having one PCB available, all these mistakes need to be worked around later on. After further learning and adapting to surface-mount soldering, these mistakes are less common. Therefore, it is possible to minimise the problem in the event of the achievement of another PCB. Unfortunately, this is not the case, and the already damaged PCB and their workarounds greatly increased the circuit parasitic effect.

Other issues occur due to components that were lost or destroyed during construction, including a 4.7nF capacitor and multiple $100k\Omega$ resistors. In an attempt to solve this issue, the team decided to use other available components, in which these inaccurate component values create further problems for the circuit. Lastly, the biggest problem that was faced, was not an easily avoidable one. The transistors that were used, the 2N3866, were very old, with the ones in the final circuit being created in 1985, 1989 and 1992. However, the data sheet used was for a later model, where the collector-emitter direction was reversed. This was not obvious, as it was mentioned nowhere that there were older models.

Due to the unexpected fault lying in the data sheet, the attempt to identify and solve the issue took multiple days of problem solving, resulting in further damaged PCB and oddly soldered transistors, because they were required to be mirrored. In addition to the time lost in problem solving, the soldered solution created more parasitic losses for the system.

Due to a combination of all these problems, it was not possible to create a circuit that oscillated at 400 MHz, with the output being a combination of two lower frequency (about 60 MHz and 120 MHz) signals.

In conclusion, the electronics of our wireless transmission system worked well in simulation. Including parasitic impedances, the design was able to output 39.431 mW of power. Unfortunately, a combination of very small components and

lack of experience led to the PCB being badly soldered and so, very difficult to debug. In the end, we were not able to accomplish the goal's set for the electronics in practice.

IV. ANTENNA

A. Theory

Due to the size constraint and polarization limitations, being $1m^3$ and linear respectively, the antenna design choices have been reduced to the Yagi-Uda antenna. The Yagi-Uda antenna was modified by adding a folded dipole instead of a half wave dipole and a corner reflector. Moreover, a folded dipole increases the antenna's input impedance to reach the 200Ω goal. To improve power transfer efficiency, a balun is implemented to match the impedances of the coax cable and the antenna.

a) Balun: Based on the materials we have access to, the balun can be made by using a transformer or a coax cable. The main advantage of the transformer balun is that its ratio has a greater range compared to the coax balun, at the cost of requiring a ferrite core and precise coil turns. The coax cable balun was chosen as it can be made of any available coax cable and since its ratio begins at 4:1, the exact ratio we need to match a 50Ω coax cable with a 200Ω antenna. Moreover, this type of balun is designed for single band antenna's, which also matches with the yagi design.



Fig. 19. Coax cable balun schematic, conducting core of one end of balun connects into feedline core and all the ground shieldings are connected.

The schematic of the balun design shows that the output of the coax is increased to two. Using the power formula shown in Equation 14, the balun ratio can be found by equating power in with power out.

$$P_{in} = \frac{(V)^2}{Z_{in}}, P_{out} = \frac{(2V)^2}{Z_{out}} \quad (14)$$

$$Z_{out} = 4Z_{in} \Rightarrow 1 : 4 \quad (15)$$

The folded dipole is balanced while the feedline is unbalanced. Therefore, the balun not only creates a balanced output but also tries to make the output signal's in phase by shifting the signal going to one half by 180° if its length is equal to $\frac{1}{2}\lambda$ [7]. The length of the balun can be determined using Equation 14.

$$\text{Length} = \frac{(c)(v.f.)}{2(f)} \quad (16)$$

where c is the speed of light, v.f. being the coax cable's velocity factor, and f the target frequency. Using a velocity

factor of 0.66 found in the datasheet [8], the length of the balun is calculated to be $\approx 0.25\text{m}$.

b) Yagi-Uda: To reduce the antenna's power output losses, a linearly polarized antenna was chosen to match the linearly polarized receiver antenna. The antenna will have one active element, with the rest being passive elements. The spacing between and the size of each element is proportional to the wavelength of the target frequency of 400MHz. Yagi-Uda antennas are designed for the radiated waves to constructively interfere with the director elements and destructively interfere at the back with the reflector [9]. The reflector and director elements will be longer and shorter than the driven element and so will have an inductive and capacitive reactance respectively.

To achieve an antenna input impedance of 200Ω , varying the spacing between the elements should change the antenna's reactance and so, its impedance[10].

B. Simulation

a) Balun: To observe and tune the 4:1 balun's performance, a 200Ω resistor was used to model the antenna's input impedance.

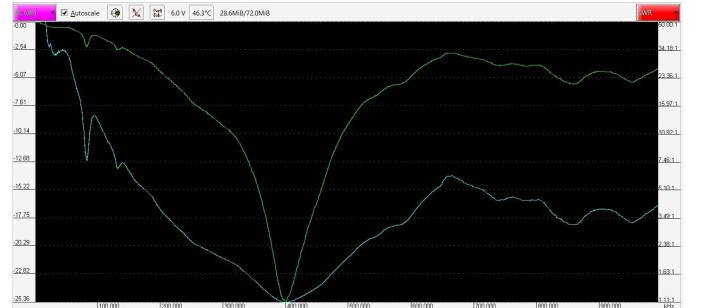


Fig. 20. Return loss (Green) and SWR (Blue) measurement of Balun using 200Ω resistor.

Measurement	Value
Return Loss (dB)	-25.36
SWR	1.11:1
Frequency (Hz)	401.7 MHz
$ Z (\Omega)$	49.6

TABLE I
MEASUREMENTS TAKEN FROM RESONANT FREQUENCY SHOWN IN FIGURE 20.

Figure 20 illustrates the RL and SWR graphs of the balun using a VNA under a frequency sweep from 1Hz to 1GHz and Table I shows the measurements at the resonant frequency peak of 401.7MHz.

It was observed that the RL and SWR can be further reduced by using coax cables to connect the balun to the antenna and reducing the space between the two, shown in Figure 21 as the cables wrapped in white electrical tape. This is expected as making the space smaller reduces power losses through mutual inductance between the cables and the coax reduces EM losses.



Fig. 21. Constructed 4:1 coax cable balun using RG174/U.

b) Yagi-Uda: The 4nec2 software was used to simulate the antenna. The final design choices were mainly based on the simulations. The simulations were performed in ideal conditions. This means that the antenna was simulated in free space with the conductivity of copper for the elements. The reasoning behind this is that if an antenna works better in ideal conditions it will also work better in real conditions. After the final design was determined this was simulated with realistic conditions.

There are three scenario's that will be discussed. First the spacing between the elements was changed from the 'old' spacing to the 'new' spacing (Fig. 22), which increased the gain. After that the angle between the plates was changed from 90 degrees to 60 degrees, which reduced the imaginary component of the impedance. Finally the plates were made smaller based on the theory behind it, however the gain and resistance of the antenna dropped, thus the bigger plates were used in the final design.[11] The gain and impedance results of these different situations can be seen in table II.

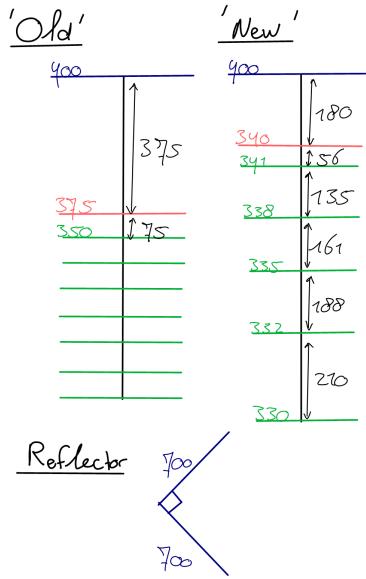


Fig. 22. The old dimensions (left)[12] versus the new dimensions (right)[13] and the dimensions of the reflector, which is the same for both cases[11], measurements in mm.

For the final simulation the antenna was placed in the position it is going to be when testing. The conducting material was changed from copper to aluminium. And finally instead

Situation	Gain (dBi)	Impedance (Ω)
Old spacing	7.89	$37.8 + j234$
New spacing (with 45 degrees)	11.3	$279 - j196$
New spacing with 30 degrees	11.5	$312 + j76.4$
Reduced reflector plates	9.32	$39.5 + j88.6$

TABLE II
THE SIMULATED GAIN AND IMPEDANCE OF DIFFERENT SITUATIONS

of in free space the antenna is simulated with the real ground setting. This leads to the output below in figure 23 and 24. This leads to a final maximum gain of 10.3 dBi at a 65 degree angle. The impedance is $67.1 + j107$. Thus the goal of 200Ω was not met. The reason for this is that there were still mistakes in the simulations, that were only fixed after the antenna was already built.

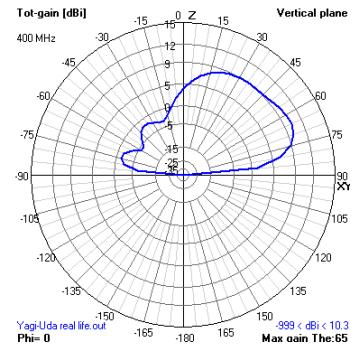


Fig. 23. Polar plot of the vertical plane of the final simulation

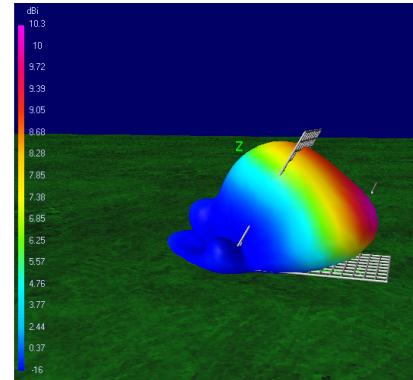


Fig. 24. Radiation pattern of the final simulation

C. Realization

a) Balun: Figure 25 shows the frequency sweep from 1Hz to 1GHz using a vna upon connecting the balun to the folded dipole antenna and Table III gives the measurement values at the resonant frequency of 402.6 MHz. These measurements verifies the functionality of the balun as they are an improvement to the ones shown Table I.

b) Yagi-Uda: The antenna was built with 4mm aluminium rods for the dipole and reflectors. These elements were attached to a wooden boom. At the back of the boom the reflector was built with a rectangular piece of cardboard on which aluminium foil was glued and the edges are taped



Fig. 25. RL(db) graph when connecting balun to the antenna's folded dipole.

Measurement	Value
Return Loss (dB)	-40.96
SWR	1.02:1
Frequency (Hz)	402.6 MHz
$ Z (\Omega)$	49.3

TABLE III

MEASUREMENTS TAKEN FROM RESONANT FREQUENCY SHOWN IN FIGURE 25.

with aluminium tape. The cardboard was attached to a wooden frame to make it sturdy.



Fig. 26. Built folded dipole yagi antenna with a slab corner frequency reflector

D. Results and Discussion

Figure 25 illustrates that the signal with the lowest power reflected back into the circuit, is the one with the frequency of about 402.6 MHz. For exactly 400MHz, although the return loss is higher than -40.96db at around -25dB, it still satisfies our goal for maximizing power transfer efficiency as it is still less than -20db.

Moreover, the impedance $|Z| = 49.3$ implies that the antenna's input impedance is approximately 200Ω at the resonant frequency of 402.6MHz as the balun ratio is 4:1 which satisfies our antenna input impedance goal.

An issue with the balun however, stems from it being very fragile and so is prone to being disconnected from the antenna. To fix this, electrical tape was used to secure the connections.

For the Yagi-Uda antenna, since the directors only had a difference of 3mm between them, it was very important

to get them to the exact length. The team did their best to implement this, but there are still differences of 1mm in the director lengths. The dipole was constructed through bending the aluminium rod, however this introduced a difference of 0.5cm on one side of the dipole. The corner reflector was built out of two halves to form the corner. The two pieces don't align properly with a one centimeter shift. Since no screws could be used to built the antenna the reflector was glued at the back, however this didn't hold that well and thus the boom is pointing crooked out of the reflectors.

During the demonstration the antenna was tested by using a Pluto as input device and the receiver in Horst tower. The received signal had a strength of -60.46dB. Unfortunately no other testing could be performed, because of time limits with lending out the Pluto devices.

V. COMBINED SYSTEM

The output of the LTspice simulations shown in Section III already accounted for the expected impedance of 50 ohms of the coax cable connecting to the antenna. It is also measured that the antenna with the balun is at around 50 ohm at 402Mhz illustrating its functionality. However, due to the mistakes made in the process of creating the electronic circuit, the combined system was not able to be realized. In hindsight, it would have been possible to complete the electronics if we had another PCB and spare components to work with, as a lot was learned during the process of assembling the circuit.

VI. CONCLUSION

In conclusion, for a target resonant frequency of 400MHz, the design involves the utilization of an FM modulator and amplifying the 400MHz harmonic frequency of a 200MHZ Colpitts oscillator using class C amplifiers. A yagi-uda antenna design was chosen for its polarisation and directivity, which was further improved by utilizing a corner reflector. The antenna system managed to transmit a power of -60 dB at a distance of around 100 meters. While the Antenna section tuned successfully for an input signal of around 400MHz, due to technical and physical difficulties, the electronics design proved to be problematic. Due to the process of soldering and desoldering components multiple times, the PCB was damaged and contaminated with the soldering iron, which led to incorrect output. Due to the time constraint and lack of a spare PCB, the electronics system failed to be implemented. Therefore, the combined system of electronics and antenna was unable to be realized.

VII. AI-STATEMENT

During the preparation of this work the author(s) used ChatGPT, Gemini and the AI-spelling checkers of LanguageTool, Grammarly, Writefull, and Overleaf in order to check the text for errors. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the content of the work.

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