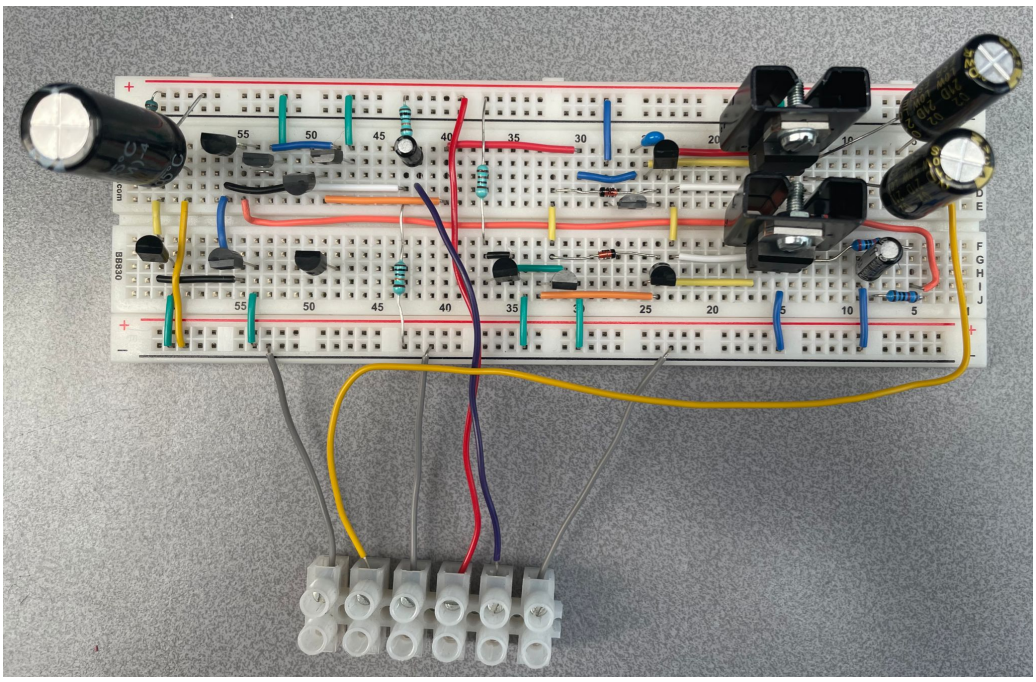


Audio Power Amplifier

Date:
April 6, 2025

Authors:
P. Geronimo (s2522373)
M. Rais (s3152731)
B. Ersayin (s3256472)
N. Juscenko (s3097218)

Group:
7

Module 3: Electronics project

Contents

Abstract

The importance of audio amplifiers is significant in an interconnected world. Most smart devices that produces audio would not work properly without an amplifier. Audio amplifiers allow designers to fine tune the clarity as well as the volume of the device. While modern audio amplifier designs involves the use of Integrated circuits, this project will be focused on creating one through the use of only transistors and passive components. Our amplifier draws approximately 0.1A from the power supply and produces clear sounds within the audible range of 20Hz to 20kHz. Distortion only happens at high input signal amplitudes.

1 Introduction

In this project an audio power amplifier with feedback will be designed and realized. The audio amplifier must have a bandwidth from 20Hz to 20kHz, to cover all hearing range of humans. The gain margin must be about 30 for a load impedance between 4Ω and 16Ω, and input impedance of 50kΩ. Finally, with all these specifications satisfied, final design must be powered with a single 10V supply, needs to have output power bigger than 2W at 10% of Total Harmonic Distortion (THD) in 4Ω, and (THD) by itself for a 1kHz sinusoidal output voltage with an amplitude that generates 1W (average) in a 4Ω load, should be lower than 1%. Our goal is to meet all these specifications mentioned above and present fully working soldered audio amplifier in the end of the project.

Since the use of integrated circuits such as manufactured operational amplifiers are not allowed in the project, one will have to be built using passive components and transistors.
This poses a question of as to what happens within the many stages of an amplifier and whether we can apply that to our audio amplifier design.

In this report, there will be analysis of the challenges that will need to be solved. That will consist of detailed step by step overview of designed and each stage design. This will consist of Input stage, Intermediate stage and finally the output stage and feedback. This can be view from the block diagram 3. After there will be done analysis the design and its simulations. Finally there will be presented results and measurement analysis of final audio amplifier and conclusion of the problem.

This report will look into the overall design of our amplifier in Section 2, the motivation for the chosen components for every stage in Section 3, the simulations conducted using LTSpice in Section 4 and finally the Realization and measurements in Section 5.

2 Overall Design

Our audio power amplifier design follows the three main stages that are common in creating the internals of modern operational amplifiers: a differential, an intermediate and an output stage. A negative feedback is included to reduce the gain of the amplifier as well as increase its stability.[2]

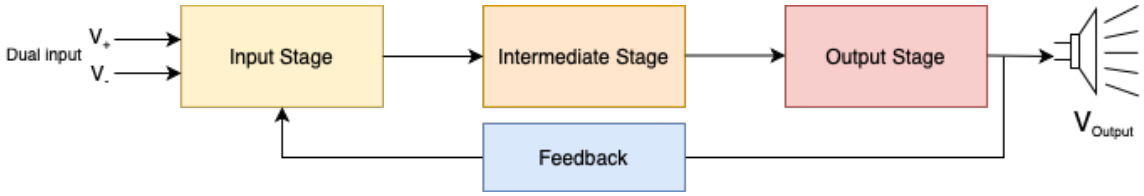


Figure 1: Design block diagram

Figure **??** shows the block diagram of the design and Figure 2 illustrates the schematic of the audio power amplifier prior to the realization stage of the project. The simulation of this circuit is shown in Section 4.

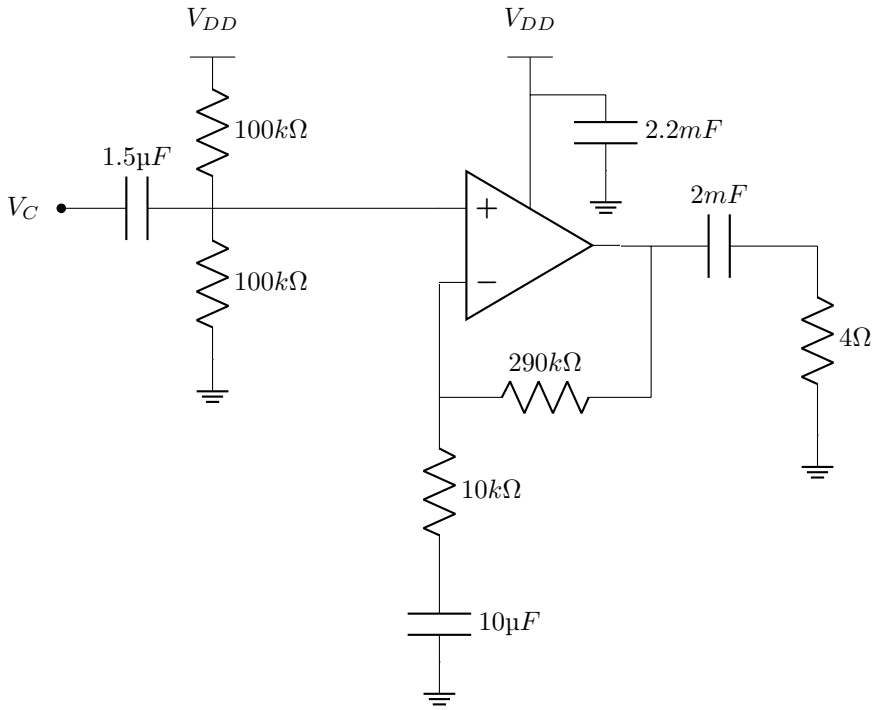


Figure 2: Audio power amplifier schematic

The audio amplifier specifications are listed below.

- Bandwidth: 20Hz - 20kHz
- Voltage gain: 30x
- Load impedance: 4-16Ω
- Single 10V supply.
- Output power > 2W at 10% THD in 4Ω
- Input Impedance > 50kΩ
- THD < 1% at 1kHz, 1W in 4Ω

Bandwidth The bandwidth requirement can be achieved by adjusting the frequency dependent segments of the design. The capacitors located at the non-inverting input, the feedback and at the output are tuned such that the bode plot has a cutoff frequency at 20Hz. The capacitor placed within the intermediate stage takes advantage of the miller effect to achieve a cutoff frequency of 20kHz. Therefore, a segment of the input, the intermediate and the output stages contribute to the amplifiers bandwidth.

30x Voltage gain A feedback is implemented not only to bias the entire circuit, but also to limit the voltage gain to 30. This feedback is placed after the output stage of the amplifier. The feedback stage's resistor ratio controls the final gain of the circuit

Load impedance The 4Ω resistor represents the load of the amplifier.

Single 10V supply The project only allows for one supply voltage of 10V. Therefore the use of -10V will not be possible and heavily influences the final design.

Output power > 2W at 10% THD in 4Ω and THD < 1% at 1kHz, 1W in 4Ω We believe that these two requirements are dependent on each other. In order to achieve an output power of greater than 2W at 10% THD, the amplifier must already achieve the 1W requirement at less than 1% THD. To achieve this, the output stage must deliver enough current to the load. Therefore, a high gain current amplifier was implemented on the output stage via a BJT sziklai pair.

Input impedance > 50kΩ The high pass filter at the non-inverting input from Figure 2 form an input impedance of more than 50kΩ.

3 Design Analysis

3.1 Input stage (Step by Step)

Differential Pair (Long Tailed Pair) The differential pair is the input stage in op-amps.

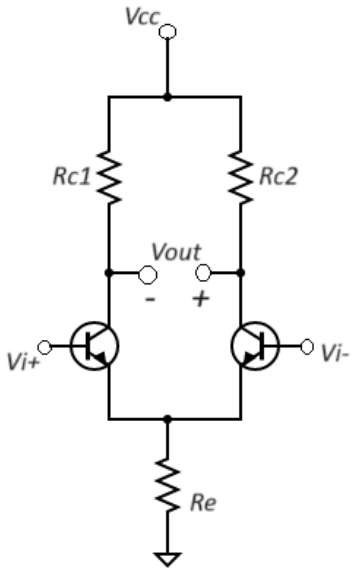


Figure 3: Differential Pair Circuit Model

The purpose of the differential amplifier circuit given in Fig. 3 is to amplify the difference between two input signals while rejecting the part of the signal common in the both inputs which is also known as common-mode signals.

This common-mode signal component is nothing more or less than the average value of the two input signals. In other words, common-mode voltage refers to the voltage present on both input signals.

Common-Emitter Amplifier Transistor Q1 is biased by resistors R1 and R2 to some operating point as follows below in Fig. 4

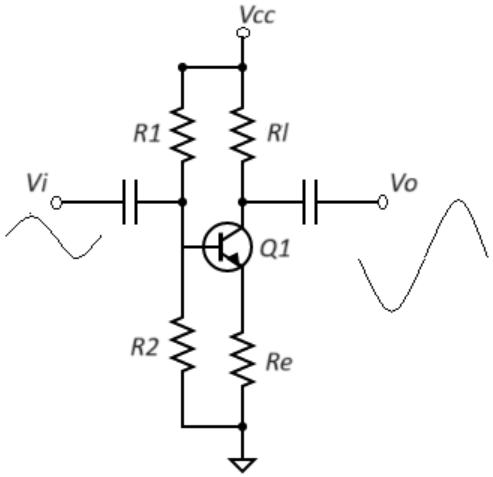


Figure 4: Common-Emitter Amplifier Circuit Model

When AC signal is applied to the input terminal, it results in a change to the base emitter voltage of the transistor Q1. Lets say the input signal is increasing a that instant. Since the input signal is voltage at base it is known that:

$$V_B - V_E = V_{BE} \tag{1}$$

Thus, the base emitter voltage will increase. It is also known that:

$$I_C \approx I_{C0} \cdot (e^{\frac{q \cdot V_{BE}}{k \cdot T}} - 1) \tag{2}$$

Hence, the collector current will increase. This will result in a increase in voltage across the load resistor Rl. By using Kirchhoff Voltage Law, it is observed that

$$V_{out} = V_{cc} - V_{Rl} \tag{3}$$

Thus, the output voltage will decease at the instant when the input voltage is increased. Therefore this is a inverting amplifier where the output signal is inverted. Lastly, the gain can be expressed as:

$$A = -gm \cdot R_l \tag{4}$$

Common-Base Amplifier The configuration of common-base amplifier circuit given below in Fig.5 is identical to the configuration of the common-emitter amplifier circuit given in Fig. 4. The only difference is the alternating input voltage signal is applied through the emitter as given in Fig.5.

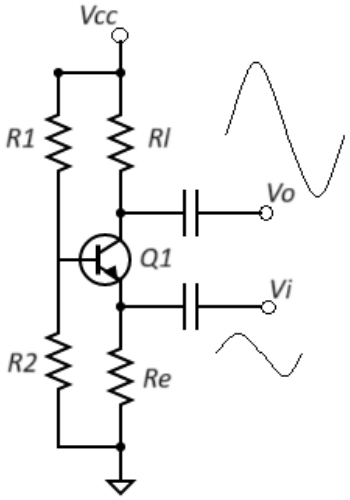


Figure 5: Common-Base Amplifier Circuit Model

Assume that at a particular instant input voltage signal is increasing. By using the same approach used at the common-emitter amplifier circuit in Fig. 4, it is obvious that base emitter voltage is decreased hence the collector current. Thus, the voltage across the resistor Rl is decreased. By using Kirchhoff Voltage Law, the output voltage is shown to be increasing at the instant when the input voltage signal is increasing.

Therefore, the common-base amplifier circuit in Fig. 5 does not invert the signal unlike the common-emitter amplifier circuit in 4. Lastly, the gain can be expressed as:

$$A = gm \cdot R_l \tag{5}$$

Single Transistor Crude Differential Amplifier A single transistor crude differential amplifier circuit can be formed with just one transistor and also by using properties of both common-emitter and common-base amplifier circuits as follows below in Fig. 6

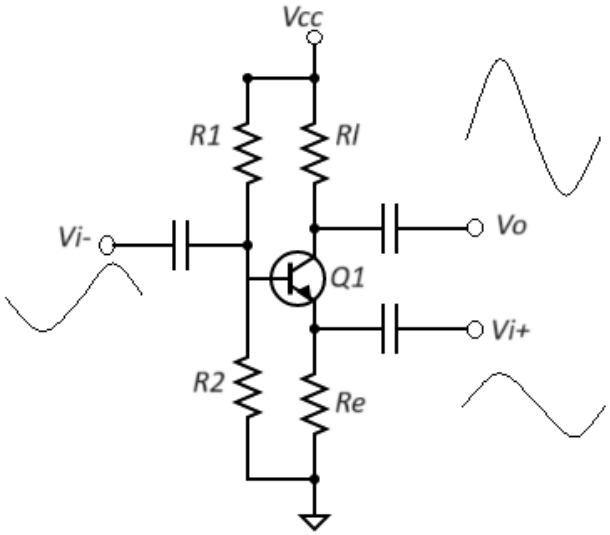


Figure 6: Single Transistor Crude Differential Amplifier Circuit Model

The base and emitter are considered to be the inverting input and non-inverting input respectively. That being said, the gain can be expressed as:

$$A = (V_{i+} - V_{i-}) \cdot gm \cdot R_l \tag{6}$$

However, it can be seen that the differential input signal that is to be amplified is symmetrical around the common part of the input voltage signal. To properly and symmetrically operate on something that is symmetrical, one usually needs to be something that is also symmetrical.

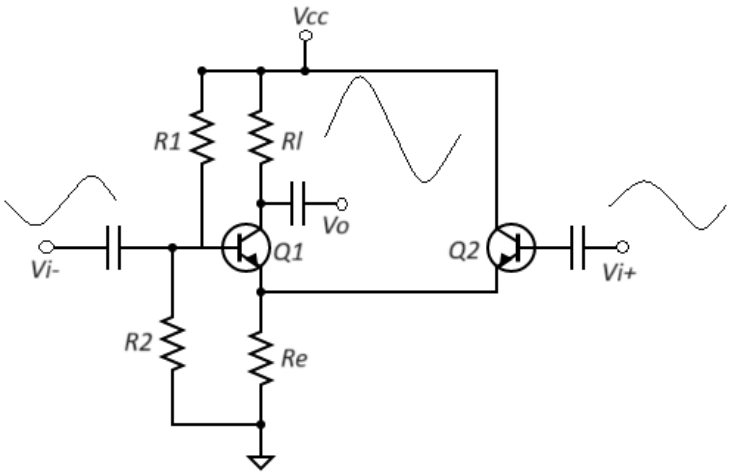


Figure 7: Crude Differential Amplifier Circuit Model (Long-tailed alike)

This can be solved by introducing an emitter follower transistor Q2 into the non-inverting as follows below in Fig. 7. Now, the amplifier circuit started to look like a classic differential pair amplifier as desired.

Constructing Differential Pair (Long-tailed Pair) By getting rid of the AC-coupling and the bias resistors and introducing a second load resistor, a differential pair amplifier circuit is obtained as follows given below in Fig. 8:

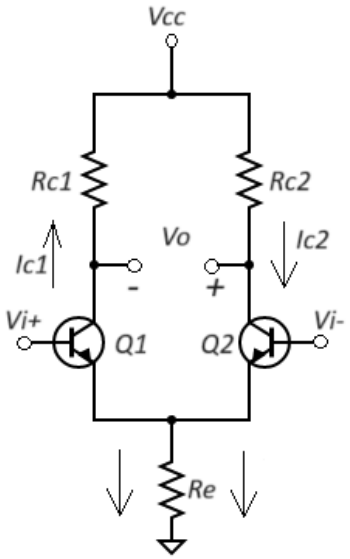


Figure 8: Differential Pair Amplifier Circuit Model (More detailed)

The bias point is established by ensuring that a relatively constant current flows through the emitter resistor. This is done by using a fairly high value resistor which results in a relatively high voltage across it compared to the input signal range. This is where the name "Long Tailed Pair" comes into play with no differential input voltage signal. In other words, the transistor bases are at the same voltage.

The bias current will split equally between the two transistors. When a differential voltage appears, the current will increase in one transistor and decrease in the other. Moreover, their sum in the tail resistor will remain somewhat constant.

That being said, the output of the transistor Q1 is going to be:

$$A = \frac{(V_{i+} - V_{i-})}{2} \cdot gm \cdot R_l \tag{7}$$

Also, the output of the transistor Q2 is going to be the inverse of the transistor Q1:

$$A = \frac{(V_{i-} - V_{i+})}{2} \cdot gm \cdot R_l \tag{8}$$

Common Mode Rejection It has been stated before that the desired outcome is differential amplifier to amplify the differential signals and reject common-mode signal.

There is a common-voltage source connected in the classic way to the inputs as follows below in Fig. 9

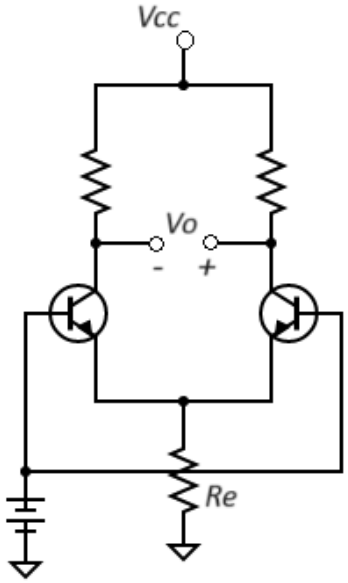


Figure 9: Common Mode Voltage Source

As the transistor base voltage increases, the current through the emitter resistor increase hence the voltage across the emitter resistor.

However, there is a significant problem with this particular circuit design (Fig. 9). The emitter resistor can be sized as large as possible but it will still throw off the bias of the amplifier due to the common-mode voltage. Hence the gain changes along with the common-mode voltage.

On top that, the power supply noise is considered common-mode too. Therefore, the common-mode voltage signal which could be observed in the form such as external noise or interference, power supply noise, DC offset; has to be eliminated. The usual way to make a current independent on a voltage is to use a current source.

Constant Current Source with Common Mode Input Now, the emitter resistor at the differential pair amplifier circuit (9) is replaced by a constant current source labelled as follows below at

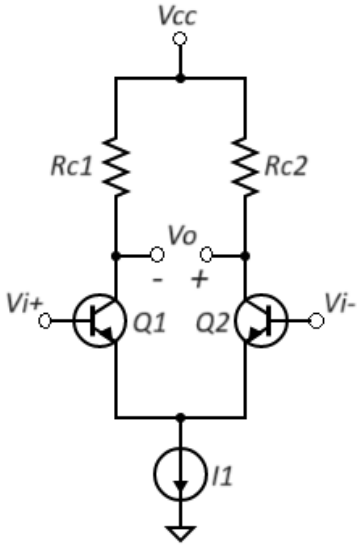


Figure 10: Replacing emitter resistor Re with current source I1 in a Differential Amplifier

As the common-mode voltage changes, the current in the current emitter tail stays constant. (Fig. 9) This makes superb power supply rejection since the DC power noise is a common-mode as well. That being said, this works hand to hand with the differential signals.

As voltage Vi+ increases, the current through the transistor Q1 increases. (Fig. 9) This steals current from the constant current source I1. Hence, the current through Q2 decreases or vice versa.

Single Ended Output Another duty of the operational amplifier is to take differential inputs and give out a single-ended outputs. This can be done by simply taking the output from one of the collectors as given below in Fig. 11

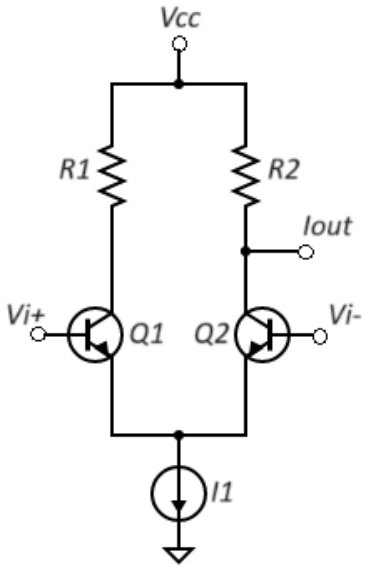


Figure 11: Single ended current output in a Differential Amplifier

However, the gain coming from the transistor Q1 is wasted during the process and no gain must be thrown away inside the internals of an op-amp. Therefore, to properly use the differential output current of a differential pair, these 2 currents need to be subtracted from each other.

Adding currents is straightforward, as is reversing the direction of a current. Therefore, subtracting currents from on another is also straightforward. First, one of the currents has to be inverted with a current mirror configuration. Then, both currents are going to be added in a relatively low ohmic node.

Transistor Transconductance It is common knowledge that applying an increasing voltage across the emitter base junction of a bipolar transistor results in an exponentially increasing collector current.

If a voltage is applied to the base-emitter junction of transistor as an input quantity and the collector current is taken as an output quantity, the transistor will act as an exponential voltage to current converter.

Transistor "Backward" current to voltage converter By applying negative feedback (simply by joining the base and collector) the transistor can be 'reversed' as given above in Fig. 12. This will lead the transistor to behave as the opposite logarithmic current to voltage converter. Now, it will adjust the 'output' base-emitter voltage as to pass the applied 'input' collector current.

Introducing Current Mirror Configuration If we take the two circuits and combine them together, the logarithmic current to voltage converter with the exponential voltage to current converter, the current mirror configuration achieved as given below in Fig. 13

The nonlinearities of the logarithmic current to voltage converter and the exponential voltage to current converter compliment each other and makes properly working linear current mirror circuit.

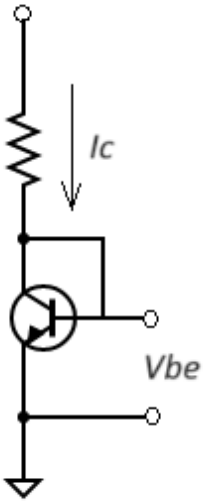


Figure 12: Applying negative feedback to a transistor

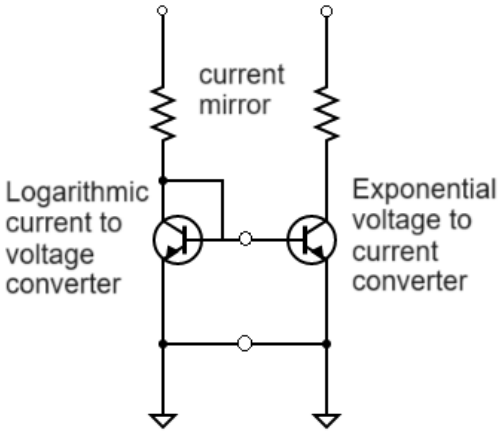


Figure 13: Current Mirror Configuration

However, before proceeding with combining the the differential amplifier circuit and current mirror circuit together, the decision of using BJT transistors or MOSFET transistors should be made.

It is commonly known that the main advantage of using the Mosfets from the BJTs is almost infinite input impedance. Mosfets are more appropriate for processing signal so they transfer less noise into the signal compared to the Mosfets. On the other hand Mosfets have lower differential gain and are more sensitive to temperature, what increases its resistance. Therefore, Mosfet transistors are going to be chosen to build the input stage. (This disadvantage of mosfets in terms of the temperature aspect is going to taken account in the experimental stage.)

Design and Construction of Input Stage The full design of the input stage is given below in Fig. 14

As can be seen in Fig.14, by using two resistors that each have hundred thousand resistors, a voltage is created across the differential input so that 5V of DC from the 10V DC power supply is provided to V+ part of the differential pair. On top of that, AC sine input of 0.1V amplitude is supplied to V+ part of the differential pair. The 1.5 macro fahrad capacitor is chosen to be put in front of the AC input signal to block any DC signal and manage the cutoff frequency.

In order to replicate 1 milli Ampere current tail with circuit components, current mirror configuration by using BJT transistors is implemented as can be seen in Fig.14.As can be seen that between the base and emitter junction of transistor Q4 there is a 0.6V voltage drop. So, by choosing the bias resistor to be 9.4 kilo ohms, 1 milli Ampere will flow thorugh the bias resistor which is mirrored on the transistor Q1 as desired.

In Fig.14, the current through MP2 is mirrored into MP1. As can be observed the the output current is

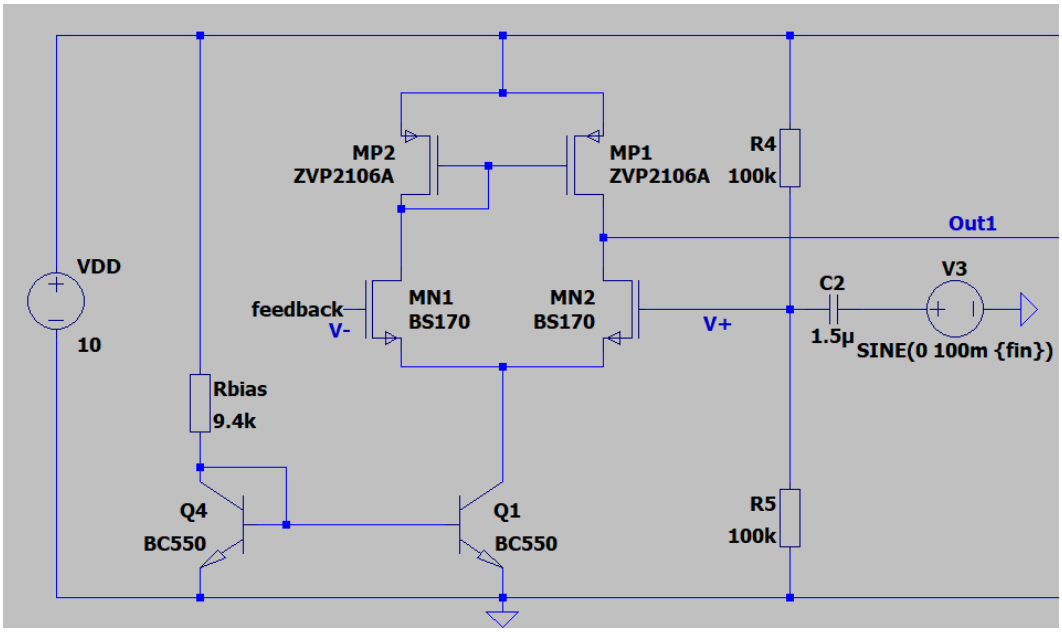


Figure 14: Input Stage of Opamp Internal (Full Design)

going to be zero. However, when it comes to the output voltage is can easily be seen that the output voltage is going to be the voltage supplied from power supply subtracted by the voltage across source drain of MP1. Also the drain source voltage across MP2 is the same as the drain source voltage across MP1 because of mirroring. Moreover, due to the mirroring configuration, voltage across drain source at MP2 is the same as voltage across gate source at MP2. Therefore, we can conclude the output voltage as:

$$Vout = VDD - Vsg(MP2) \tag{9}$$

Small Signal Analysis and Small Signal Equivalent Circuit of Input Stage At first, the input stage given in Fig.14 can be reduced as follows below:

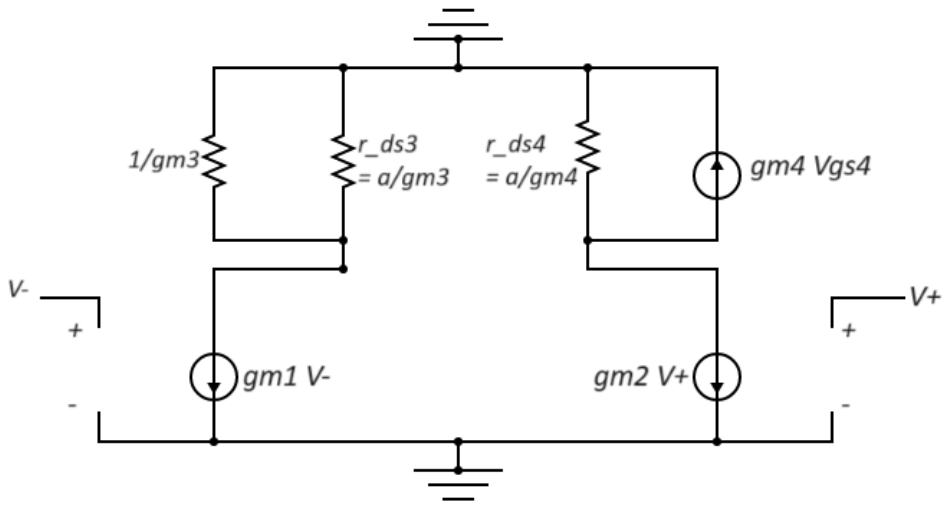


Figure 15: First step of finding SSEQ of Input Stage

As can be observed in Fig. 15, the current tail is going to be expressed as a virtual ground since it is DC along with DC voltage source VDD becoming a short. For mosfets; MN1, MN2 and MP1 (can be seen in Fig. 14), regular definition of SSEQ are used. However for MP2 (can be seen in Fig. 14), due to the current mirroring, MP2 has diode-connected configuration.

As we proceed with the SSEQ, we conclude the model as follows below in Fig. 16

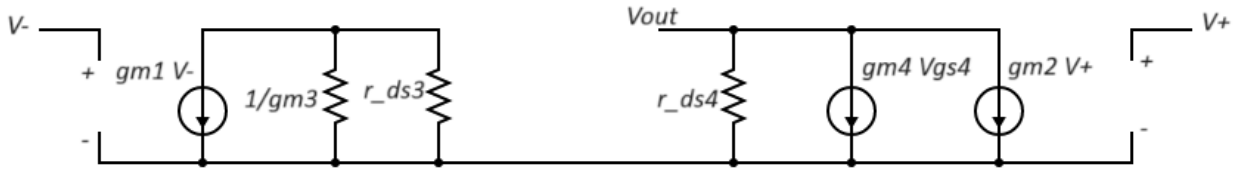


Figure 16: Second step of finding SSEQ of Input Stage

3.2 Intermediate stage

The intermediate stage is required to not only provide a low input impedance and high output impedance but also provide a bias current for the transistors in the intermediate and output stages.
A common source PMOS amplifier supplied with a biasing current source replaced with a current mirror is used. A capacitor is placed on the amplifier's gain stage to take advantage of the miller effect and achieve a first order frequency response at 20khz [6]. A 1mA biasing current was chosen for the intermediate stage, this is because the output stage has a sziklai pair that has a high current gain so that the load will be supplied with enough power to meet the requirement.

3.3 Output stage

For the Output stage we require a high input impedance and low output impedance which an emitter follower circuit can accomplish. There exists several types of output stages (A,B, AB,C D, E, F, G,...), which are divided into two types of designs: linear and switching. However, the options we have for the circuit, given the time availability for the project, are class A, B and AB.

Class A: Class A allows for the circuit to match the input signal with little to no distortion as the transistor is always turned on.. The drawback however, is that the efficiency of the transistor suffers as being turned on at all times means dissipating heat and consuming power even without any input. This drops the circuits efficiency to about a maximum of 25%.

Class B: Class B provides an improvement on efficiency since one of the two transistors will always be off per half cycle of the input signal and so less power is consumed and heat dissipated. This presents a problem though since one transistor per half cycle will remain off until the base voltage reaches about 0.7V. This creates a crossover distortion since these 'dead zones' produces a lot of harmonic noise visible using FFT. The efficiency of this class goes up to about 78% [3].

Class AB: Class AB combines the performance of the Class A and high efficiency of Class B by supplying a very small amount of base voltage into the transistors such that it remains on even with no input signal [1]. This can be done by having a diode connected in parallel to the transistors' base junction as the voltage drop across a diode is the same as the required voltage for the transistor to be on. The efficiency of this class is greater than that of Class A but less than that of Class B.

Problems For our design, the class AB circuit was chosen for the output stage mostly to avoid the crossover distortion the class B presents. However, the current output of the transistors are only about a few milli amps, making the average power on the load go below the requirement of 1W. Our initial solution for increasing the current gain in the output stage is to implement two BJT Darlington pairs to each handle the positive and negative half cycles of the signal. This makes it so the current is amplified using Equation 10 where h_{FE1} and h_{FE2} represents the current gain of each of the transistors. The class A BC550 has a minimum gain of 110 and the MJE2955T has a minimum gain of about 20, thus making the darlington pair gain to be about 2320.

$$h_{FE} = h_{FE1} * h_{FE2} + h_{FE1} + h_{FE2} \tag{10}$$

A drawback of darlington pairs however is that both the transistors within the pair need to be supplied with a minimum of $\approx (0.7 * 2)$V to turn on. Therefore a constant voltage drop of 2.8V is required for the two

darlington pairs to be in Class AB operation which might cause some overheating of the BJT's and requires 4 diodes to maintain.

Solution As for a solution, the final design uses a Sziklai pair in place of the Darlington pair. A Sziklai pair makes the combined npn and pnp transistor makes the minimum voltage drop for it to be turned on to be only 0.7V and so two diodes instead of four can be used. The new current gain calculation is shown in Figure 11 which is comparable to the darlington pair's gain since $h_{FE1} * h_{FE2} >> h_{FE2}$ [4].

$$h_{FE} = h_{FE1} * h_{FE2} + h_{FE2} \tag{11}$$

Bandwidth: Filters As mentioned in Section 2, the bandwidth is determined by the filters throughout the amplifier design.
The first filter is located on the non-inverting input, the cutoff frequency calculation is shown in Equation 12.

$$f_c = \frac{1}{(2\pi)(100k//100k)(1.5\mu)} \approx 2.12Hz \tag{12}$$

The second filter is within the feedback circuit, formed by the $10\mu F$ and the $10K\Omega$. The cutoff frequency is shown in Equation 13.

$$f_c = \frac{1}{(2\pi)(10k)(10\mu)} \approx 1.59Hz \tag{13}$$

The third filter is after the output stage and is shown in Equation 14.

$$f_c = \frac{1}{(2\pi)(2m)(4)} \approx 19.89Hz \tag{14}$$

Problem The aforementioned filters are enough to have a bandwidth of 20Hz+ but still not enough since there is no cutoff frequency at 20kHz to complete the bandwidth requirement. Initially a high pass filter with a cutoff frequency of 20kHz was added after the output stage. This did not work since the high pass filter cuts off low frequencies as well. This is the reason why the high pass filters were chosen to have low cutoff frequencies.

Solution Where a voltage amplification is present, there will be an apparent large increase in capacitance due to the Miller effect. Therefore, placing a capacitor at this point in the circuit allows for a high cutoff frequency. In our design a capacitor is placed between the gate and drain of the PMOS. This capacitor value was manually adjusted so that there is a cutoff at 20kHz. A capacitor of 1nF was chosen for this.

Feedback As for the feedback stage, the gain equation is:

$$A = 1 + \frac{R_2}{R_1} \tag{15}$$

Therefore the 290k was chosen for R_2 and 10k for R_1 for the op amp to have a gain be limited to 30.

4 Simulations and Design Evaluation

This section will look into how the simulation of the amplifier circuit design meet each of the requirements listed in Section 2. The full LTSpice circuit will be shown along with the results of transient and ac analyses.

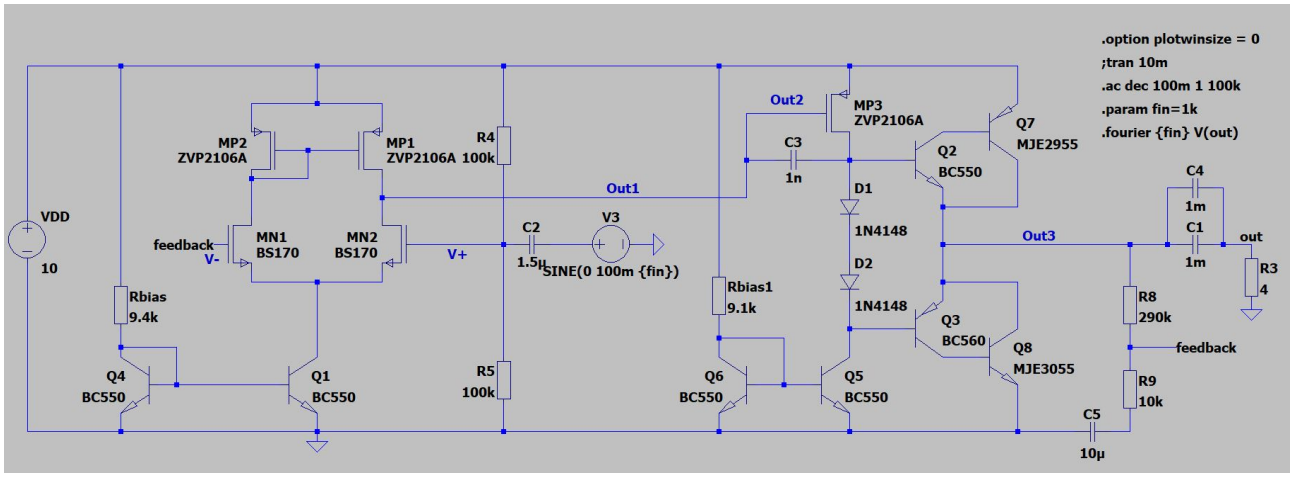


Figure 17: Full LTSpice audio amplifier circuit.

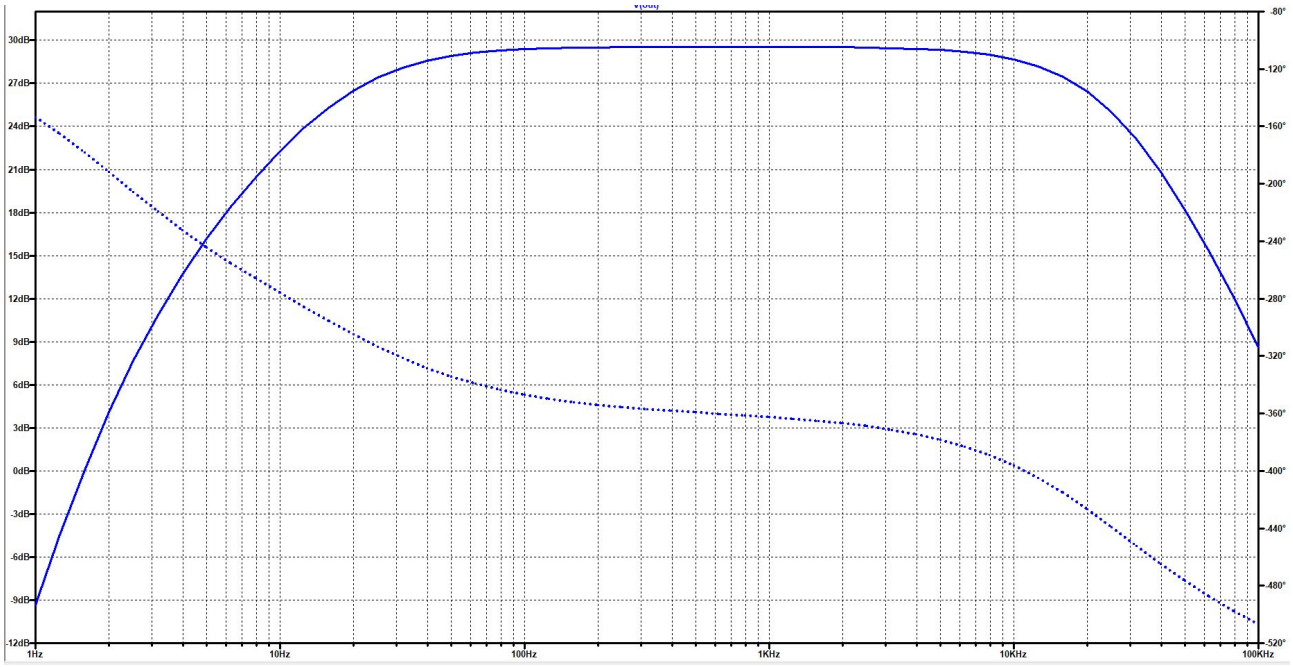
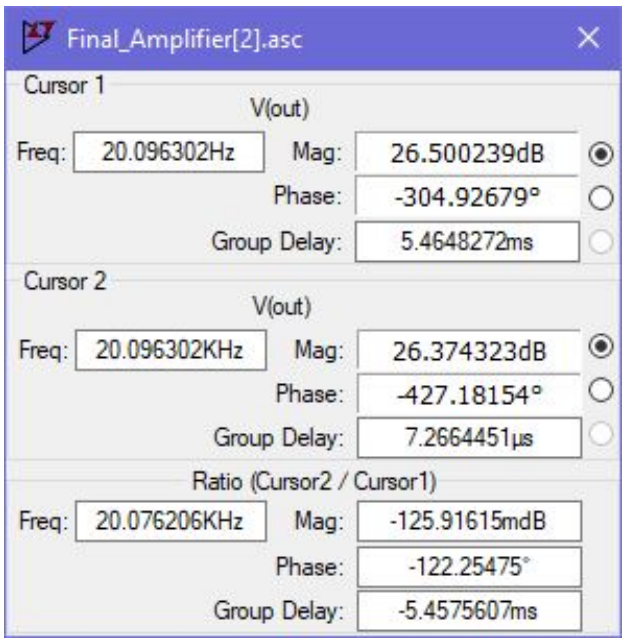
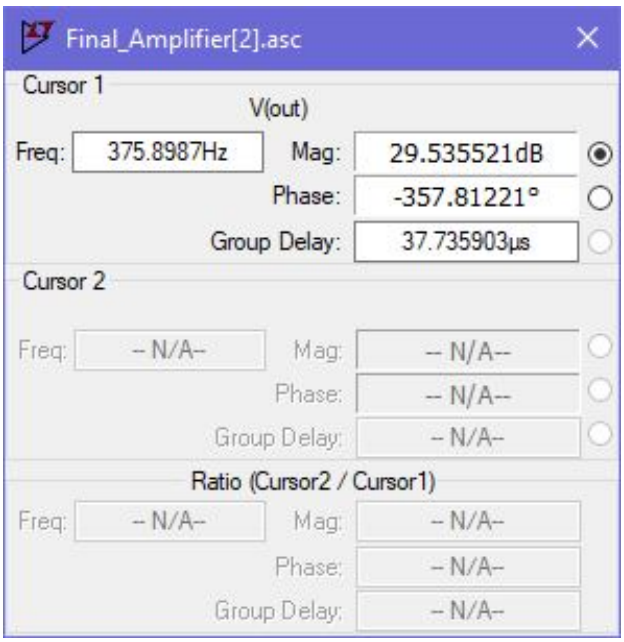


Figure 18: Bode plot simulation of the audio amplifier.

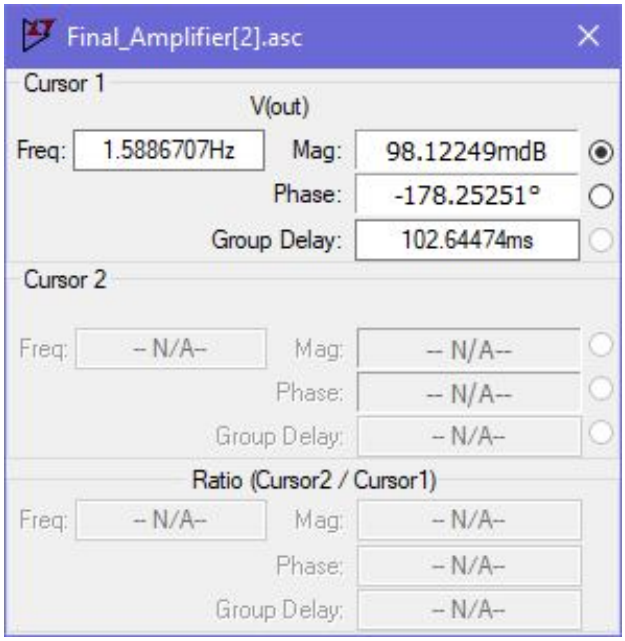


(a) Bode plot simulation cutoff frequency values.

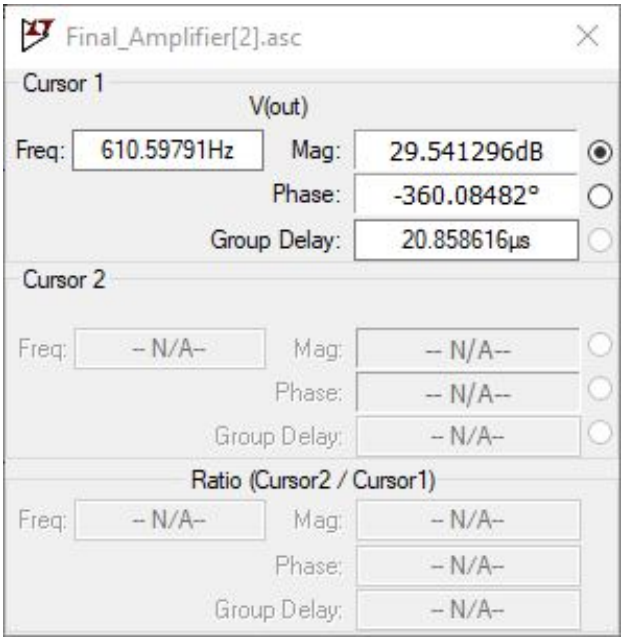


(b) Bode plot cursor output of the max gain as ≈ 29.5 dB.

Figure 19: Bode plot analysis 1



(a) Phase at a magnitude of about 0db is about -180°



(b) Phase at a magnitude of about 29.5db is about -360°

Figure 20: Bode plot analysis 2

Figure 17 illustrates the input, intermediate and output stages of the amplifier circuit. The bode plot shown in Figure 18 is the bandwidth of the circuit. Figure 19a shows the -3db or cutoff frequencies of the bode plot being 20Hz and 20kHz at ≈ 26.5db, satisfying the bandwidth requirement. Figure 19b shows the maximum gain of the circuit as ≈ 29.5db which shows that the gain is limited to 30x by the feedback circuit. Moreover, at 0db the phase is about -180° shown in Figure 20a and is -360° at 29.5db shown in Figure 20b which further illustrates that the gain margin is indeed at about 30db.

The first THD with the corresponding average power requirement are met on LTSpice and are shown in Figures 21 and 22. Figure 21 shows the output power across the 4Ω load and the THD being ≈ 0.26% and Figure 22 shows the average power output to be 1.120W.
Increasing the amplitude of the input signal from 100mV to 176mV yields a THD of ≈ 10% (Figure 23). At this point, the average power is shown in Figure 24 to be about 2.79W.

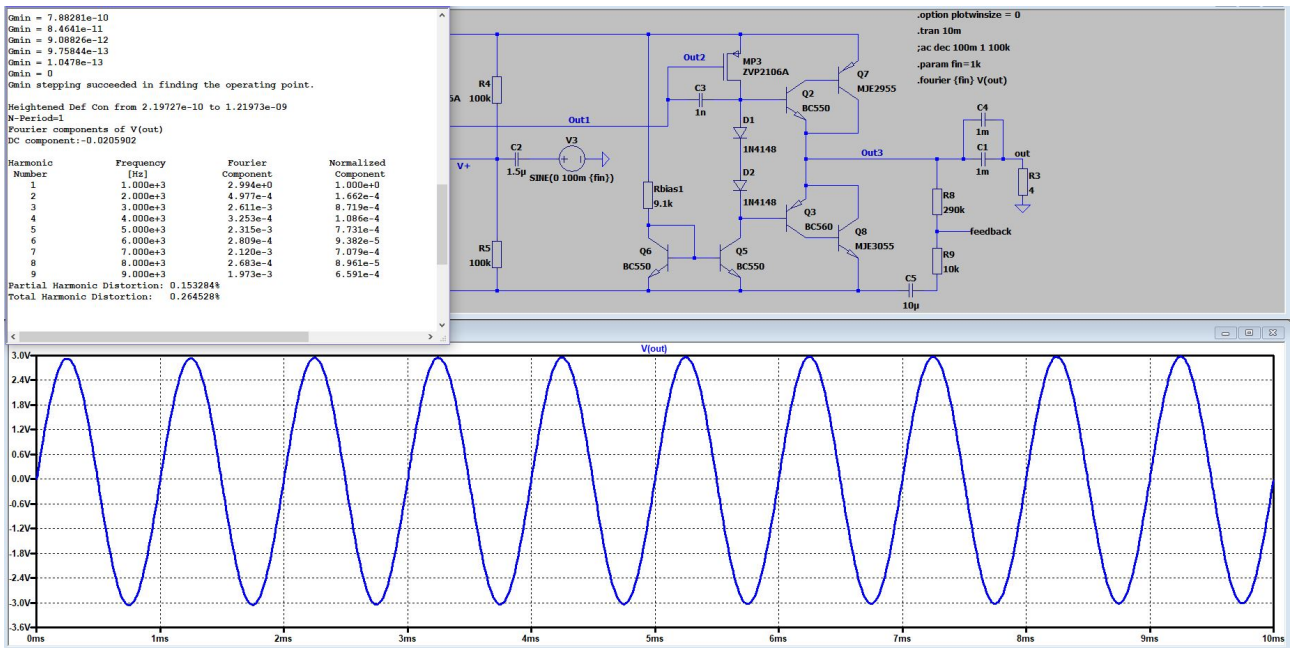


Figure 21: Output power at less than 1% THD.

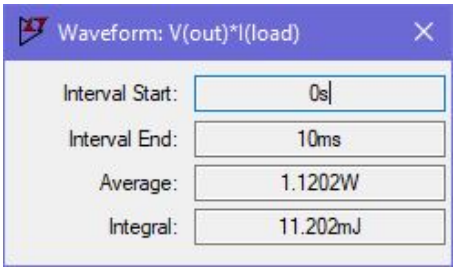


Figure 22: Average output power at less than 1% THD.

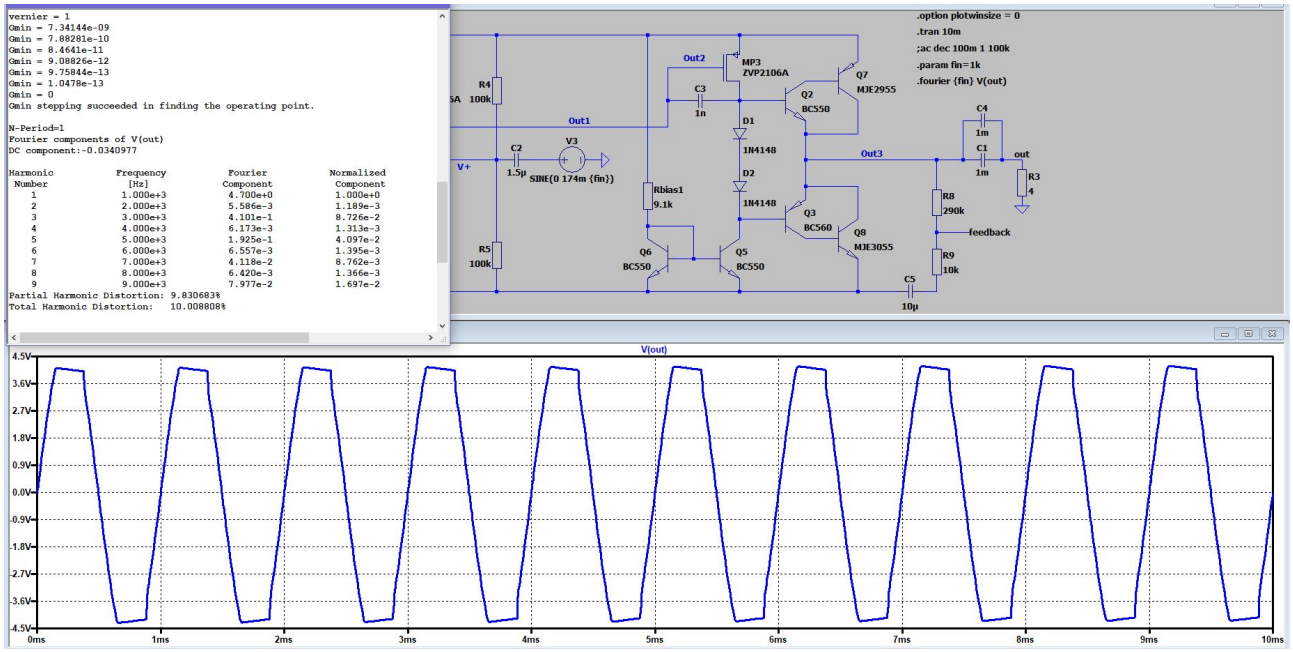


Figure 23: Output at 10% THD

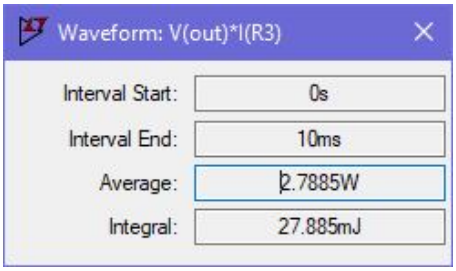


Figure 24: Average output power greater than 2W at 10% THD.

5 Realization and Measurements

This section will look into how the realisation of the amplifier circuit design meet each of the requirements listed in Section 2, and simulated results in Section 4. For the breadboard testing, a 4.7Ω load was used for the AC analysis and output voltage measurements, this was done to avoid sound to be made by the speaker during testing. The breadboard THD tests however, was done using the 4Ω load of the speaker.

The circuit shown in Figure 17 was built on a breadboard and tested. The built circuit will be shown along with the results of the FFT and AC analyses.

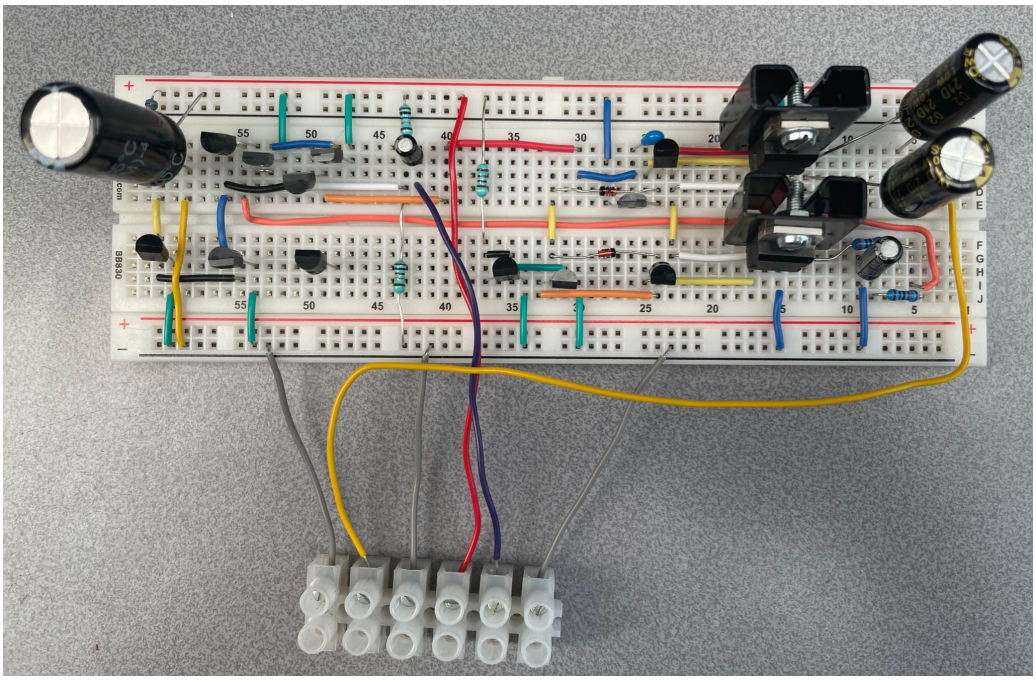


Figure 25: Full audio amplifier circuit built on breadboard.

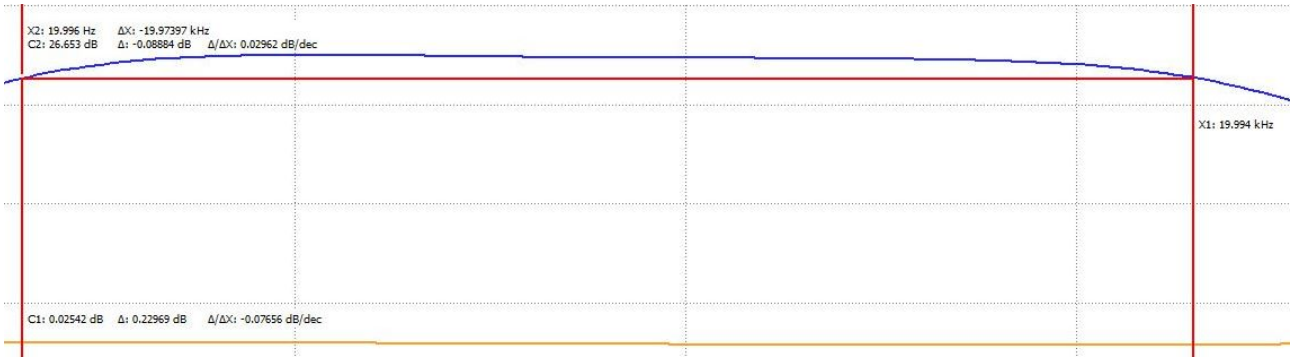


Figure 26: Bode plot measurement of the audio amplifier on a breadboard shown in blue, using the network analyzer function in the AD2. Illustrating 20Hz and 20kHz cutoff frequencies at ≈ 26.6db

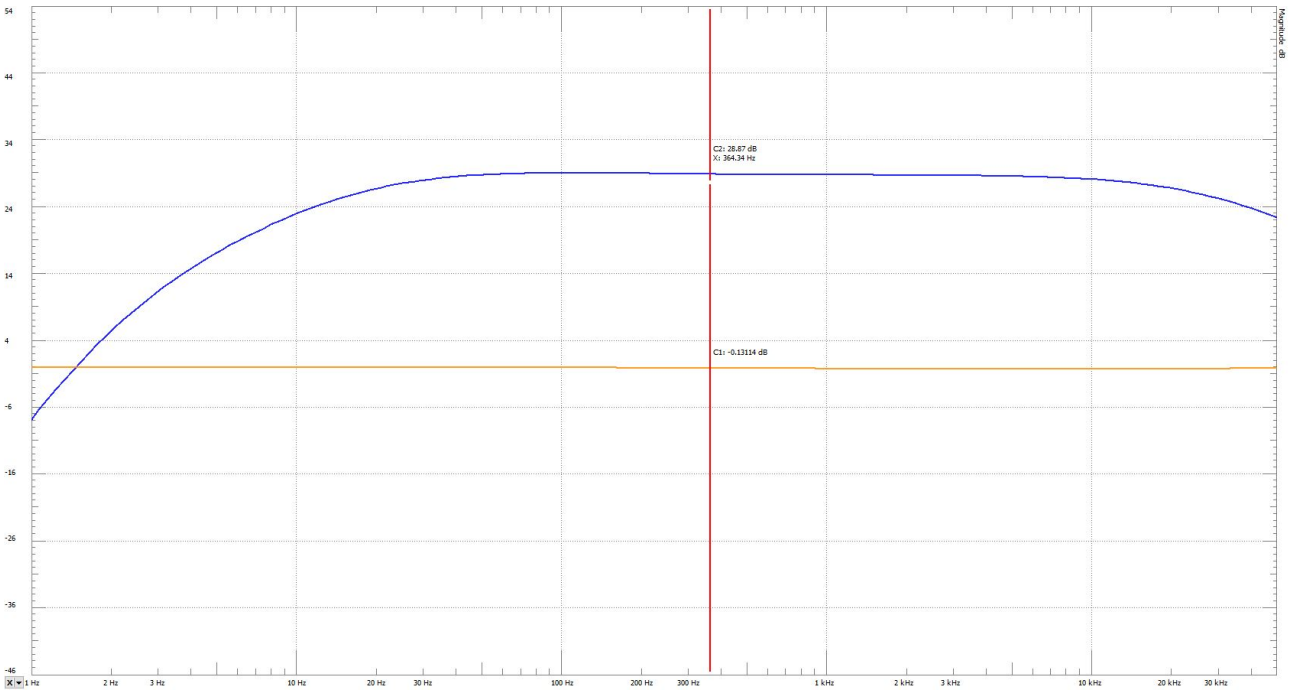


Figure 27: Bode plot cursor output of the max gain as ≈ 29db.

Figure 25 shows the input, intermediate and output stages of the amplifier circuit built on a breadboard. The bode plot shown in Figure 26 is the bandwidth of the circuit. Results are similar to simulated ones, shown in Figure 18. It shows the -3db or cutoff frequencies of the bode plot being 20Hz and 20kHz at ≈ 26.5db, same as simulated in Figure 19a, satisfying the bandwidth requirement.

Figure 27 shows the maximum gain of the circuit as ≈ 29db. This result is almost exactly the same as in the bode plot of the circuit in LTSpice which is shown in Figure 19b to be also 29.5 db.

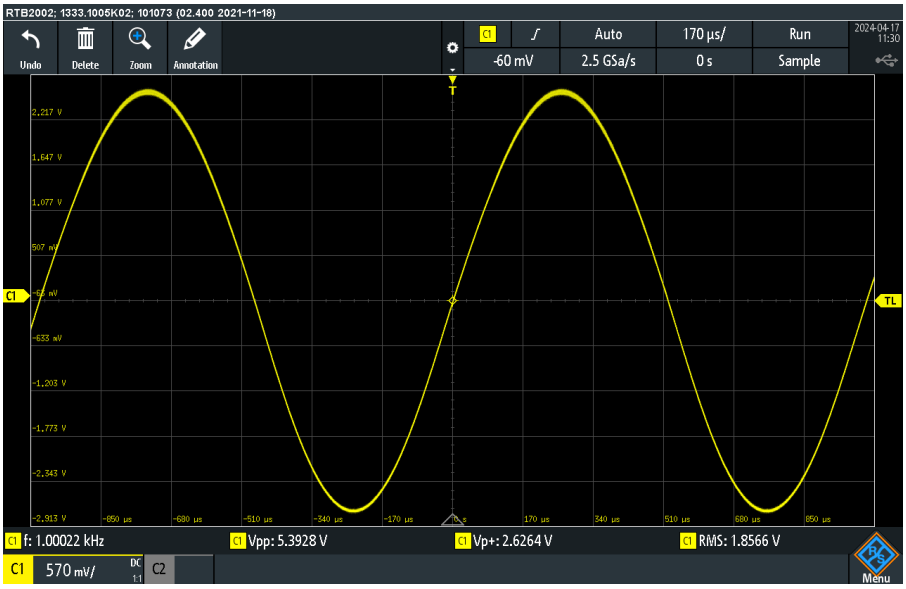


Figure 28: Breadboard Output voltage at about 1% THD.

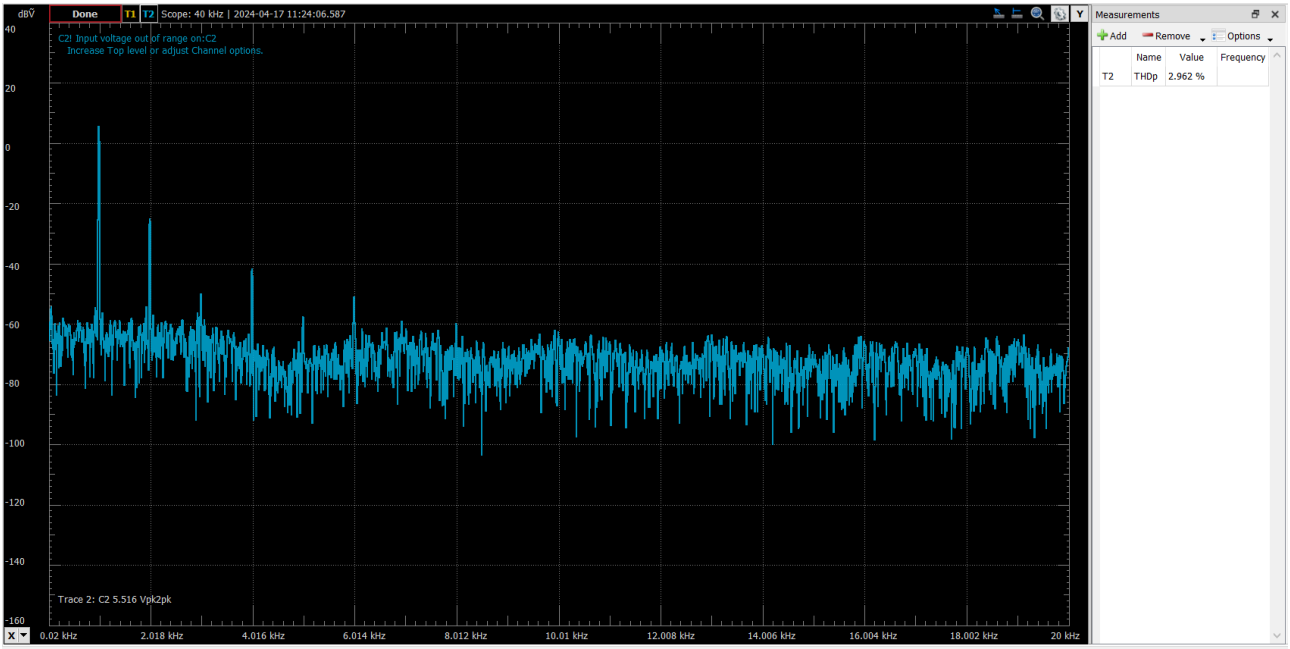


Figure 29: Measured Total harmonic distortion as a percentage.

Figure 28 shows the output voltage across the 4.7Ω load and Figure 29 shows the output THD being ≈ 2.96% which is higher than the expected 0.2% THD using a 100mV input from the simulation.
The average power of Figure 28 was calculated using formula:

$$P_{RMS} = \frac{{V_{RMS}}^2}{R} \tag{16}$$

RMS value of output signal is ≈ 1.85V, and the output power then is ≈ 0.73W. Measurements still differ from theoretical ones. THD is less than 1% as required, but more than simulated 0.26% shown in figure 21. Output power is less than 1W. This could be due to the circuit being built on a breadboard.

Instead of an amplitude of 170mV as in Section 4, the signal reaches a THD of ≈ 11%, shown in Figure 31, at 120mV signal input. At this point, the output voltage is clipping, and is shown in Figure 30, RMS of which is ≈ 2.57V. Then, using already known equation for calculating power in Equation 16, it results to ≈ 1.4W. This is 1.39W less than simulated value shown in Figure 24.

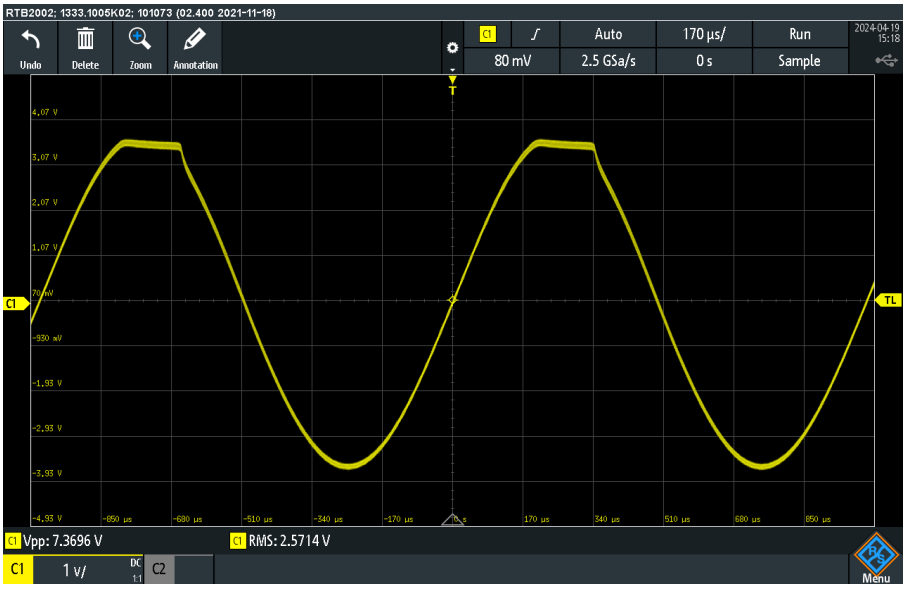


Figure 30: Breadboard Output voltage at about 10% THD

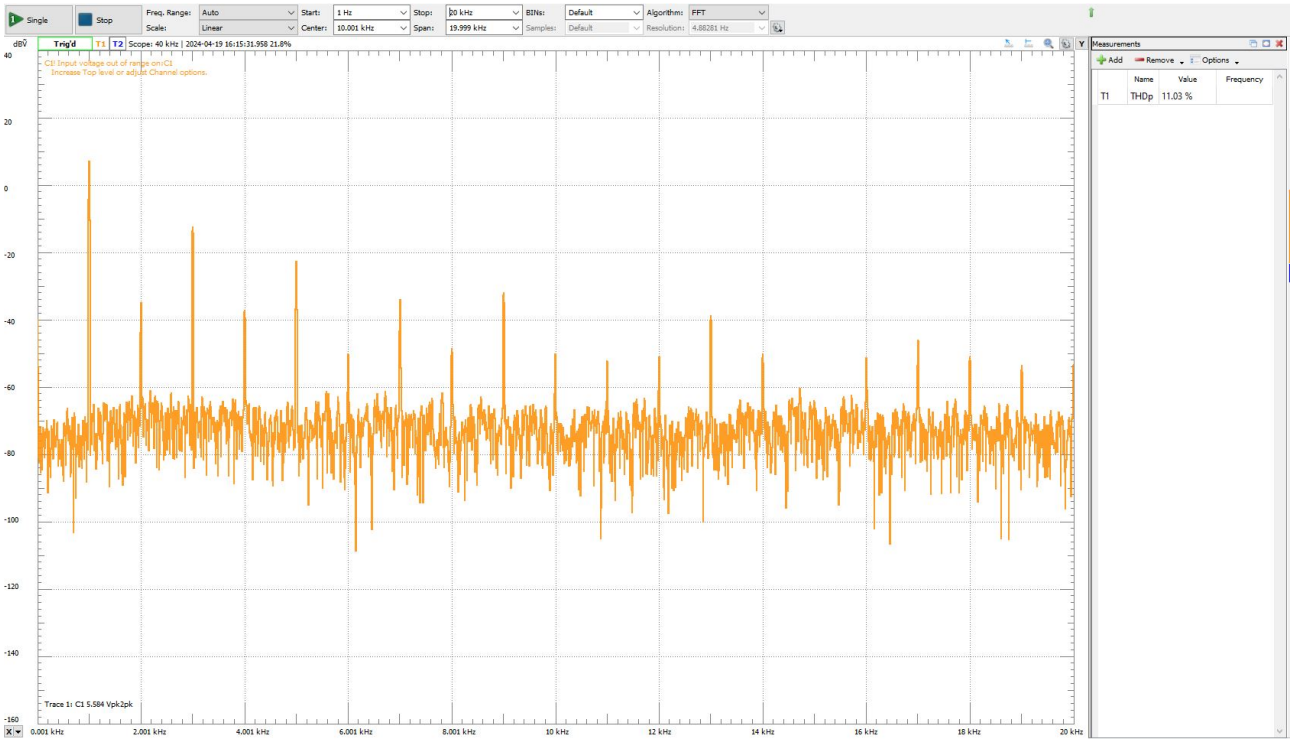


Figure 31: Spectrum analysis at about 10% THD.

Soldering the audio amplifier The entire audio power amplifier has been soldered twice. The first board 32 used a different component placement than that shown in Figure 5 and the second being the exact copy of how it was placed on the breadboard. However that should not affect the final soldered circuit and even after step by step analysis of circuit there was one mistake analysed which was affected by a faulty data sheet of power mosfets. This mistake was changed, however there was delivered only one half of sine wave as output. A day spending on further analysis and finding a mistake the initial signal was lost and hence we suspect the first board has broken transistors as no current was being drawn. Later there were identified broken transistors, however even after replacement there was no change. As for the second board, we were getting a square wave on the output of the differential pair stage and so for the output stage as well. This was probably due to the feedback not properly limiting the gain of the amplifier as well as of some broken transistor in the output stage.

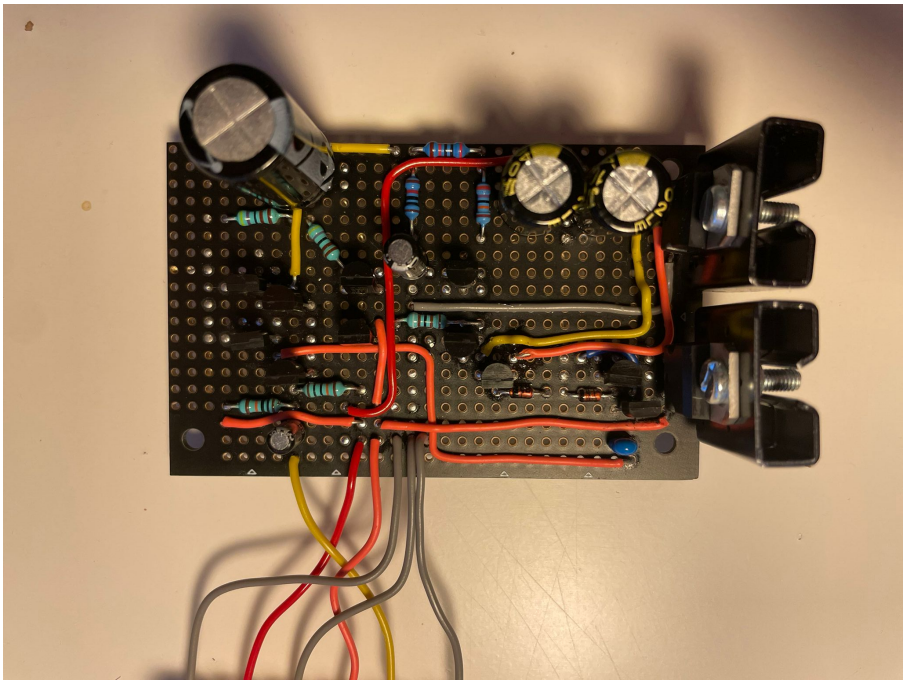


Figure 32: First soldered audio amplifier

6 Conclusion

The amplifier was built using a design of the main three stages of op-amp: Input, Intermediate and Output stage including a feedback circuit from the output stage to our inverting input. The input stage in the design is mainly used for reducing the input noise, the intermediate stage is for providing the bias current to the output stage and for adjusting the high frequency bandwidth and lastly the output stage is to act as a voltage follower with no crossover distortion. Additionally, the feedback circuit ensures that the entire circuit is biased at 5V. Our simulations results matches our theoretical expectations and breadboard measurements aside from our THD and output power measurement.

Conclusively, a working audio power amplifier can be created through the use of transistors and passive components if the design follows that of the internals of operational amplifiers. We were able to to successfully complete and design individual parts of each stage. We were not able to manage present working soldered amplifier, however it was successfully presented on the breadboard. The output of the sound was good and draws about 0.1A of current with a load of 4Ω but has slight distortions at high input signal amplitudes.

Future improvements would be to rebuild and successfully make a soldered circuit, one capable of meeting all specifications and producing a satisfactory sound output within the audible range.

7 References

[1] “Class AB Amplifier Design and Class AB Biasing,” Basic Electronics Tutorials, Jun. 16, 2018. https://www.electronics-tutorials.ws/amplifier/class-ab-amplifier.html
[2] ”Op-amp internals”, Electronics Project, EE B1-2A, University of Twente, 2023-2024
[3] S. Arar, “Introduction to the Class B Power Amplifier,” https://www.allaboutcircuits.com
[4] “Sziklai Pair: Compound / Complementary Electronics Notes,”
[5] “MOSFET Differential Amplifier: Part 4- Current Mirror as Load,” https://www.youtube.com/watch?v=9zXUwTX3hNg (last checked Apr. 21, 2024).
[6] “Miller Capacitance,” GeeksforGeeks, Jan. 08, 2024. https://www.geeksforgeeks.org/miller-capacitance/

8 Appendix

During the preparation of this work the author(s) used ChatGPT in order to paraphrase and research about overleaf codes. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the con- tent of the work. During the preparation of this work the author(s) used Office spelling correction in order to check spelling. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the content of the work.

9 Work Contribution

Bilge Report writing, input stage theory and calculations.

Nikita Soldering second board, report writing

Michal Breadboard building, soldering first board, input stage design and circuit simulations, report writing.

Patrick Output stage, Simulation and Realization measurements, scheduling, report writing.