Release 14.7 - xst P.20131013 (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.16 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.16 secs

--> Reading design: hybrid\_adder.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "hybrid\_adder.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "hybrid\_adder"

Output Format : NGC

Target Device : xc3s100e-4-tq144

---- Source Options

Top Module Name : hybrid\_adder

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 24

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "hybrid.v" in library work

Module <four\_carry\_lookahead\_adder> compiled

Module <two\_carry\_lookahead\_adder> compiled

Module <hybrid\_adder> compiled

No errors in compilation

Analysis of file <"hybrid\_adder.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <hybrid\_adder> in library <work>.

Analyzing hierarchy for module <four\_carry\_lookahead\_adder> in library <work>.

Analyzing hierarchy for module <two\_carry\_lookahead\_adder> in library <work>.

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\* HDL Analysis \*

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Analyzing top module <hybrid\_adder>.

Module <hybrid\_adder> is correct for synthesis.

Analyzing module <four\_carry\_lookahead\_adder> in library <work>.

Module <four\_carry\_lookahead\_adder> is correct for synthesis.

Analyzing module <two\_carry\_lookahead\_adder> in library <work>.

Module <two\_carry\_lookahead\_adder> is correct for synthesis.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <four\_carry\_lookahead\_adder>.

Related source file is "hybrid.v".

Found 1-bit xor2 for signal <s0>.

Found 1-bit xor2 for signal <s1>.

Found 1-bit xor2 for signal <s2>.

Found 1-bit xor2 for signal <s3>.

Found 1-bit xor2 for signal <p0>.

Found 1-bit xor2 for signal <p1>.

Found 1-bit xor2 for signal <p2>.

Found 1-bit xor2 for signal <p3>.

Unit <four\_carry\_lookahead\_adder> synthesized.

Synthesizing Unit <two\_carry\_lookahead\_adder>.

Related source file is "hybrid.v".

Found 1-bit xor2 for signal <s0>.

Found 1-bit xor2 for signal <s1>.

Found 1-bit xor2 for signal <p0>.

Found 1-bit xor2 for signal <p1>.

Unit <two\_carry\_lookahead\_adder> synthesized.

Synthesizing Unit <hybrid\_adder>.

Related source file is "hybrid.v".

Unit <hybrid\_adder> synthesized.

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HDL Synthesis Report

Macro Statistics

# Xors : 36

1-bit xor2 : 36

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# Xors : 36

1-bit xor2 : 36

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\* Low Level Synthesis \*

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Optimizing unit <hybrid\_adder> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block hybrid\_adder, actual ratio is 2.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : hybrid\_adder.ngr

Top Level Output File Name : hybrid\_adder

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 60

Cell Usage :

# BELS : 36

# LUT3 : 36

# IO Buffers : 60

# IBUF : 37

# OBUF : 23

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Device utilization summary:

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Selected Device : 3s100etq144-4

Number of Slices: 21 out of 960 2%

Number of 4 input LUTs: 36 out of 1920 1%

Number of IOs: 60

Number of bonded IOBs: 60 out of 108 55%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 27.086ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 481 / 23

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Delay: 27.086ns (Levels of Logic = 20)

Source: b<0> (PAD)

Destination: c<4> (PAD)

Data Path: b<0> to c<4>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 2 1.218 0.622 b\_0\_IBUF (b\_0\_IBUF)

LUT3:I0->O 2 0.704 0.482 f1/Mxor\_s1\_Result11 (N3)

LUT3:I2->O 2 0.704 0.526 f1/c21 (f1/c2)

LUT3:I1->O 2 0.704 0.482 f1/c31 (f1/c3)

LUT3:I2->O 3 0.704 0.610 f1/c41 (c\_0\_OBUF)

LUT3:I1->O 2 0.704 0.482 f2/Mxor\_s1\_Result11 (N4)

LUT3:I2->O 2 0.704 0.526 f2/c411 (N01)

LUT3:I1->O 2 0.704 0.482 f2/c31 (f2/c3)

LUT3:I2->O 3 0.704 0.610 f2/c41 (c\_1\_OBUF)

LUT3:I1->O 2 0.704 0.482 f3/Mxor\_s1\_Result11 (N5)

LUT3:I2->O 2 0.704 0.526 f3/c411 (N11)

LUT3:I1->O 2 0.704 0.482 f3/c31 (f3/c3)

LUT3:I2->O 3 0.704 0.610 f3/c41 (c\_2\_OBUF)

LUT3:I1->O 2 0.704 0.482 f4/Mxor\_s1\_Result11 (N6)

LUT3:I2->O 2 0.704 0.526 f4/c411 (N2)

LUT3:I1->O 2 0.704 0.482 f4/c31 (f4/c3)

LUT3:I2->O 3 0.704 0.610 f4/c41 (c\_3\_OBUF)

LUT3:I1->O 2 0.704 0.482 f5/Mxor\_s1\_Result11 (N7)

LUT3:I2->O 1 0.704 0.420 f5/c21 (c\_4\_OBUF)

OBUF:I->O 3.272 c\_4\_OBUF (c<4>)

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Total 27.086ns (17.162ns logic, 9.924ns route)

(63.4% logic, 36.6% route)

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 5.49 secs

-->

Total memory usage is 4534612 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)