



Avnet's Blackfin BF609 DSP
Embedded Vision Starter Kit

Hardware User Guide



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1 Introduction

The purpose of this manual is to describe the functions of FinBoard from Avnet Electronics Marketing. This document includes a description of the hardware features, hardware jumper setups and explanations of the factory test code.

1.1 Description

FinBoard and the Embedded Vision Starter Kit provide a complete development platform for designing and verifying applications based on the Analog Devices Blackfin BF609 dual-core DSP processor. The kit enables designers to use the BF609 DSP with on board standard interface peripherals.

1.2 FinBoard Hardware Features:

FinBoard has the following features and interfaces:

- Analog Devices Blackfin BF609 dual-core 500MHz DSP processor
- 128MB DDR2 SDRAM
- 32Mb Quad SPI FLASH
- Aptina MT9M114 HD 720p CMOS Color Image Sensor
- 2 OSRAM High Intensity LEDs for target illumination + 2 unpopulated pads for additional LEDs
- National Semiconductor DP83848J 10/100 Ethernet Phy
- uSD Flash memory card interface
- 4GB microSD card with SD adapter
- ADV7511 HDMI video transmitter
- 5 programmable user LEDs
- 2 user programmable pushbutton switches
- 2 user programmable slide switches
- USB-OTG Mini B interface
- USB-UART Mini B interface for serial terminal console
- ADM1032 Temperature Sensor
- IDT5V9885T programmable clock synthesizer with spread-spectrum capability
- Tripod mount
- Analog Device's ICE-100B JTAG emulator and debug interface

1.3 Test Files

The evaluation kit comes pre-programmed with bootable factory test software programmed in QSPI flash and a user application (such as VisionDotCount) in the uSD card. Please refer to <http://www.finboard.org> for the latest application software. This is provided as an aid for the design engineer to confirm board functionality and assist in the development effort of new applications. These programs test and confirm the functionality of the following interfaces/peripherals:

- ADSP-BF609 (both cores) including the Pipelined Vision Processor (PVP)
- Aptina MT9M114 Camera
- DDR2 SDRAM
- QSPI Flash
- USB-UART
- 10/100 Mb Ethernet
- uSD CARD
- HDMI 720p video output
- OSRAM HB LEDs
- User Pushbuttons

Updated test files for FinBoard are available at <http://www.finboard.org>.

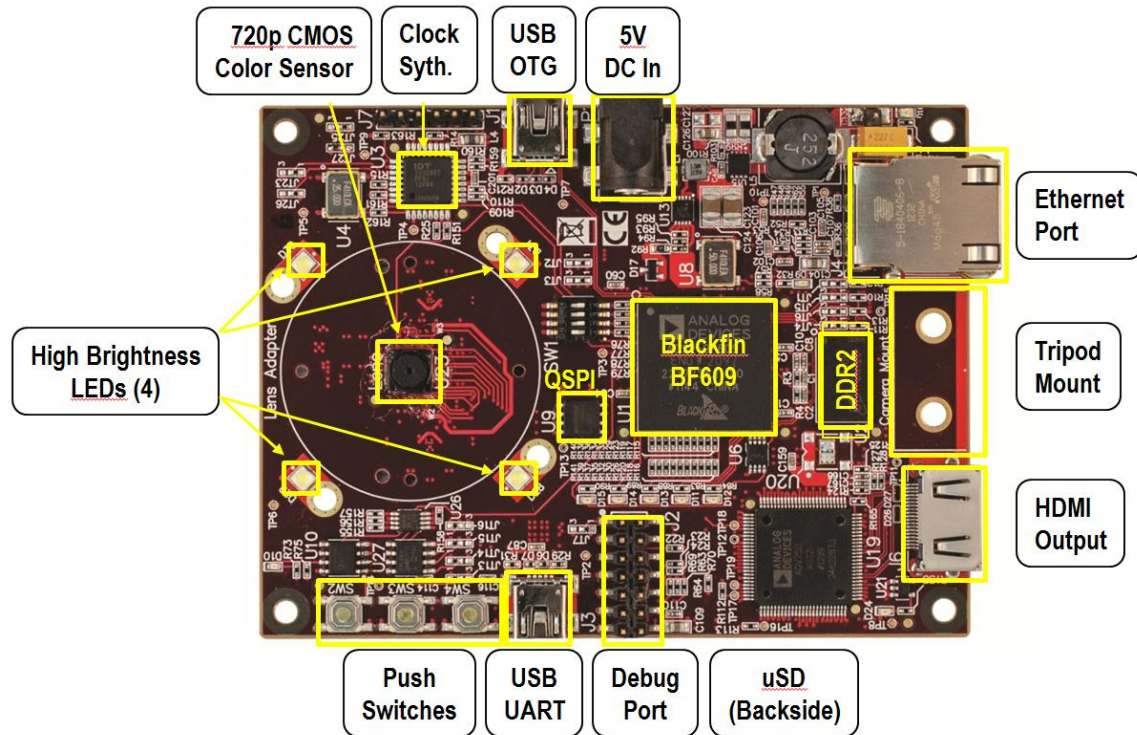


Figure 1: BF609 DSP Evaluation Board

2 Topology and Interfaces

A high-level block diagram of the Board is shown below. This will be followed by a more detailed functional description of the items contained in the diagram.

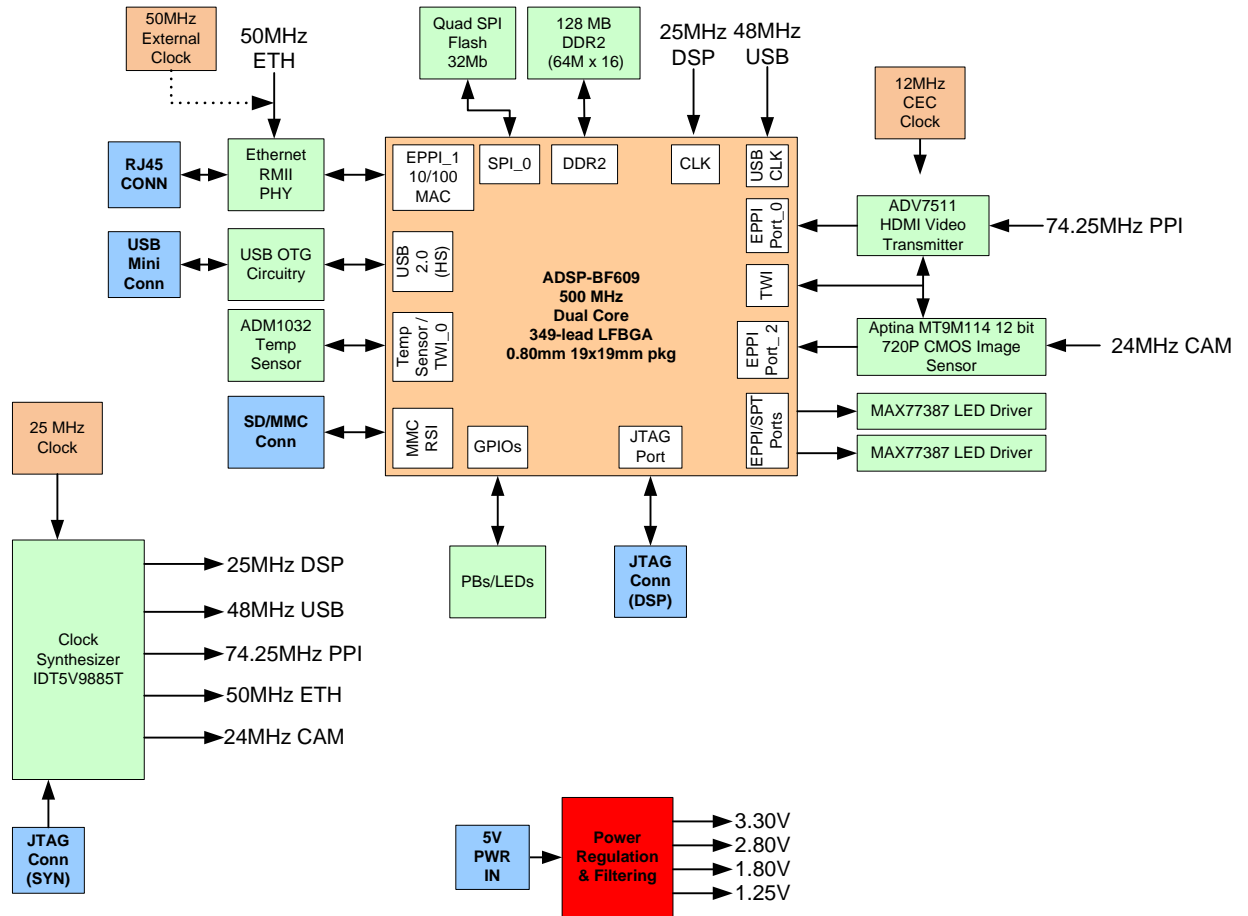


Figure 2: BF609 FinBoard DSP Evaluation Kit Block Diagram

2.1 BF609 dual-core embedded DSP

The ADSP-BF609 is a 500MHz dual-core high performance DSP with embedded peripheral controllers that make it ideal for a number of I/O and processing intensive applications, including vision analytics. For detailed BF609 processor information (latest datasheets, application notes, tutorials, community development, etc...) please visit the product website at: <http://www.analog.com/bf609>

2.2 Internal BF609 Memory:

1. Each core of the BF609 contains 148KB of L1 data/instruction SRAM with multi-parity bit protection.
2. The BF609 die also contains 256KB of L2 SRAM with ECC protection and a 32KB boot and safety function ROM.

2.3 FinBoard Memory:

1. DDR2 SDRAM - the FinBoard uses a single Micron MT47H64M16 8M x16 x 8 (1Gb) DDR2 SDRAM IC which is accessed via the BF609's 16 bit Dynamic Memory Controller interface.
2. Bootable microSD Card interface – a high speed 4 bit wide microSD card interface is placed on the bottom of the PCB. This is where large custom applications can be easily placed. The BF609 is also able to boot from the microSD interface. The maximum addressing space is 8 Gigabytes for the microSD card.
3. Bootable Quad SPI memory - A 32Mb Winbond W25Q32BVSSIG QSPI FLASH memory IC is installed on the FinBoard. This memory can be used to boot from and store custom applications without the need to use the microSD card slot. By default this memory has Avnet's Power On Self Test program installed for developers convenience. See the section on POST for further information on how to interface to the POST program via a terminal program.
4. Non-Bootable Camera EEPROM – 24LC64B. This MicroChip Technology 24LC64B-I/SN device is used to store the Aptina MTM114 HD camera factory configuration and calibration values. By default these values do not require user adjustments. If user adjustments are desired, refer to the schematic for address selection (default is 0xA4 for read) and the MTM114 Datasheet for detailed information.

2.4 BF609 DSP JTAG Header:

J2 header is connected directly to the BF609 processor for code download and debug purposes. The interface provides easy access for debugging development code and to perform QSPI FLASH programming. The connector pin out is based on Analog Devices ICE-100B emulator.

JTAG-DSP (J2)			
Connection	Pin #		Connection
GND	1	2	EMU_N
GND	3	4	GND
10K PU	5	6	TMS
GND	7	8	TCK
GND	9	10	TRST_N
GND	11	12	TDI
GND	13	14	TDO

Table 1: ICE 100B DSP JTAG connection

Please refer to the schematic for further information.

2.5 10/100 Ethernet

The BF609 FinBoard evaluation kit provides the user with the ability to communicate with 10/100 Ethernet networks. The PHY is a National DP83848J and is connected to the BF609 DSP via RMII.

The default base PHY address is 00001 and is selectable via JT9. Please see [Table 6: Jumper Terminal \(JT\) Table](#) and refer to the schematic for further information.

2.6 USB-OTG Interface – Host, Power, and Slave

1. The USB 2.0 On-The-Go (OTG) dual-role interface allows the FinBoard to act as a USB host to other USB slave devices such as USB flash drives, cameras, MP3 players, cellphones, etc.... This direct USB to slave connection allows the FinBoard to perform data I/O operations without the need for a PC. In Host mode the port also provides the necessary slave device power (+5.0V, <500mA) and enumeration protocols.
2. USB-OTG FinBoard power option: The FinBoard can also be powered through the USB-OTG interface if desired. The power limit is 500mA and therefore the High Bright LEDs in the FLASH mode should not be used. To put the FinBoard into USB Only power mode, place R170 with a 0 ohm resistor and do not use the wall power supply adapter to power the board.
3. When not in the Host Mode, the FinBoard acts as a slave device to an attached USB Host such as a PC. In Slave mode the FinBoard will enumerate and provide data I/O operations.

2.7 BF609 and Ambient Temperature Sensor

The FinBoard has an onboard Analog Devices I2C ADM1032 user programmable temperature sensor IC. This IC is used to measure ambient temperature and to initiate two user defined threshold alarm signals. The IC is located at address 0x4C.

1. ALERT_N (TEMP_IRQ_N) signal is asserted when the temperature measurements are out of a defined range. The signal is connected to the BF609 as an interrupt and an ISR can be initiated upon occurrence.
2. The THERM_N (TEMP_THERM_N) signal is asserted when the temperature measurements reach the programmed trip value. This signal is connected to the BF609 via the TWI0 interface for monitoring and also drives LED D15, which illuminates when the signal is asserted.

2.8 High Bright LEDs

FinBoard has the ability to run four High Bright (HB) OSRAM OSOLON series LEDs for target illumination and flash applications. Two LEDs (D28 & D30) are populated by default, while D29 & D31 are left open for the user to experiment with. The default LEDs are OSRAM OSOLON LCW CR7P.PC-LQLS-5H7I-1 LEDs. Each LED is configured to be run in parallel mode (see Maxim 77387 LED driver section).

Locations D29 & D31 can be populated with the same LEDs for greater illumination of target, but will require JT10 and JT12 to be placed at locations 2-3. See JT10 & JT12 section for further information.

In addition to using the default white LCW CR7P.PC-LQLS-5H7I-1 LEDs, a user can select infrared LEDs (OSOLON Black 850nm SFH 4715 series) or different color temperature LEDs (OSOLON SSL LUW CQ7P series) for night vision applications.

2.9 MAXIM 77387 High Bright LED Boost Mode Driver IC

The MAX77387 LED driver IC is used to drive the High Bright LEDs in two modes of operation, Torch and Flash. The IC is designed in as a boost controller and features the ability to drive the LEDs in PWM or DAC mode. The default mode that FinBoard uses is DAC and Torch mode. See the Maxim datasheet for comprehensive information and application notes. www.maximintegrated.com

2.10 HDMI Port

FinBoard has an HDMI video output port, and can be used to drive a monitor with the on board Aptina camera image. This port is based on the Analog Devices ADV7511 HDMI transmitter IC, capable of transmitting 1080p resolution video. Please refer to Analog Devices ADV7511 datasheet, Hardware User's Guide and Programming guide at www.analog.com for detailed information. The IC is configured via the I2C interface at address 0x72, based on the PD pin being pulled low.

2.11 720p HD Camera - Aptina MT9M114 CMOS image sensor

FinBoard's on board camera uses Aptina's 720p HD MT9M114 CMOS image sensor configured in 8 bit YCbCr interleaved mode. Please refer to the Aptina online documentation for further details at www.aptna.com.

2.12 Programmable Clock Synthesizer

FinBoard uses Integrated Device Technologies (IDT) IDT5V9885TPFGI I2C user programmable clock synthesizer for on-board clock generation. This part allows the user to program multiple clock outputs in various configurations, including spread spectrum. The primary input clock is provided by U4, a 25.0000 MHz clock IC. The default synthesizer output frequencies are listed in Table 2, below.

IDT5V9885 Synthesizer	
Output Frequency (MHz):	Clock Function:
25.0000	System
48.0000	USB
24.0000	Camera
74.2500	PPI
50.0000	Ethernet

Table 2: IDT Synthesizer values

2.13 USB-UART interface

FinBoard provides a USB-UART connection through the mini-B USB connector J3. This port connects to a Silicon Labs CP2102 USB-UART transceiver IC and the BF609 UART to provide debug and monitoring purposes during design development.

This port is the primary port for interfacing to the POST application factory loaded onto the QSPI Flash. While the Si Labs CP2102 part can operate in all standard RS-232 modes up to 1Mb/s, Avnet's default port configuration is 9600 bps, 8, N, 1. Please refer to Silicon Labs CP2102 datasheet for further information. The Si Labs CP2102 driver can be downloaded from Si Labs website, www.silabs.com or <http://www.silabs.com/products/mcu/pages/usbtouartbridgevcpdrivers.aspx>

3 Configuration and Switch settings

3.1 Switch 1 Boot Mode and User Inputs

The dip Switch SW1 is used to select the boot mode of the BF609 processor. The chart below shows the required switch setting to enable each mode with the factory default being highlighted in green.

SW1.1 Boot Mode Select	
Mode	SW1.1
Boot from on-board QSPI (SPI)	on
Boot from uSD Card (RSIO)	off

Table 3: Boot Mode Selection table

The remaining positions on Switch 1 Table 4 (SW1: .2, .3, & .4) are user selectable switches. These are attached to GPIO on the BF609 and can be programmed to meet customer needs. The default position for these switches are closed (pulled down via 10K ohm resistor). When in the “on” position they provide a +3.3V logic high to the BF609 GPIO pin. See schematic for further information.

SW1: .2, .3, .4 Switches		
Signal Name:	Switch 1 position:	BF609 GPIO Pin:
USER_SW0	SW1.2	PA13/PPI2_D13/LP1_D5
USER_SW1	SW1.3	PA14/PPI2_D14/LP1_D6
USER_SW2	SW1.4	PA15/PPI2_D15/LP1_D7

Table 4: Switch 1 User signals table

3.2 Pushbutton SW2, SW3, SW4

There are three pushbutton switches on FinBoard. SW2 is used as a global reset and cannot be remapped for general use. See the below table for functions during specific application execution.

Pushbutton Switch	POST Function:	Vision App function:
SW2	Reset	Reset
SW3	“0” Input	Edge Detection Enable
SW4	“1” Input	HB LED Intensity select

Table 5: Pushbutton Switch functions

3.3 Jumper Terminal (JT) configurations

There are 27 configurable Jumper Terminals (JT) on the Finboard. See Figure 3. The JTs are used to customize the electrical functionality of the board. Each JT is made of a three position 0402 resistor pad array and can be populated with a user's resistor for custom configuration purposes.

The default JT configuration values are shown in the below table. Detailed JT descriptions for user configurable jumpers are in the appropriate sections within this document and on the schematic diagram.

NOTE: Incorrect placement of these jumpers can cause board malfunction or damage and it is recommended only advanced users modify the settings from the factory default.

JT#:	Function:	Default Pads:	Alternate Pads:	Description:
1,4	I2C TWI MUX selection	1 – 2	2 – 3	Change TWI0 to TWI1. Default is TWI0.
5,6	I2C TWI HDMI selection	1 – 2	2 – 3	Change TWI0 to TWI1. Default is TWI0.
7	JTAG DSP Pulldown	1 – 2	2 – 3	ICE-100B Pin 1 pull up or down. Default is pulled down.
8	USB Reset voltage	1 – 2	2 – 3	USB_UART Vdd or board +3.3V. Default is USB_UART Vdd.
9	Ethernet PHY Address	1 – 2	2 – 3	Select PHY ADDR: 00001 or 10001. Default is 00001
10,12	HB LED Series or Parallel drive	2 – 3	1 – 2	D28/D30 parallel driven OR D28/29/30/31 series driven. Default is D28/30 parallel driven.
11,19	MAX77387 Thermistor	1 – 2	2 – 3	Temperature monitoring via thermistors. Default is no temperature monitoring.
13	EEPROM Write Protect	1 – 2	2 – 3	EEPROM writable or not writable. Default is writable.
14,15,16	EEPROM Address	1 – 2	2 – 3	EEPROM Address select. Default is 0xA4.
17	Aptina MT9M114 ADDR	1 – 2	2 – 3	Camera Address select – 0x90 or 0xBA. Default is 0x90.
18	Aptina MT9M114 Config	1 – 2	2 – 3	Allow configuration of device via I2C interface. Default is allow configuration.
20, 21, 24	IDT Clock Synthesizer configuration	open	Any	JTAG or I2C programming pins for synthesizer. Default is I2C configures synthesizer at factory.
22	JTAG TMS pullup	2 – 3	1 – 2	Default is 10K placed 2 – 3 for TMS pullup.
23	Synthesizer suspend	1 – 2	2 – 3	Suspend the synthesizer. Default is synthesizer on.
25	Synthesizer Clock input select	1 – 2	2 – 3	Selects clock input type: clock or crystal/ref_in. Default is clock input.
26	Synthesizer Output Enable	1 – 2	2 – 3	Enable or disable all outputs. Default is enable all outputs.
27	Synthesizer I2C or JTAG	1 – 2	2 – 3	Configuration mode for synthesizer. Default is a 10K resistor and I2C configuration.

Table 6: Jumper Terminal (JT) Table

The Jumper Terminals used to configure the electrical functionality of the FinBoard have the following attributes: 0402 size, and pin 1 has a silkscreen box around it. The default setting is typically pads 1-2 populated with 0 ohm resistor, but please reference Table 6 for complete configuration information.

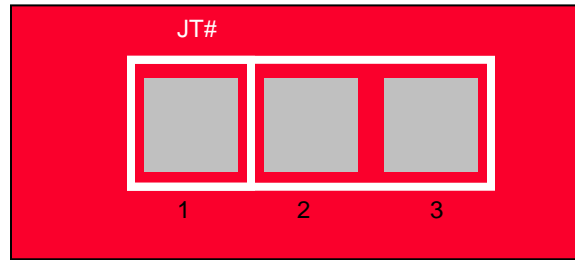


Figure 3: Jumper Terminal Pad layout

3.4 JT13 – JT18

JT13-JT18 are used to configure the I2C device addresses. The table below shows the default production addresses. See schematic diagram for further information.

I2C Slave Address Map:	
SEEPROM	= 0xA4
Temp Sensor	= 0x4C
Camera	= 0x90
MUX:	
MAX77387	= 0xE0
MAX77387	= 0x94
Clock Synthesizer	= 0xD4

Table 7: I2C Memory map

3.5 JT11 & JT19 – NTC – Negative Temperature Coefficient Thermistors

JT11 and JT19 are 0402 footprints arranged in a Single Pole Dual Throw switch configuration. The user can place a Negative Temperature Coefficient thermistor (NTC) between pins 2 and 3 on each JT to monitor the selected MAX77387 High Bright LED driver temperatures. The NTC provides a nonlinear voltage response to temperature. As the temperature rises, the resistance decreases, thereby reducing the voltage sensed across it. The MAX77387 NTC pin sources 200uA to bias the thermistor for the voltage development. The NTC voltage developed across the thermistor is compared to the user defined trip threshold programmed by the NTC_CNTL register.

Default configuration is a zero ohm resistor placed between pins 1 and 2, thereby bypassing the thermal sensing. See Maxim Semiconductors MAX77387 data sheet for recommended NTCs and detailed information. www.maximintegrated.com.
Error! Reference source not found.

Figure 4: High Brightness (HB) LED drive circuit - 1 of 2

3.6 JT10 & JT12 – High Bright LED configuration

JT10 and JT12 are 0402 footprints arranged in a Single Pole Dual Throw switch configuration. Each jumper performs the same serial or parallel drive function with each MAX77387 driver IC and LEDs. JT10 selects whether LED D28 is driven in parallel (outputs FLED1 and FLED2 drive a single LED) or if both LEDs D28 and D29 are driven by U22. LED D29 is not populated by default and therefore only LED 28 is driven. The same configuration is implemented with JT12 and its respective LEDs D30 and D31.

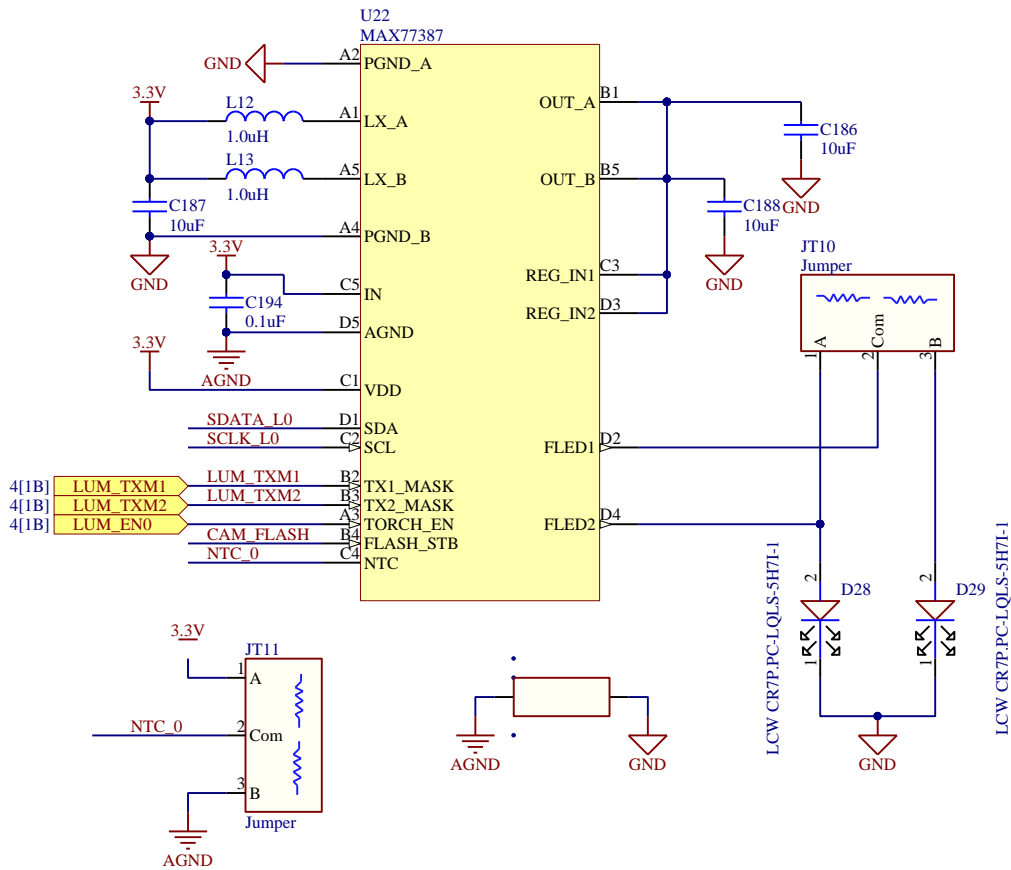


Figure 5: High Brightness (HB) LED drive circuit – 2 of 2

3.7 System LEDs

There are four user programmable amber LEDs on FinBoard (D11 – D14). These LEDs are provided for the design engineers' use and to display some POST status at various test points during POST operation.

1. Temperature LED – D15 is used to indicate a user programmable temperature event set in the ADM1032 Temp Sense IC.
2. Board Power LED - D16. A green LED used to indicate the presence of +3.3Volts
3. Reset LED – D10. A RED LED indicating a power reset or user reset has occurred. Extinguishes after the reset event has occurred. This LED is driven by the Analog Devices ADM708RARZ voltage monitor IC.
4. Ethernet LED – D9. A green LED indicating DP83848 Phy IC functionality.
5. Ethernet Jack LEDs – Green indicates Ethernet Link and Amber indicates Ethernet link activity.
6. HDMI LED – D24. An amber LED is used to indicate the presence of a valid HDMI connection and is driven by the ADV7511 HDMI transmitter IC.
7. USB-UART LED – D8. An amber LED is used to indicate a USB connection has been made. This LED is located on the bottom of the board under the USB-UART connector, J1.

4 Power On Self Test (POST) interface and setup

The POST application provides the user the ability to test some of the hardware interfaces of FinBoard. The POST is factory installed onto the QSPI Flash on FinBoard and is accessed using a standard serial terminal interface such as TeraTerm or HyperTerminal running on a host PC and the USB-UART connection on FinBoard. Below is a detailed description of how to access the POST.

4.2 POST Setup:

NOTE: you will need to build or purchase an RJ-45 Ethernet loopback cable for the POST to pass the Ethernet test. See Table 8 and Table 9 for Ethernet wiring.

1. Place FinBoard on a flat, stable surface.
2. Move the switch SW1.1 to the “ON” position for QSPI boot. Remaining SW1 switches should be in the “OFF” position.
3. Apply power to the board via P1, +5.0V, 2.0A wall power adapter. Observe the following LED illumination:
 - i. LED D9 & D11 – Green LEDs should illuminate upon plug-in.
 - ii. LED D10 – RED LED remains on during SW2 reset depression while D9 extinguishes.
 - iii. Attach HDMI cable, LED D24 – Amber LED turns on.
4. Attach USB cable to J3 and the PC.
5. Open a serial terminal on the host PC, such as TeraTerm or HyperTerminal. Set the com port to 9600, 8, N, 1. Save if necessary. See [Figure 6: Initial Power On Self Test screen](#)
6. Install the Ethernet Loopback cable to J4.
7. Attach an HDMI cable to J6 and attach to the monitor.
8. Power on the monitor and make sure it's set to HDMI input mode. No image will appear on the HDMI monitor while performing POST testing. However, the monitor should indicate a device is attached. Typically this will be the monitor power LED changing color from amber or red to green.
9. Follow the instructions in section 4.3 to execute a POST test.

Reference Ethernet loopback cable wiring for POST test:

Pin	Name
1	TX_D1+
2	TX_D1-
3	RX_D1+
4	BI_D3+
5	BI_D3-
6	RX_D2-
7	BI_D4+
8	BI_D4-

Table 8: RJ45 Pins

4.4 POST HB LED Test:

CAUTION: Do NOT look directly at the LEDs without proper UV eyewear protection or LED UV diffusion (paper or something similar over the LEDs).

4. At the AES> prompt type: “led 1” and press enter. Observe white HB LEDs D28 and D30 to turn on. You can set the value from 1 to 7, increasing LED brightness each time the number is entered. Type “led 0” to turn off the HB LEDs.
5. At the AES> prompt type: led 0 to turn off the LEDs.

```

COM6:9600baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help

*****
~~~ AVNET BF609-EVSK Power-On Self-Test
*****
Built on Mar 27 2013, at 10:42:09
Firmware version: 1.0

AES> led 1
Setting LED intensity to 1
AES> led 7
Setting LED intensity to 7
AES> led 0
Setting LED intensity to 0
AES>

```

Figure 7: POST LED intensity test

4.5 POST Standard Loop Test:

1. At the AES> prompt type “test”, press enter and follow the on screen prompts. Pressing SW3 five times will enter five pink zeros as shown in [Figure 8: all POST tests selected](#). This will execute all factory POST tests. The successful POST results are shown in [Figure 9: Successful POST screen](#).

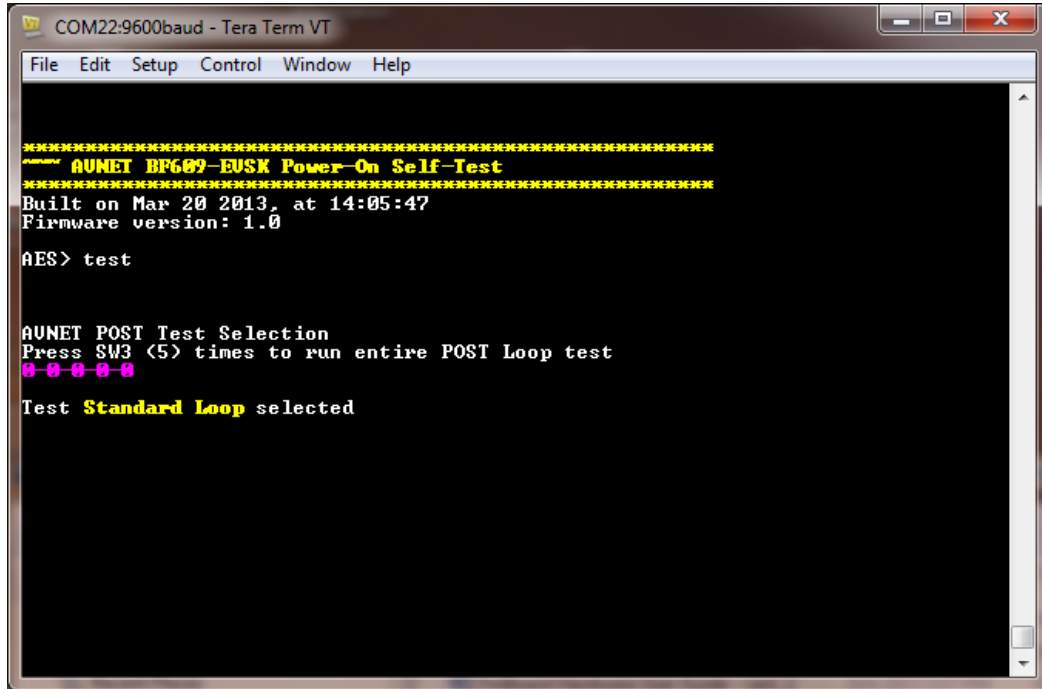


Figure 8: all POST tests selected

```

*****
Manufacture ID: 0x41

Read Temperature Value
Temperature: 95.0 deg F

Init remote temperature is: 41.625 degrees C
Test Passed
Temp Sensor: pass 1 fail 0

*****
~~~ Ethernet Test
*****

Test Passed
Ethernet: pass 1 fail 0

POST stats:

=====
TEST NAME      PASS  FAIL  STD LOOP  ONE TIME  IGNORE
=====
Proc Version   1      0      1          1          1
Pushbuttons/LED 0      0      0          0          1
  UART         0      0      0          0          1
    Rotary     0      0      0          0          1
  SPI Flash    0      0      0          0          1
    SD         1      0      1          1          1
DDR Memory Test 0      0      0          0          1
Not Used #8     0      0      0          0          1
Temp Sensor     1      0      1          1          1
Test CAN RX     0      0      0          0          1
Test CAN TX     0      0      0          0          1
  Ethernet     1      0      1          0          1
Display FW Ver  0      0      0          0          1
Not Used #17    0      0      0          0          1
Not Used #18    0      0      0          0          1
Display Status  0      0      1          1          1
Not Used #20    0      0      0          0          1
Toggle LoopFlag 0      0      1          0          1

Display Status: pass 1 fail 0
Test loop flag state changed to 1
Toggle LoopFlag: pass 1 fail 0
Standard Loop: pass 1 fail 0
POST Complete - Check FAIL Results
AES>
  
```

Figure 9: Successful POST screen

2. After the POST completes execution, ensure there are no **RED** fail indicators. If all green, POST has passed.

3. Specific POST tests can be selected and executed using Table 10: POST Test selections. Please note SW3 is logic “0” and SW4 is logic “1”.

Test Name:	Pushbutton Sequence:
Standard Loop	0-0-0-0-0
Test Version	0-0-0-0-1
Test Tempsense	0-1-0-0-1
Test Ether(net)	0-1-1-0-0
Display POST Status	1-0-0-0-0
Toggle Loop Flag	1-0-0-1-0

Table 10: POST Test selections

4.6 POST IDT Synthesizer configuration:

NOTE: Use this command line to confirm the factory values or to re-program the synthesizer and confirm the changed values. Incorrect use of this utility can cause your board to become non-operational, therefore it is strongly recommended a backup of the original synthesizer values is saved.

1. At the AES prompt, type “idt program” and press enter.
2. At the AES prompt, type “idt verify” and press enter.
3. Observe the “Passed!” prompt. See below - Figure 10: IDT Synthesizer programmed

```

COM6:9600baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
*****
Built on Mar 27 2013, at 10:42:09
Firmware version: 1.0

AES> idt program
Programming IDT with factory defaults
Committing to IDT firmware
0x00 : 0x00 0x00 0x00 0x00 0x00 0xFF 0x30 0x00
0x08 : 0x15 0x00 0x00 0x00 0xFF 0x00 0x00 0x00
0x10 : 0x19 0x00 0x00 0x00 0x2E 0x00 0x00 0x00
0x18 : 0x30 0x00 0x00 0x00 0x20 0x40 0x00 0x10
0x20 : 0x3E 0x00 0x00 0x00 0x74 0x00 0x00 0x00
0x28 : 0x0A 0x00 0x00 0x00 0x93 0x00 0x00 0x00
0x30 : 0x20 0x00 0x00 0x00 0x47 0xB9 0x00 0x00
0x38 : 0x63 0x00 0x00 0x00 0x22 0x00 0x00 0x00
0x40 : 0x01 0x00 0x00 0x00 0x30 0x00 0x00 0x00
0x48 : 0x00 0x00 0x00 0x00 0x10 0xBD 0x01 0x00
0x50 : 0x10 0xBA 0x03 0x00 0x10 0xBF 0x00 0x00
0x58 : 0x10 0xBB 0x02 0x00 0x13 0xBB 0xEF 0x00
0x60 : 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x68 : 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

AES> idt verify
Reading IDT firmware
Verifying IDT firmware against factory defaults
0x00 : 0x00 0x00 0x00 0x00 0x00 0xFF 0x30 0x00
0x08 : 0x15 0x00 0x00 0x00 0xFF 0x00 0x00 0x00
0x10 : 0x19 0x00 0x00 0x00 0x2E 0x00 0x00 0x00
0x18 : 0x30 0x00 0x00 0x00 0x20 0x40 0x00 0x10
0x20 : 0x3E 0x00 0x00 0x00 0x74 0x00 0x00 0x00
0x28 : 0x0A 0x00 0x00 0x00 0x93 0x00 0x00 0x00
0x30 : 0x20 0x00 0x00 0x00 0x47 0xB9 0x00 0x00
0x38 : 0x63 0x00 0x00 0x00 0x22 0x00 0x00 0x00
0x40 : 0x01 0x00 0x00 0x00 0x30 0x00 0x00 0x00
0x48 : 0x00 0x00 0x00 0x00 0x10 0xBD 0x01 0x00
0x50 : 0x10 0xBA 0x03 0x00 0x10 0xBF 0x00 0x00
0x58 : 0x10 0xBB 0x02 0x00 0x13 0xBB 0xEF 0x00
0x60 : 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
0x68 : 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00

Passed !
AES>

```

Figure 10: IDT Synthesizer programmed

4.7 SD Card Application

The microSD card included with FinBoard is pre-loaded with a bootable vision application. This application passes the video from the on-board camera to the HDMI output. The application also uses an edge detection algorithm to show dice dot counts based on the target dice. For further application information, please see the Getting Started Guide available for download at www.FinBoard.org.

SD Card video loopback execution:

1. On FinBoard, move the switch SW1.1 to the “OFF” position for SD card boot.
2. Remove P1 power from the FinBoard.
3. Place the programmed microSD card in the J5 slot.
4. Re-attach P1 power to FinBoard.
5. Observe LEDs D28 and D30 to illuminate.
6. Observe the camera image to be displayed on the HDMI monitor.
7. Press SW4 seven times to rotate through the LED intensity settings.

4.8 Non Populated component locations

There are a few locations on the production board where components are not populated. These locations are provided for the design engineer to try different options in place of the current design. The removal of these components in no way affects the board's advertised operability or performance.

1. P2 and J7:

These connections are used to program the IDT clock synthesizer using an external JTAG programmer. In normal operation these should not be used. The design engineer can program the IDT synthesizer using the clock programming reference design found on the www.FinBoard.org website.

2. Clocks:

FinBoard has two non-populated clock locations.

1. One is for the 12MHz CEC clock. This clock is derived from the BF609 and therefore is not required for normal operation. To achieve custom HDMI resolutions, a clock can be placed in this location to change the CEC frequency of the ADV7511 HDMI IC as necessary. Please refer to the Analog Devices ADV7511 datasheet for application recommendations. <http://www.analog.com/en/audiovideo-products/analoghdmi-interfaces/adv7511/products/product.html>
2. The second depopulated clock is the 50MHz Ethernet clock. This clock is derived from the IDT Clock Synthesizer and is therefore not required for normal operation. The option to put a clock in this location has been determined to be beneficial if a user would like to evaluate a discrete clock solution for their application. This may be desirable to ensure CE and FCC emission compliance in the event of long signal trace runs or to eliminate signal integrity issues on a custom board. See the schematic for further information and population options.

4.9 FinBoard Power

FinBoard includes a Universal AC wall adapter power supply for the main power input. The input requirements for the board are +5.0 VDC, +/-10%, 2.0 Amperes. The provided power supply (2.5 Ampere version as of this writing) has been confirmed to meet all national and international compliance regulations.

1. Power Domains:

The FinBoard uses multiple on-board regulators to generate the required voltage domains and tolerances for the specific functional areas. It is recommended the same components be used for custom designs to ensure performance and EMI compliance. Refer to the schematic for specific implementation details. For further information, refer to each power component's manufacturer's datasheet and application notes.

2. Power filtering:

To ensure proper operation and performance of new designs, it is **highly** recommended the power supply filtering methods used in this reference design be used exactly as designed. Not doing so may lead to poor system performance and/or non-compliance to regulatory requirements.

4.10 Fundamental FinBoard and ADI EZKit differences

There are many circuit design differences between the Avnet FinBoard and Analog Devices BF609 EZ-Board reference designs. However, there are only two major configuration differences. One is the use of a clock synthesizer IC (IDT5V9885) and the second is a PPI port change for the Camera and the HDMI ports. Below is a description of the changes:

1. IDT Clock Synthesizer:

This clock synthesizer has been placed to eliminate the need for multiple fixed frequency discrete clock ICs (reducing board cost). Using this IC also allows the design engineers the opportunity to program different clock frequencies to meet their design goals without having to change fixed frequency clock ICs. For more information please refer to section 2.12.

2. PPI Port changes:

The Analog Device's BF609 EZ Board Ports are as follows:

- PPI0 (P1A): ADV7511 Video Encoder E13 Extender Board
- PPI1 (P2A): Aptina MTM114_55CSP_DemoHead

The BF609 FinBoard Ports are as follows:

- PPI0 (P1A): Direct connect to ADV7511 Encoder IC
- PPI2 (P3A): Direct connect to Aptina MTM114 IC in 8 bit mode.

3. Additional Hardware changes from BF609 EZ Board:

- SW2 Rotary Boot switch – removed and replaced with SW1 dip switch
- UART 0 DCE DB9 connection – removed and replaced with mini USB connector
- CAN 0 – removed
- Rotary Encoder – removed
- Link Port 0 / JTAG OUT – removed
- Link Port 1 / JTAG IN – removed
- SoftConfig Switches and I/O extender ICs – removed. Replaced with Jumper Terminals and SW1.
- Unused PPI ports P1B, P1C, P2A– not populated