

DDR2 end of line terminators and VTT tracking circuit have been omitted since overall trace length is less than 2.5" per net.  
For custom designs please adhere to all EE-notes from ADI and and recommendations by the memory manufacturer.

DDR2 single-ended traces are 50 Ohms impedance  
DDR2 Differential traces are 100 Ohms differential impedance

Differential termination resistors are located near load.  
On Die Termination (ODT) is used for data lines.

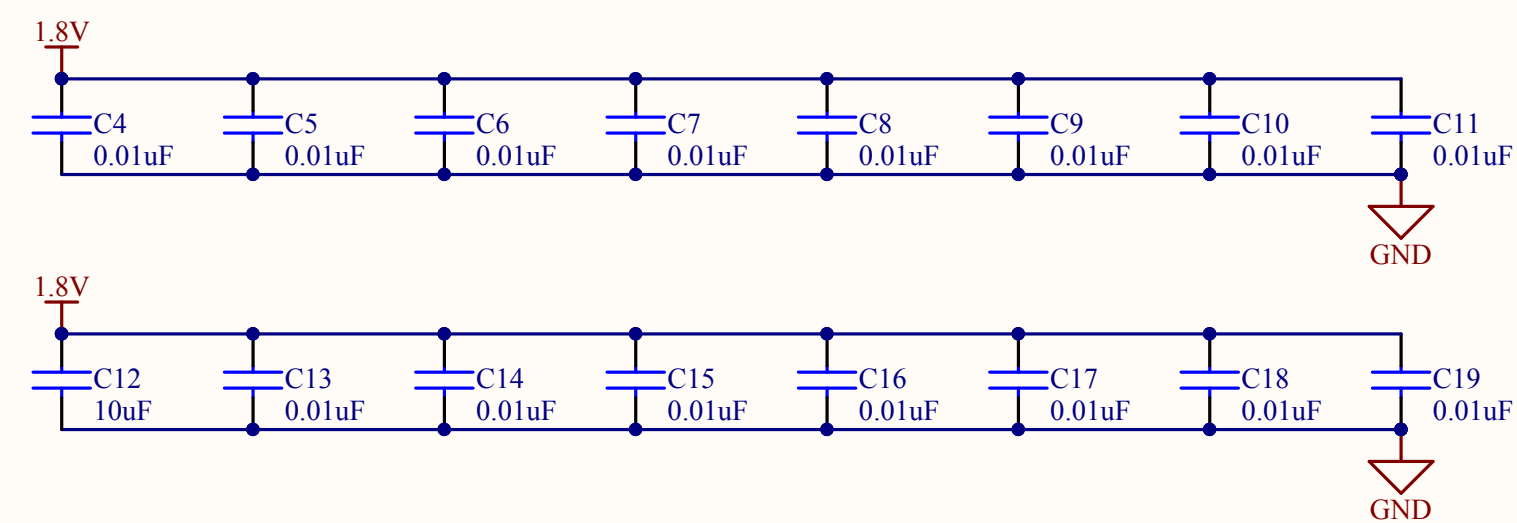
It is recommended all DDR RAM traces are matched length and less than 2500 mils. The below information is general guidance and is pending the FR4 board material composition and stack up.

Address and command trace spacing is 10 mil min for short runs, 4 mils clearance for parallel runs less than 500 mils.

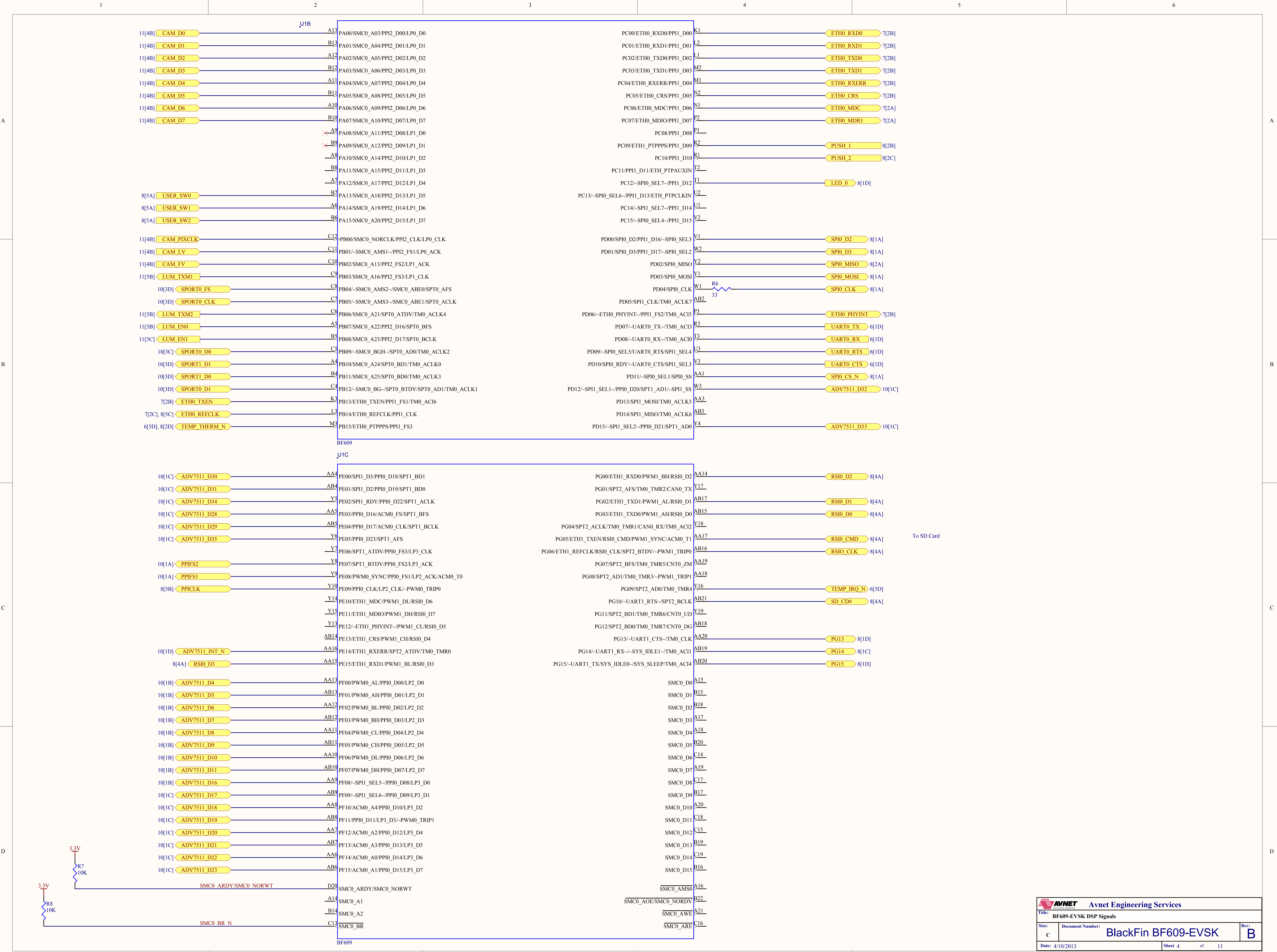
Data trace spacing is 10 mil min for short runs, 4 mils clearance for parallel runs less than 500 mils.

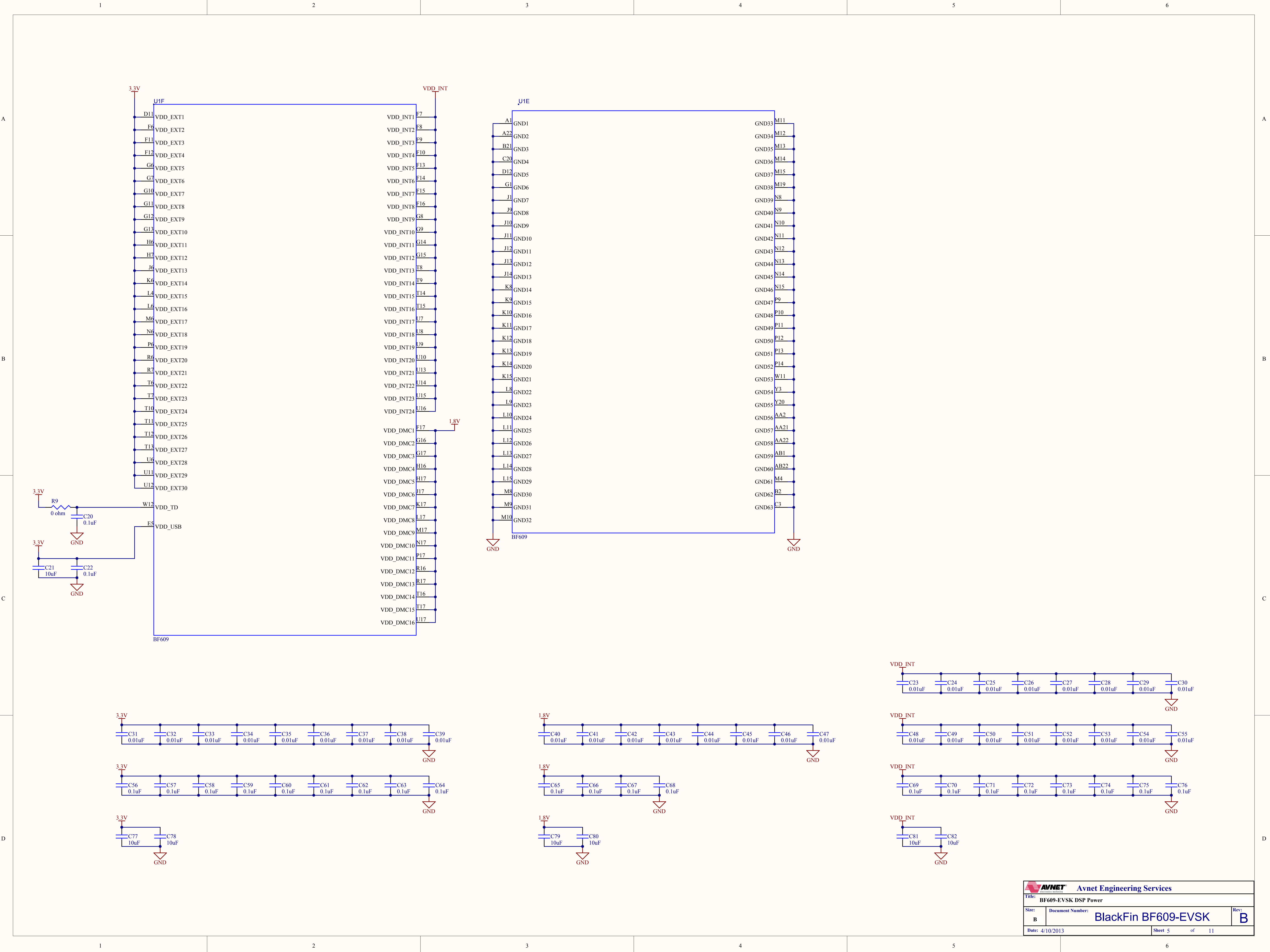
Clock pairs should be equivalent within +/- 20 mil.  
Clock and DQS should be length matched.

Clock to Address / Control should be matched within +/-400 mil.



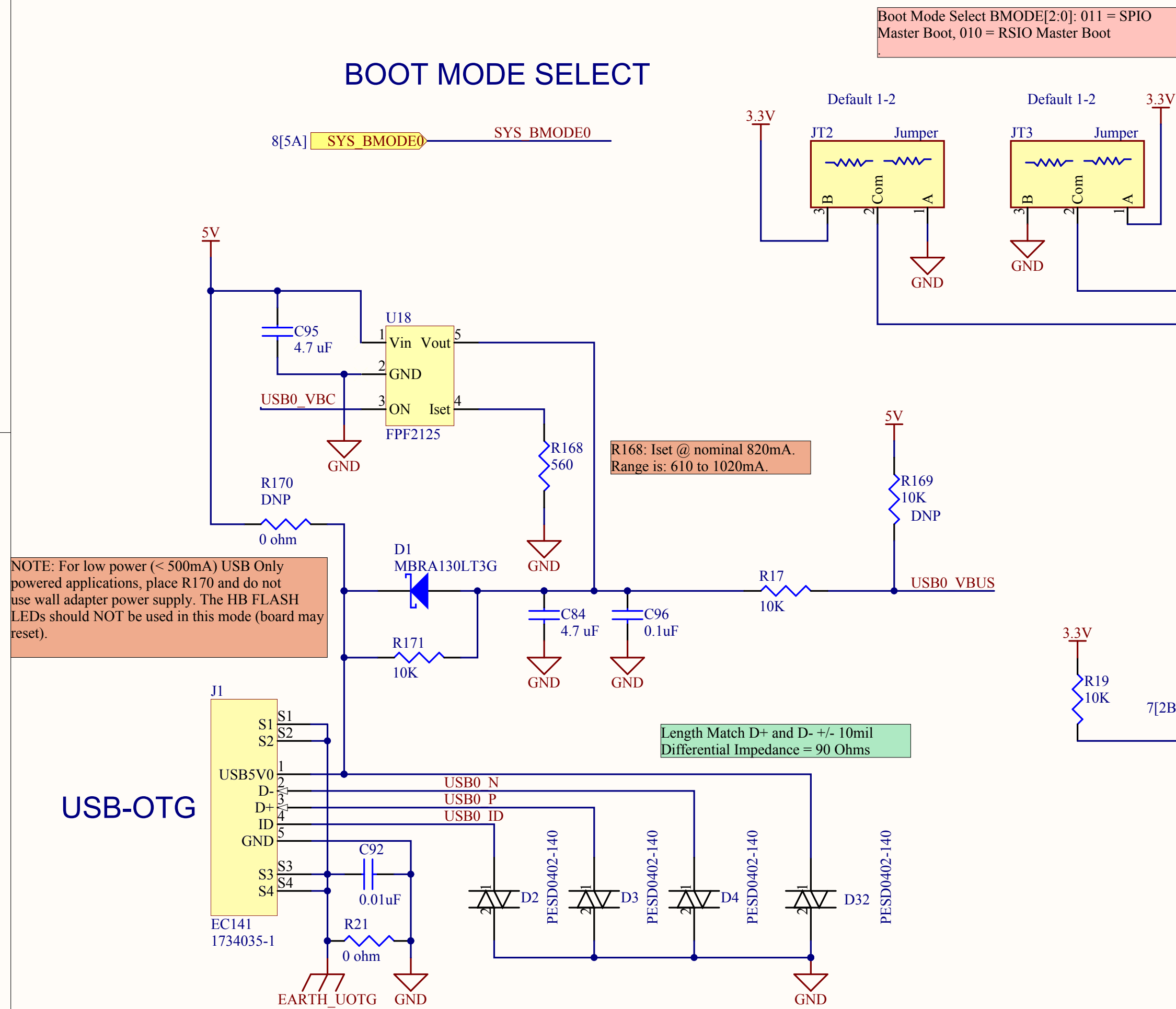




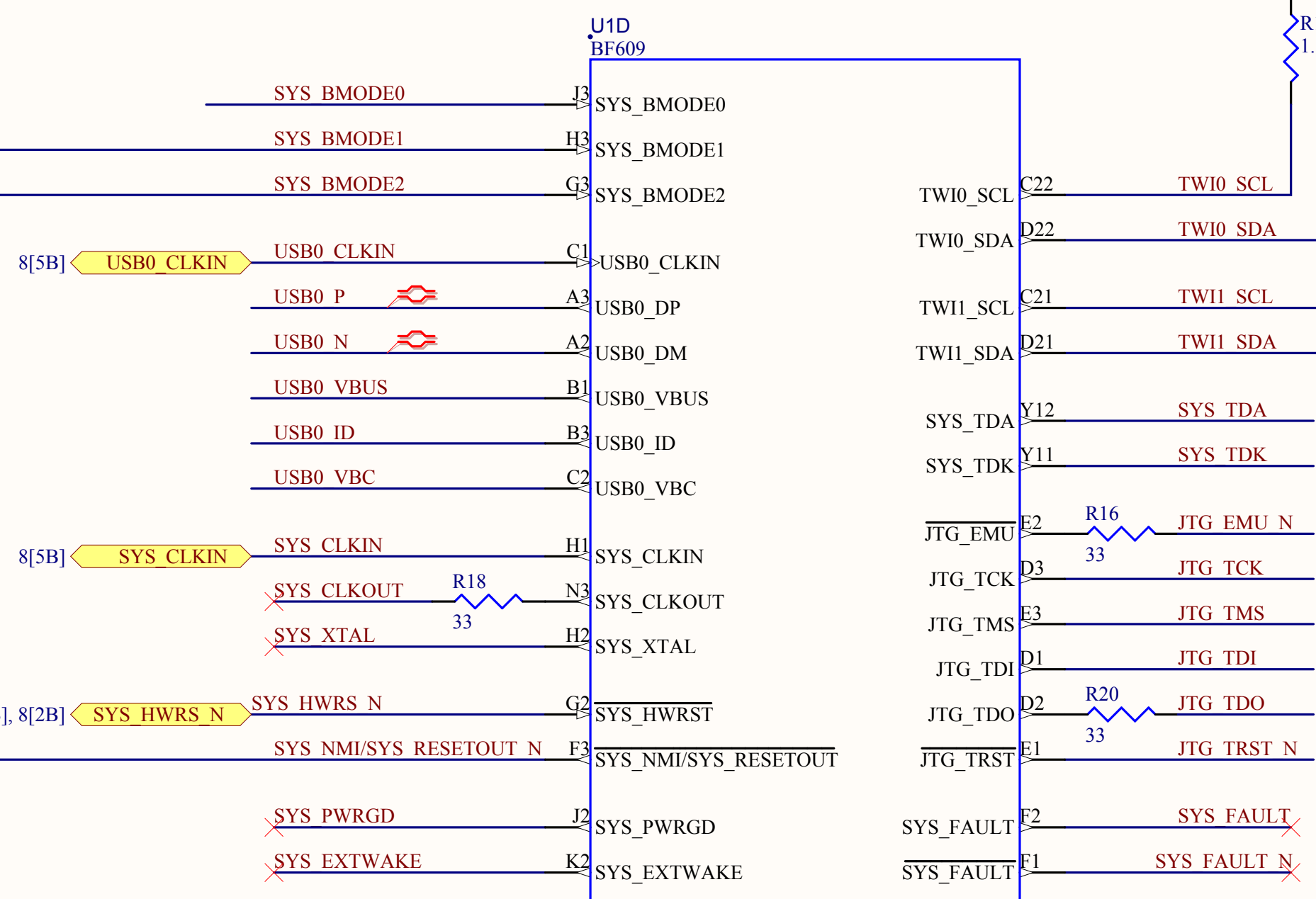




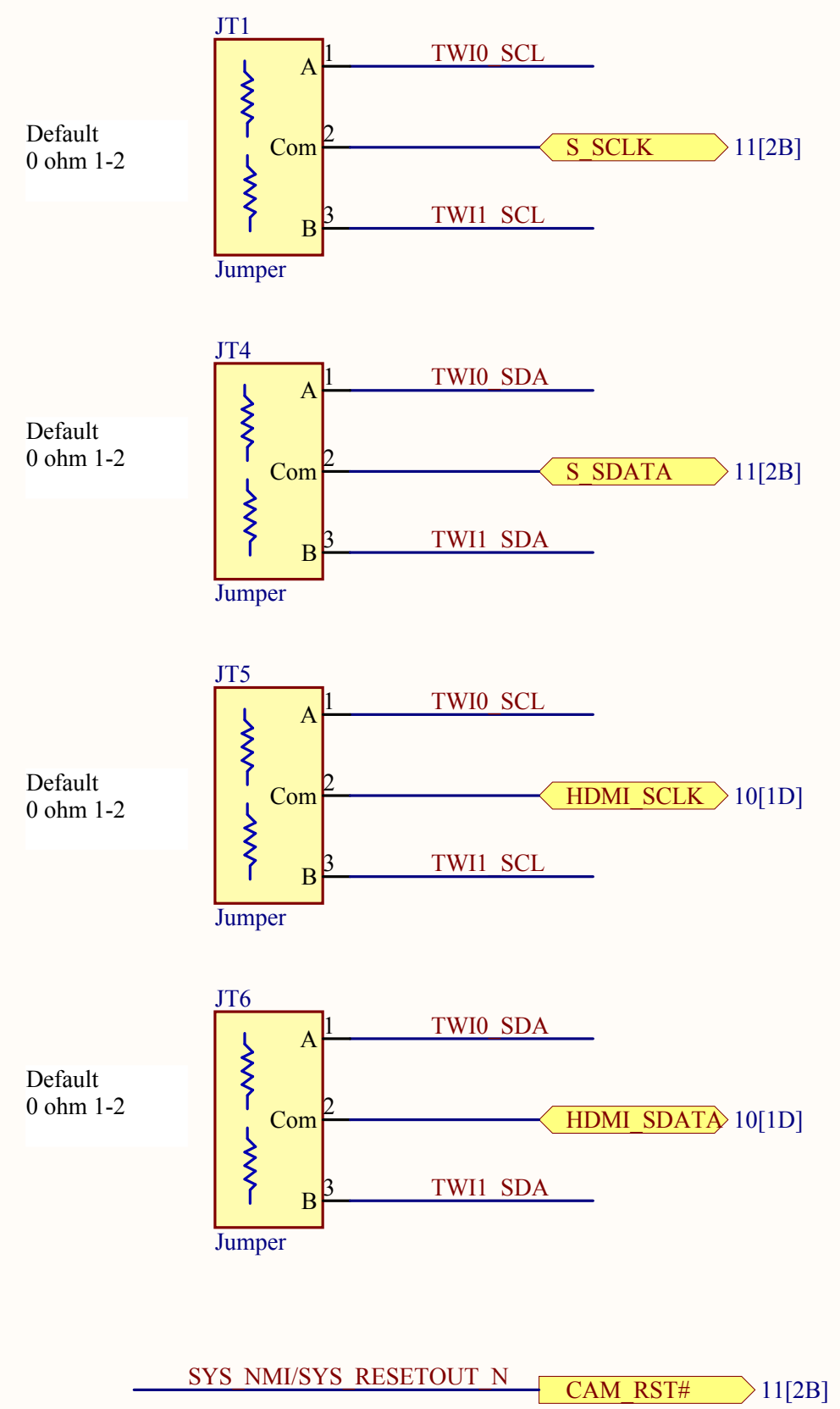
## BOOT MODE SELECT



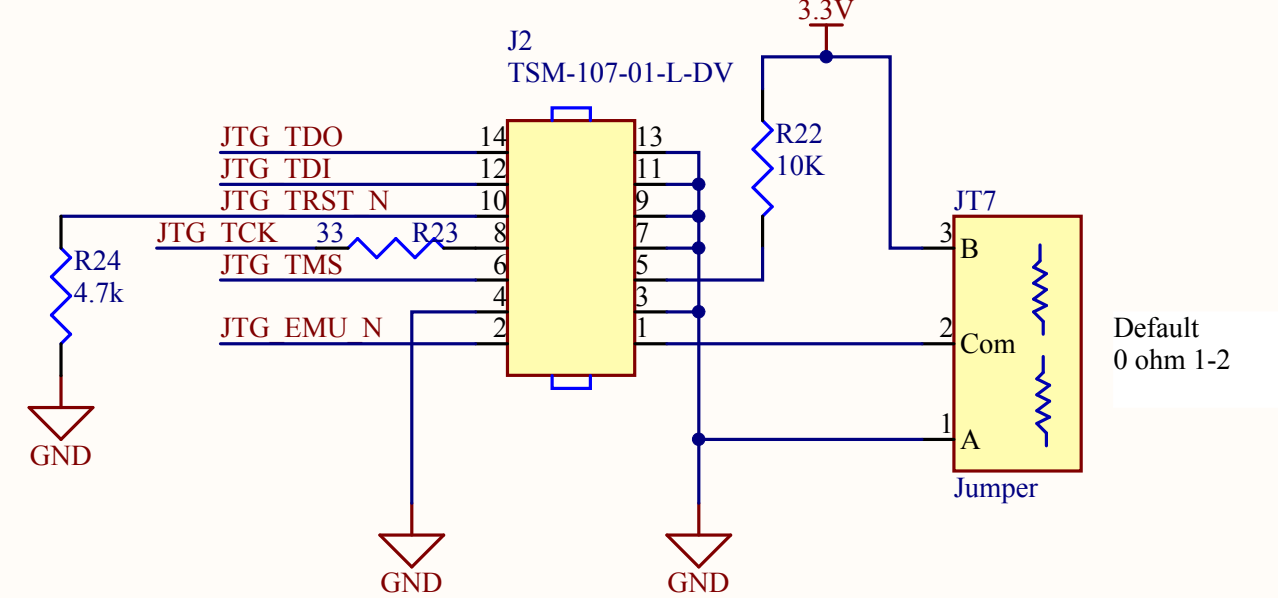
## USB-OTG



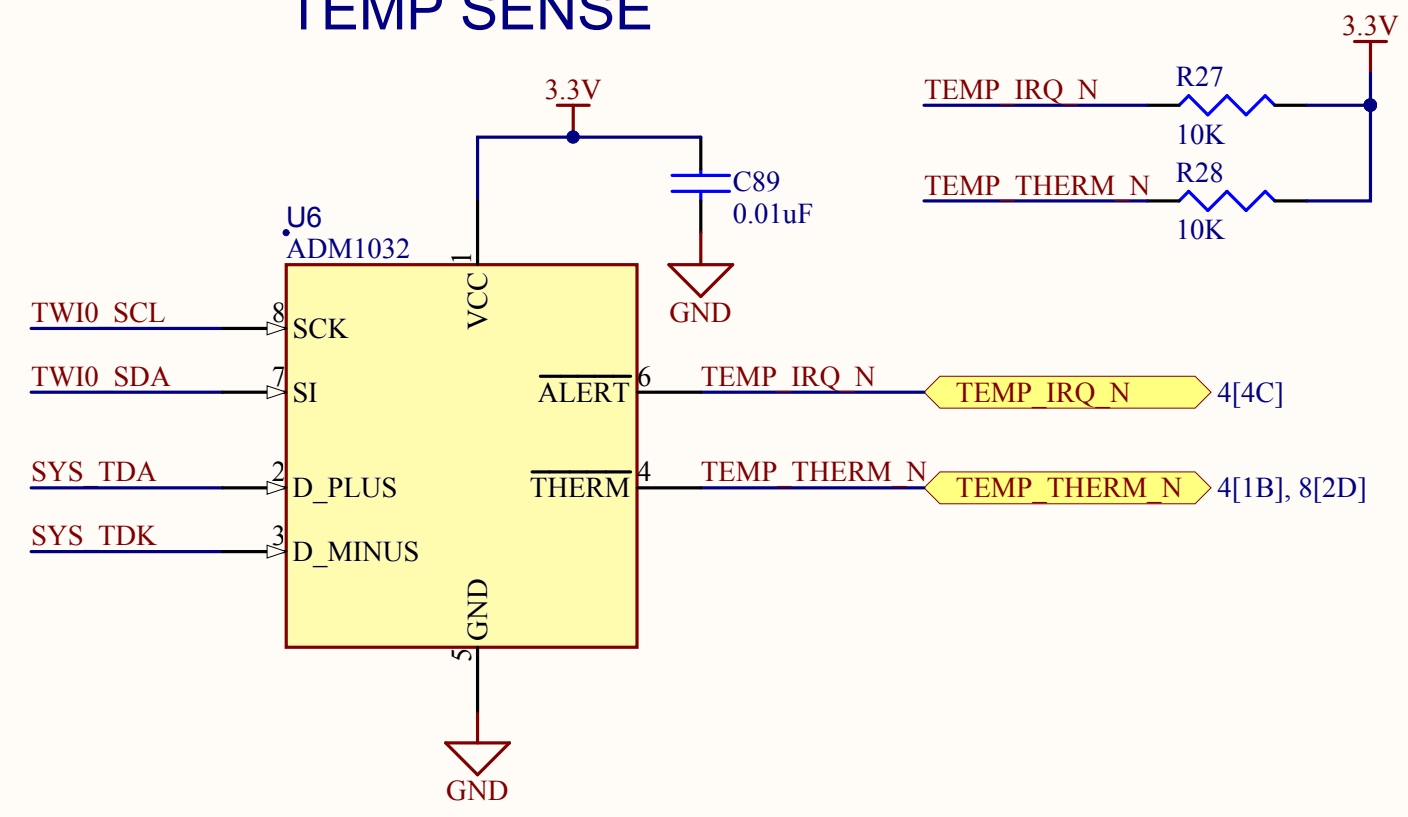
## I2C Select



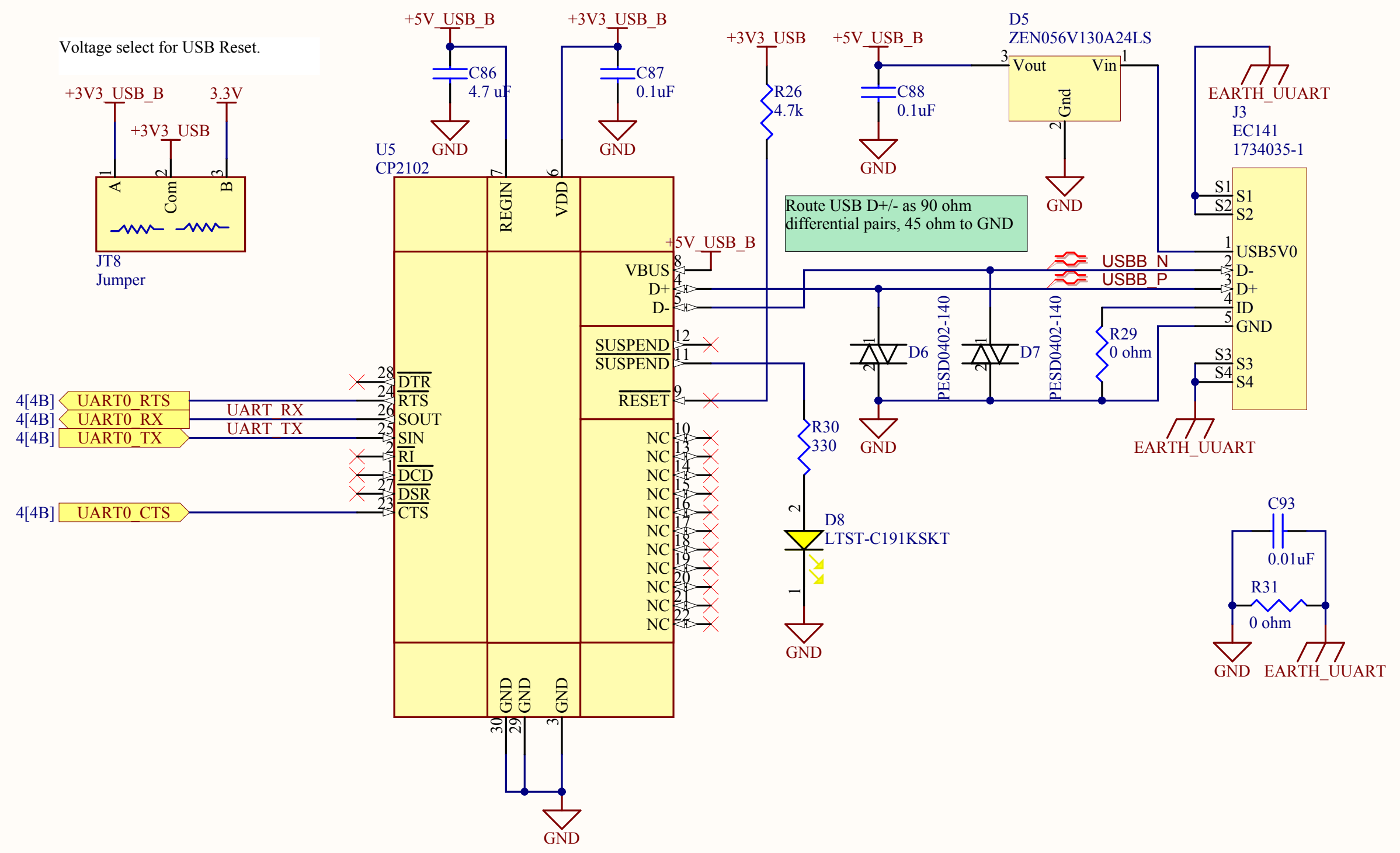
## JTAG - DSP



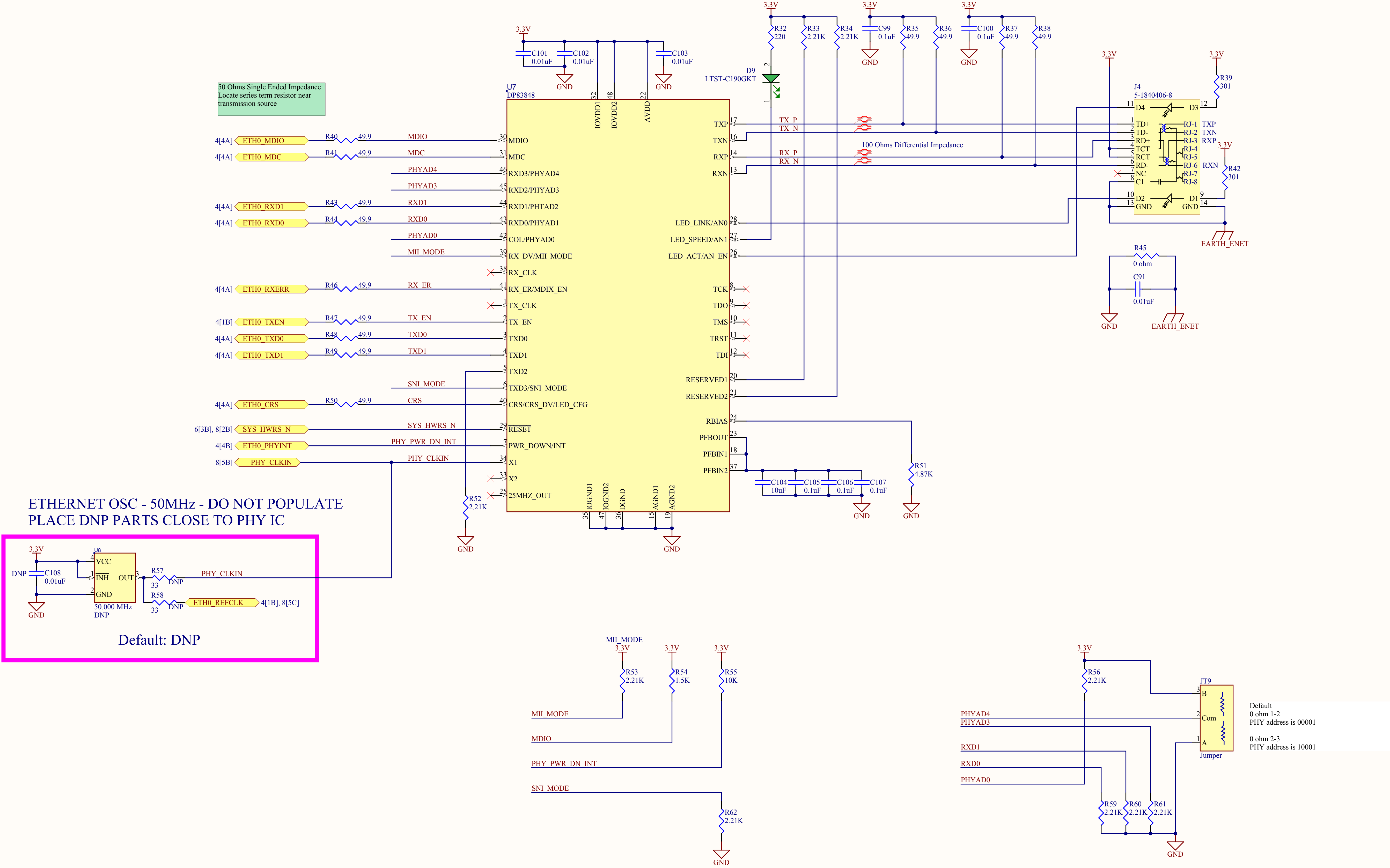
## TEMP SENSE



## USB-UART



ETHERNET





4[4B] RSIO\_D2

4[1C] RSIO\_D3

4[4C] RSIO\_CMD

4[4C] RSIO\_CLK

4[4C] RSIO\_D0

4[4C] RSIO\_D1

4[4C] SD\_CD#

R63 10K

R64 10K

R69 33

R70 33

C109 10uF

C110 0.01uF

GND

J5 1871602-1

1 DAT2

2 CD/DAT3

3 CMD

4 VCC

5 CLK

6 VSS

7 DAT0

8 DAT1

13 CD/SW-A

14 SW-B

GND

[illegible][illegible]

The schematic diagram illustrates a temperature sensing circuit with five parallel channels. Each channel is powered by a 3.3V supply and contains a resistor (R83, R84, R88, R89, R90, R91) and a diode (D11, D12, D13, D14, D15, D16). The diodes are connected to a common ground (GND). The output of the first four channels is connected to a 4[4C] input, and the output of the fifth channel is connected to a 4[1B], 6[5D] input. The temperature sensor is labeled TEMP THERM N.

**Pin 20:** DNP. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_GIN0.

**Pin 21:** DNP. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_GIN1.

**Pin 22:** DNP. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_GIN2.

**Pin 23:** DNP. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_GIN3.

**Pin 24:** 1-2. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_SHTDN/OE.

**Pin 25:** 1-2. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_SHTDN/OE.

**Pin 26:** 1-2. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_SHTDN/OE.

**Pin 27:** 1-2. Internal structure: 3.3V to B, Com to 10K to GND, A to Jumper to SYN\_SHTDN/OE.

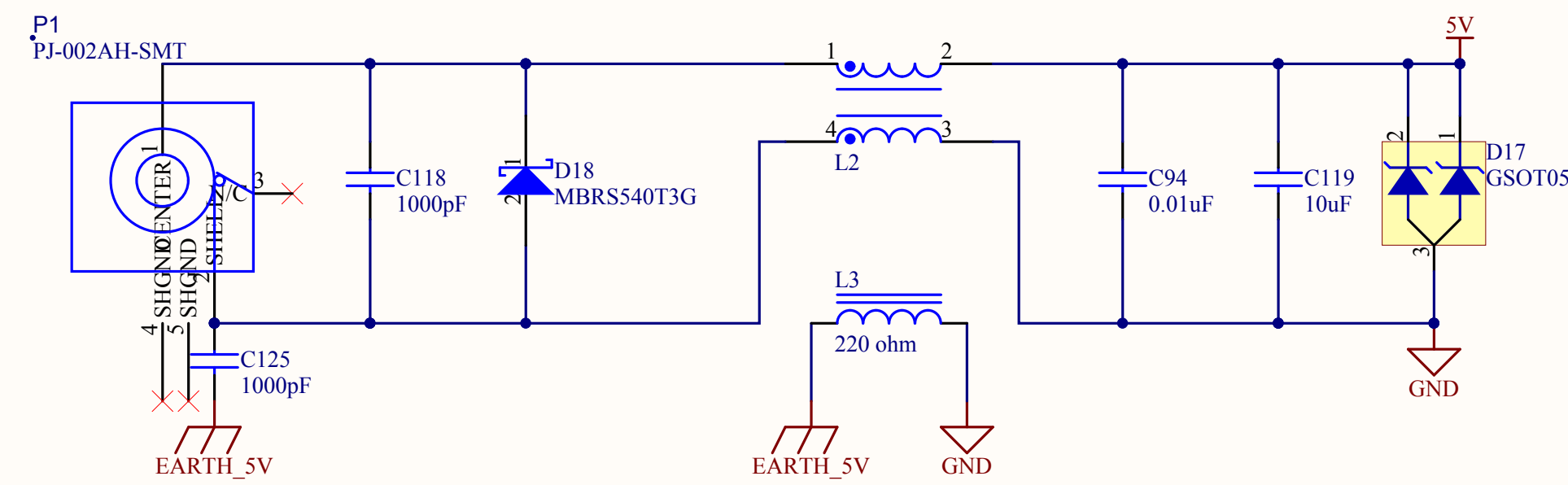
Clock Synthesizer default setup is  
JTxx: Pins connected: DNP  
means Do Not Populate

20:	DNP	24:	DNP
21:	DNP	25:	1 - 2
22:	1 - 2, 10K	26:	1 - 2
23:	1 - 2	27:	1 - 2, 10K

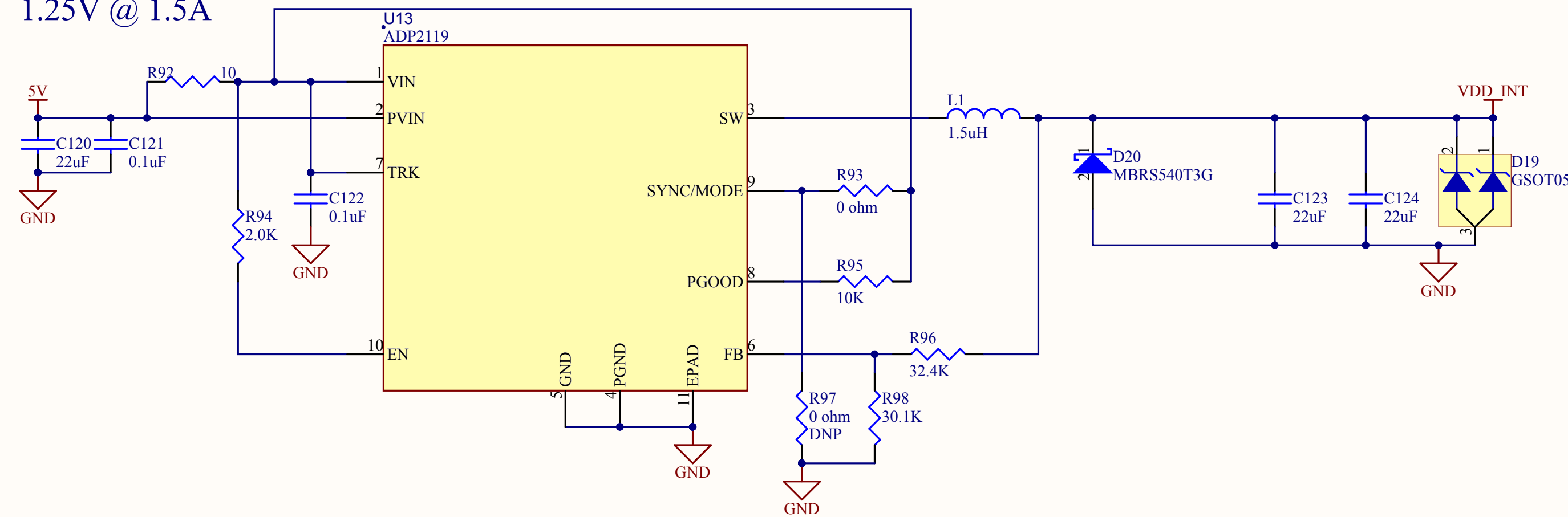
NOTE: Default configuration for synthesizer is "I2C" enabled via a 10K resistor at Pin 1 - 2. For JTAG, short JT27 2-3 or pull pin low.



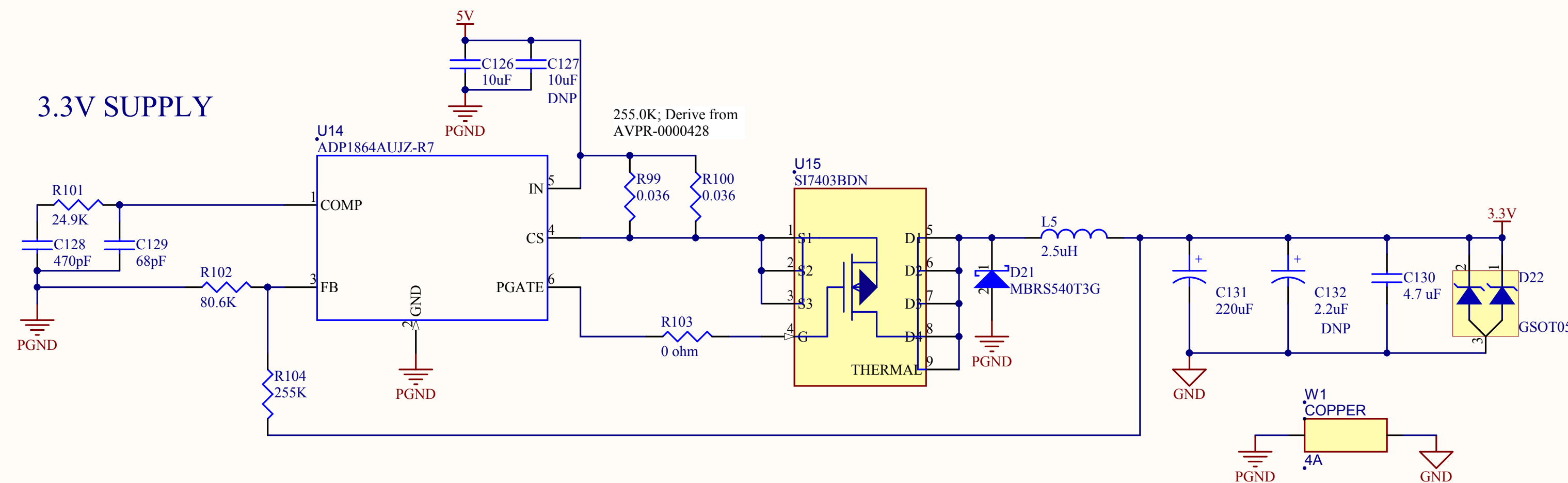
## 5V INPUT



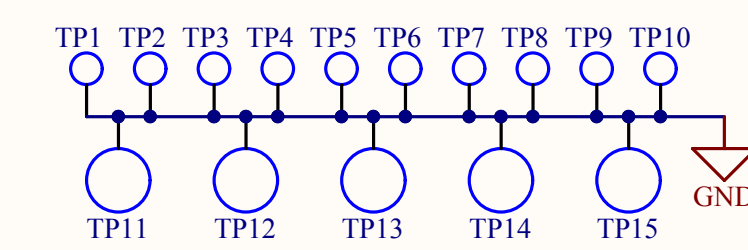
VDD\_INT SUPPLY  
1.25V @ 1.5A



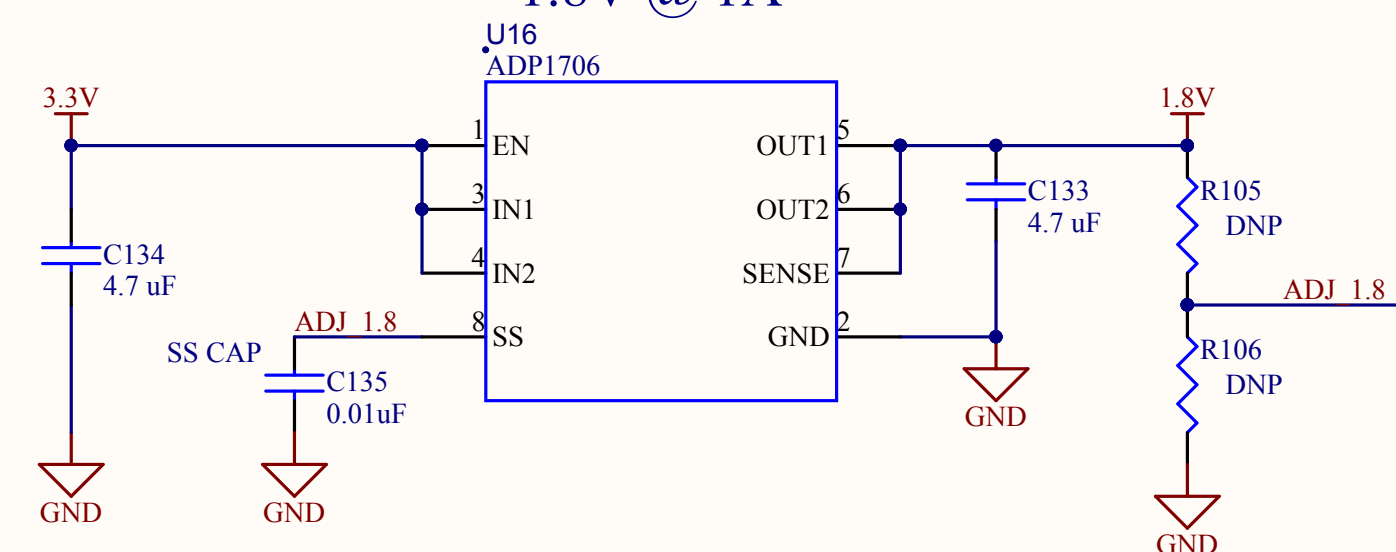
### 3.3V SUPPLY



## Add Test Points Liberally



## 1.8V @ 1A



To use ADP1708 with adjustable Vout in place of ADP1706, remove the SS CAP and place resistor divider per the formula below.

$$V_{OUT} = 0.8 \text{ V} (1 + R1/R2)$$

where:

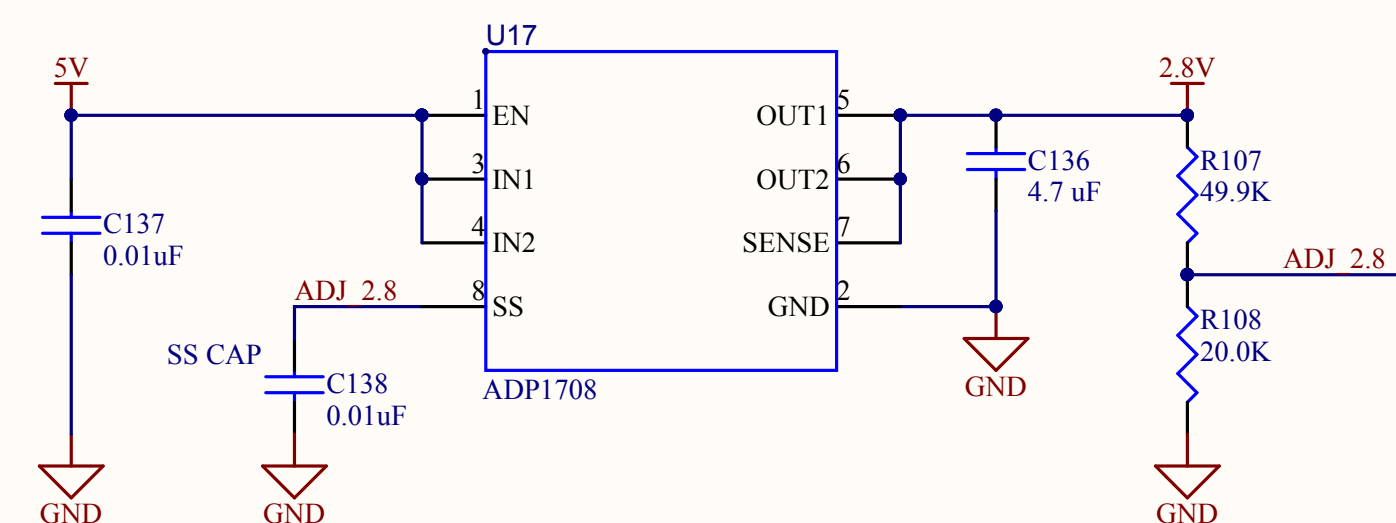
R1 is the resistor from OUT to ADJ.

R2 is the resistor from ADJ to GND. (<60K)

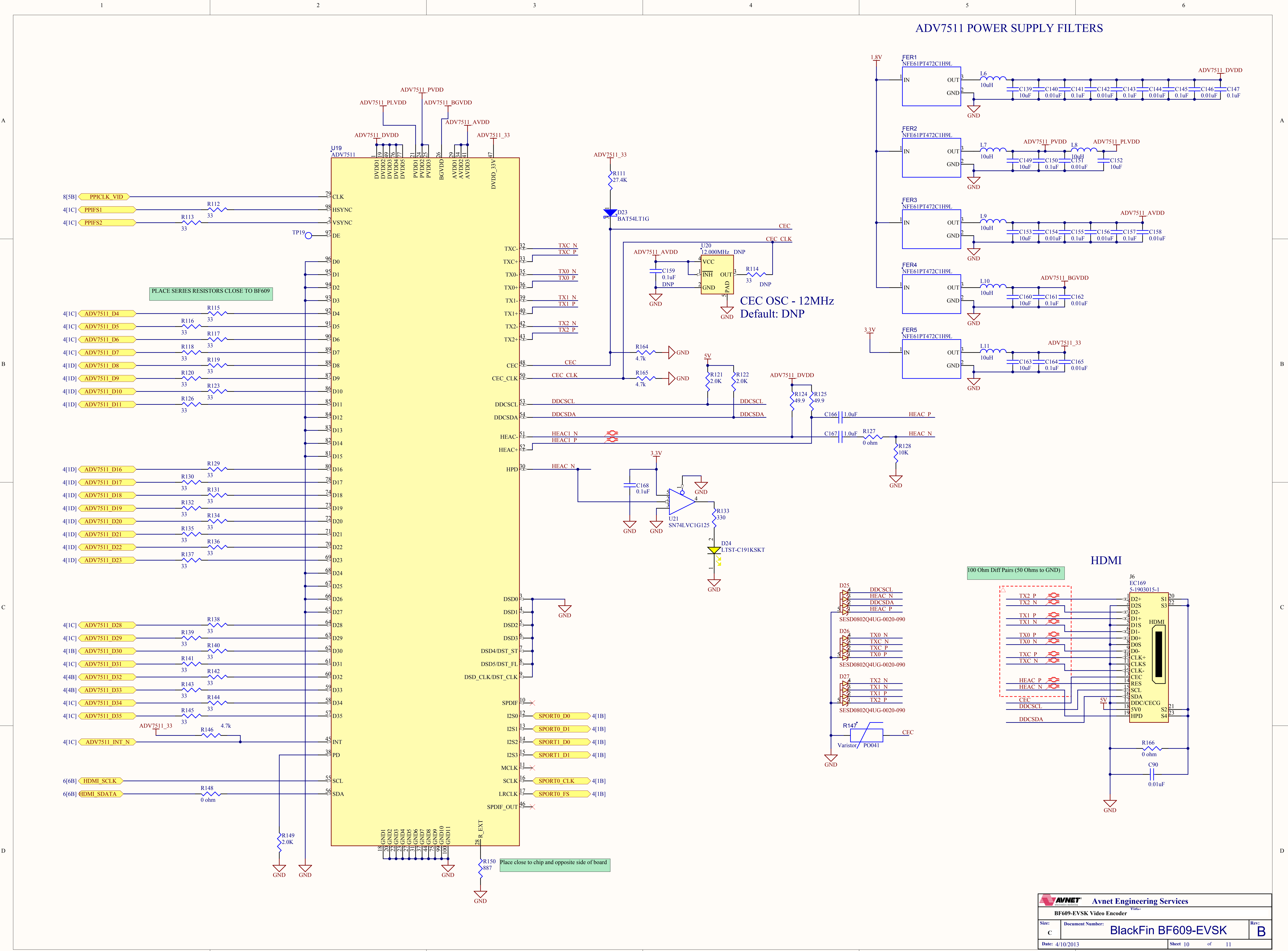
R2=20.0K, R1=24.9K yields 1.796V

R2=20.0K, R1=49.9K yields 2.796V

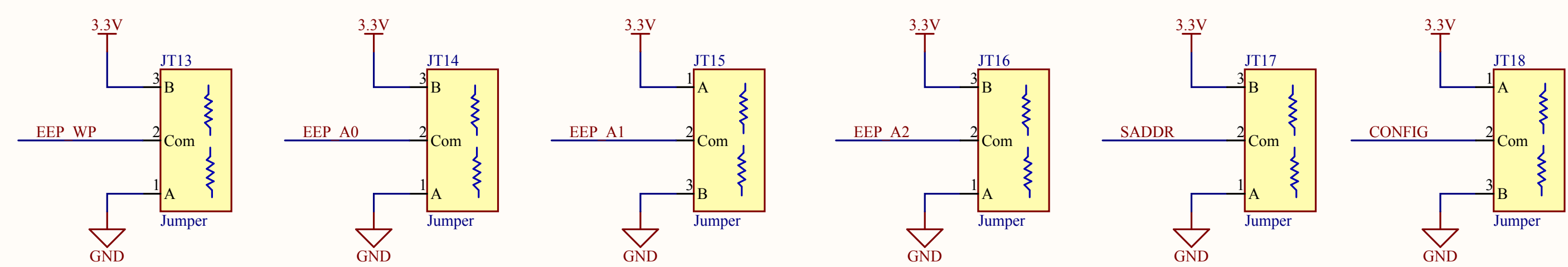
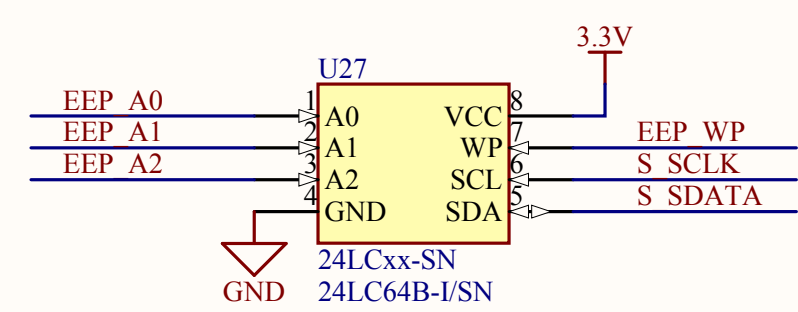
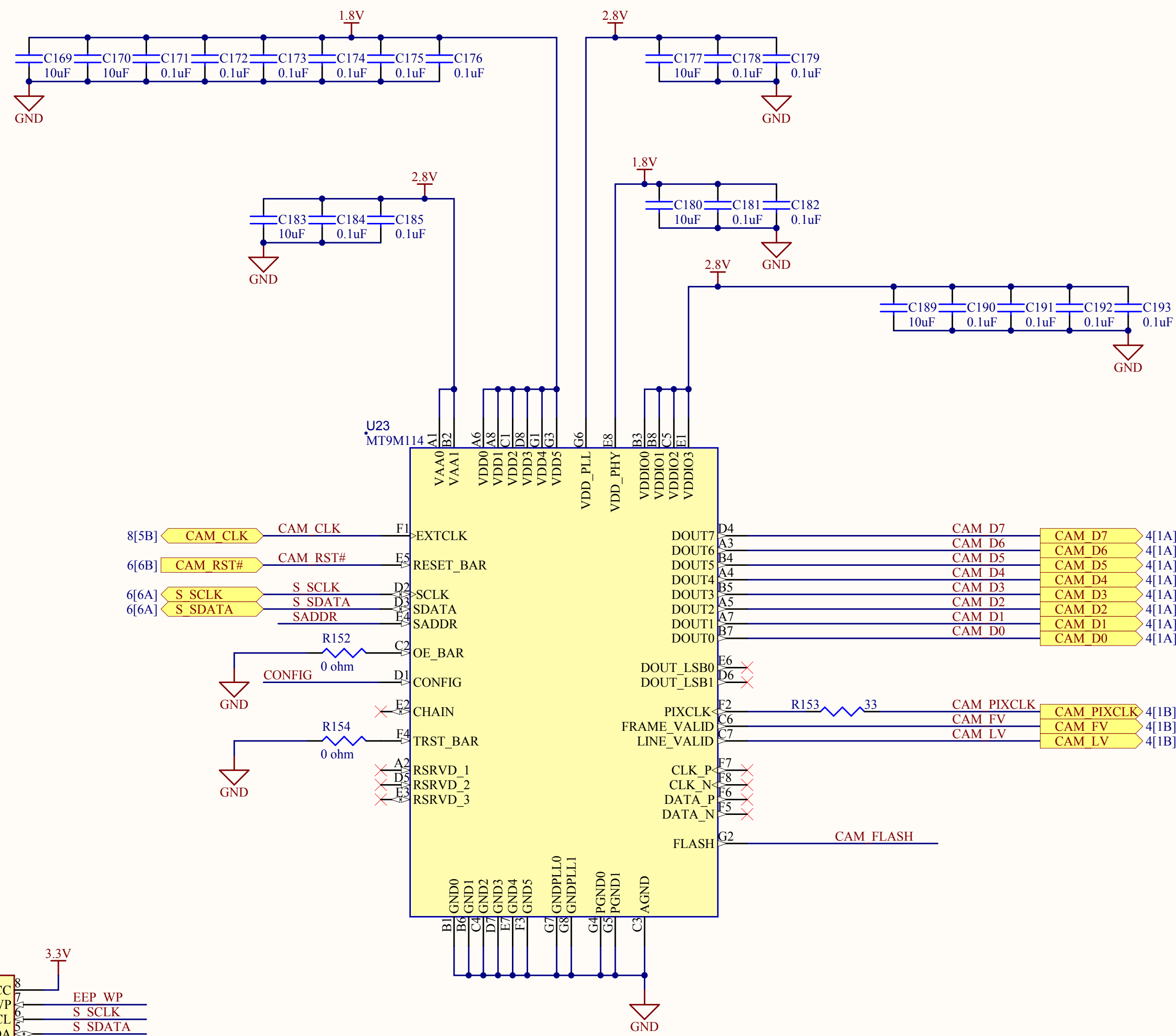
MT9M114 SUPPLY  
2.8V @ 1A



Mounting Hole Mounting Hole Mounting Hole Mounting Hole

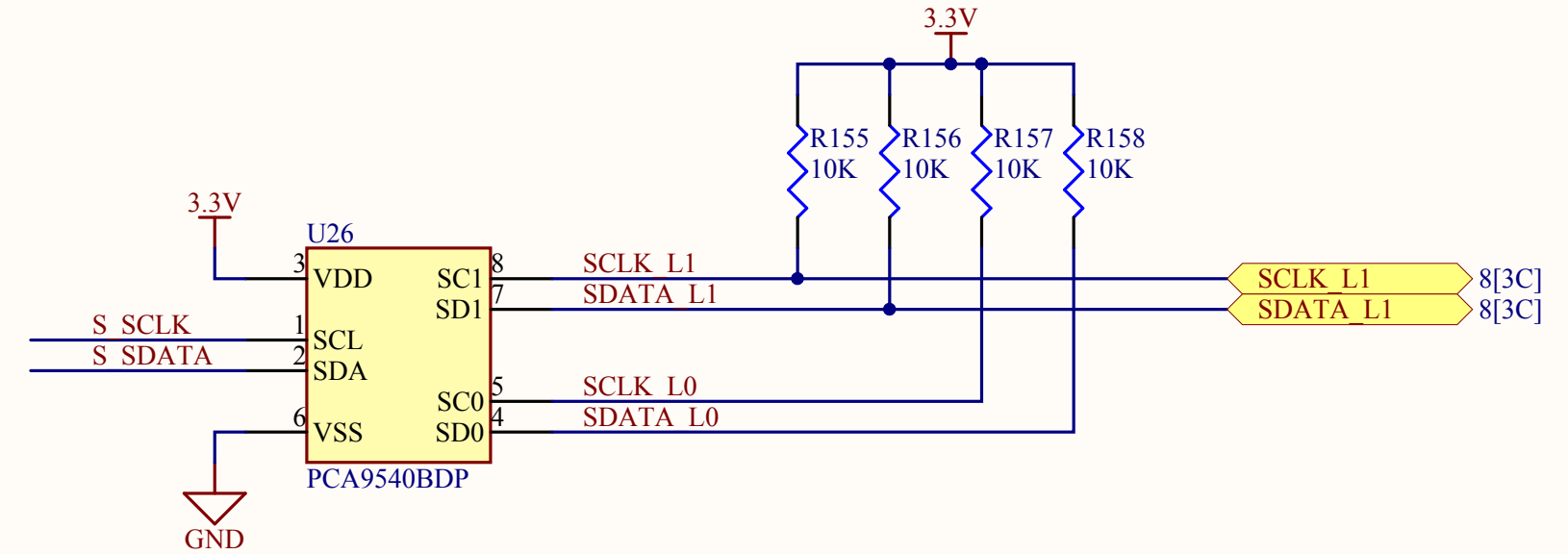




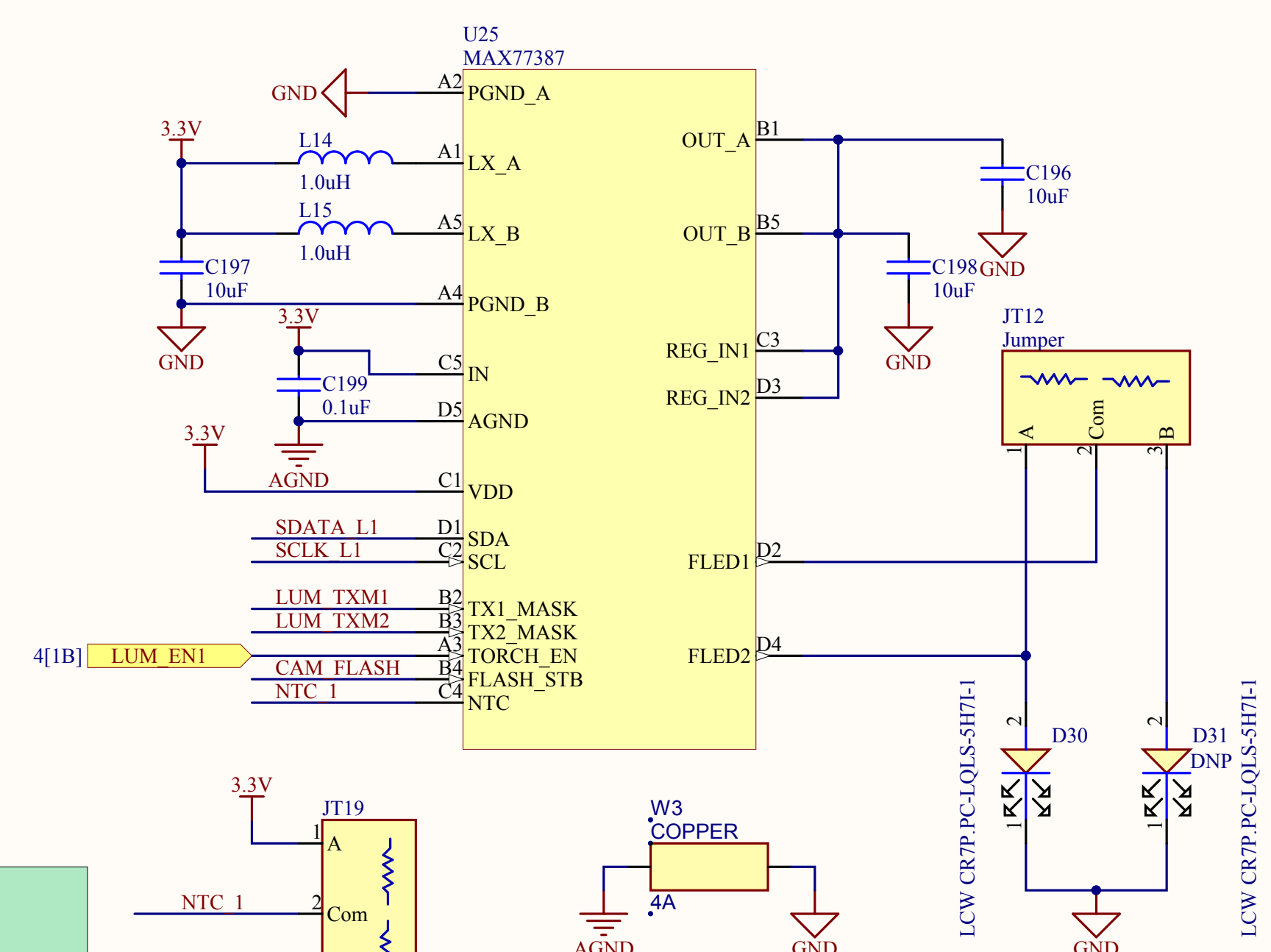
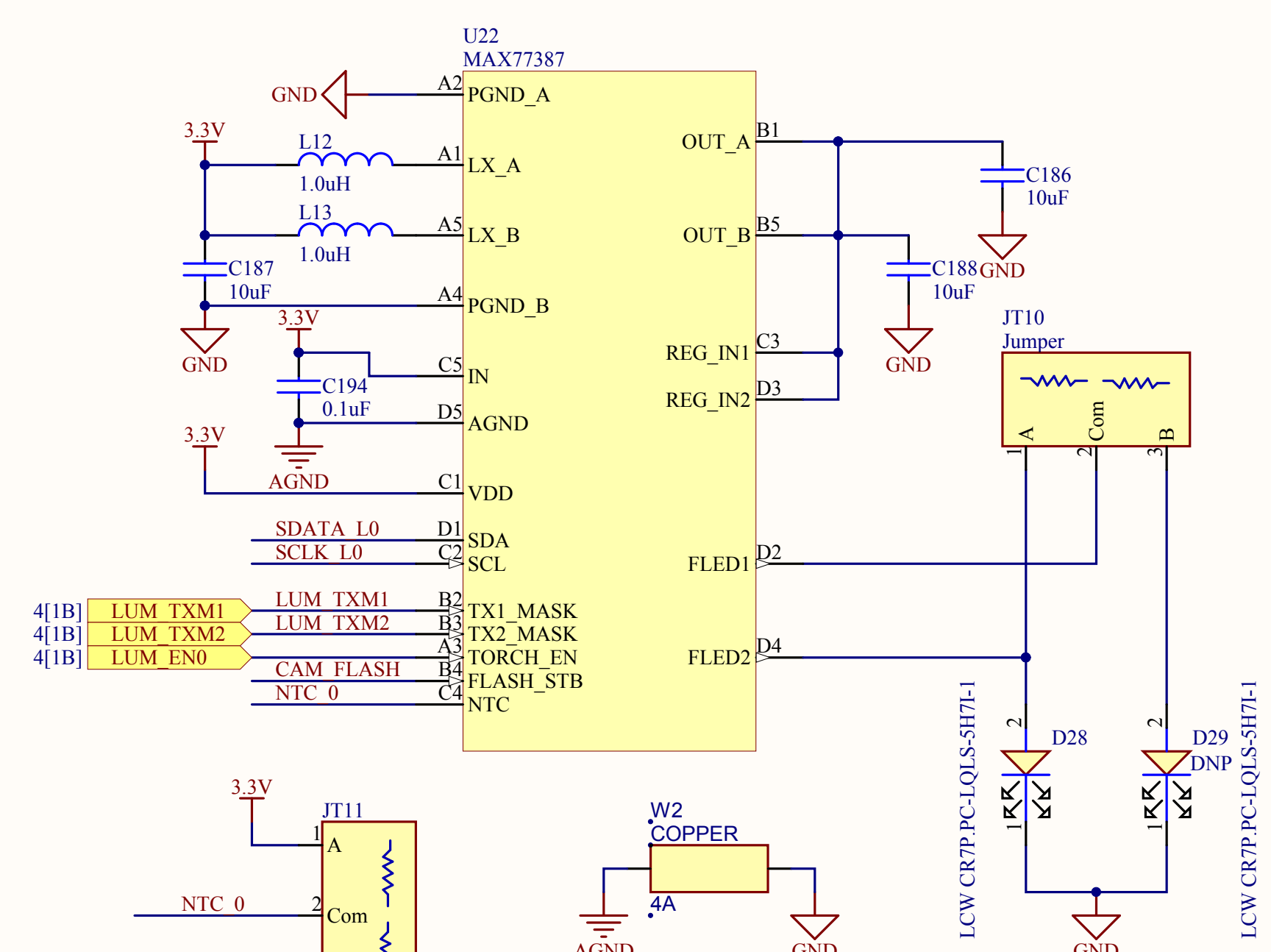


Default for all JT jumpers  
0 ohm 1-2

I2C Slave Address Map:	
EEPROM	= 0xA4
Temp Sensor	= 0x4C
Camera	= 0x90
MUX:	
MAX77387	= 0xE0
MAX77387	= 0x94
Clock Synthesizer	= 0xD4



B2	B1	B0	Command
0	X	X	no channel selected (power-up default state)
1	0	0	channel 0 enabled
1	0	1	channel 1 enabled
1	1	X	no channel selected



Place Part directly under MAX77387  
0 ohm Res 1-2 to disable NTC (Default)  
Thermistor 2-3 (Panasonic ERT-J0ER103J)