MegaChips Corporation	SPS-MA60000-EN-D
Product Specification	

TITLE

frizz Product Specification

Product Number	MA60000
Product Name	frizz
Customer Name	general-purpose

Sub Group	Revision	Final Approved	Oct.3rd,2016	T.Iwao
Product Specification	D	Approved	Sept.28th,2016	T.Iwao
		Checked	Sept.27th,2016	M.Matsumoto
		Created	Sept.13th,2016	K.Inaoka

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1. Overview

This specification is applied to frizz.

frizz is DSP consisting of high-performance 32bit core processor and peripheral that are suitable for PDR (Pedestrian Dead reckoning) processing.

The following is order code.

Table 1-2 order code

Order Code	Package	Size(mm)	Shipment form	Pack quantity
MA60000	FBGA	3.5mm x 3.5mm x 0.65mm	Tray	4,90pcs/Tray (Maximum loarding quantity)
MA60000S01	FBGA	3.5mm x 3.5mm x 0.66mm	Tape&Reel	4,900pcs/Tape &Reel (Maximum loarding quantity)

2. Specifications

Table 2-1 frizz specifications[1]

Item		Spec	Notes
Power	core	+1.2V +/-10%	
	IO	+1.8V +/-10% +3.3V +/-10%	
Package	Package shape	FBGA	
	Package size	3.5 x 3.5mm	
	Package number	49	
	Package pitch	0.4mm	
	Thickness	0.65mm	Max
System	Date RAM	256kbyte	
	Instruction RAM	256kbyte	
	Clock input method	External x1,Internal x2	
	External clock frequency	40MHz(Typ)	
	Internal clock frequency	slow:100kHz	
	Clock setting	Selected external or Internal by SELCLK PIN Selected internal frequency(slow of fast)by register	
	DSP	paraFoce(Xtensa LX4)	3way VLIW floating Point 2way SIMD
	External interrupt	2ch	Alternative GPIO
Host interface	SPI(Slave)	1ch(Alternative)	
	I2C(Slave)		
Sensor interface	SPI(Master)	1ch(4chip select)	Chip selector are alternative GPIO
	I2C(Master)		
General interface	UART	1ch	
	GPIO	4ch	
	PWM	2ch(resolution:2^16)	Alternative GPIO
Others	Ambient Operating Temp.	-20-85 degree C	

[1] frizz can work at 1.8V to 3.3V I/O voltage, it is design assurance.

3. Block Diagram

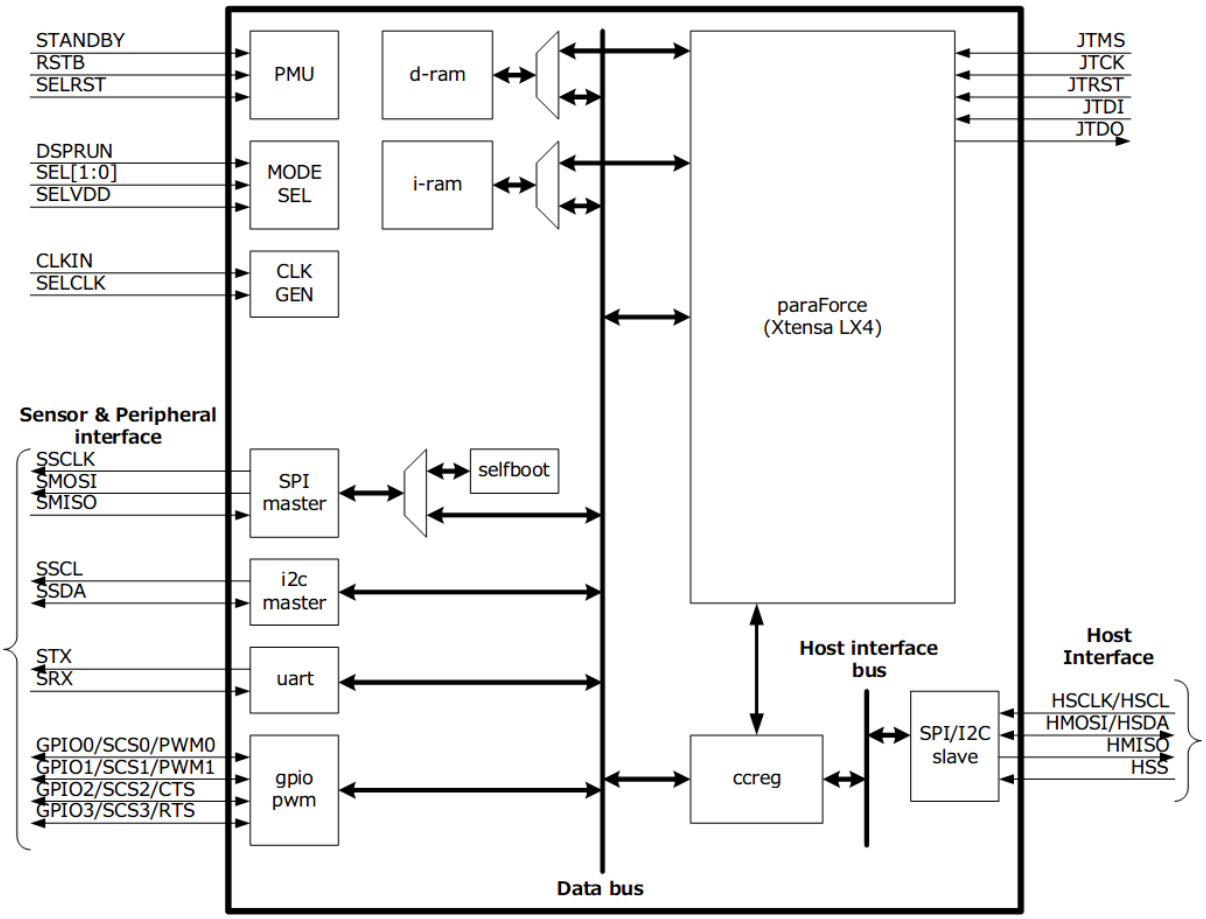


Figure 3-1 frizz block diagram

4. External Terminal Specifications

Table 4-1 List of pinout

No	Area	Pin Function Name	Alternate Function	Dir	Description	After Reset release	Recommended connection of Unused Pins
1	System	STANDBY	-	I (with Schmitt)	Standby mode setting (0:Standby,1:Normal)	Hi-Z	Connect to DVDD18
2		DSPRUN	-	I	DSP Run mode setting (0:Run,1:Stall)	Hi-Z	Connect to DVDD18 via a resistor
3		CLKIN	-	I	External CLK Input	Hi-Z	Connect to DVDD18
4		SEL0	-	I	Boot mode setting SEL0,SEL1 Boot mode 0, 0 Host Boot SPI Mode 0 0, 1 Host Boot SPI Mode 3 1, 0 Host Boot I2C 1, 1 Self-boot	Hi-Z	-
5		SEL1	-	I			
6		SELCLK	-	I	External /Internal CLK select(0:Internal,1:External)	Hi-Z	-
7		SELVDD	-	I	I/O voltage select (0:3.3V,2.4V,1:1.8V)	Hi-Z	-
8		SELRST	-	I	Reset Select (0:POR,1:External Reset)	Internal Pull-down	-
9		RSTB	-	I (with Schmitt)	External Reset Input(active low)	Internal Pull-up	NC
10	Power	DVDD18	-	P	Power supply.(IO)	-	-
11		DVDD12	-	P	Power supply.(CORE)	-	-
12		DVSS	-	P	Ground (0 V).	-	-
13		ROSC_AVDD	-	P	Power supply.(CORE)	-	-
14		ROSC_AVSS	-	P	Ground (0 V).	-	-
15	Host IF	HSCLK	HSCL	I	HOST IF SPI CLK Input / HOST IF I2C CLK Input	Hi-Z	Connect to DVDD18 via resistor
16		HMOSI	HSDA	I/O	HOST IF SPI Data Input(Input only) /HOST IF I2C SDA Signal	Hi-Z	Connect to DVDD18 via resistor
17		HMISO	-	O	HOST IF SPI Data Output	Hi-Z	NC
18		HSS	-	I	HOST IF SPI CS Input	Hi-Z	Connect to DVSS
19	Sensor IF	SSCLK	-	O	Sensor IF SPI CLK Output	Hi-Z	NC
20		SMOSI	-	O	Sensor IF SPI Data Output	Hi-Z	NC
21		SMISO	-	I	Sensor IF SPI Data Input	Hi-Z	Connect to DVSS
22		SSCL	-	O	Sensor IF I2C CLK Output	Hi-Z	Connect to DVDD18 via resistor
23		SSDA	-	I/O	Sensor IF I2C SDA Signal	Hi-Z	Connect to DVDD18 via resistor
24	UART	STX	-	O	UART Data Output	Hi-Z	NC
25		SRX	-	I	UART Data Input	Hi-Z	Connect to DVSS
26	GPIO/PWM	GPIO0	SCC0/PWM0	I/O	GPIO0 /Self-boot IF SPI CS Output 0 /PWM0	Hi-Z	Input: Connect to DVDD18 via resistor Output: Leave open
27		GPIO1	SCC1/PWM1	I/O	GPIO1 /Self-boot IF SPI CS Output 1 /PWM1	Hi-Z	Input: Connect to DVDD18 via resistor Output: Leave open
28		GPIO2	SCC1/CTS	I/O	GPIO2 with interrupt(Level only) /Sensor IF SPI CS Output 2 /UART CTS	Hi-Z	Input: Connect to DVDD18 via resistor Output: Leave open
29		GPIO3	SCC1/RTS	I/O	GPIO3 with interrupt(Level only) /Sensor IF SPI CS Output 3 /UART RTS	Hi-Z	Input: Connect to DVDD18 via resistor Output: Leave open
30	JTAG	JTMS	-	I	JTAG TMS	Internal Pull-up	NC
31		JTCK	-	I	JTAG TCK	Internal Pull-down	NC
32		JTRST	-	I	JTAG RST	Internal Pull-up	NC
33		JTDI	-	I	JTAG Data Input	Internal Pull-up	NC
34		JTDO	-	O	JTAG Data Output	Internal Pull-up	NC

5. System Specifications and settings

5.1. Mode Settings

The device carries out operation mode settings by SEL[1:0] pins. Self-boot performs a boot process from external serial flash ROM. Host download boot is conducted from host device connected to host interface. Please refer to Table 5-1 for details.

Table 5-1 Settings of boot mode and host interface mode

Ball/Pad		Boot Modes
SEL0	SEL1	
L	L	Host download boot SPI Mode0
L	H	Host download boot SPI Mode3
H	L	Host download boot I2C
H	H	Self-Boot

5.2. Low Power Modes

The device support low power modes in order to reduce power consumption when paraForce stops operating. Please refer to 5.7 Low Power Modes for details.

5.3. paraForce Initial Settings

DSPRUN pin can set paraForce initial settings after reset release. Generally, DSPRUN pin is set to “H” (Stall). When debugging by JTAG, DSPRUN pin is set to “L” (Run).

5.4. I/O Power Settings

The device I/O power can be selected from 1.8V I/O or 3.3V I/O by SELVDD pin. I/O power settings can apply to only one voltage, either 1.8V or 3.3V. When the device’s I/O power is used at 1.8V, SELVDD pin is applied to 1.8V, and when 3.3V is used, SELVDD pin is applied to 0V.

5.5. Reset Specifications

frizz has function (POR : Power On Reset) to internally generate reset signal. Therefore, the external reset forming circuit is unnecessary when you use POR.

5.5.1 POR (Power On Reset)

POR output waveform and characteristics is below Figure 5-1 and Table 5-2.

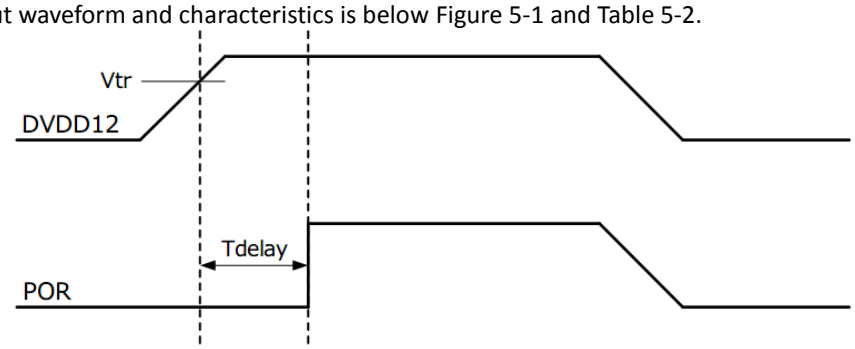


Figure 5-1 POR output waveform

Table 5-2 POR Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Reset Trigger Level	Vtr	0.4	0.6	1.0	V	
Reset Delay Time	Tdelay	20	40	1000	us	

- POR output: “L” is reset on, “H” is reset off.
- POR is available when DVDD12 rump-up time is between 1V/us and 1V/s.
- If DVDD12 is set 1.2V -> 0V -> 1.2V, DVDD12, 0V period has to be kept over 200ms as shown on Figure 5-2.

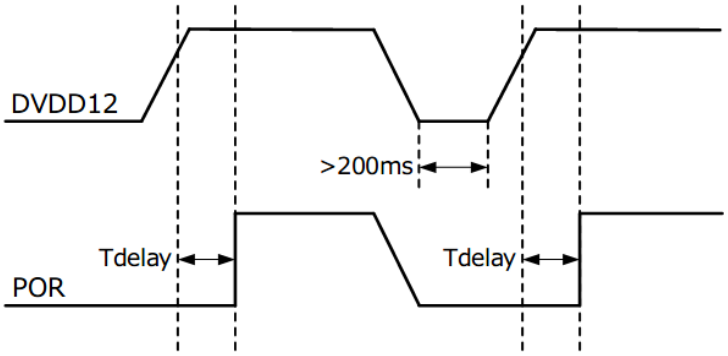


Figure 5-2 POR output waveform when DVDD12 sets OFF to ON

5.5.2 External Reset Input

It is possible to input the external reset input signal and use for frizz reset control. To activate the external reset input, set SELRST pin to “H”, and input control signal to RSTB pin. In this case, make RSTB pin logic so that “L” is reset on and “H” is reset off, same as specification of POR.

5.6. System Clock

The device has 3 clock sources that can select system clock. Specifications for 3 clock sources are as below.

- External input clock (Clock input at CLKIN pin)
- Internal slow clock (ROSC1 100kHz)
- Internal fast clock (ROSC2 40MHz)

Clock tree is shown on Figure 5-3.

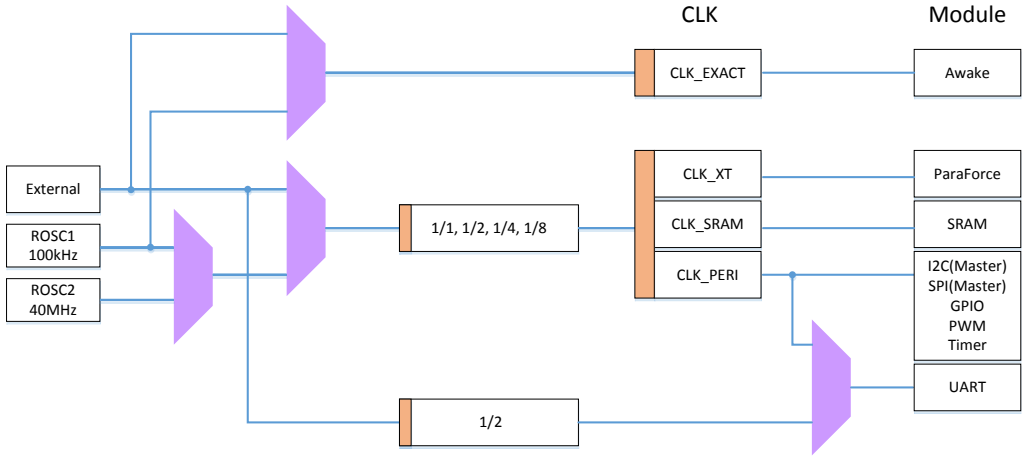


Figure 5-3 Clock tree

CLK_EXACT is for Awake timer. CLK_EXACT source can be selected by CLKIN or ROSC1. It requires CLKIN input to change CLK_EXACT source.

5.6.1 External Input Clock

This clock frequency is 40MHz (Typ).

5.6.2 Internal Slow Clock (ROSC1)

ROSC1 Electrical Characteristics is shown on Table 5-3.

Table 5-3 ROSC1 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	65	100	135	kHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		200		us	

ROSC1, 2 Startup waveform is shown on Figure 5-4. ROSC1 output is unstable during Ton1 period.

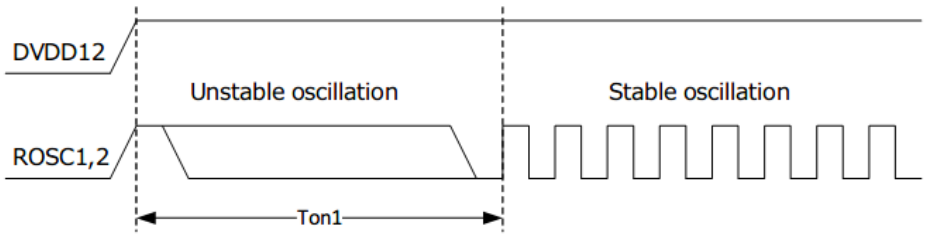


Figure 5-4 ROSC1, 2 Startup waveform

5.6.3 Internal Fast Clock (ROSC2)

ROSC2 Electrical Characteristics is shown on Table 5-4. PD (Power Down) can be controlled by xmode0[11] register.

Table 5-4 ROSC2 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	26	40	54	MHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		20		us	
Startup time when "PD" enabled	T_{on2}		20		us	

For T_{on1} and T_{on2}, please refer to Table 5-3 and Table 5-4. The unstable output at T_{on2} isn't be blocked, and when PD is changed from 1 to 0, please wait for T_{on2} to start operation.

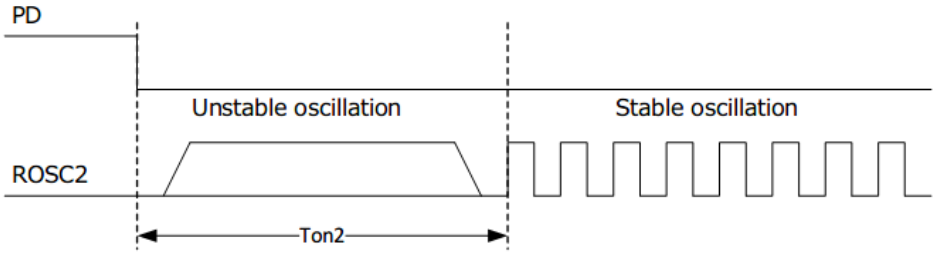


Figure 5-5 ROSC2 Startup Waveform (T_{on2})

5.7. Low Power Modes

The device support three low power modes as below.

- Sleep mode

In sleep mode, only the paraForce is stopped. All clocks are running. When system clock is set tointernal low-speed (100kHz) during sleep mode, the mode is slow-CLK sleep mode. And when system clock is set internal high-speed (40MHz) or to external clock input during sleep mode, the mode is fast-CLK sleep mode. In fast-CLK sleep mode, host device can access to frizz internal RAM and register. All peripherals continue to operate and can wake up the paraForce when an interrupt occurs.

- Stop mode

In stop mode, the paraForce is stopped and all clocks except the paraForce clock are stopped. Register needs to be set before the paraForece is stopped and can wake up the paraForce when an Awake interrupt occurs.

- Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal power switch is off so that the 1.2V domain is powered off. All clocks are stopped except the internal low speed clock (100kHz). The device enters to Standby mode when external STANDBY pin is set to L, and to be back to normal mode, external STANDBY pin needs to be set to H. All SRAM and register are initialized when the device exits the Standby mode. Please refer to Table 5-5.

Table 5-5 Low power modes specifications[2]

Low Power Mode		Sleep		Stop	Standby
		Fast-CLK	Slow-CLK		
Entry	Start	WAITI instruction	<-	STOPREG 1'b1 set and WAITI instruction	STANDBY pin H->L
Wake up	Start	All interrupt events	<-	The Awake timer interrupt	STANDBY pin L->H
	recovery time	<10us	<500us	<500us	(depend on boot program size)

[2] The recovery time and power consumption value is estimated by simulation, and there is no guarantee.

6. Host Interface Specifications

This is the interface to connect with Host Device and has two kinds of interfaces, SPI slave and I2C slave. The details of Host Interface are as follows.

6.1. Address Map

Figure 6-1 shows Address Map of Host Interface. SPI is accessible to address width of [13:0] area, and I2C is accessible to address width of [7:0] area.

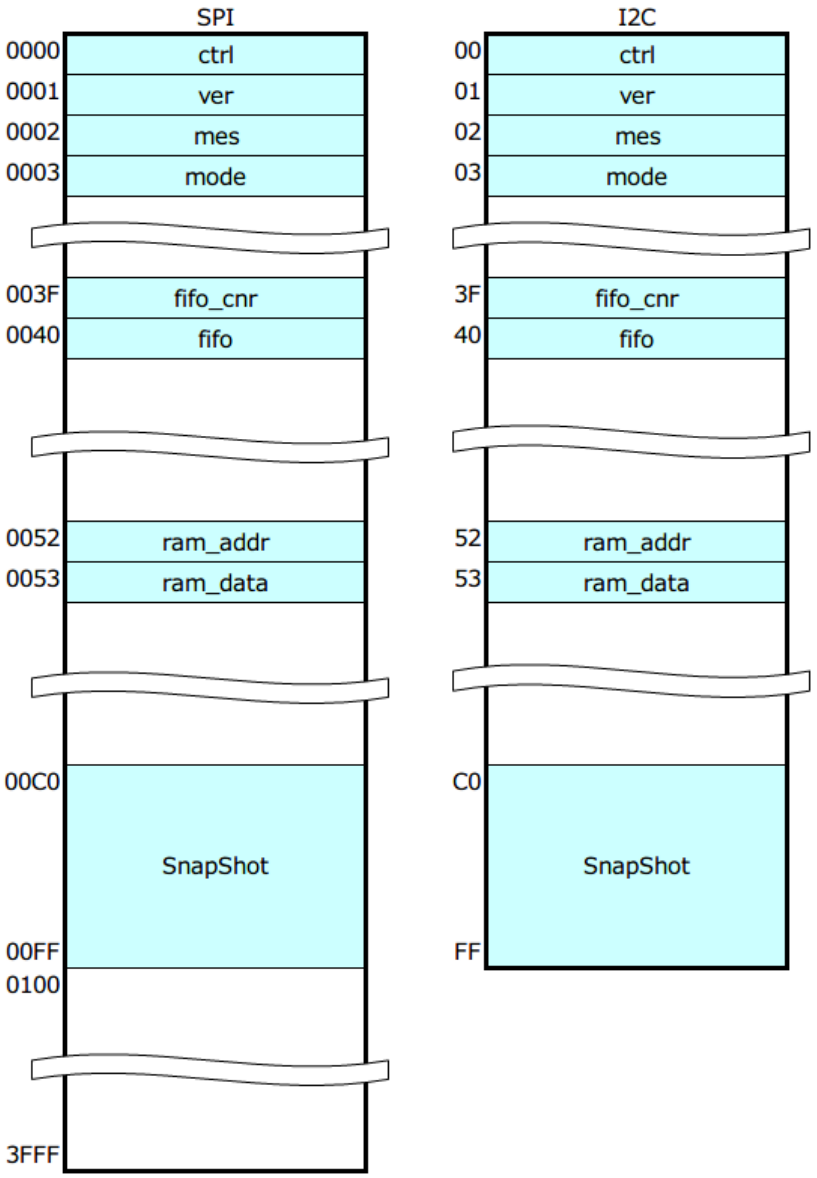


Figure 6-1 Address Map of Host Interface

6.2. SPI/I2C

SPI (Serial Peripheral Interface) interface that multiplex I2C is available. They are alternative functions and can be operated in slave mode. The external pin SEL0 and SEL1 select SPI or I2C interface.

Figure 6-2 shows Host interface SPI timing diagram.

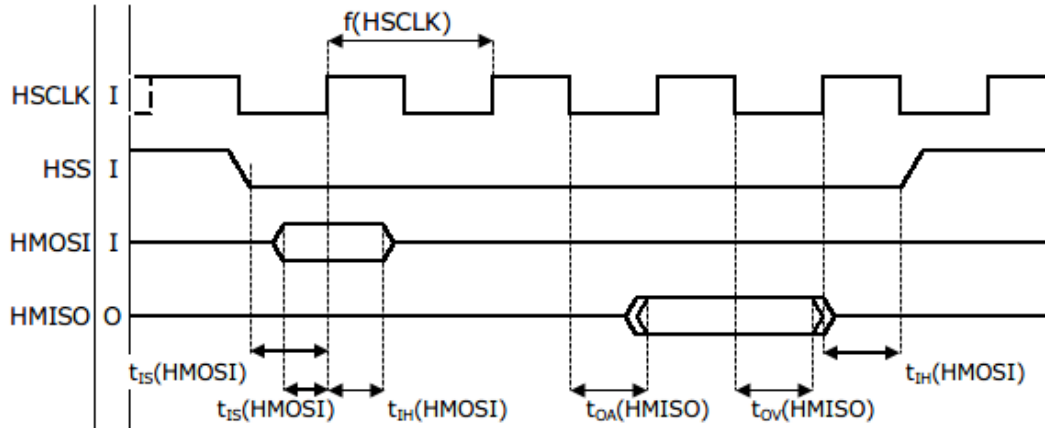


Figure 6-2 Host interface SPI timing diagram

Table 6-1,6-2 shows Host interface SPI dynamic characteristics.

Table 6-1 Host interface SPI dynamic characteristics(DVDD18=1.8V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI Clock Frequency	f (HSCLK)		-	-	20	MHz
Data input setup Time	t_{IS}(HMOSI)		4	-	-	ns
	t_{IS}(HSS)		6	-	-	ns
Data input hold Time	t_{IH}(HMOSI)		1	-	-	ns
	t_{IH}(HSS)		1	-	-	ns
Data output Access time	t_{OA}(HMISO)	20pF load	-	-	14.0	ns
		10pF load			13.0	ns
Data output Valid time	t_{OV}(HMISO)		1	-	-	ns

Table 6-2 Host interface SPI dynamic characteristics(DVDD18=3.3V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI Clock Frequency	f (HSCLK)		-	-	40	MHz
Data input setup Time	t_{IS}(HMOSI)		4	-	-	ns
	t_{IS}(HSS)		6	-	-	ns
Data input hold Time	t_{IH}(HMOSI)		1	-	-	ns
	t_{IH}(HSS)		1	-	-	ns
Data output Access time	t_{OA}(HMISO)	35pF load	-	-	9.5	ns
		20pF load	-	-	8.8	ns
		10pF load			8.2	ns
Data output Valid time	t_{OV}(HMISO)		1	-	-	ns

Figure 6-3 shows I2C waveform.

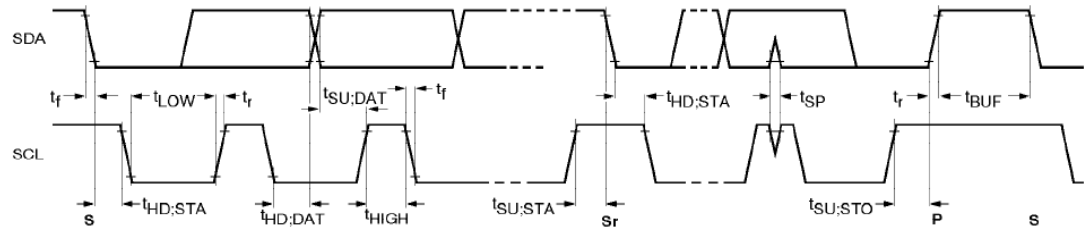


Figure 6-3 I2C waveform

Table 6-3 shows I2C Characteristics.

Table 6-3 I2C Characteristics

Parameter	Symbol	Condition	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0	100	0	400	0	1000	kHz
hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	4.0	-	0.6	-	0.26	-	us
LOW period of the SCL clock	t_{LOW}		4.7	-	1.3	-	0.5	-	us
HIGH period of the SCL clock	t_{HIGH}		4.0	-	0.6	-	0.26	-	us
set-up time for a repeated START condition	$t_{SU;STA}$		4.7	-	0.6	-	0.26	-	us
data hold time	$t_{HD;DAT}$		0	-	0	-	0	-	us
data set-up time	tSU;dAT		250	-	100	-	50	-	ns
rise time of both SDA and SCL signals	t_r		-	1000	20	300	-	120	ns
fall time of both SDA and SCL signals	t_f		-	300	20* (VDD/ 5.5V)	300	20* (VDD/ 5.5V)	120	ns
set-up time for STOP condition	$t_{SU;STO}$		4.0	-	0.6	-	0.26	-	us
bus free time between a STOP and START condition	t_{BUF}		4.7	-	1.3	-	0.5	-	us
data valid time	$t_{VD;DAT}$		-	3.45	-	0.9	-	0.45	us
data valid acknowledge time	$t_{VD;ACK}$		-	3.45	-	0.9	-	0.45	us

6.3. Access to DPBUF(Dual Purpose Buffer)

The data exchange between paraForce and Host Interface takes place via DPBUF (Dual Purpose Buffer).There are 2 operation modes, FIFO and Snapshot. The mode switching between FIFO and Snapshot is performed in register fifo_ctr[1]. Before switching mode, FIFO reset (register ctrl[3]) must be performed.

6.3.1 FIFO Mode

This is the mode to access to register fifo.

6.3.2 Snapshot Mode

This is the mode to access to 0x00C0-00FF area. Only read is available to access to this area from Host Interface.

6.4. Access to I-RAM/D-RAM

While paraForce is being stalled, internal I-RAM/D-RAM area can be accessible from Host Interface. The register ram_adr and ram_data are used to access from Host Interface to I-RAM/D-RAM. The address to set in register ram_adr must be 1 word unit. Table 6-4 shows the address number to set ram_adr. The address number is different from Sensor Interface Address Map Figure 7-1.

Table 6-4 the address number to set ram_adr

Access to RAM area	ram_adr to set address
D-RAM0	00000000h – 00007FFFh
D-RAM1	00008000h – 0000FFFFh
I-RAM0	00010000h – 00017FFFh
I-RAM1	00018000h – 0001FFFFh

7. Sensor Interface and Peripheral Specifications

The device provides following interfaces to collect sensor data and connect to other devices.

- I2C master
- SPI master
- GPIO
- PWM
- UART
- Timer

These interfaces are controlled by paraForce and connected to Data Bus. The details of Sensor Interface and Peripherals are given below.

7.1. Address Map

Figure 7-1 shows Address Map of Sensor Interface.

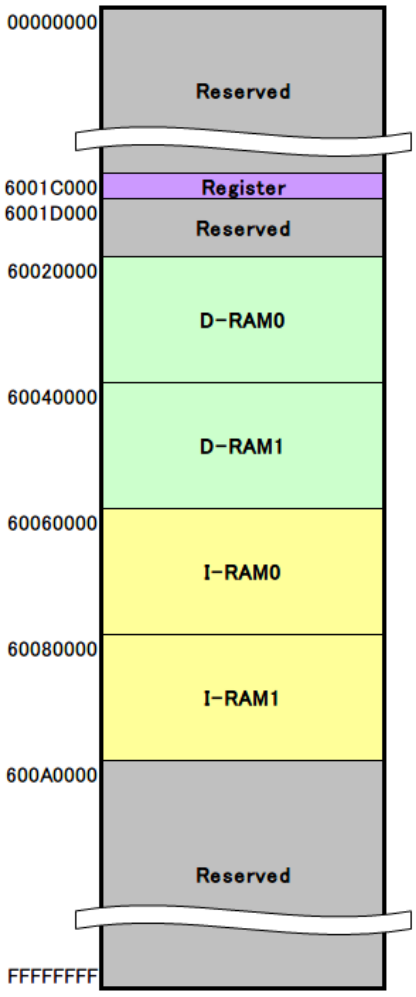


Figure 7-1 Address Map of Sensor Interface

7.2. I2C

Table 7-1 shows Sensor Interface I2C implementation.

Table 7-1 Sensor Interface I2C implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	• Data width : 8bit (ACK signal of 1 bit data is added after 8 bit data) • I2C bus format is based on Philips 1995 Update. The device can distinguish between start-condition and stop-condition form the state of I2C bus line. • Standard-mode (transfer at rates of up to 100kbit/s) is available. • Fast-mode (transfer at rates of up to 400kbps) is available.
Interrupt signal	int_i2c

For I2C characteristics, please refer to Figure 6-3 and Table 6-3.

7.3. SPI

Table 7-2 shows Sensor Interface SPI implementation.

Table 7-2 Sensor Interface SPI implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	• 3-wired serial interface • Slave select signal are available up to 4 • Data width : 8bit • Fast bit of serial data : Alternative of MSB or LSB
Interrupt signal	int_spim

Figure 7-2 shows Sensor Interface SPI Timing Diagram.

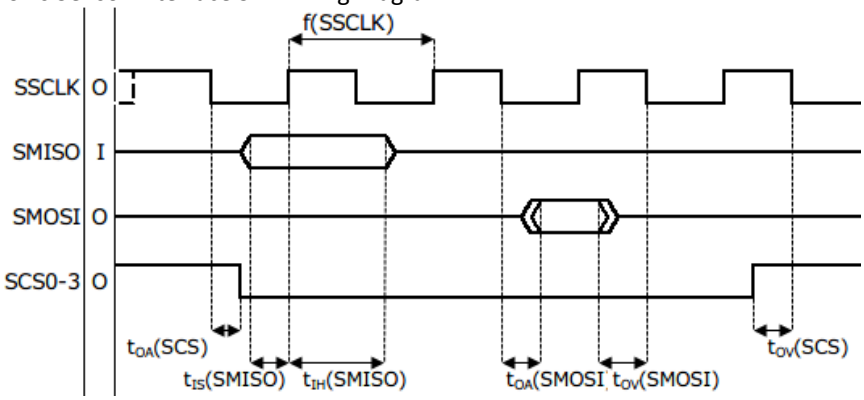


Figure 7-2 Sensor Interface SPI Timing Diagram

Table 7-3 shows Sensor Interface SPI dynamic characteristics.

Table 7-3 Sensor Interface SPI dynamic characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI Clock Frequency	f(SSCLK)		-	8	10.8[3]	MHz
Data input setup Time	t_{IS}(SMISO)		14.5	-	-	ns
Data input hold Time	t_{IH}(SMISO)		0	-	-	ns
Data output Access time	t_{OA}(SMOSI)	output load 35pF@3.3V or 20pF@1.8V	-	-	2.5	ns
	t_{OA}(SCS)	↑	-	-	2.5	ns
Data output Valid time	t_{OV}(SMOSI)	↑	-	-	8	ns
	t_{OV}(SCS)	↑	-	-	8	ns

[3] SPI clock maximum frequency is one five of CLK_PERI.

7.4. GPIO

Table 7-4 shows Peripheral GPIO implementation.

Table 7-4 Peripheral GPIO implementation

Function	Content
Port number	Up to 4 (alternative of SS signal for SPI, PWM output, and CTS/RTS signal for UART)
Specification	• General purpose input and output • Hi-Z output after reset-release • GPIO2 and GPIO3 can be used external interrupt input.
Interrupt signal	int_gpio2, int_gpio3

7.5. PWM

Table 7-5 shows Peripheral PWM implementation.

Table 7-5 Peripheral PWM implementation

Function	Content
Channel number	Up to 2
Specification	• Duty setting : 0.0015-99.9985% • Period setting : Divide CLK_PERI into 1/2-1/65535 • Minimum resolution : (2 / CLK_PERI) sec
Interrupt signal	(none)

7.6. UART

Table 7-6 shows Peripheral UART .

Table 7-6 Peripheral UART implementation

Function	Content
Clock	CLK_PERI
Specification	• Baud rate : CLKsource / 4080 – CLKsource / 16 bps • CLKsource: CLK_PERI or External input clock/2 • Format : ・ Data bit : 5 - 8bits ・ Stop bit : 1 or 2 bits ・ Parity bit : odd, even, not use • FIFO size : Transfer 128byte, Receiver 128byte • Hardware flow control is available
Interrupt signal	int_uart

7.7. Timer

7.7.1 General-purpose timers

Table 7-7 shows General-purpose timers implementation.

Table 7-7 General-purpose timers implementation

Function	Content
Channel number	3 independent channels
Specification	• 32-bit resolution interval timer • Counter clock : CLK_XT • Interval period settings : 0 ~ 2^{32} - 1
Interrupt signal	TIM0, TIM1, TIM2

7.7.2 Awake timer

Table 7-8 shows Awake timer implementation.

Table 7-8 Awake timer implementation

Function	Content
Channel number	1
Specification	• 32-bit resolution interval timer • Counter clock : ROSC1 (100kHz) or external clock • Interval period settings : 0 ~ 2^{32} - 1
Interrupt signal	int_awake

8. Interrupt

There are 16 interrupt at the paraForce, including 4 external interrupt. Please refer User's Manual about interrupt details.

Table 8-1 Interrupt controller

#	Name	Interrupt Event	Priority level	type
0	TIM0	General-purpose timer0	1	Timer
1	TIM1	General-purpose timer1	2	Timer
2	message		4	Level
3	TIM2	General-purpose timer	3	Timer
4	AWake	Awake timer	4	Level
5	I2C master		1	Level
6	UART Master		1	Level
7	GPIO3	External interrupt 1	1	Level
8	(not use)	-	-	-
9	SPI Master		1	Level
10	GPIO2	External interrupt 0	1	Level
11	(not use)	-	-	-
12	(not use)	-	-	-
13	FIFO RD	DPBUS FIFO	1	Edge
14	GPIO3	External interrupt 1	1	Edge
15	GPIO2	External interrupt 0	1	Edge

9. Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Ratings	Symbol	Min.	Max.	Unit
I/O Power Supply Voltage	DVDD18	-0.5	3.63	V
Core Power Supply Voltage	DVDD12	-0.5	1.32	V
Analog Power Supply Voltage	ROSC_AVDD	-0.5	1.32	V
IO Voltage	VPAD	-0.5	DVDD18 + 0.5	V
Junction Operating Temperature	Tj	-40	125	C

10. Recommended Operating Conditions

Table 10-1 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I/O Power Supply	DVDD18	1.8V	1.62	1.8	1.98	V
		2.5V	2.25	2.5	2.75	V
		2.8V	2.52	2.8	3.08	V
		3.0V	2.7	3	3.3	
		3.3V	2.97	3.3	3.63	V
Core Power Supply	DVDD12	1.2V	1.08	1.2	1.32	V
Analog Power Supply	ROSC_AVDD	1.2V	1.08	1.2	1.32	V
Ambient Temperature	Ta	-	-20	-	85	C

11. DC Characteristics

Table 11-1 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-Level Input Voltage	VIH	DVDD18=1.8V	0.7*DVDD18	-	DVDD18+0.3	V
		DVDD18=3.3V	0.7*DVDD18	-	DVDD18+0.3	V
Low-Level Input Voltage	VIL	DVDD18=1.8V	DVSS-0.3	-	0.3*DVDD18	V
		DVDD18=3.3V	DVSS-0.3	-	0.3*DVDD18	V
Hysteresis Schmitt Trigger	VHYS	-	0.4	-	-	V
Output current STX,GPIO(0,1,2,3), JTDO	IOH	DVDD18=1.8V,VOH=DVDD18-0.4	-	-	7.3	mA
		DVDD18=2.5V,VOH=DVDD18-0.4	-	-	5.7	mA
		DVDD18=3.3V,VOH=DVDD18-0.4	-	-	7.3	mA
	IOL	DVDD18=1.8V,VOH=0.4V	-8.7	-	-	mA
		DVDD18=2.5V,VOH=0.4V	-6.6	-	-	mA
		DVDD18=3.3V,VOH=0.4V	-8.2	-	-	mA
Output current HSDA,HMiSO,SSCLK, SMOSI,SSCL,SSDA	IOH	DVDD18=1.8V,VOH=DVDD18-0.4	-	-	9.8	mA
		DVDD18=2.5V,VOH=DVDD18-0.4	-	-	9.5	mA
		DVDD18=3.3V,VOH=DVDD18-0.4	-	-	12.3	mA
	IOL	DVDD18=1.8V,VOH=0.4V	-11.7	-	-	mA
		DVDD18=2.5V,VOH=0.4V	-11.1	-	-	mA
		DVDD18=3.3V,VOH=0.4V	-13.8	-	-	mA
Static Output Voltage STX,GPIO(0,1,2,3), JTDO	VOH	DVDD18=1.62V,4mA	DVDD18-0.4	-	-	V
		DVDD18=2.97V,4mA	DVDD18-0.4	-	-	V
	VOL	DVDD18=1.62V,4mA	-	-	0.4	V
		DVDD18=2.97V,4mA	-	-	0.4	V
Static Output Voltage HSDA,HMiSO,SSCLK, SMOSI,SSCL,SSDA	VOH	DVDD18=1.62V,8mA	DVDD18-0.4	-	-	V
		DVDD18=2.97V,8mA	DVDD18-0.4	-	-	V
	VOL	DVDD18=1.62V,8mA	-	-	0.4	V
		DVDD18=2.97V,8mA	-	-	0.4	V
Input leakage current	IL	DVDD18=1.8V,3.3V VI=0,DVDD18	-	-	<1	uA
Pull-down current	IPD	DVDD18=1.8V	23	42	85	uA
		DVDD18=3.3V	44	81	154	uA
Pull-up current	IPU	DVDD18=1.8V	29	51	91	uA
		DVDD18=3.3V	54	89	144	uA
Leakage current	$IDDQ_{on}$	DVDD12=1.32V, Core: Active (STANDBY pin = “H”)	-	-	4	mA
	$IDDQ_{off}$	DVDD12=1.32V, Core: Standby (STANDBY pin = “L”)	-	-	0.06	mA
Dynamic current	IDD_{on}	DVDD12=1.32V, Core: Active (STANDBY pin = “H”)	-	-	20	mA
	IDD_{off}	DVDD12=1.32V, Core: Standby (STANDBY pin = “L”)	-	-	0.2	mA

12. AC Characteristics

Table 12-1 AC Characteristics [STX,GPIO(0,1,2,3),JTDO] (DVDD18=1.8V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 4mA	CLOAD=5pF	0.7	1.2	1.9	ns
		Input	CLOAD=0.2pF	-	1.1	-	ns
		Input with schmitt		-	1.2	-	ns
Rise Time 10% to 90%	tr	Output 4mA	CLOAD=5pF	0.7	1.2	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 4mA	CLOAD=5pF	0.7	1.2	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

Table 12-2 AC Characteristics [STX,GPIO(0,1,2,3),JTDO] (DVDD18=3.3V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 4mA	CLOAD=5pF	1.3	2.0	2.9	ns
		Input	CLOAD=0.2pF	-	0.7	-	ns
		Input with schmitt		-	0.9	-	ns
Rise Time 10% to 90%	tr	Output 4mA	CLOAD=5pF	0.8	1.3	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 4mA	CLOAD=5pF	0.8	1.3	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

Table 12-3 AC Characteristics [HSDA,HMiSO,SSCLK,SMOSI,SSCL,SSDA] (DVDD18=1.8V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 8mA	CLOAD=10pF	2.0	3.2	4.9	ns
		Input	CLOAD=0.2pF	-	1.1	-	ns
		Input with schmitt		-	1.2	-	ns
Rise Time 10% to 90%	tr	Output 8mA	CLOAD=10pF	1.1	1.8	2.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 8mA	CLOAD=10pF	0.9	1.5	2.4	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

Table 12-4 AC Characteristics [HSDA,HMiSO,SSCLK,SMOSI,SSCL,SSDA] (DVDD18=3.3V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 8mA	CLOAD=10pF	1.5	2.3	3.3	ns
		Input	CLOAD=0.2pF	-	0.7	-	ns
		Input with schmitt		-	0.9	-	ns
Rise Time 10% to 90%	tr	Output 8mA	CLOAD=10pF	0.8	1.3	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 8mA	CLOAD=10pF	0.8	1.3	1.9	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

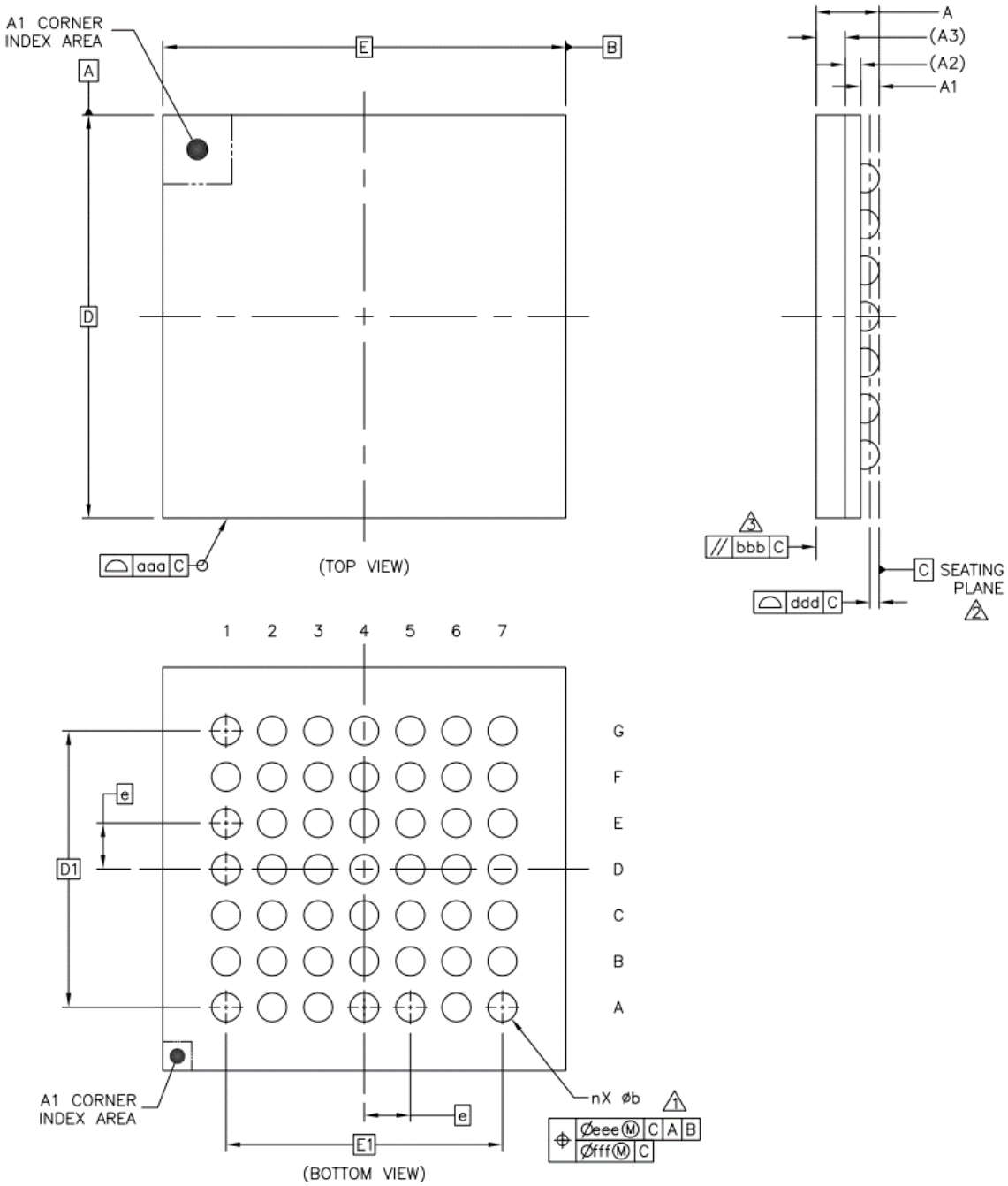
13. Ball Map

	1	2	3	4	5	6	7	
A	NC	DVSS	CLKIN	DVDD12	DVSS	DVDD18	NC	A
B	DVDD12	DVDD18	SELCLK	DSPRUN	STANDBY	HSS	HMISO	B
C	GPIO0	GPIO3	SEL0	SEL1	SELVDD	HMOSI	HSCLK	C
D	JTCK	GPIO1	GPIO2	DVSS	SELRST	DVDD12	ROSC_ AVDD	D
E	JTRST	JTDO	SRX	DVSS	RSTB	DVSS	ROSC_ AVSS	E
F	JTMS	JTDI	STX	SMISO	SSCLK	SMOSI	DVDD18	F
G	NC	DVDD18	DVSS	DVDD12	SSCL	SSDA	NC	G
	1	2	3	4	5	6	7	

Figure 13-1 Ball Map (Top View)

In Figure 13-1, NC pin MUST be non-connection, be careful not to connect to Power Pin (DVDD12, DVDD18, ROSC_AVDD), GND pin (DVSS, ROSC_DVSS), and other signal pins.

14. Outline Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.65
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.136	REF
MOLD THICKNESS	A3		0.25	REF
BODY SIZE	D		3.5	BSC
	E		3.5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.22	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.4	BSC
BALL COUNT	n		49	
EDGE BALL CENTER TO CENTER	D1		2.4	BSC
	E1		2.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

⚠1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.

⚠2 DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

⚠3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

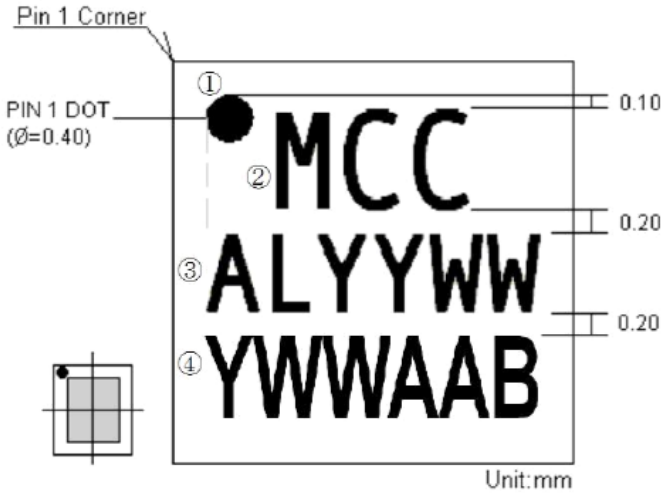
Figure 14-1 Package Outline Drawing[4][5][6]

[4] The unit of package outline drawing is a millimeter.
[5] REF stands for Reference. BSC stands for Basic Spacing between Centers.
[6] BALL DIAMETER means ball size before ball mount, BALL WIDTH means ball size after ball mount.

15. Marking Specification

① A1 Indicator Mark
② Line1 / Company Name : MCC
③ Line2 / Factory Code + Date Code : ALYYMM
- Factory Code : AL (AL : ASE Chung-LI)
- Date Code : YYWW
  - YY : Bottom 2 figures if A.D. are filled
  - WW : Work Week is filled
- ex) Manufacture date : Work Week 38, 2014 -> AL1438

④ Line3 / Assembly Lot Number : YWWAAB
- Y : Year of assemble working order issued
- WW : Work week of assembly working order issued
- AA : Running number starting from 00 to 99
- B : Split code during assembly process



Line#	Description		Position	Font Type	Character				
					Height	Width	Space	Max Width	Max. Chars
Line1	Company Name	MCC	Center	ARIAL-0.FT	0.88mm	0.50mm	0.10mm	1.70mm	3
Line2	Factory Code + Date Code	ALYYWW	Center	ARIAL-0.FT	0.70mm	0.40mm	0.10mm	2.90mm	6
Line3	Assembly Lot Number	YWWAAB	Center	ARIAL-0.FT	0.70mm	0.40mm	0.10mm	2.90mm	6

Figure 15-1 Marking Specification

16. Recommended Land Pattern

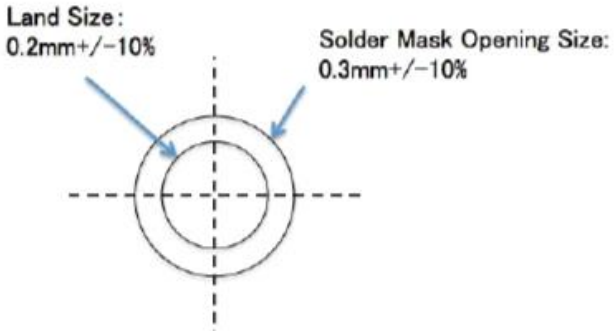


Figure 16-1 Recommended Land Pattern

17. Power Sequence

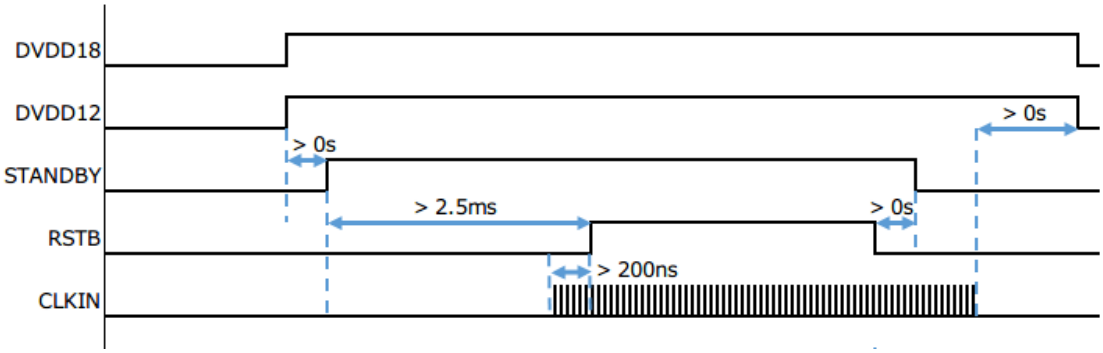


Figure 17-1 Power Sequence

All input signals, including STANDBY pin, should be worked after DVDD18 and DVDD12 are stable.

18. Pin Process/ Peripherals

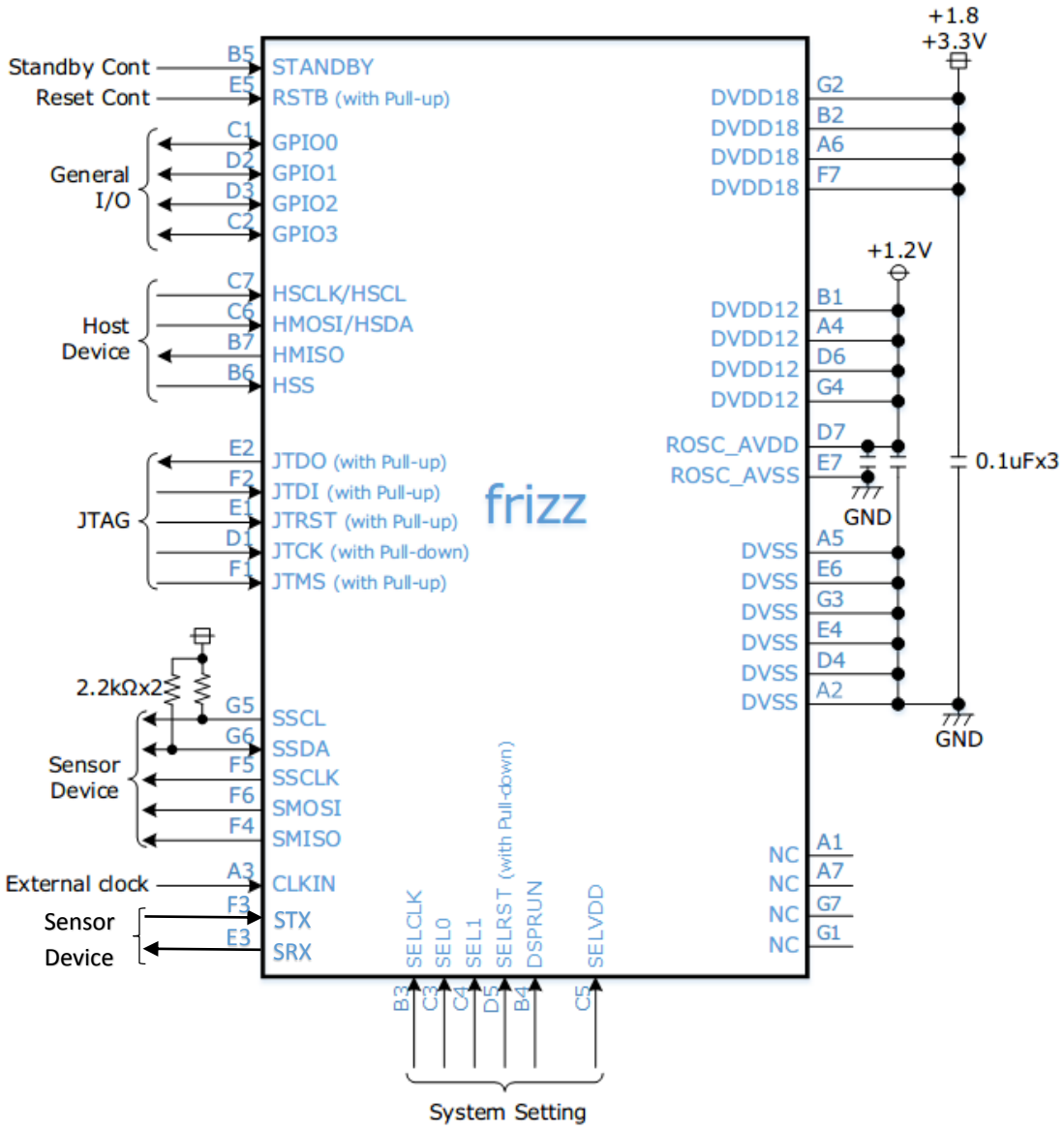
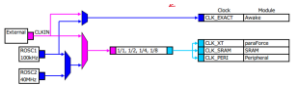
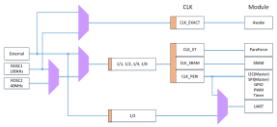


Figure 18-1 Pin Process/Peripherals

Definition/Revision History			
Standard	frizz Product Specification	No.	SPS-MA60000-EN-D

Date of D/R/A	Rev.	Contents of Definition/Revision	D/R/A by			
			Final Aprv.	Aprv.	Rvw.	Crt.
09/02/2014		Released	Hayashi	Naka-mura	Matsu-moto	Yoshi-mura
11/26/2014	A	Title: changed from “frizz ES1” to “frizz” 5.3 paraForce Initial Settings : DSPRUN changed function description as below. <Before>DSPRUN pin can set paraForce initial settings after reset release. Generally, DSPRUN pin is set to “L” (Run). When debugging by JTAG, DSPRUN pin is set to “H” (Stall). <After>DSPRUN pin can set paraForce initial settings after reset release. Generally, DSPRUN pin is set to **“H” (Stall)**. When debugging by JTAG, DSPRUN pin is set to **“L” (Run)**. 2 Specification, add bottom note as below. frizz can work at 1.8V to 3.3V I/O voltage, it is design assurance. 5.6 System Clock, add description as below. CLK_EXACT is for Awake timer. … It requires CLKIN input to change CLK_EXACT source. 5.7 Low Power Modes: Power consumption value is deleted at Table 5-5 Low power modes specifications. 11 DC Characteristics: Updated IPU and IPD at Table 11-1. 17 Power Sequence: Updated Figure 17-1.	Sasaki	Naka-mura	Matsu-moto	Yoshi-mura
6/1/2015	B	5.6.3 Change description as below. <Before> by xmode1[11] register. <After> by xmode0[11] register. 11 DC Characteristics: Added Leakage current and Dynamic current at Table 11-1.	Sasaki	Naka-mura	Matsu-moto	Yoshi-mura
5/11/2016	C	15 Marking Specification: updated marking specification.	Iwao	Asakura	Matsu-moto	Yoshi-mura
Oct.3rd,2016	D	1.Overview :add table as below. Table 1-2 order code 4.External Terminal Specification Table4-1: Change description as below. complete revision Main change: add Recommended connection of Unused Pins, Power Pins. 5.5.1 POR(Power On Reset) table 5-2 :delete condition content. 1V/1s power up ratio, 1V/1us power up ratio	Iwao	Iwao	Matsu-moto	Inaoka

Definition/Revision History			
Standard	frizz Product Specification	No.	SPS-MA60000-EN-D

Date of D/R/A	Rev.	Contents of Definition/Revision	D/R/A by			
			Final Aprv.	Aprv.	Rvw.	Crt.
		5.6 System Clock Figure 5-3: Change description as below. <Before>  <After> 				
		5.7 Low power modesTable5-5: Change description as below. recovery time of Sleep(Slow –CLK) <Before> <2ms <After> <500us recovery time of Stop <Before> 50us-2ms <After> <500us				
		6.2 SPI/I2C Table 6-1: Change description as below. <Before> Table 6 1 Host interface SPI dynamic characteristics <After> Table 6 1 Host interface SPI dynamic characteristics(DVDD18=1.8V) Table 6 2 Host interface SPI dynamic characteristics(DVDD18=3.3V				
		6.2 SPI/I2C Table 6-2: Change description as below. <Before> Table 6-2 I2C Characteristics <After> Table 6-3 I2C Characteristics Change of the line (Parameter/ Symbol)				
		7.6 UART Table 7-6 :add Specification as below. <Before> Baud rate : CLK_PERI / 4080 – CLK_PERI / 16bps <After> Baud rate : CLKsource / 4080 – CLKsource / 16 bps CLKsource: CLK_PERI or External input clock/2				
		9.Absolute Maximum Ratings Table9-1:delete Storage Temperature and Humidity				
		11.DC Characteristics Table 11-1: Change DC current as below. <Before> DC current <After> Output current *change to the electric current for Pin name.				
		Add input leakage current as below. Input Leakage current IL DVDD18=1.8V,3.3V…..uA				

Definition/Revision History			
Standard	frizz Product Specification	No.	SPS-MA60000-EN-D

Date of D/R/A	Rev.	Contents of Definition/Revision	D/R/A by			
			Final Aprv.	Aprv.	Rvw.	Crt.
		12.AC Characteristics Table12-1,12-2: Change description as below. <Before> Table 12 1 AC Characteristics (DVDD=1.8V) Table 12 2 AC Characteristics (DVDD=3.3V) <After> Table 12 1 AC Characteristics [STX,GPIO(0,1,2,3),JTDO] (DVDD18=1.8V) Table 12 2 AC Characteristics [STX,GPIO(0,1,2,3),JTDO] (DVDD18=3.3V) Table 12 3 AC Characteristics [HSDA,HMiSO,SSCLK,SMOSI,SSCL,SSDA] (DVDD18=1.8V) Table 12 4 AC Characteristics [HSDA,HMiSO,SSCLK,SMOSI,SSCL,SSDA] (DVDD18=3.3V) 18 Pin Process/Peropherals Figure 18-1:add uart pin as below