HT32F50220/HT32F50230
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 32 KB Flash and 4 KB SRAM with 1 MSPS ADC,
DIV, UART, SPI, I²C, GPTM, PWM, BFTM, WDT, RTC

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1 General Description

The Holtek HT32F50220/HT32F50230 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 20 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and 4 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, I^2C, UART, SPI, GPTM, PWM, BFTM, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application controllers, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor controllers and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 20 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O port, hardware multiplier and low latency interrupt respond time.

On-chip Memory

- Up to 32 KB on-chip Flash memory for instruction/data and options storage
- 4 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F50220/HT32F50230 series of devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word program/page erase functions are also provided.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, Load in 1 clock cycle
- Divide by zero error Flag

The divider is the truncated division and need a software triggered start signal by using the control register "START" bit, after 8 clock cycles, the divider calculate complete flag will be set to 1, and if divisor register data is zero, the divide zero error flag will be set to 1.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power on Reset / Power down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 20 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 20 MHz RC oscillator trimmed to ±2 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Flexible power supply: V_{DD} power supply (2.5 V ~ 5.5 V), V_{DDIO} for I/O (1.8 V ~ 5.5 V)
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- Three power domains: V_{DD}, V_{DDIO} and 1.5 V.
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many

types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

I/O Ports – GPIO

- Up to 40 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current

There are up to 40 General Purpose I/O pins, GPIO, named from PA0 ~ PA15, PB0 ~ PB15 and PC0 ~ PC7 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

PWM Generation and Capture Timers – GPTM

- One 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Pulse Width Modulation – PWM

- One 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse Width Modulator consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- One 32-bit compare/match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V_{DD15} power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: (1). 100 kHz in the Standard mode, (2). 400 kHz in the Fast mode and (3). 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides a SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 24/28-pin SSOP, 28-pin SOP, 24/33-pin QFN and 44/48-pin LQFP packages
- Operation temperature range: -40 °C to +85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F50220	HT32F50230
Main Flash (KB)		16	31
Option Bytes Flash (KB)		1	1
SRAM (KB)		4	4
Timers	GPTM	1	
	PWM	2	
	BFTM	1	
	WDT	1	
	RTC	1	
Communication	SPI	2	
	UART	2	
	I^2C	1	
Hardware Divider		1	
EXTI		16	
12-bit ADC Number of channels		1	
		12 Channels	
GPIO		Up to 40	
CPU frequency		Up to 20 MHz	
Operating voltage		2.5 V ~ 5.5 V	
Operating temperature		-40 °C ~ +85 °C	
Package		24/28-pin SSOP, 28-pin SOP, 24/33-pin QFN and 44/48-pin LQFP	

Block Diagram

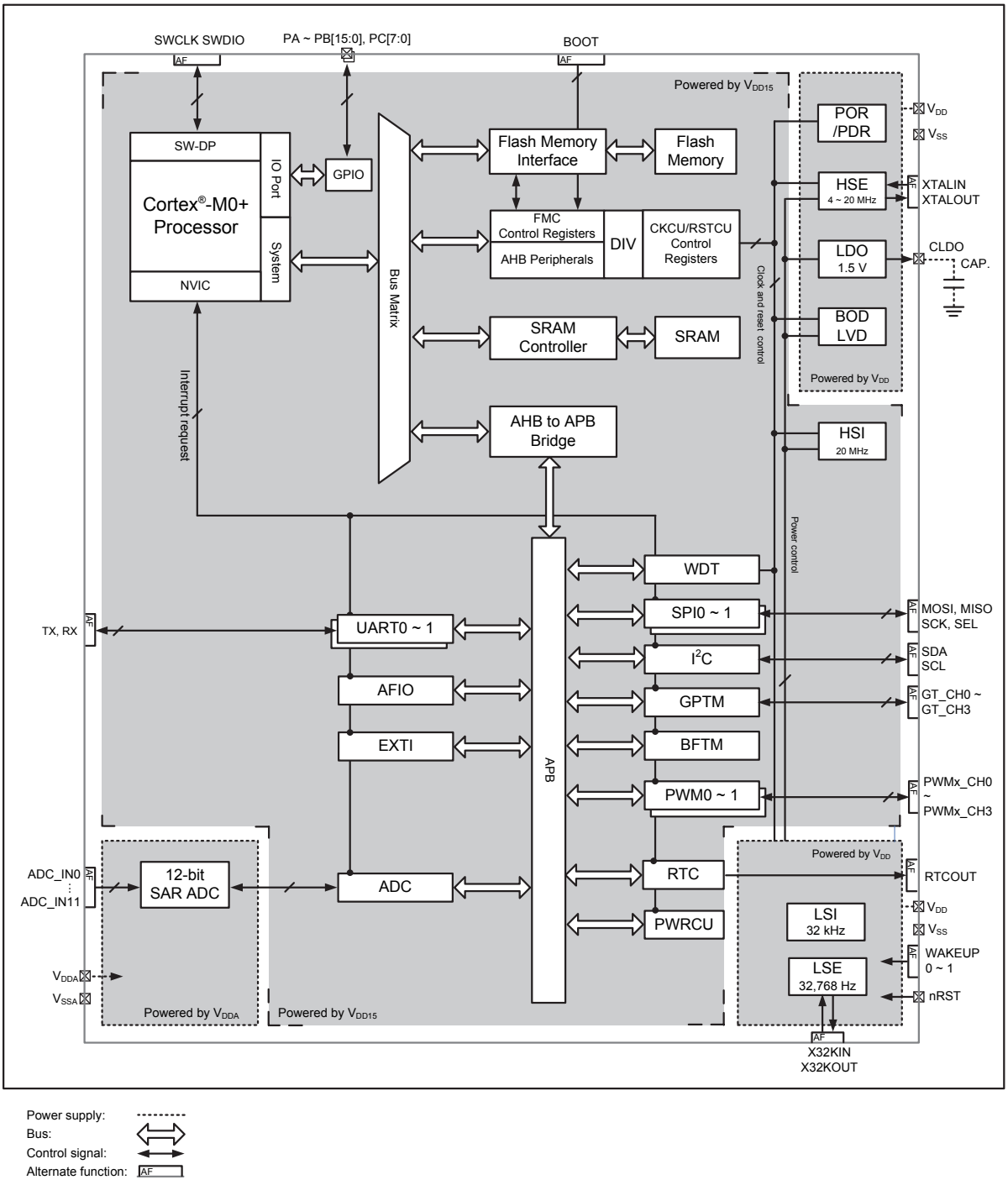


Figure 1. Block Diagram

Memory Map

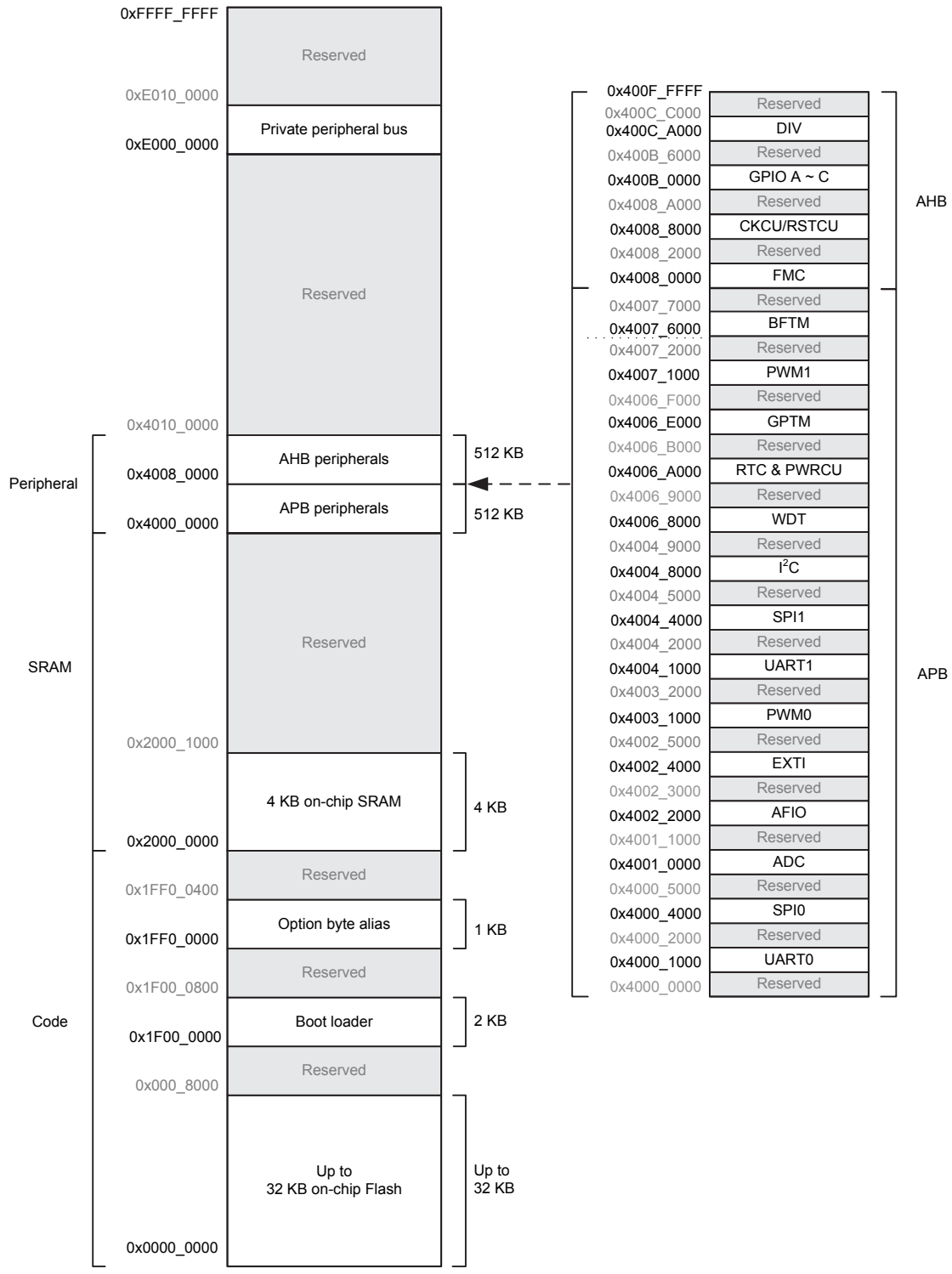


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	APB
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	
0x4007_2000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	AHB
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

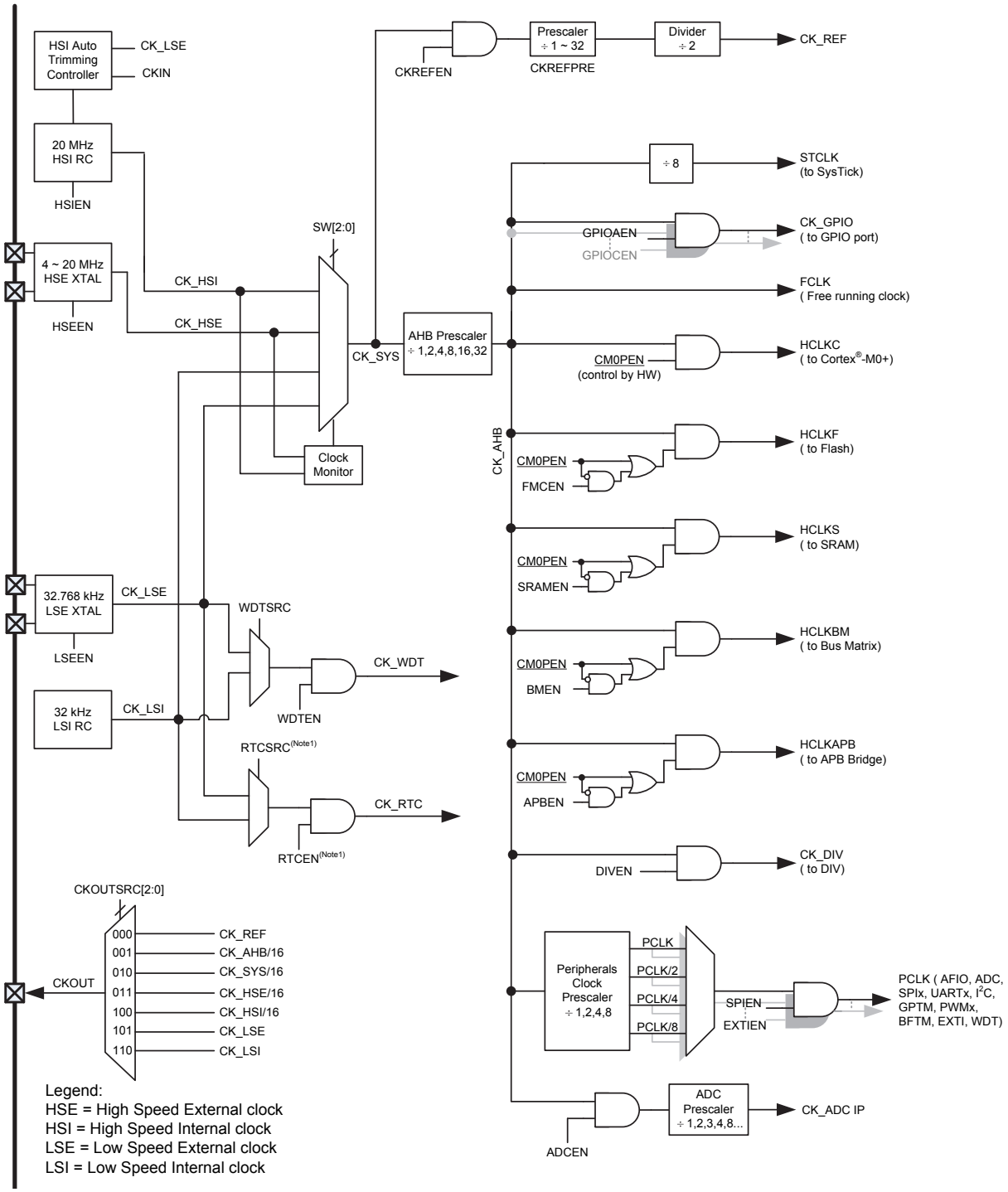


Figure 3. Clock Structure

4 Pin Assignment

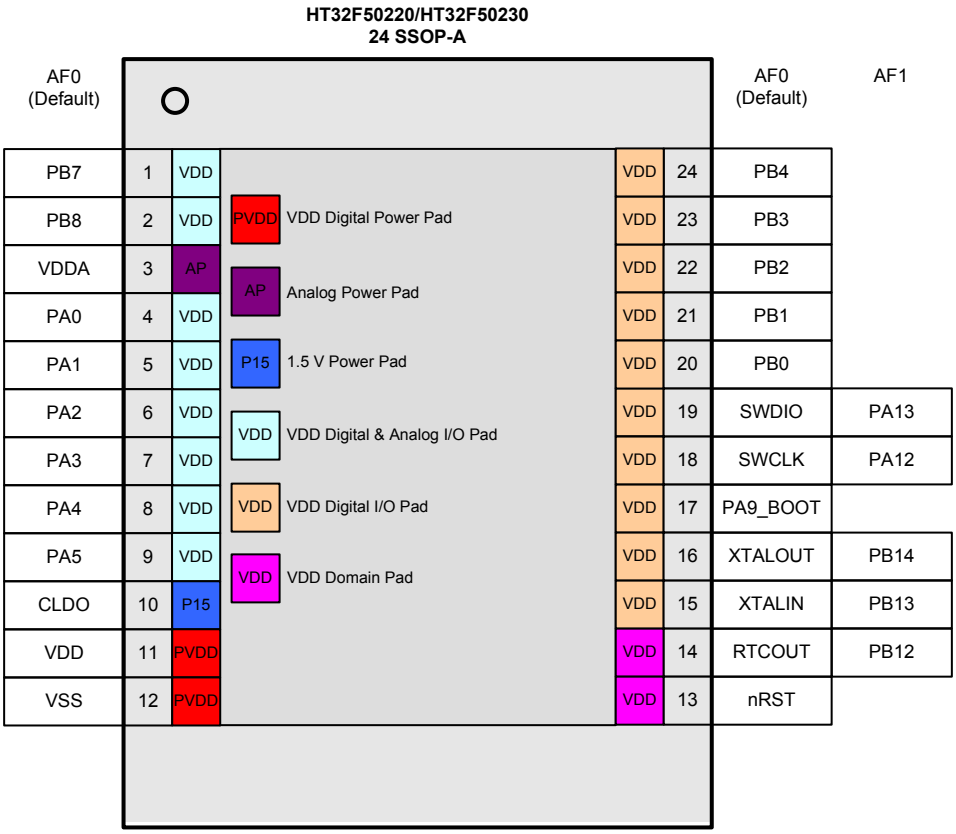


Figure 4. 24-pin SSOP Pin Assignment

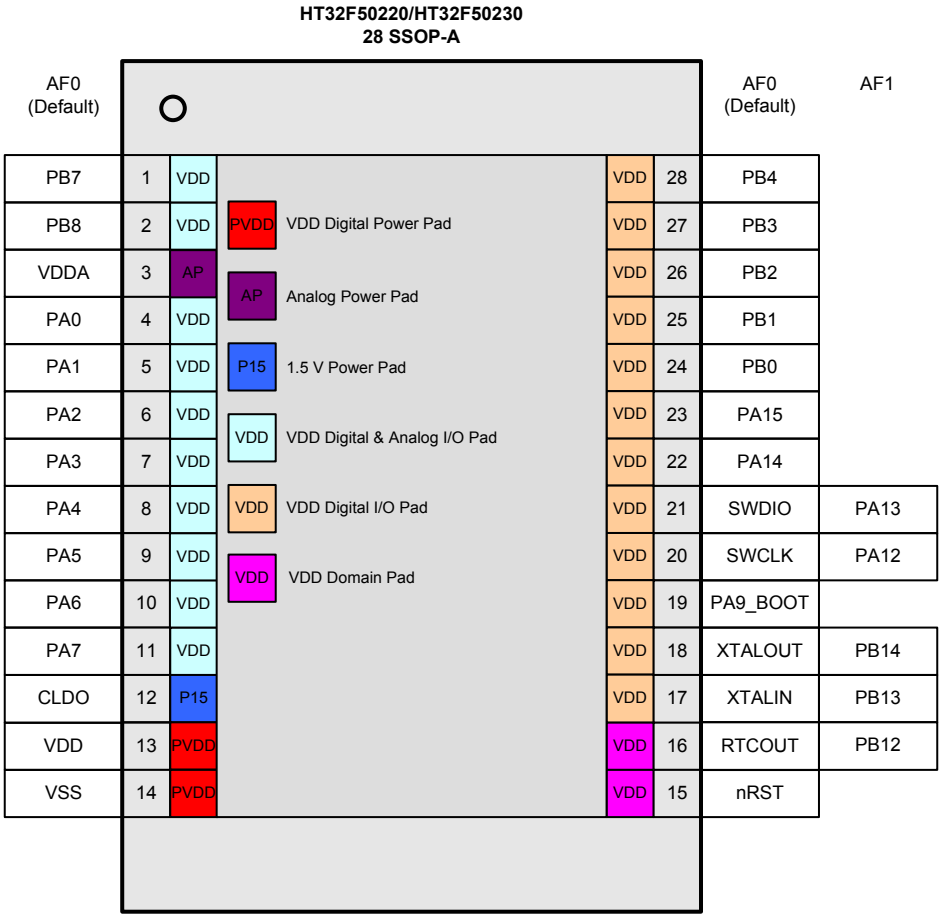


Figure 5. 28-pin SSOP Pin Assignment

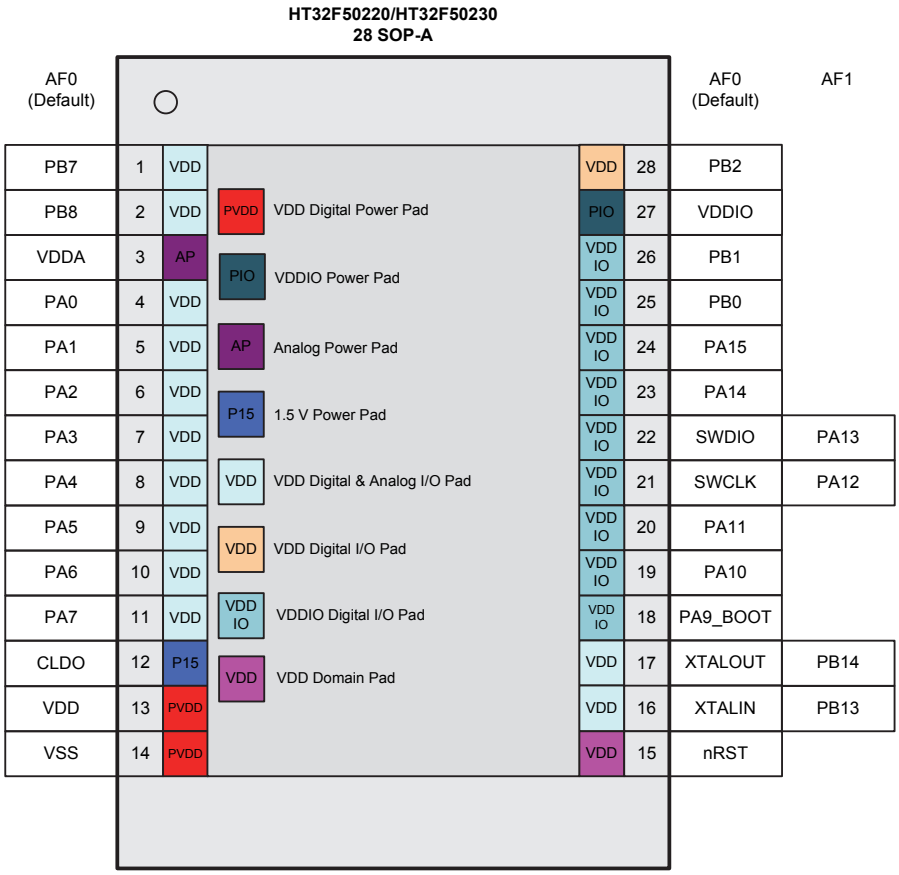


Figure 6. 28-pin SOP Pin Assignment

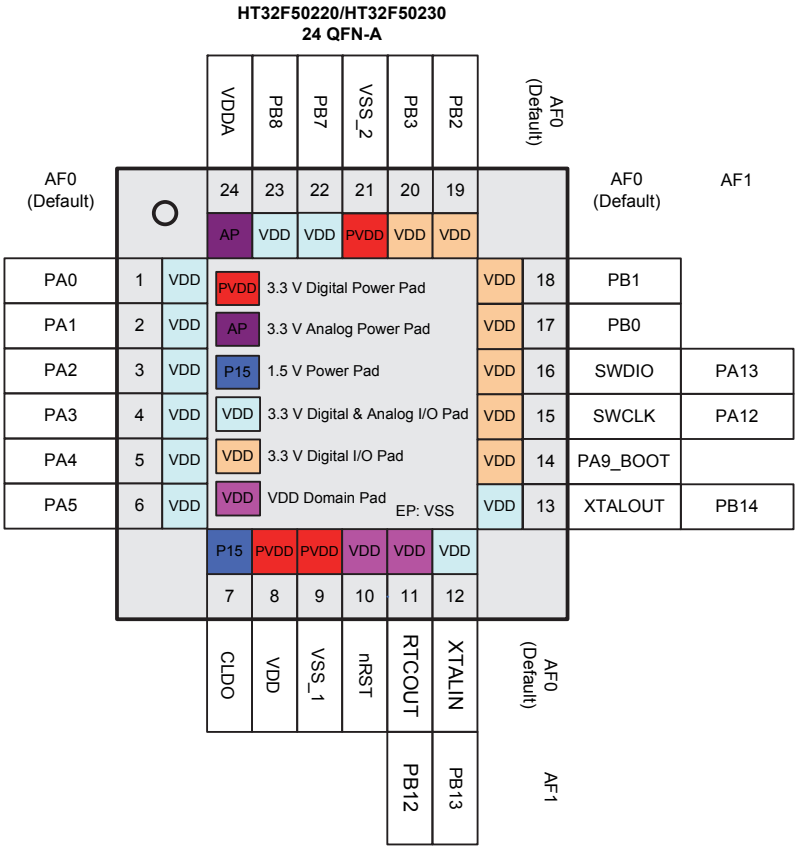


Figure 7. 24-pin QFN Pin Assignment

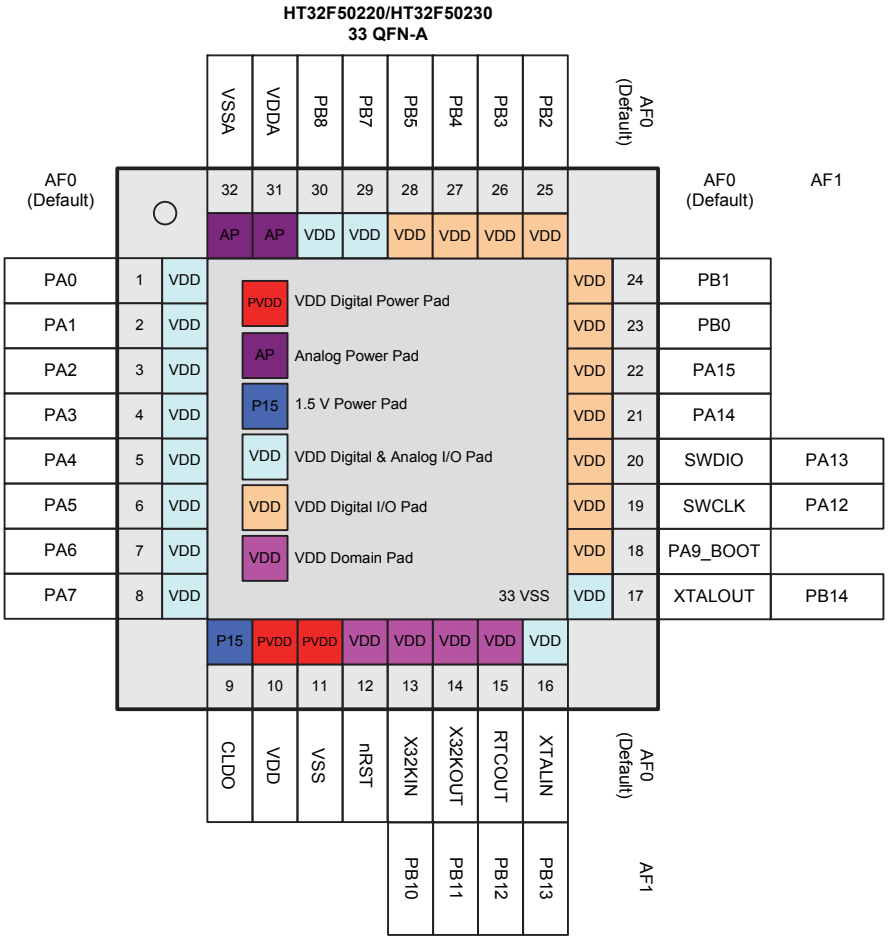


Figure 8. 33-pin QFN Pin Assignment

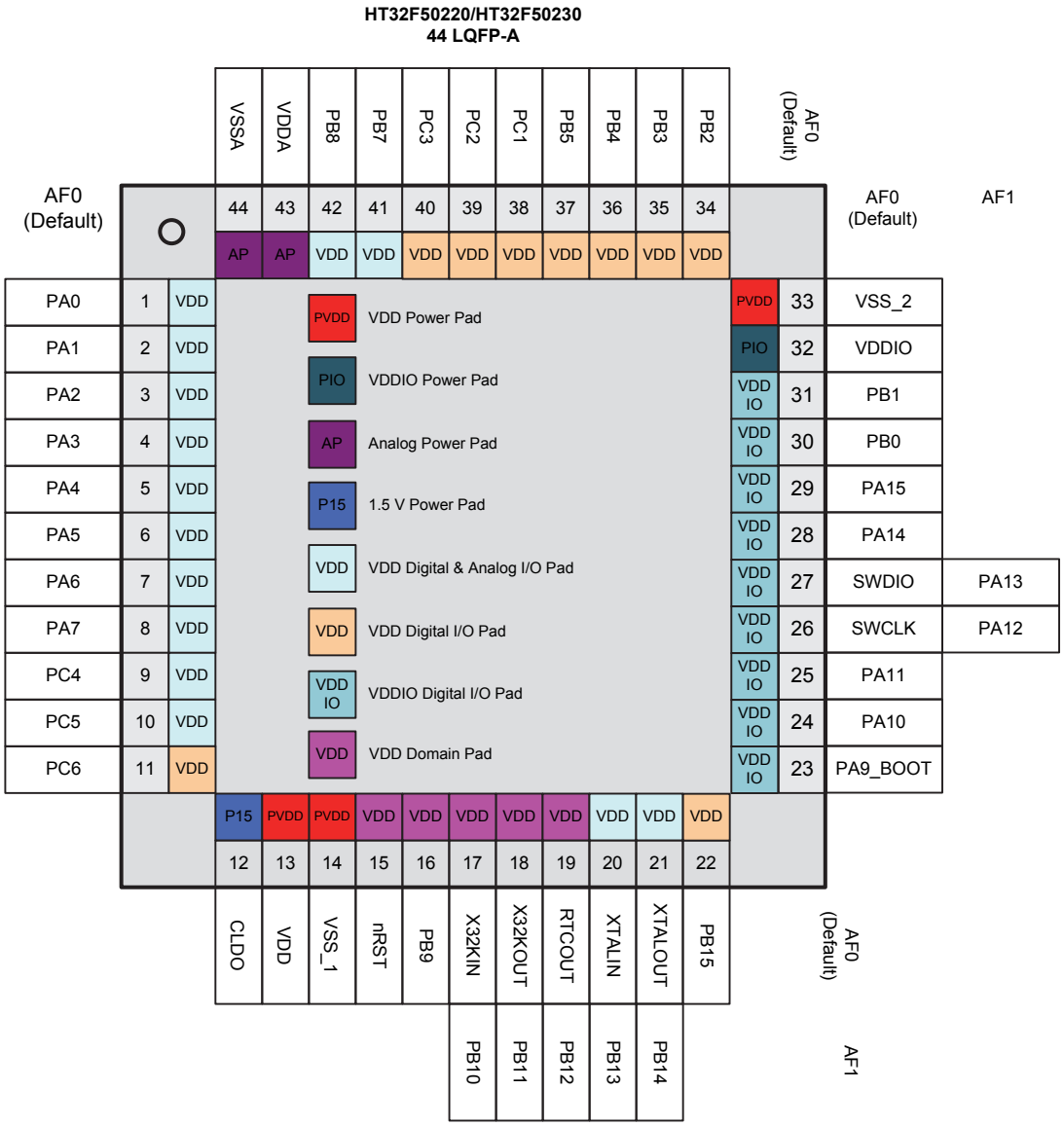


Figure 9. 44-pin LQFP Pin Assignment

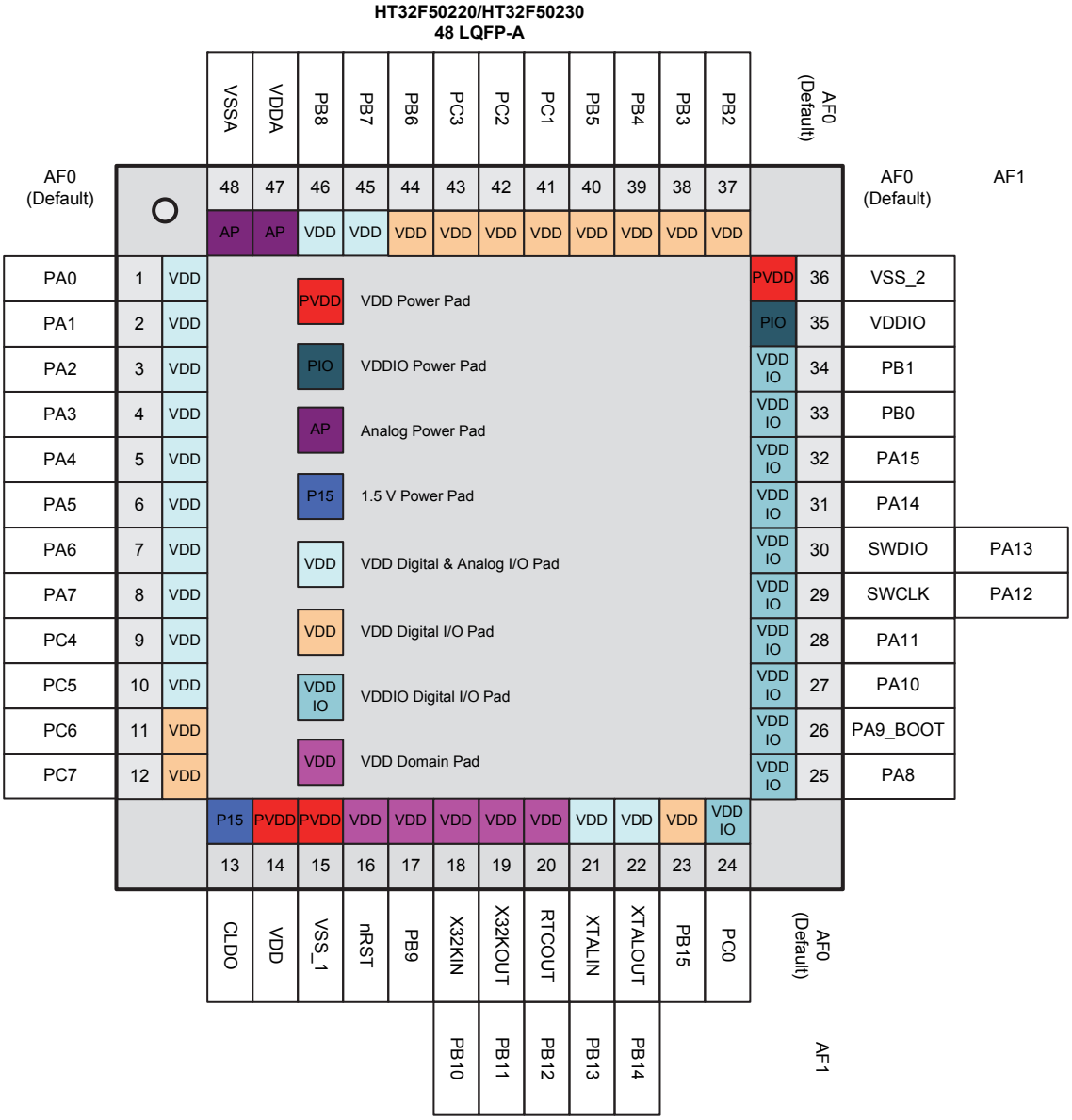


Figure 10. 48-pin LQFP Pin Assignment

Table 3. Pin Assignment

Packages							Alternate Function Mapping														
							AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	44 LQFP	33 QFN	28 SOP	28 SSOP	24 SSOP	24 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I2C	N/A	N/A	N/A	N/A	N/A	PWM	N/A	System Other
1	1	1	4	4	4	1	PA0		ADC_IN2		GT_CH0	SPI1_SCK		I2C_SCL								
2	2	2	5	5	5	2	PA1		ADC_IN3		GT_CH1	SPI1_MOSI		I2C_SDA								
3	3	3	6	6	6	3	PA2		ADC_IN4		GT_CH2	SPI1_MISO	UR0_TX									
4	4	4	7	7	7	4	PA3		ADC_IN5		GT_CH3	SPI1_SEL	UR0_RX									
5	5	5	8	8	8	5	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C_SCL								
6	6	6	9	9	9	6	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C_SDA								
7	7	7	10	10			PA6		ADC_IN8		GT_CH2	SPI0_MISO										
8	8	8	11	11			PA7		ADC_IN9		GT_CH3	SPI0_SEL										
9	9						PC4		ADC_IN10				UR1_TX							PWM1_CH0		
10	10						PC5		ADC_IN11				UR1_RX							PWM1_CH1		
11	11						PC6				GT_CH0		UR0_TX	I2C_SCL								
12							PC7				GT_CH1		UR0_RX	I2C_SDA								
13	12	9	12	12	10	7	CLDO															
14	13	10	13	13	11	8	VDD															
15	14	11	14	14	12	9	VSS_1															
16	15	12	15	15	13	10	nRST															
17	16						PB9				GT_CH3									PWM1_CH2		WAKEUP1
18	17	13					X32KIN	PB10			GT_CH0	SPI1_SEL	UR1_TX							PWM1_CH3		
19	18	14					X32KOUT	PB11			GT_CH1	SPI1_SCK	UR1_RX							PWM0_CH3		
20	19	15		16	14	11	RTCOUT	PB12				SPI0_MISO	UR0_RX							PWM0_CH0		WAKEUP0
21	20	16	16	17	15	12	XTALIN	PB13					UR0_TX	I2C_SCL								
22	21	17	17	18	16	13	XTALOUT	PB14					UR0_RX	I2C_SDA								
23	22						PB15				GT_CH0	SPI0_SEL		I2C_SCL						PWM0_CH1		
24							PC0				GT_CH1	SPI0_SCK		I2C_SDA						PWM0_CH2		
25							PA8						UR1_TX							PWM1_CH3		
26	23	18	18	19	17	14	PA9_BOOT					SPI0_MOSI								PWM1_CH0		CKOUT
27	24		19				PA10				GT_CH2	SPI0_MOSI	UR1_RX							PWM0_CH1		
28	25		20				PA11				GT_CH3	SPI0_MISO								PWM0_CH2		
29	26	19	21	20	18	15	SWCLK	PA12														
30	27	20	22	21	19	16	SWDIO	PA13														
31	28	21	23	22			PA14				GT_CH0	SPI1_SEL	UR1_TX	I2C_SCL						PWM0_CH0		
32	29	22	24	23			PA15				GT_CH0	SPI1_SCK	UR1_RX	I2C_SDA						PWM1_CH2		
33	30	23	25	24	20	17	PB0				GT_CH1	SPI1_MOSI	UR0_TX	I2C_SCL						PWM0_CH1		
34	31	24	26	25	21	18	PB1				GT_CH1	SPI1_MISO	UR0_RX	I2C_SDA						PWM1_CH1		
35	32		27				VDDIO															
36	33	33				21	VSS_2															
37	34	25	28	26	22	19	PB2				GT_CH2	SPI0_SEL	UR1_TX							PWM0_CH2		CKIN
38	35	26		27	23	20	PB3				GT_CH2	SPI0_SCK	UR1_RX							PWM1_CH2		

Packages							Alternate Function Mapping														
							AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	44 LQFP	33 QFN	28 SOP	28 SSOP	24 SSOP	24 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I2C	N/A	N/A	N/A	N/A	N/A	PWM	N/A	System Other
39	36	27		28	24		PB4					SPI0_ MOSI	UR1_ TX							PWM0_ CH3		
40	37	28					PB5				GT_ CH2	SPI0_ MISO	UR1_ RX									
41	38						PC1				GT_ CH0	SPI1_ SEL	UR1_ TX							PWM0_ CH0		
42	39						PC2				GT_ CH1	SPI1_ SCK								PWM1_ CH0		
43	40						PC3					SPI1_ MOSI	UR1_ RX							PWM1_ CH1		
44							PB6				GT_ CH3	SPI1_ MISO	UR0_ TX									
45	41	29	1	1	1	22	PB7		ADC_ IN0		GT_ CH3	SPI0_ MISO	UR0_ TX	I2C_ SCL						PWM0_ CH3		
46	42	30	2	2	2	23	PB8		ADC_ IN1		GT_ CH3	SPI0_ SEL	UR0_ RX	I2C_ SDA						PWM1_ CH3		
47	43	31	3	3	3	24	VDDA															
48	44	32					VSSA															

Note: 1. For the 24QFN package, the EP VSS is internally connected to the pin number 21. The EP is meant the exposed pad of the QFN package.
2. The pin number 33 of the QFN33 is located at the exposed pad of the QFN package.

Table 4. Pin Description

Pin Number							Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	44 LQFP	33 QFN	28 SOP	28 SSOP	24 SSOP	24 QFN					Default function (AF0)
1	1	1	4	4	4	1	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	2	2	5	5	5	2	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	3	3	6	6	6	3	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	4	4	7	7	7	4	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	5	5	8	8	8	5	PA4	AI/O	5V	4/8/12/16 mA	PA4
6	6	6	9	9	9	6	PA5	AI/O	5V	4/8/12/16 mA	PA5
7	7	7	10	10			PA6	AI/O	5V	4/8/12/16 mA	PA6
8	8	8	11	11			PA7	AI/O	5V	4/8/12/16 mA	PA7
9	9						PC4	AI/O	5V	4/8/12/16 mA	PC4
10	10						PC5	AI/O	5V	4/8/12/16 mA	PC5
11	11						PC6	I/O	5V	4/8/12/16 mA	PC6
12							PC7	I/O	5V	4/8/12/16 mA	PC7
13	12	9	12	12	10	7	CLDO	P	—	—	Core power LDO 1.5 V output It is recommended to connect a 2.2 μF capacitor as close as possible between this pin and VSS_1.
14	13	10	13	13	11	8	VDD	P	—	—	Voltage for digital I/O
15	14	11	14	14	12	9	VSS_1	P	—	—	Ground reference for digital I/O
16	15	12	15	15	13	10	nRST(3)	I	5V_PU	—	External reset pin
17	16						PB9(3)	I/O (VDD)	5V	4/8/12/16 mA	PB9
18	17	13					PB10(3)	AI/O (VDD)	5V	4/8/12/16 mA	X32KIN
19	18	14					PB11(3)	AI/O (VDD)	5V	4/8/12/16 mA	X32KOUT
20	19	15		16	14	11	PB12(3)	I/O (VDD)	5V	4/8/12/16 mA	RTCOUT
21	20	16	16	17	15	12	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	21	17	17	18	16	13	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT

Pin Number							Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	44 LQFP	33 QFN	28 SOP	28 SSOP	24 SSOP	24 QFN					Default function (AF0)
23	22						PB15	I/O	5V	4/8/12/16 mA	PB15
24							PC0	I/O (VDDIO)	5V	4/8/12/16 mA	PC0
25							PA8	I/O (VDDIO)	5V	4/8/12/16 mA	PA8
26	23	18	18	19	17	14	PA9	I/O (VDDIO)	5V_PU	4/8/12/16 mA	PA9_BOOT
27	24		19				PA10	I/O (VDDIO)	5V	4/8/12/16 mA	PA10
28	25		20				PA11	I/O (VDDIO)	5V	4/8/12/16 mA	PA11
29	26	19	21	20	18	15	PA12	I/O (VDDIO)	5V_PU	4/8/12/16 mA	SWCLK
30	27	20	22	21	19	16	PA13	I/O (VDDIO)	5V_PU	4/8/12/16 mA	SWDIO
31	28	21	23	22			PA14	I/O (VDDIO)	5V	4/8/12/16 mA	PA14
32	29	22	24	23			PA15	I/O (VDDIO)	5V	4/8/12/16 mA	PA15
33	30	23	25	24	20	17	PB0	I/O (VDDIO)	5V	4/8/12/16 mA	PB0
34	31	24	26	25	21	18	PB1	I/O (VDDIO)	5V	4/8/12/16 mA	PB1
35	32		27				VDDIO	P	—	—	Voltage for digital I/O
36	33	33				21	VSS_2	P	—	—	Ground reference for digital I/O
37	34	25	28	26	22	19	PB2	I/O	5V	4/8/12/16 mA	PB2
38	35	26		27	23	20	PB3	I/O	5V	4/8/12/16 mA	PB3
39	36	27		28	24		PB4	I/O	5V	4/8/12/16 mA	PB4
40	37	28					PB5	I/O	5V	4/8/12/16 mA	PB5
41	38						PC1	I/O	5V	4/8/12/16 mA	PC1
42	39						PC2	I/O	5V	4/8/12/16 mA	PC2
43	40						PC3	I/O	5V	4/8/12/16 mA	PC3
44							PB6	I/O	5V	4/8/12/16 mA	PB6
45	41	29	1	1	1	22	PB7	AI/O	5V	4/8/12/16 mA	PB7
46	42	30	2	2	2	23	PB8	AI/O	5V	4/8/12/16 mA	PB8
47	43	31	3	3	3	24	VDDA	P	—	—	Analog voltage for ADC
48	44	32					VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = power supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = pull-up.
3. These pins are located at the V_{DD} power domain.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External main supply voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C
P_D	Total power dissipation	—	500	mW
V_{ESD}	Electrostatic discharge voltage – human body mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	—	2.5	5.0	5.5	V
V_{DDIO}	I/O operating voltage	—	1.8	5.0	5.5	V
V_{DDA}	Analog operating voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal regulator output voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming.	1.425	1.5	1.57	V
I_{LDO}	Output current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply current (Run mode)	V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, All peripherals enabled	—	5.7	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, All peripherals disabled	—	4.0	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 10 MHz, f_{PCLK} = 10 MHz, All peripherals enabled	—	3.1	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 10 MHz, f_{PCLK} = 10 MHz, All peripherals disabled	—	2.2	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 5 MHz, f_{PCLK} = 5 MHz, All peripherals enabled	—	1.8	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 5 MHz, f_{PCLK} = 5 MHz, All peripherals disabled	—	1.4	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 2.5 MHz, f_{PCLK} = 2.5 MHz, All peripherals enabled	—	1.2	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 2.5 MHz, f_{PCLK} = 2.5 MHz, All peripherals disabled	—	0.95	—	mA
		V_{DD} = 5.0 V, HSI off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, All peripherals enabled	—	30	—	μA
		V_{DD} = 5.0 V, HSI off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, All peripherals disabled	—	27	—	μA
	Supply current (Sleep mode)	V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, All peripherals enabled	—	2.7	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, All peripherals disabled	—	0.8	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 10 MHz, All peripherals enabled	—	1.6	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 10 MHz, All peripherals disabled	—	0.65	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 5 MHz, All peripherals enabled	—	1.1	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 5 MHz, All peripherals disabled	—	0.6	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 2.5 MHz, All peripherals enabled	—	0.8	—	mA
		V_{DD} = 5.0 V, HSI = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 2.5 MHz, All peripherals disabled	—	0.55	—	mA
	Supply current (Deep-Sleep1 mode)	V_{DD} = 5.0 V, All clock off (HSE/HSI/LSE), LDO in low power mode, LSI on, RTC on	—	22	—	μA
	Supply current (Deep-Sleep2 mode)	V_{DD} = 5.0 V, All clock off (HSE/HSI/LSE), LDO off (DMOS on), LSI on, RTC on	—	6.4	—	μA

Note: 1. HSI means 20 MHz high speed internal oscillator.
2. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power on reset threshold (Rising Voltage on V_{DD})	T_A = -40 °C~ +85 °C	2.22	2.35	2.48	V
V_{PDR}	Power down reset threshold (Falling Voltage on V_{DD})		2.12	2.2	2.33	V
$V_{PORHYST}$	POR hysteresis	—	—	150	—	mV
t_{POR}	Reset delay time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C ~ 85 °C After factory-trimmed, V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C ~ 85 °C, V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3,53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD active delay time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation current (3)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.5	—	5.5	V
f_{HSE}	High Speed External oscillator frequency (HSE)	V_{DD} = 2.5 V ~ 5.0 V	4	—	20	MHz
C_{LHSE}	Load capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 20 MHz	—	—	12	pF
R_{FHSE}	Internal feedback resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 20 MHz, HSEDR = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 20 MHz, HSEDR = 1				
D_{HSE}	HSE oscillator Duty cycle	—	40	—	60	%
I_{DDHSE}	HSE oscillator current consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEDR = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 20 MHz, HSEDR = 1	—	3.0	—	
I_{PWDHSE}	HSE oscillator power down current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE oscillator startup time	V_{DD} = 5.0 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 12. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	20	—	MHz
ACC_{HSI}	Factory calibrated HSI oscillator frequency accuracy	V_{DD} = 5 V @ 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ +85 °C	-3	—	3	%
Duty	Duty cycle	f_{HSI} = 20 MHz	35	—	65	%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DDHSI}	Oscillator supply current	f_{HSI} = 20 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	—	μA
	Power down current		—	—	0.01	μA
T_{SUHSI}	Startup time	f_{HSI} = 20 MHz	—	—	10	μs

Table 13. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 5.0 V, T_A = -40 °C ~ +85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency accuracy	After factory-trimmed, V_{DD} = 5.0 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator startup time	V_{DD} = 5.0 V	—	—	100	μs

Memory Characteristics

Table 14. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of guaranteed program/erase cycles before failure. (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	K cycles
t_{RET}	Data retention time	T_A = -40 °C ~ +85 °C	10	—	—	Years
t_{PROG}	Word programming time	T_A = -40 °C ~ +85 °C	20	—	—	μs
t_{ERASE}	Page erase time	T_A = -40 °C ~ +85 °C	2	—	—	ms
t_{MERASE}	Mass erase time	T_A = -40 °C ~ +85 °C	10	—	—	ms

I/O Port Characteristics

Table 15. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low level input current	5.0 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High level input current	5.0 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low level input voltage	5.0 V I/O		-0.5	—	0.35 × V_{DD}	V
		Reset pin		-0.5	—	0.35 × V_{DD}	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage	5.0 V I/O	0.65 × V_{DD}	—	V_{DD} + 0.5	V
		Reset pin	0.65 × V_{DD}	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt trigger input voltage hysteresis	5.0 V I/O	—	0.12 × V_{DD}	—	mV
		Reset pin	—	0.12 × V_{DD}	—	mV
I_{OL}	Low level output current (GPIO Sink current)	5.0 V I/O 4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.4 V	16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 5.0 V, V_{OL} = 0.4 V, PB10, PB11, PB12	4	—	—	mA
I_{OH}	High level output current (GPIO Source current)	5.0 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V	4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V	8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V	12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V	16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 5.0 V, V_{OL} = V_{DD} - 0.4 V, PB10, PB11, PB12.	—	—	2	mA
V_{OL}	Low level output voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.4	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.4	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.4	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.4	V
V_{OH}	High level output voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	V
R_{PU}	Internal pull-up resistor	5.0 V I/O	—	—	—	kΩ
R_{PD}	Internal pull-down resistor	5.0 V I/O	—	—	—	kΩ

ADC Characteristics

Table 16. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter input voltage range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current consumption	V_{DDA} = 5.0 V	—	0.85	1	mA
I_{ADC_DN}	Power down current consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter clock	—	0.7	—	16	MHz
f_S	Sampling rate	—	0.05	—	1	MHz
t_{DL}	Data latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & hold time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter conversion time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input sampling switch resistance	—	—	—	TBD	kΩ
C_I	Input sampling capacitance	No pin/pad capacitance included	—	—	TBD	pF
t_{SU}	Startup up time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset error	—	—	—	±10	LSB
E_G	Gain error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

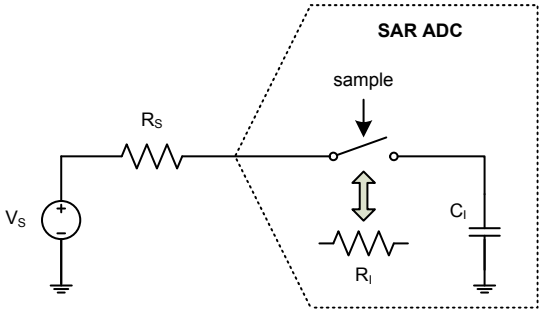


Figure 11. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

GPTM/PWM Characteristics

Table 17. GPTM/PWM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer clock source for GPTM and PWM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer resolution time	—	1	—	—	f_{TM}
f_{EXT}	External single frequency on channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 18. I²C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL clock high time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL clock low time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA fall time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA rise time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA data setup time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time (Note 5)	0	—	0	—	0	—	ns
	SDA data hold time (Note 6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA data valid time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START condition setup time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START condition hold time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP condition setup time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

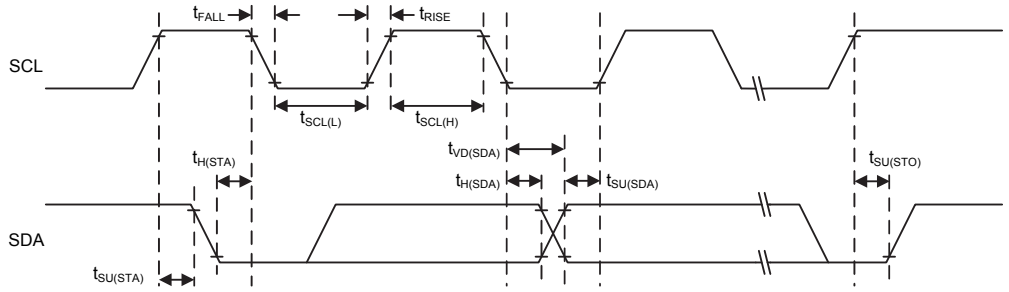


Figure 12. I²C Timing Diagrams

SPI Characteristics

Table 19. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master mode						
f_{SCK}	SPI master output SCK clock frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK clock high and low time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data output valid time	—	—	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI Slave mode						
f_{SCK}	SPI slave input SCK clock frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI slave input SCK clock duty cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL enable setup time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

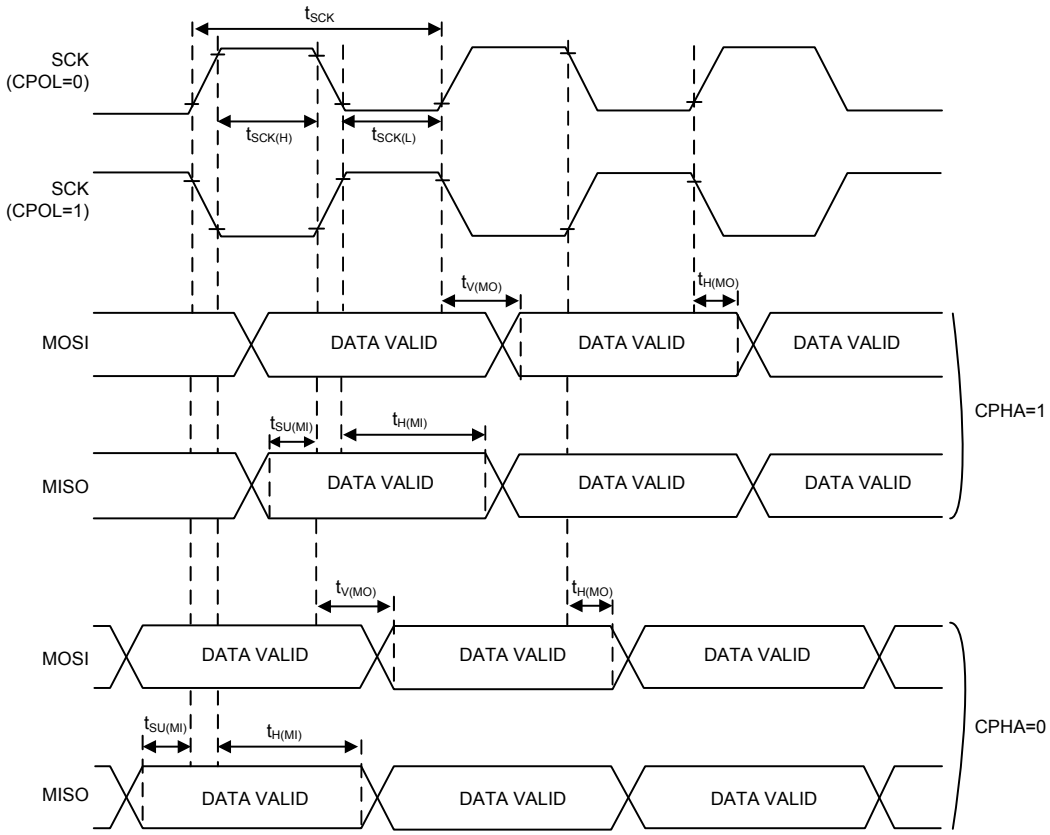


Figure 13. SPI Timing Diagrams – SPI Master Mode

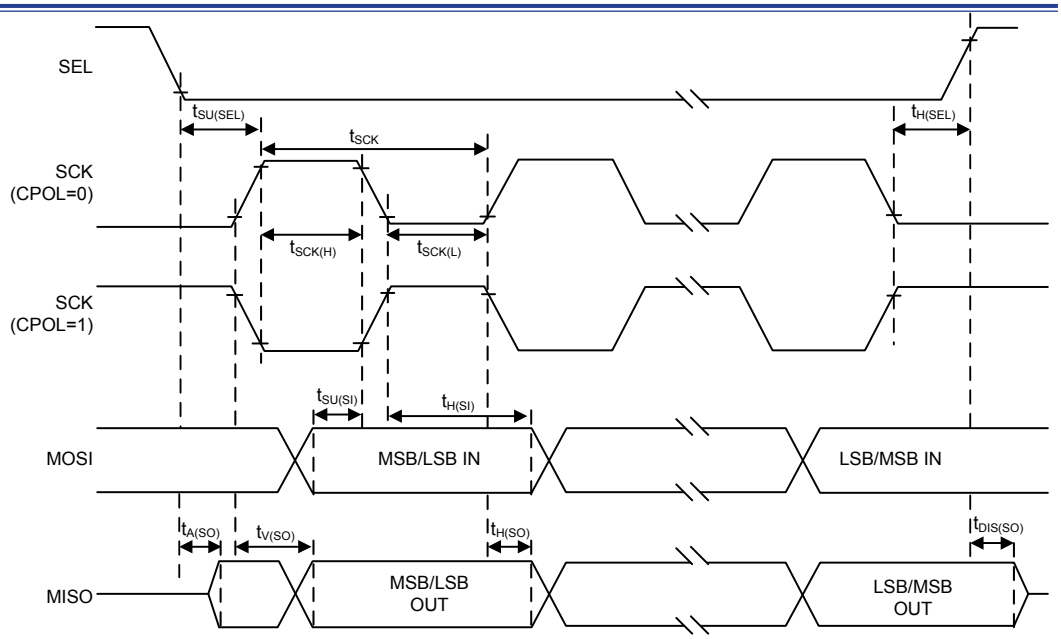


Figure 14. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

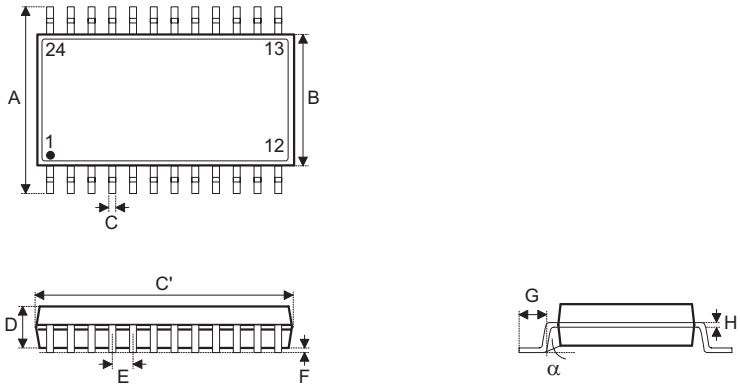
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

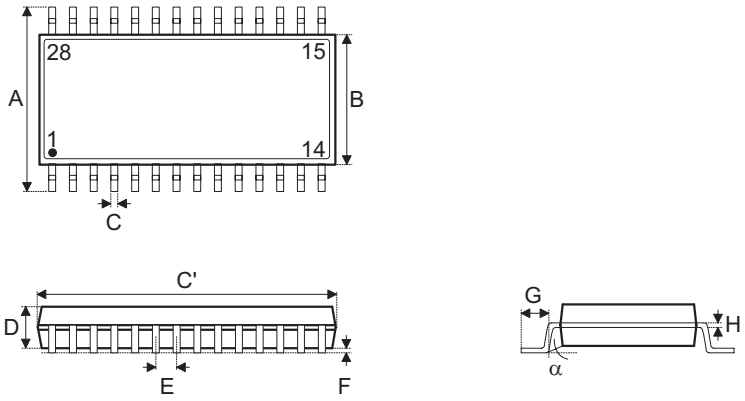
24-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C’	—	8.66 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

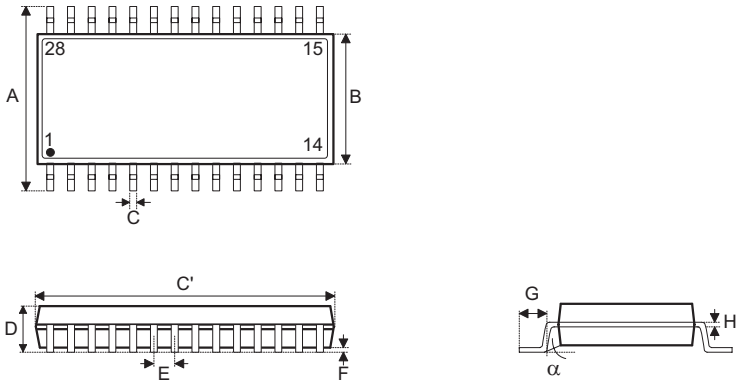
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C’	—	9.90 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

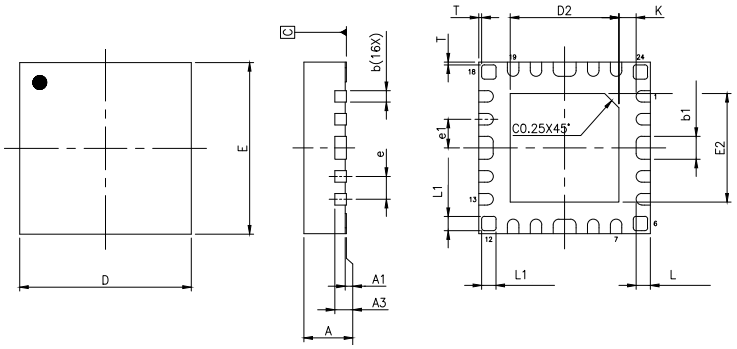
28-pin SOP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.406 BSC	—
B	—	0.295 BSC	—
C	0.012	—	0.020
C’	—	0.705 BSC	—
D	—	—	0.104
E	—	0.050 BSC	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	10.30 BSC	—
B	—	7.50 BSC	—
C	0.31	—	0.51
C’	—	17.90 BSC	—
D	—	—	2.65
E	—	1.27 BSC	—
F	0.10	—	0.30
G	0.40	—	1.27
H	0.20	—	0.33
α	0°	—	8°

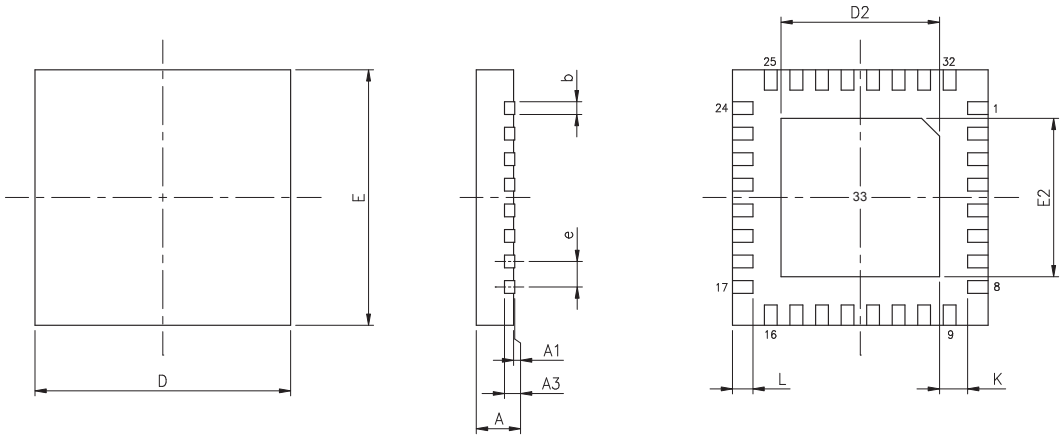
SAW Type 24-pin QFN (3mm×3mm×0.55mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.020	0.022	0.024
A1	0.000	0.001	0.002
A3	—	0.006 BSC	—
b	0.006	0.008	0.010
b1	0.014	0.016	0.018
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.016 BSC	—
e1	—	0.020 BSC	—
D2	0.073	0.075	0.077
E2	0.073	0.075	0.077
L	0.006	0.010	0.014
L1	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	—	0.150 BSC	—
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	—	3.00 BSC	—
E	—	3.00 BSC	—
e	—	0.40 BSC	—
e1	—	0.50 BSC	—
D2	1.85	1.90	1.95
E2	1.85	1.90	1.95
L	0.15	0.25	0.35
L1	0.20	0.25	0.30
K	0.20	—	—

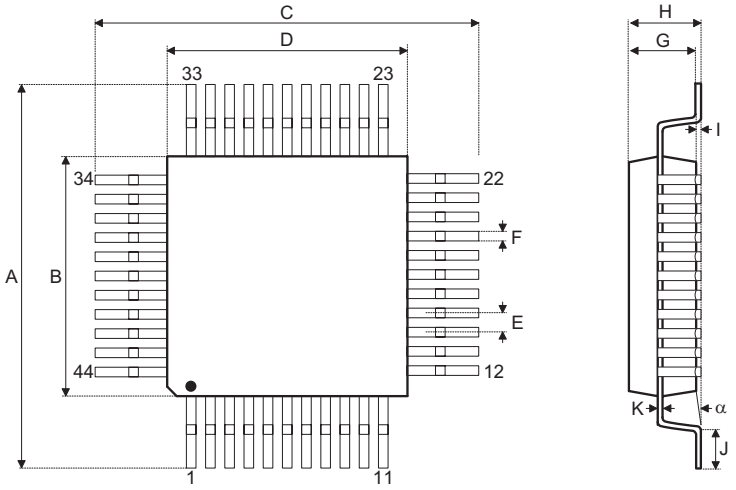
SAW Type 33-pin QFN (4mm×4mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

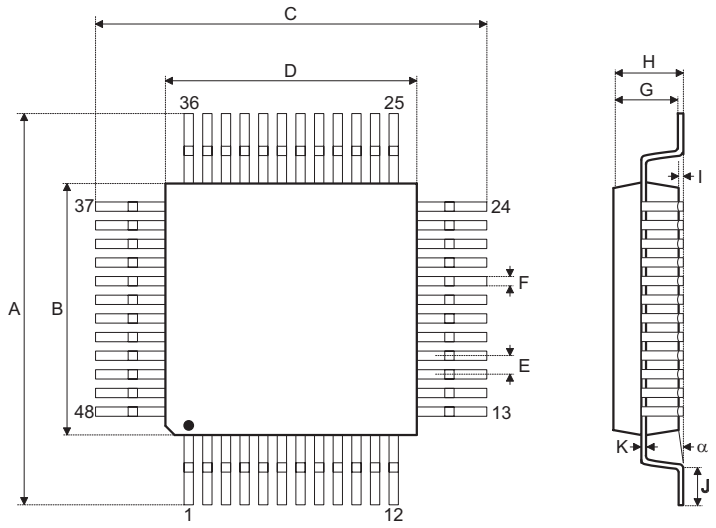
44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.032 BSC	—
F	0.012	0.015	0.018
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.80 BSC	—
F	0.30	0.37	0.45
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°