

### Features

- 2400-2483.5MHz ISM band operation
- Support 250Kbps, 1Mbps and 2Mbps air data rate
- Programmable output power
- Low power consumption
- Tolerate  $\pm 60$ ppm 16MHz crystal
- Variable payload length from 1 to 32bytes
- Automatic packet processing
- 6 data pipes for 1:6 star networks
- 1.9V to 3.6V power supply
- 4-pin SPI interface with maximum 8MHz clock rate
- 20-pin QFN package

### Applications

- Wireless PC peripherals
- Wireless mice and keyboards
- Wireless gamepads
- Wireless audio
- VOIP and wireless headsets
- Remote controls
- Consumer electronics
- Home automation
- Toys
- Personal health and entertainment

### General Description

BC9824 is a GFSK transceiver operating in the world wide ISM frequency band at 2400~2483.5 MHz. Burst mode transmission and up to 2Mbps air data rate make them suitable for applications requiring ultra low power consumption. The embedded packet processing engines enable their full operation with a very simple MCU as a radio system. Auto re-transmission and auto acknowledge give reliable link without any MCU interference.

BC9824 operates in TDD mode, either as a transmitter or as a receiver.

The RF channel frequency determines the center of the channel used by BC9824. The frequency is set by the RF\_CH register in register bank 0 according to the following formula:  $F_0 = 2400 + \text{RF\_CH (MHz)}$ . The resolution of the RF channel frequency is 1MHz.

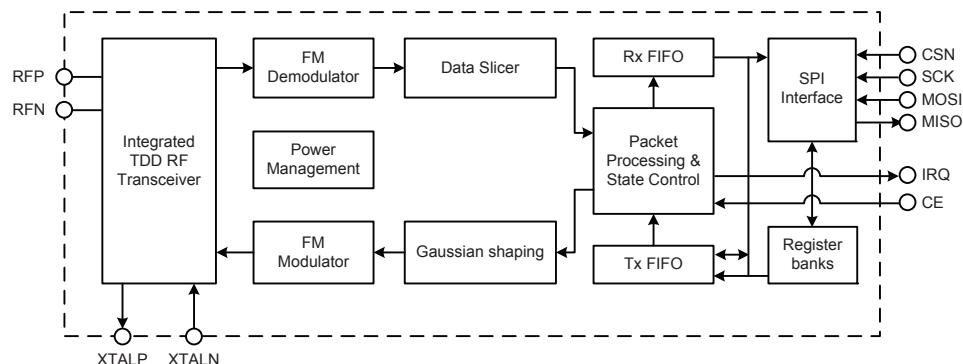
A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

The output power of BC9824 is set by the RF\_PWR bits in the RF\_SETUP register.

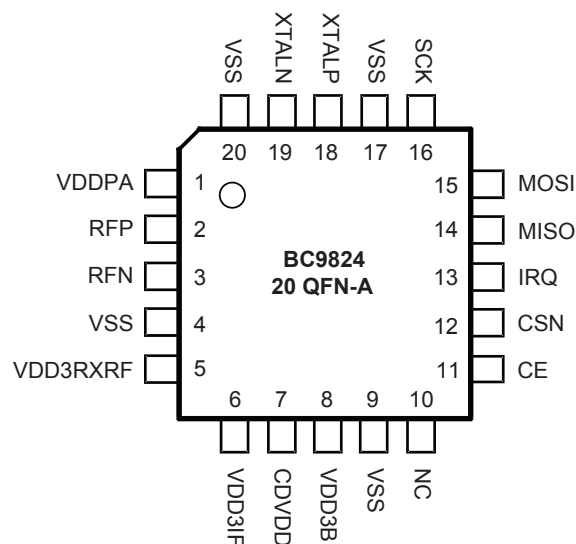
Demodulation is done with embedded data slicer and bit recovery logic. The air data rate can be programmed to 250Kbps, 1Mbps or 2Mbps by RF\_DR\_HIGH and RF\_DR\_LOW register. A transmitter and a receiver must be programmed with the same setting.

In the following chapters, all registers are in register bank 0 except with explicit claim.

### Block Diagram



## Pin Assignment



## Pin Description

Pin No.	Symbol	I/O	Function Description
<b>RF and Analog</b>			
2	RFP	RF	RF output (PA)/input (LNA), port P
3	RFN	RF	RF output (PA)/input (LNA), port N
7	CDVDD	O	Digital regulator output decoupling capacitor
18	XTALP	O	Crystal oscillator, node P (inverter output)
19	XTALN	I	Crystal oscillator, node N (inverter input)
<b>Digital</b>			
11	CE	DI	Chip enable activates RX or TX mode
12	CSN	DI	SPI chip select, active low
13	IRQ	DO	Maskable interrupt pin, active low
14	MISO	DO	SPI slave data output with tri-state option
15	MOSI	DI	SPI slave data input
16	SCK	DI	SPI clock
<b>Power and Ground</b>			
1	VDDPA	Power	1.8V regulator output for PA, TX:1.8V, RX:0V
5	VDD3RXRF	Power	RX front-end power supply (1.9V to 3.6V DC)
6	VDD3IF	Power	RX/TX IF power supply (1.9V to 3.6V DC)
8	VDD3B	Power	Digital power supply (1.9V to 3.6V DC)
4	VSS	Ground	Ground (0V)
9	VSS	Ground	Ground (0V)
17	VSS	Ground	Ground (0V)
20	VSS	Ground	Ground (0V)
10	NC	-	No connection

## Electrical Characteristics

Name	Parameter (Condition)	Min	Typical	Max	Unit	Comment
<b>Operating Condition</b>						
V <sub>DD</sub>	Voltage	1.9	3.0	3.6	V	
TEMP	Temperature	-20	+27	+85	°C	
<b>Digital input Pin</b>						
V <sub>IH</sub>	High level	0.7V <sub>DD</sub>	—	5.25	V	
V <sub>IL</sub>	Low level	V <sub>SS</sub>	—	0.3V <sub>DD</sub>	V	
<b>Digital output Pin</b>						
V <sub>OH</sub>	High level (I <sub>OH</sub> =-0.25mA)	V <sub>DD</sub> - 0.3	—	V <sub>DD</sub>	V	
V <sub>OL</sub>	Low level(I <sub>OL</sub> =0.25mA)	0	—	0.3	V	
<b>Normal condition</b>						
I <sub>VDD</sub>	Power Down current	—	4	—	uA	
I <sub>VDD</sub>	Standby-I current	—	90	—	uA	
I <sub>VDD</sub>	Standby-II current	—	330	—	uA	
<b>Normal RF condition</b>						
f <sub>OP</sub>	Operating frequency	2400	—	2527	MHz	
f <sub>XTAL</sub>	Crystal frequency	—	16	—	MHz	
R <sub>FSK</sub>	Air data rate	250	—	2000	Kbps	
<b>Transmitter</b>						
P <sub>RF</sub>	Output power	-40	0	3	dBm	
P <sub>BW</sub>	Modulation 20 dB bandwidth(2Mbps)	—	2.5	—	MHz	
P <sub>BW</sub>	Modulation 20 dB bandwidth (1Mbps)	—	1.8	—	MHz	
P <sub>BW</sub>	Modulation 20 dB bandwidth (250Kbps)	—	1.6	—	MHz	
I <sub>VDD</sub>	Current at -35 dBm output power	—	8	—	mA	
I <sub>VDD</sub>	Current at -25 dBm output power	—	9	—	mA	
I <sub>VDD</sub>	Current at -20 dBm output power	—	10	—	mA	
I <sub>VDD</sub>	Current at -10 dBm output power	—	12	—	mA	
I <sub>VDD</sub>	Current at -6 dBm output power	—	13	—	mA	
I <sub>VDD</sub>	Current at -1dBm output power	—	18	—	mA	
I <sub>VDD</sub>	Current at 3 dBm output power	—	25	—	mA	
<b>Receiver</b>						
I <sub>VDD</sub>	Current (2Mbps)	—	18	—	mA	RX no signal
I <sub>VDD</sub>	Current (1Mbps)	—	18	—	mA	RX no signal
I <sub>VDD</sub>	Current (250Kbps)	—	18	—	mA	RX no signal
Max Input	1 E-3 BER	—	20	—	dBm	
RX <sub>SENS</sub>	1 E-3 BER sensitivity (2Mbps)	—	-87	—	dBm	
RX <sub>SENS</sub>	1 E-3 BER sensitivity (1Mbps)	—	-90	—	dBm	
RX <sub>SENS</sub>	1 E-3 BER sensitivity (250Kbps)	—	-96	—	dBm	
C/I <sub>CO</sub>	Co-channel C/I (2Mbps)	—	6	—	dB	
C/I <sub>+1ST</sub>	ACS C/I 2MHz (2Mbps)	—	2	—	dB	
C/I <sub>-1ST</sub>	ACS C/I 2MHz (2Mbps)	—	-6	—	dB	
C/I <sub>+2ND</sub>	ACS C/I 4MHz (2Mbps)	—	-21	—	dB	
C/I <sub>-2ND</sub>	ACS C/I 4MHz (2Mbps)	—	-12	—	dB	
C/I <sub>+3RD</sub>	ACS C/I 6MHz (2Mbps)	—	-29	—	dB	
C/I <sub>-3RD</sub>	ACS C/I 6MHz (2Mbps)	—	-18	—	dB	
C/I <sub>CO</sub>	Co-channel C/I (1Mbps)	—	6	—	dB	
C/I <sub>+1ST</sub>	ACS C/I 1MHz (1Mbps)	—	4	—	dB	
C/I <sub>-1ST</sub>	ACS C/I 1MHz (1Mbps)	—	-6	—	dB	

Name	Parameter (Condition)	Min	Typical	Max	Unit	Comment
C/I <sub>+2ND</sub>	ACS C/I 2MHz (1Mbps)	—	-24	—	dB	
C/I <sub>-2ND</sub>	ACS C/I 2MHz (1Mbps)	—	-12	—	dB	
C/I <sub>+3RD</sub>	ACS C/I 3MHz (1Mbps)	—	-28	—	dB	
C/I <sub>-3RD</sub>	ACS C/I 3MHz (1Mbps)	—	-16	—	dB	
C/I <sub>CO</sub>	Co-channel C/I (250Kbps)	—	9	—	dB	
C/I <sub>+1ST</sub>	ACS C/I 1MHz (250Kbps)	—	-13	—	dB	
C/I <sub>-1ST</sub>	ACS C/I 1MHz (250Kbps)	—	-16	—	dB	
C/I <sub>+2ND</sub>	ACS C/I 2MHz (250Kbps)	—	-25	—	dB	
C/I <sub>-2ND</sub>	ACS C/I 2MHz (250Kbps)	—	-9	—	dB	
C/I <sub>+3RD</sub>	ACS C/I 3MHz (250Kbps)	—	-33	—	dB	
C/I <sub>-3RD</sub>	ACS C/I 3MHz (250Kbps)	—	-33	—	dB	

Note: \* Device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883H Method 3015.8. MM (Machine Mode) is based on JEDEC EIA/JESD22-A115.

## Function Description

### State Control

#### State Control Diagram

- Pin signal: VDD, CE
- SPI register: PWR\_UP, PRIM\_RX, EN\_AA, NO\_ACK, ARC, ARD
- System information: Time out, ACK received, ARD elapsed, ARC\_CNT, TX FIFO empty, ACK packet transmitted, Packet received

BC9824 has built-in state machines that control the state transition between different modes.

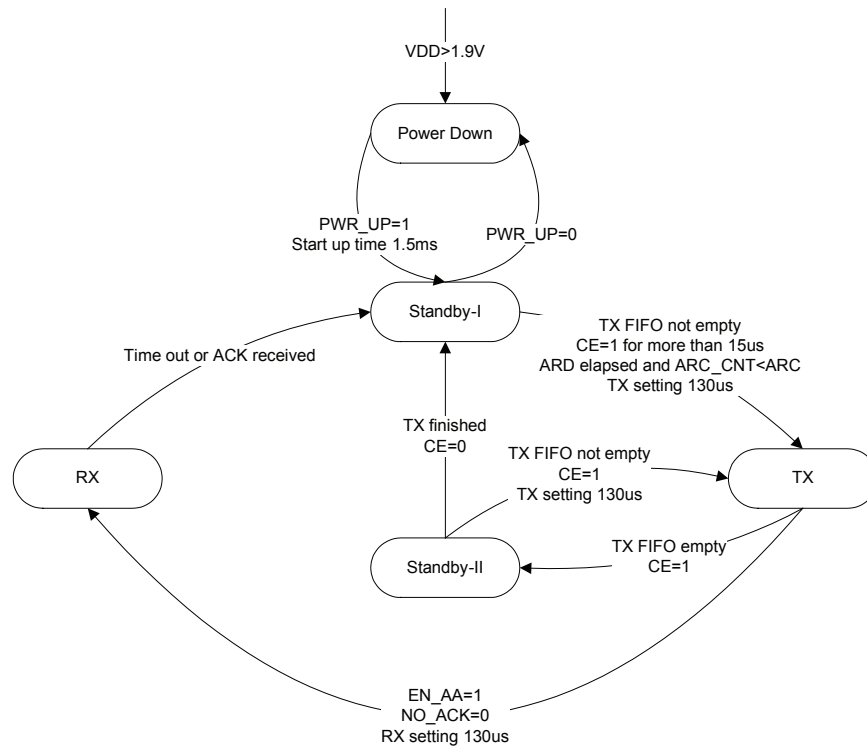
When auto acknowledge feature is disabled, state transition will be fully controlled by MCU.

### Power Down Mode

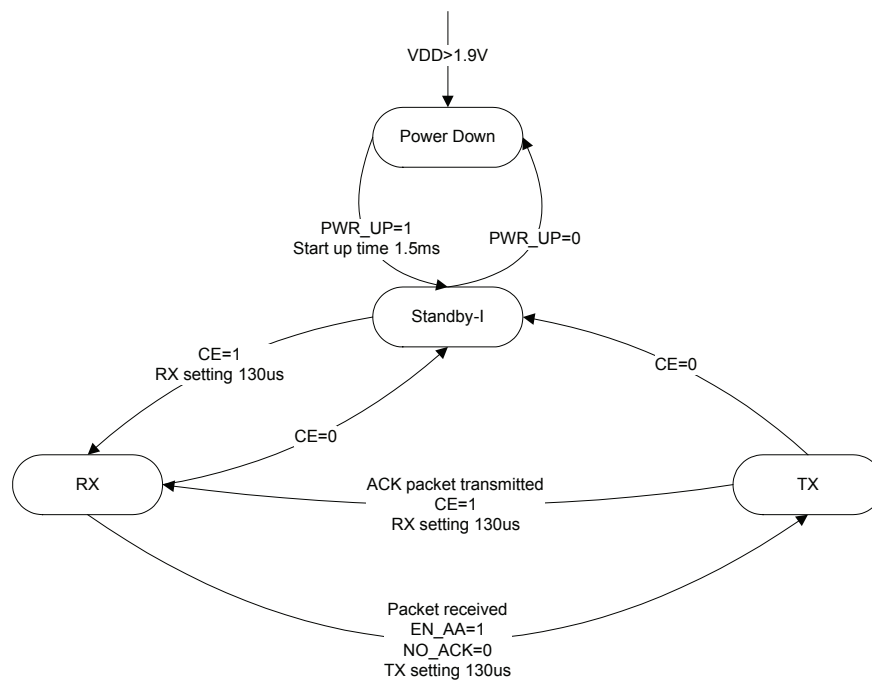
In power down mode BC9824 is in sleep mode with minimal current consumption. SPI interface is still active in this mode, and all register values are available by SPI. Power down mode is entered by setting the PWR\_UP bit in the CONFIG register to low.

### Standby-I Mode

By setting the PWR\_UP bit in the CONFIG register to 1 and de-asserting CE to 0, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start-up time. In this mode, part of the crystal oscillator is active. This is also the mode which the BC9824 returns to from TX or RX mode when CE is set low.



**PTX (PRIM\_RX=0) State Control Diagram**



**PRX (PRIM\_RX=1) State Control Diagram**

**Standby-II Mode**

In standby-II mode more clock buffers are active than in standby-I mode and much more current is used. Standby-II occurs when CE is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO in this mode, the device will automatically enter TX mode and the packet is transmitted.

**TX Mode**

- PTX device (PRIM\_RX=0)

The TX mode is an active mode where the PTX device transmits a packet. To enter this mode from power down mode, the PTX device must have the PWR\_UP bit set high, PRIM\_RX bit set low, a payload in the TX FIFO, and a high pulse on the CE for more than 10 $\mu$ s.

The PTX device stays in TX mode until it finishes transmitting the current packet. If CE = 0 it returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the PTX device remains in TX mode, transmitting the next packet. If the TX FIFO is empty the PTX device goes into standby-II mode. It is important to never stay in TX mode for more than 4ms at one time.

If the auto retransmit is enabled (EN\_AA=1) and auto acknowledge is required (NO\_ACK=0), the PTX device will enter TX mode from standby-I mode when ARD elapsed and number of retries is less than ARC.

- PRX device (PRIM\_RX=1)

The PRX device will enter TX mode from RX mode only when EN\_AA=1 and NO\_ACK=0 in received packet to transmit acknowledge packet with pending payload in TX FIFO.

**RX Mode**

- PRX device (PRIM\_RX=1)

The RX mode is an active mode where the BC9824 radio is configured to be a receiver. To enter this mode from standby-I mode, the PRX device must have the PWR\_UP bit set high, PRIM\_RX bit set high and the CE pin set high. Or PRX device can enter this mode from TX mode after transmitting an acknowledge packet when EN\_AA=1 and NO\_ACK=0 in received packet.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the packet processing engine. The packet processing engine continuously searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The PRX device remains in RX mode until the MCU configures it to standby-I mode or power down mode.

In RX mode a carrier detection (CD) signal is available. The CD is set to high when a RF signal is detected inside the receiving frequency channel. The internal CD signal is filtered before presented to CD register. The RF signal must be present for at least 128  $\mu$ s before the CD is set high.

- PTX device (PRIM\_RX=0)

The PTX device will enter RX mode from TX mode only when EN\_AA=1 and NO\_ACK=0 to receive acknowledge packet.

## Packet Processing

### Packet Format

The packet format has a preamble, address, packet control, payload and CRC field.

- Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

- Address

This is the address for the receiver. An address ensures that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long by the AW register.

The PRX device can open up to six data pipes to support up to six PTX devices with unique addresses. All six PTX device addresses are searched simultaneously. In PRX side, the data pipes are enabled with the bits in the EN\_RXADDR register. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the RX\_ADDR\_PX registers.

Each pipe can have up to 5 bytes configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSB byte must be unique for all 6 pipes.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

On the PRX, the RX\_ADDR\_Pn, defined as the pipe address, must be unique. On the PTX the TX\_ADDR must be the same as the RX\_ADDR\_P0 on the PTX, and as the pipe address for the designated pipe on the PRX.

No other data pipe can receive data until a complete packet is received by a data pipe that has detected its address. When multiple PTX devices are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

- Packet Control

When Dynamic Payload Length function is enabled, the packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO\_ACK flag.

- Payload length

The payload length field is only used if the Dynamic Payload Length function is enabled.

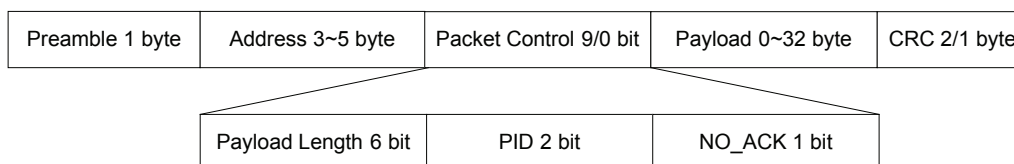
- PID

The 2 bit PID field is used to detect whether the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields are used by the PRX device to determine whether a packet is old or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, BC9824 compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

- NO\_ACK

The NO\_ACK flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

The PTX can set the NO\_ACK flag bit in the Packet Control Field with the command: W\_TX\_PAYLOAD\_NOACK. However, the function must first be enabled in the FEATURE register by setting the EN\_DYN\_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.



**Packet Format**

- **Payload**

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide, and it is transmitted on-air as it is uploaded (unmodified) to the device.

The BC9824 provides two alternatives for handling payload lengths, static and dynamic payload length. The static payload length of each of six data pipes can be individually set.

The default alternative is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX\_PW\_Px registers. The payload length on the transmitter side is set by the number of bytes clocked into the TX\_FIFO and must equal the value in the RX\_PW\_Px register on the receiver side. Each pipe has its own payload length.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With DPL feature the BC9824 can decode the payload length of the received packet automatically instead of using the RX\_PW\_Px registers. The MCU can read the length of the received payload by using the command: R\_RX\_PL\_WID.

In order to enable DPL the EN\_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register has to be set. A PTX that transmits to a PRX with DPL enabled must have the DPL\_P0 bit in DYNPD set.

- **CRC**

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. It may be either 1 or 2 bytes and is calculated over the address, Packet Control Field, and Payload.

The polynomial for 1 byte CRC is  $X^8 + X^2 + X + 1$ . Initial value is 0xFF.

The polynomial for 2 byte CRC is  $X^{16} + X^{12} + X^5 + 1$ . Initial value is 0xFFFF.

No packet is accepted by receiver side if the CRC fails.

### **Packet Handling**

BC9824 uses burst mode for payload transmission and receive.

The transmitter fetches payload from TX FIFO, automatically assembles it into packet and transmits the packet in a very short burst period with 1Mbps or 2Mbps air data rate.

After transmission, if the PTX packet has the NO\_ACK flag set, BC9824 sets TX\_DS and gives an active low interrupt IRQ to MCU. If the PTX is ACK packet, the PTX needs receive ACK from the PRX and then asserts the TX\_DS IRQ.

The receiver automatically validates and disassembles received packet, if there is a valid packet within the new payload, it will write the payload into RX FIFO, set RX\_DR and give an active low interrupt IRQ to MCU.

When auto acknowledge is enabled (EN\_AA=1), the PTX device will automatically wait for acknowledge packet after transmission, and re-transmit original packet with the delay of ARD until an acknowledge packet is received or the number of re-transmission exceeds a threshold ARC. If the later one happens, BC9824 will set MAX\_RT and give an active low interrupt IRQ to MCU. Two packet loss counters (ARC\_CNT and PLOS\_CNT) are incremented each time a packet is lost. The ARC\_CNT counts the number of retransmissions for the current transaction. The PLOS\_CNT counts the total number of retransmissions since the last channel change. ARC\_CNT is reset by initiating a new transaction. PLOS\_CNT is reset by writing to the RF\_CH register. It is possible to use the information in the OBSERVE\_TX register to make an overall assessment of the channel quality.

The PTX device will retransmit if its RX FIFO is full but received ACK frame has payload.

As an alternative for PTX device to auto retransmit it is possible to manually set the BC9824 to retransmit a packet a number of times. This is done by the REUSE\_TX\_PL command.

When auto acknowledge is enabled, the PRX device will automatically check the NO\_ACK field in received packet, and if NO\_ACK=0, it will automatically send an acknowledge packet to PTX device. If EN\_ACK\_PAY is set, and the acknowledge packet can also include pending payload in TX FIFO.



## Data and Control Interface

### TX/RX FIFO

The data FIFOs are used to store payload that is to be transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFO is accessible in both PTX mode and PRX mode.

There are three levels 32 bytes FIFO for both TX and RX, supporting both acknowledge mode or no acknowledge mode with up to six pipes.

- TX three levels, 32 byte FIFO
- RX three levels, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH\_TX command.

The RX FIFO in PRX may contain payload from up to three different PTX devices.

A TX FIFO in PTX can have up to three payloads stored.

The TX FIFO can be written to by three commands, W\_TX\_PAYLOAD and W\_TX\_PAYLOAD\_NO\_ACK in PTX mode and W\_ACK\_PAYLOAD in PRX mode. All three commands give access to the TX\_PLD register.

The RX FIFO can be read by the command R\_RX\_PAYLOAD in both PTX and PRX mode. This command gives access to the RX\_PLD register.

The payload in TX FIFO in a PTX is NOT removed if the MAX\_RT IRQ is asserted.

In the FIFO\_STATUS register it is possible to read if the TX and RX FIFO are full or empty. The TX\_REUSE bit is also available in the FIFO\_STATUS register. TX\_REUSE is set by the SPI command REUSE\_TX\_PL, and is reset by the SPI command: W\_TX\_PAYLOAD or FLUSH TX.

### Interrupt

In BC9824 there is an active low interrupt (IRQ) pin, which is activated when TX\_DS IRQ, RX\_DR IRQ or MAX\_RT IRQ are set high by the state machine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

The 3 bit pipe information in the STATUS register is updated during the IRQ pin high to low transition. If the STATUS register is read during an IRQ pin high to low transition, the pipe information is unreliable.

### SPI Interface

- SPI Command

The SPI commands are shown in the below table. Every new command must be started by a high to low transition on CSN.

In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin.

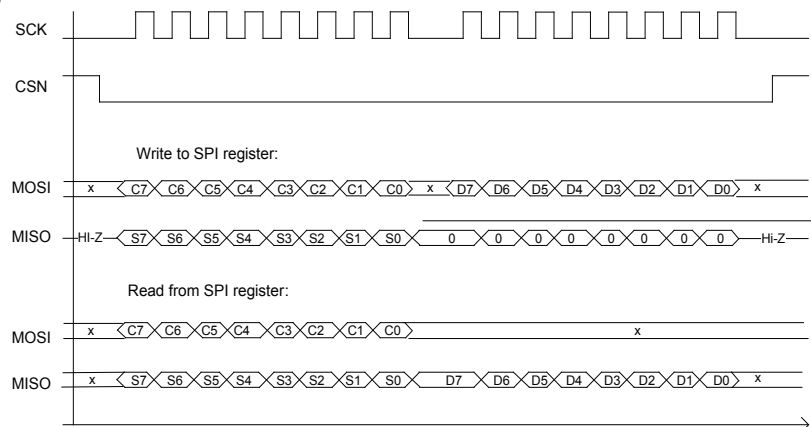
The serial shifting SPI commands is in the following format:

- <Command word: MSB bit to LSB bit (one byte)>
- <Data bytes: LSB byte to MSB byte, MSB bit in each byte first> for all registers at bank 0 and register 9 to register 14 at bank 1
- <Data bytes: MSB byte to LSB byte, MSB bit in each byte first> for register 0 to register 8 at bank 1

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSB byte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSB byte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSB byte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSB byte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: <ul style="list-style-type: none"> <li>• R_RX_PL_WID</li> <li>• W_ACK_PAYLOAD</li> <li>• W_TX_PAYLOAD_NOACK</li> </ul> A new ACTIVATE command with the same data deactivates them again. This is executable in power down or stand by modes only. The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on MISO. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register. Use the same command and data to deactivate the registers again. This write command followed by data 0x53 toggles the register bank, and the current register bank number can be read out from REG7 [7]
R_RX_PL_WID	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSB byte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32 LSB byte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

**SPI Command**

• SPI Timing



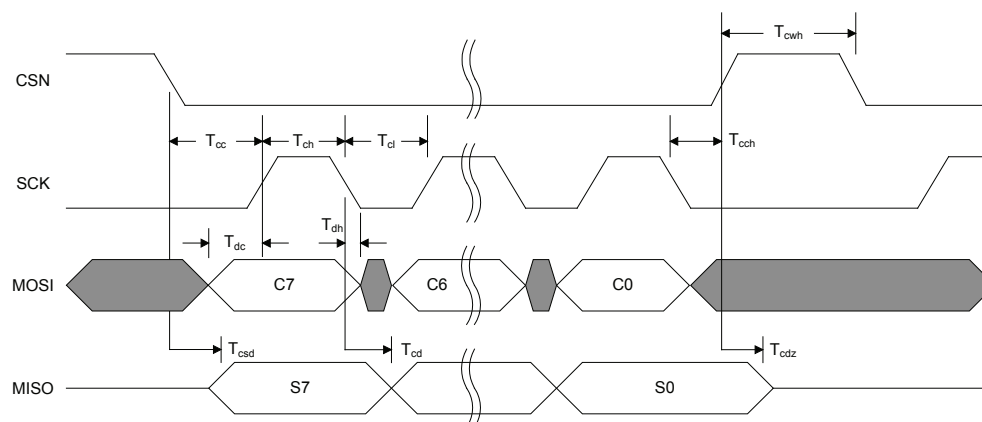
SPI Timing

Cn: SPI command bit

Sn: STATUS register bit

Dn: Data Bit (LSB byte to MSB byte, MSB bit in each byte first)

Note: The SPI timing is for bank 0 and register 9 to 14 at bank 1. For register 0 to 8 at bank 1, the byte order is inverted that the MSB byte is R/W before LSB byte.



SPI NOP Timing Diagram

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	10		ns
Tdh	SCK to Data Hold	20		ns
Tcsd	CSN to Data Valid		38	ns
Tcd	SCK to Data Valid		55	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	8	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		38	ns

SPI Timing Parameter

## Register Map

There are two register banks, which can be toggled by SPI command “ACTIVATE” followed with 0x53 byte, and bank status can be read from Bank0\_REG7 [7].

### Register Bank 0

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' - 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0: POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control, 1: PRX, 0: PTX
01	EN_AA				Enable 'Auto Acknowledgment' Function
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
03	SETUP_AW				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' - 5 bytes LSB bytes are used if address width is below 5 bytes

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmission Delay '0000' – Wait 250 us '0001' – Wait 500 us '0010' – Wait 750 us ..... '1111' – Wait 4000 us (Delay defined from end of transmission to start of next transmission)
	ARC	3:0	0011	R/W	Auto Retransmission Count '0000' – Re-Transmit disabled '0001' – Up to 1 Re-Transmission on fail of AA ..... '1111' – Up to 15 Re-Transmission on fail of AA
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel
06	RF_SETUP				RF Setup Register
	Reserved	7:6	0	R/W	Only '00' allowed
	RF_DR_LOW	5	0	R/W	Set Air Data Rate. See <b>RF_DR_HIGH</b> for encoding.
	PLL_LOCK	4	0	R/W	Force PLL lock signal. Only used in test
	RF_DR_HIGH	3	1	R/W	Set Air Data Rate. Encoding: RF_DR_LOW, RF_DR_HIGH: '00' – 1Mbps '01' – 2Mbps (default) '10' – 250Kbps '11' – 2Mbps
	RF_PWR[1:0]	2:1	11	R/W	Set RF output power in TX mode RF_PWR[1:0] '00' – -26 dBm '01' – -14 dBm '10' – -6 dBm '11' – -1 dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain 0:Low gain(20dB down) 1:High gain

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
07	STATUS				Status Register (In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)
	RBANK	7	0	R	Register bank selection states. Switch register bank is done by SPI command "ACTIVATE" followed by 0x53 0: Register bank 0 1: Register bank 1
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt Asserted when new data arrives RX FIFO Write 1 to clear bit.
	TX_DS	5	0	R/W	TX FIFO Data Sent Status 0: No data is transmitted from TX FIFO 1: New data has been transmitted from TX FIFO
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full 0: Available locations in TX FIFO
08	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0000	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0000	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
09	CD				
	Reserved	7:1	0000000	R	
	CD	0	0	R	Carrier Detect
0A	RX_ADDR_P0	39:0	0xE7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSB byte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSB byte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	000000	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	000000	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	000000	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	000000	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	000000	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	000000	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0: not used 1 = 1 byte ... 32 = 32 bytes

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
17	FIFO_STATUS				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. The packet is repeatedly retransmitted as long as CE is high. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI command W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO full; 0: Available locations in TX FIFO
	TX_EMPTY	4	0	R	TX FIFO empty flag. 1: TX FIFO empty 0: Data in TX FIFO
	Reserved	3:2	00	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO full 0: Available locations in RX FIFO
	RX_EMPTY	0	1	R	RX FIFO empty flag 1: RX FIFO empty 0: Data in RX FIFO
N/A	ACK_PLD	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command Used in RX mode only Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only
N/A	RX_PLD	255:0	X	R	Read by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO.
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only '00' allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only '00000' allowed
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command
Note: Don't write reserved registers and registers at other addresses in register bank 0					

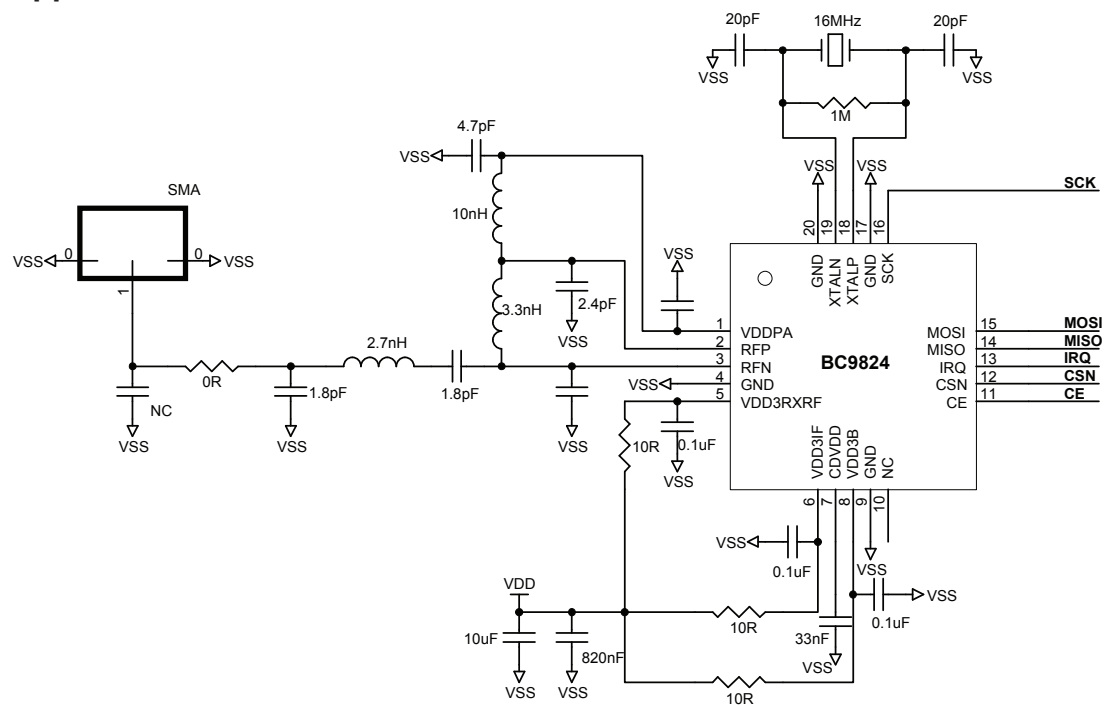


## Register Bank 1

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00		31:0	0		Write when normal mode. Read received total bits when BER test mode. Must write with 0x858AC01C
01		31:0	0		Write when normal mode. Read received error bits when BER test mode. Must write with 0x1103C960
02		31:0	0	W	Must write with 0x00000004
03		31:0	0x03001200	W	Must write with 0x00000004
04		31:0	0	W	For normal work mode: 1Mbps, 2Mbps: 0x437D5D5F 250Kbps: 0x437D6D5F For single carrier mode: 1Mbps, 2Mbps: 0xC37D5D5D 250Kbps: 0xC37D6D5D
05		31:0	0	W	250kbps: 0x74106C9F 1Mbps: 0x14126C9F 2Mbps: 0x74114C9F
06		31:0	0	W	1Mbps: 0x0007C022 250Kbps and 2Mbps: 0x0007C002
07		6:0 31:8	0	W	Reserved
	RBANK	7	0	R	Register bank selection states. Switch register bank is done by SPI command "ACTIVATE" followed by 0x53 0: Register bank 0 1: Register bank 1
08	Chip ID	31:0	0	R	Store the chip ID
09			0	R/W	Reserved
0A			0	R/W	Reserved
0B			0	R/W	Reserved
0C		31:0	0	R/W	Please initialize with 0x05731200
0D		31:0	0	R/W	1Mbps and 2Mbps: 0x0080B434 250Kbps: 0x0080B436
0E	RAMP	87:0	NA	R/W	Ramp curve Please write with 0x CFEFBEF7DF7CF3CF208104

Note: Don't write reserved registers and no definition registers in register bank 1

## Application Circuit



## Abbreviations

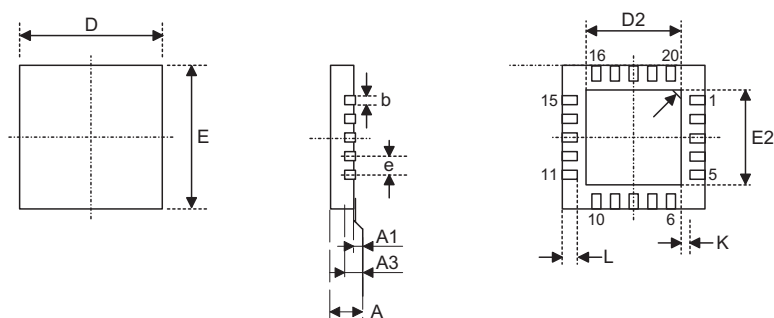
ACK	Acknowledgement
ARC	Auto Retransmission Count
ARD	Auto Retransmission Delay
CD	Carrier Detection
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select Not
DPL	Dynamic Payload Length
FIFO	First-In-First-Out
GFSK	Gaussian Frequency Shift Keying
GHz	Gigahertz
LNA	Low Noise Amplifier
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
MAX_RT	Maximum Retransmit
Mbps	Megabit per second
MCU	Microcontroller Unit
MHz	Megahertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PID	Packet Identity Bits
PLD	Payload
PRX	Primary RX
PTX	Primary TX
PWD_DWN	Power Down
PWD_UP	Power Up
RF_CH	Radio Frequency Channel
RSSI	Received Signal Strength Indicator
RX	Receive
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
TX	Transmit
TX_DS	Transmit Data Sent
XTAL	Crystal

## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of [the package information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Further Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [Packing Materials Information](#)
- [Carton information](#)

**SAW Type 20-pin (4mm×4mm) QFN Outline Dimensions**


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.007	0.010	0.012
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.020 BSC	—
D2	0.075	0.079	0.081
E2	0.075	0.079	0.081
L	0.012	0.016	0.020
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	0.020	0.050
A3	—	0.203 BSC	—
b	0.180	0.250	0.300
D	—	4.000 BSC	—
E	—	4.000 BSC	—
e	—	0.50 BSC	—
D2	1.90	2.00	2.05
E2	1.90	2.00	2.05
L	0.30	0.40	0.50
K	0.20	—	—

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