Logic and Computer Design Fundamentals

Chapter 3 – Combinational Logic Design

Part 1 – Implementation Technology and Logic Design

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Overview

- Part 1

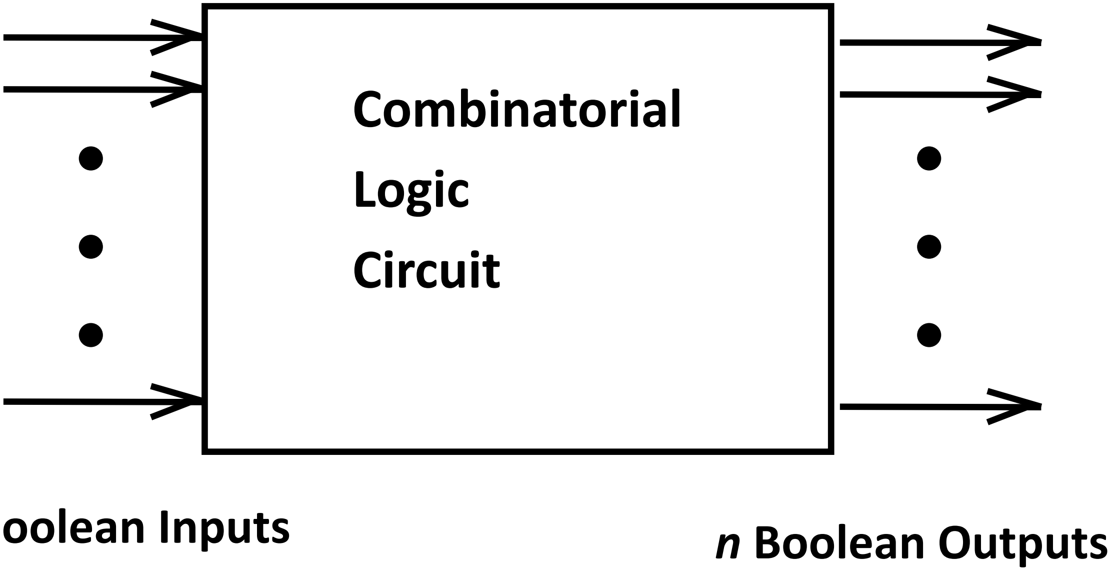
  What is Combinational Circuits?

  Design Procedure

  - Steps
    - Specification
    - Formulation
    - Optimization
    - Technology Mapping
    - Verification

Combinational Circuits

- **A combinational logic circuit has:**
  - **A set of *m* Boolean inputs,**
  - **A set of *n* Boolean outputs, and**
  - ***n* switching functions, each mapping the 2^m input combinations to an output such that the current output depends only on the current input values**
- **A block diagram:**



Combinatorial Logic Circuit

m Boolean Inputs

n Boolean Outputs

Design Procedure

1. Specification
   - Write a specification for the circuit if one is not already available
2. Formulation
   - Derive a truth table or initial Boolean equations that define the required relationships between the inputs and outputs, if not in the specification
3. Optimization
   - Optimize the expression until meets the smallest literals using K-Map technique

Design Procedure

4. **Technology Mapping**
   - **Draw a logic diagram for the resulting circuit using ANDs, ORs, and inverters**
5. **Verification (optional step)**
   - **Verify the correctness of the final design manually or using simulation**

Design Example

1. ## Specification

- <u>BCD to Excess-3 code converter</u>
- Transforms BCD code for the decimal digits to Excess-3 code for the decimal digits
- BCD code words for digits 0 through 9: 4-bit patterns 0000 to 1001, respectively
- Excess-3 code words for digits 0 through 9: 4-bit patterns consisting of 3 (binary 0011) added to each BCD code word
- Implementation:
  - multiple-level circuit
  - NAND gates (including inverters)

Design Example (continued)

2. Formulation

- Conversion of 4-bit codes can be most easily formulated by a truth table
- Variables
  - <u>BCD</u>: A,B,C,D
- Variables
  - <u>Excess-3</u> W,X,Y,Z
- Don't Cares
  - BCD 1010 to 1111

Input BCD A B C D	Output Excess-3 WXYZ
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0

Design Example (continued)

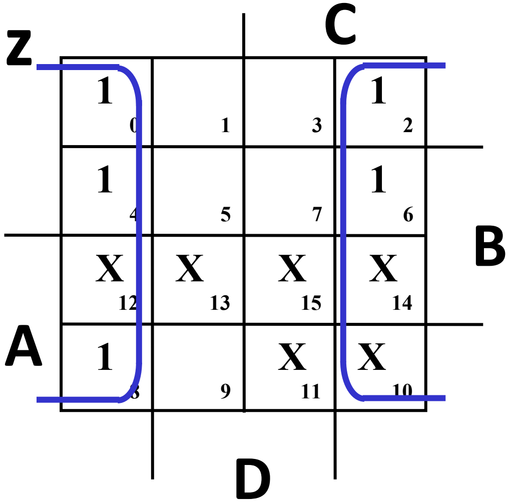
3. **Optimization**
   a. **2-level using K-maps**

$W = A + BC + BD$

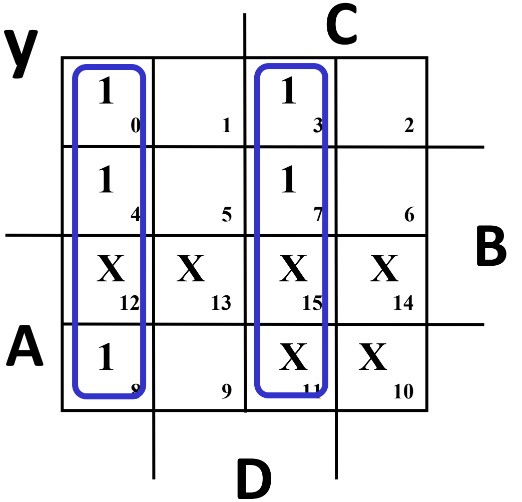
$X = \overline{B}C + \overline{B}D + B\overline{C}\,\overline{D}$

$Y = CD + \overline{C}\,\overline{D}$

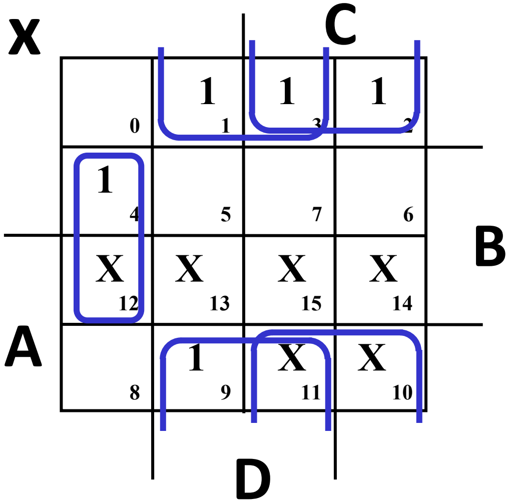
$Z = \overline{D}$



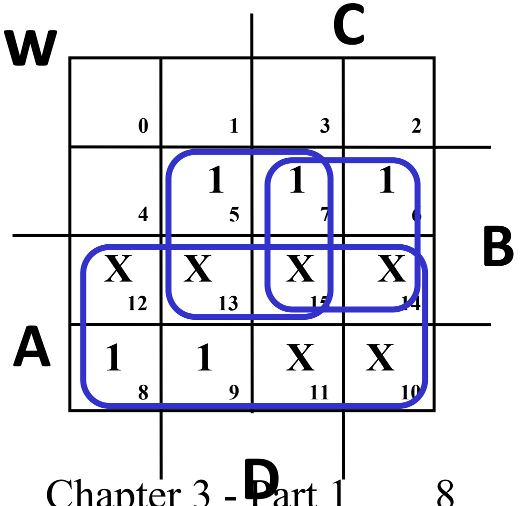
1 0	1	3	1 2
1 4	5	7	1 6
X 12	X 13	X 15	X 14
1 8	9	X 11	X 10



1 0	1	1 3	2
1 4	5	1 7	6
X 12	X 13	X 15	X 14
1 8	9	X 11	X 10



0	1 1	1 3	1 2
1 4	5	7	6
X 12	X 13	X 15	X 14
8	1 9	X 11	X 10

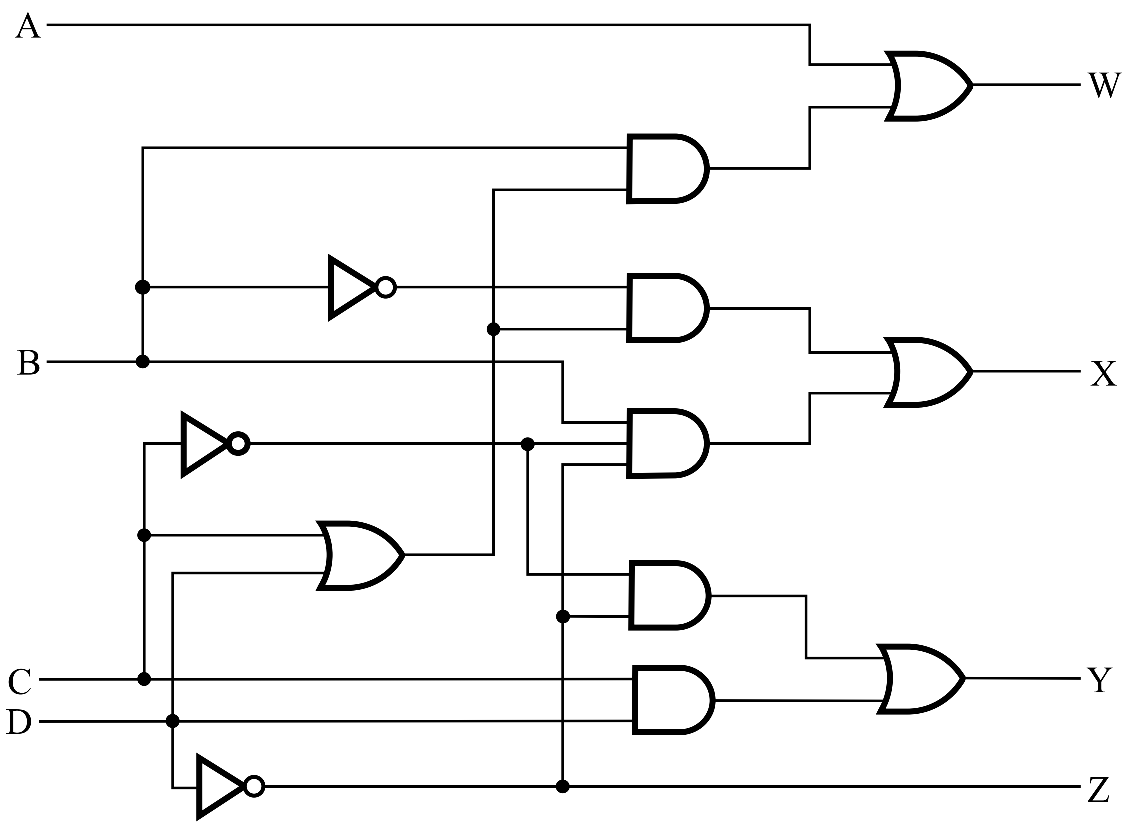


0	1	3	2
4	1 5	1 7	1 6
X 12	X 13	X 15	X 14
1 8	1 9	X 11	X 10

Design Example (continued)

4. Technology Mapping

- Mapping to a final logic diagram



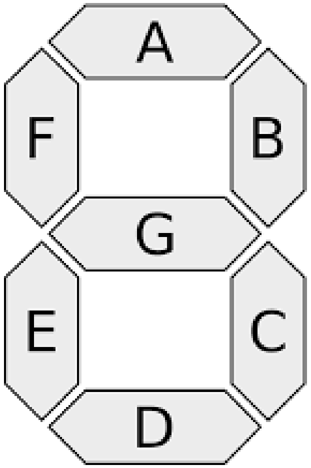
2nd Example

Design of a BCD-to-Seven-Segment Decoder

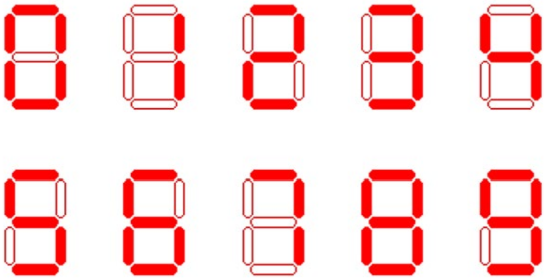
Sample:
https://www.youtube.com/watch?v=dS7VLZwz6bY
https://www.youtube.com/watch?v=-aCqfE2330w

Design Procedure

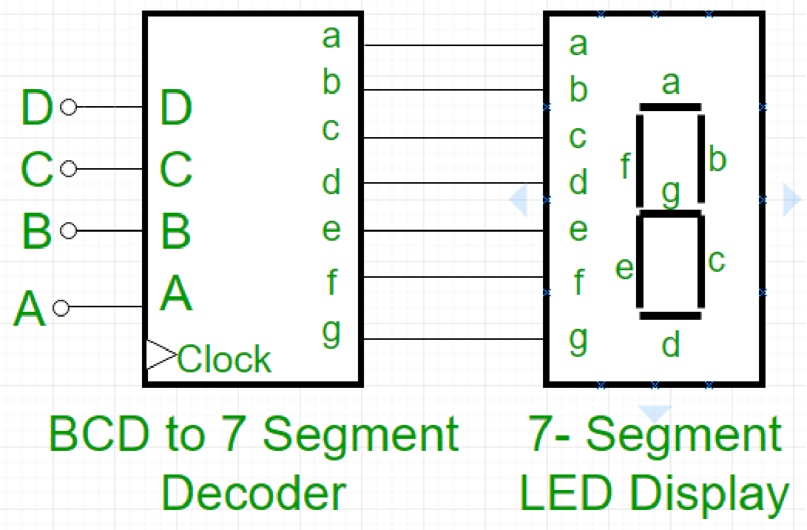
Step 1 Specification



1.1 Segment Designation



1.2 Display LED Designation



Design Procedure

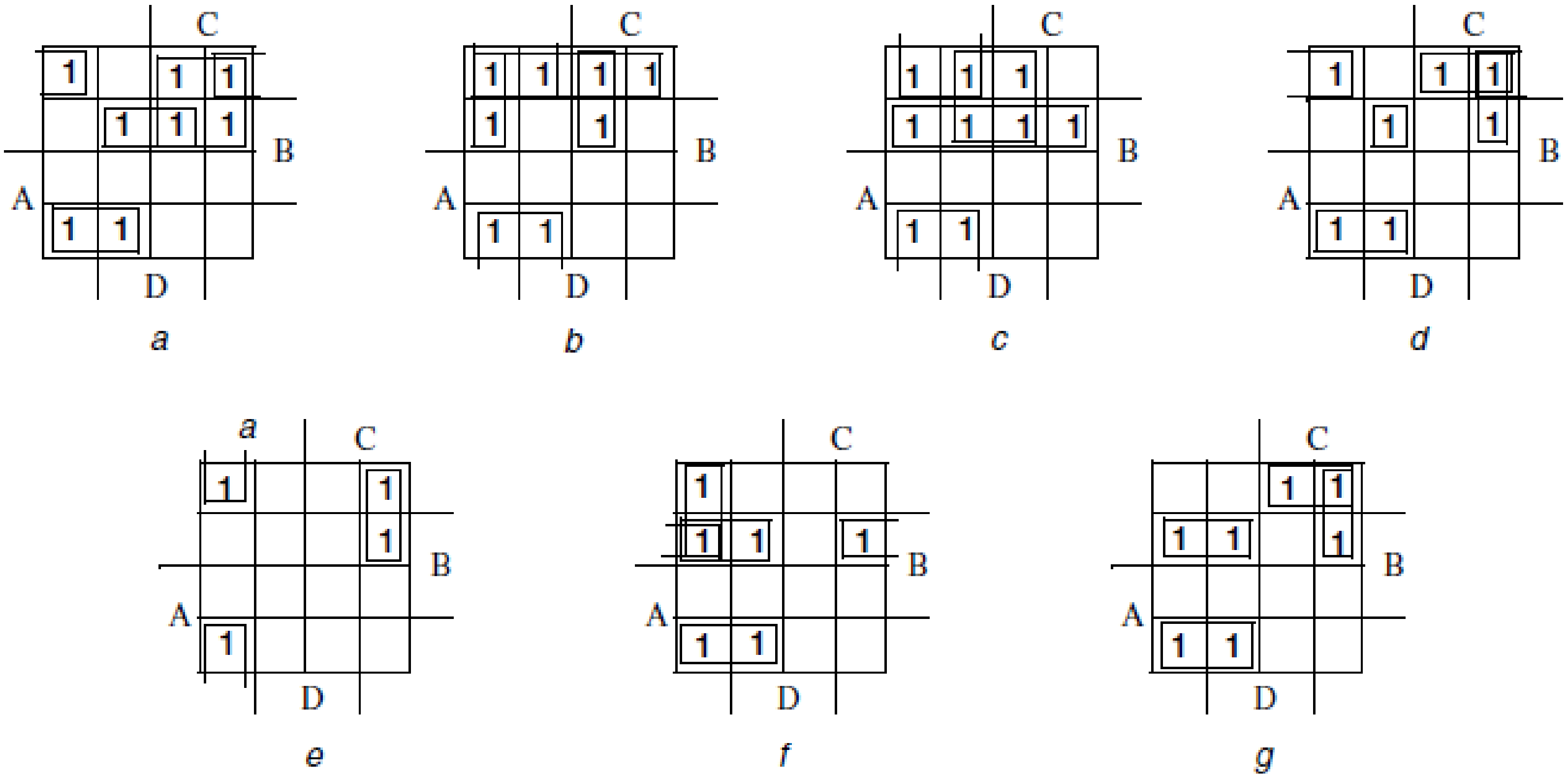
Step 2 Formulation (Truth table)

Method 1
Without
“Don’t care”

	Input				Output						
Dec	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
All other inputs					0	0	0	0	0	0	0

Design Procedure

Step 3 Optimization (K-Map)



Design Procedure

Step 3 Optimization (results Boolean functions)

$$a = \overline{A}C + \overline{A}\,\overline{B}\,\overline{D} + \overline{A}BD + A\overline{B}\,\overline{C}$$

$$b = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}CD$$

$$c = \overline{A}B + \overline{B}\,\overline{C} + \overline{A}D$$

$$d = \overline{A}B\overline{C}D + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{D} + \overline{A}\,\overline{B}C + \overline{A}C\overline{D}$$

$$e = \overline{B}\,\overline{C}\,\overline{D} + \overline{A}C\overline{D}$$

$$f = A\overline{B}\,\overline{C} + \overline{A}B\overline{D} + \overline{A}B\overline{C} + \overline{A}\,\overline{C}\,\overline{D}$$

$$g = A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}C + \overline{A}C\overline{D}$$

Design Procedure

Step 4 Technology Mapping (Logic Diagram)

refer to your solution of “In-class Activity 9”

Design Procedure

Step 2 Formulation (Truth table)

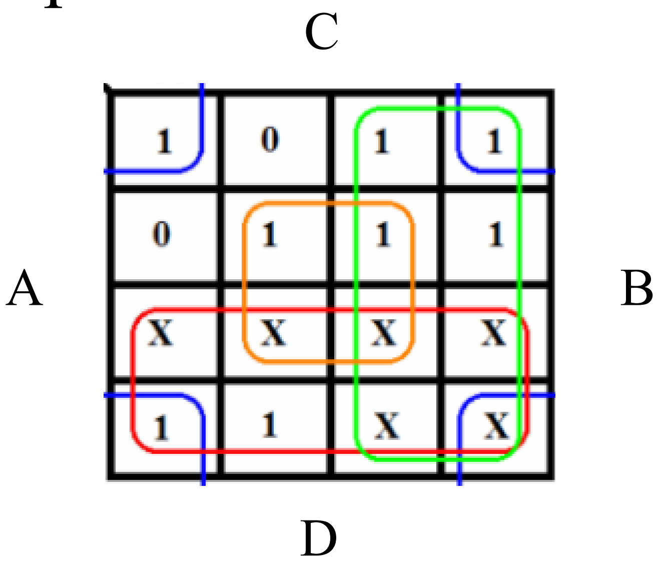
Method 2
With
“Don’t care”

	Input				Output						
Dec	**A**	**B**	**C**	**D**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
All other inputs					X	X	X	X	X	X	X

Design Procedure

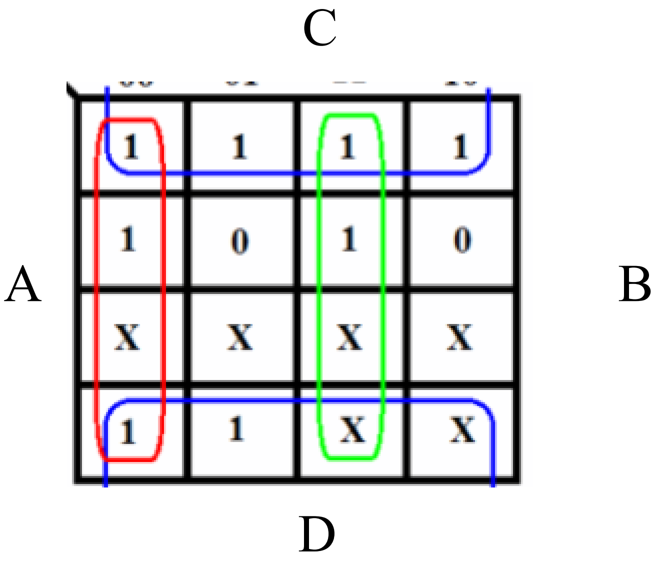
Step 3 Optimization (K-Map)

Output “a”



1	0	1	1
0	1	1	1
X	X	X	X
1	1	X	X

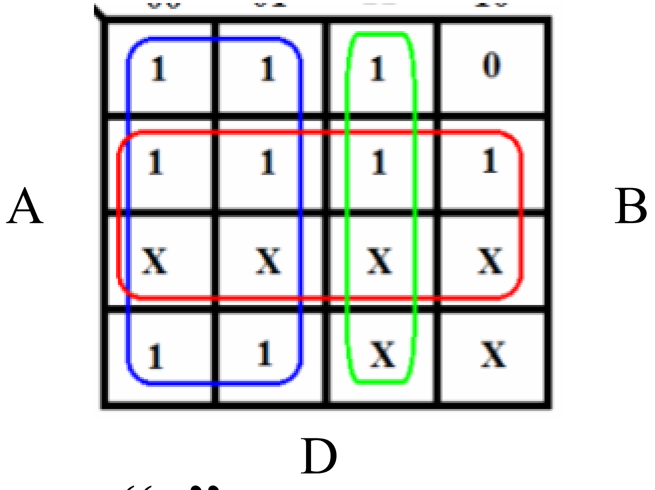
Output “b”



1	1	1	1
1	0	1	0
X	X	X	X
1	1	X	X

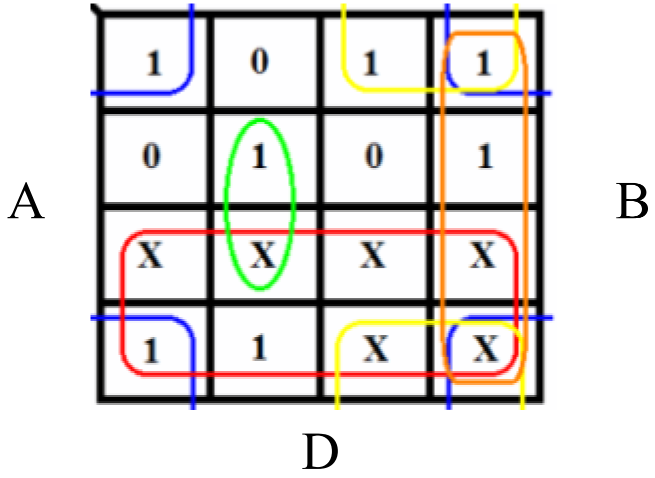
Design Procedure

Output “c”



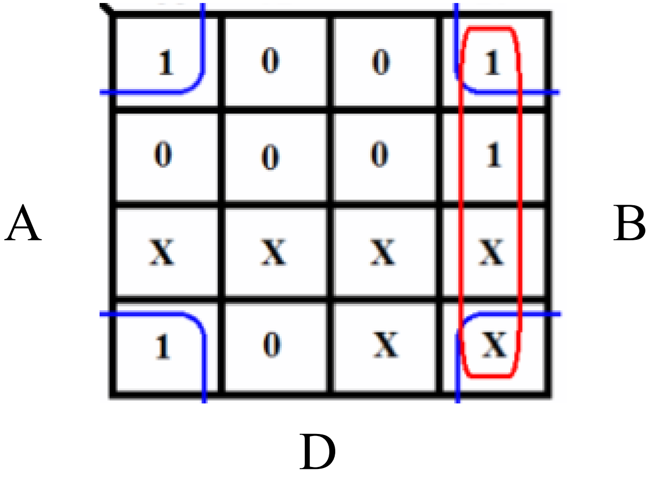
1	1	1	0
1	1	1	1
X	X	X	X
1	1	X	X

Output “d”



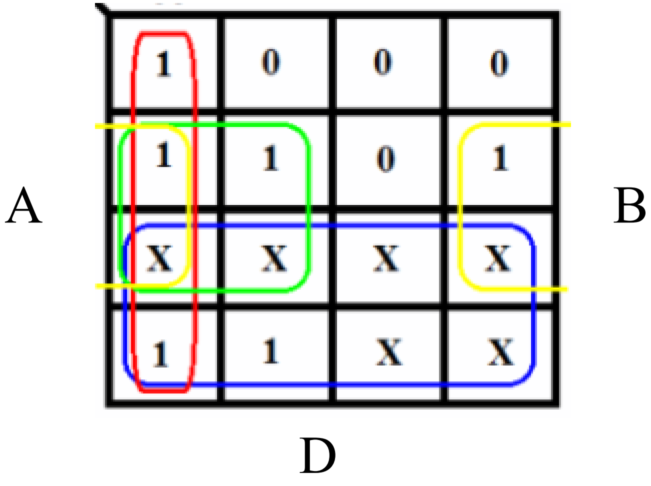
1	0	1	1
0	1	0	1
X	X	X	X
1	1	X	X

Output “e”



1	0	0	1
0	0	0	1
X	X	X	X
1	0	X	X

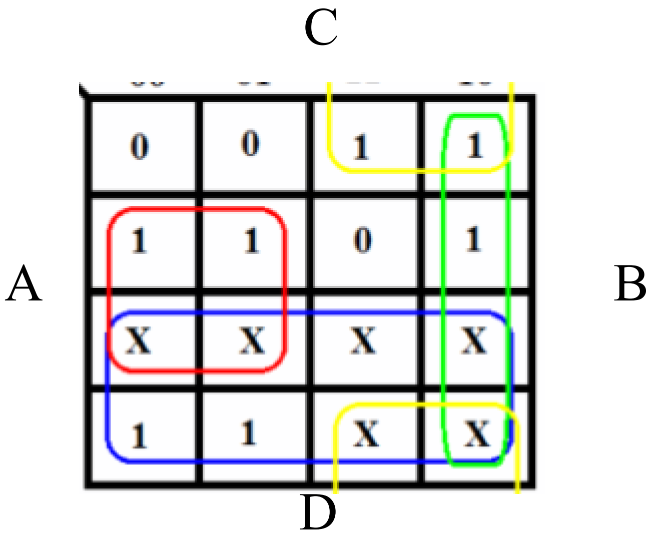
Output “f”



1	0	0	0
1	1	0	1
X	X	X	X
1	1	X	X

Design Procedure

Output "g"



0	0	1	1
1	1	0	1
X	X	X	X
1	1	X	X

$a = A + C + BD + \bar{B}\,\bar{D}$

$b = \bar{B} + \bar{C}\,\bar{D} + CD$

$c = B + \bar{C} + D$

$d = \bar{B}\,\bar{D} + C\bar{D} + B\bar{C}D + \bar{B}C + A$

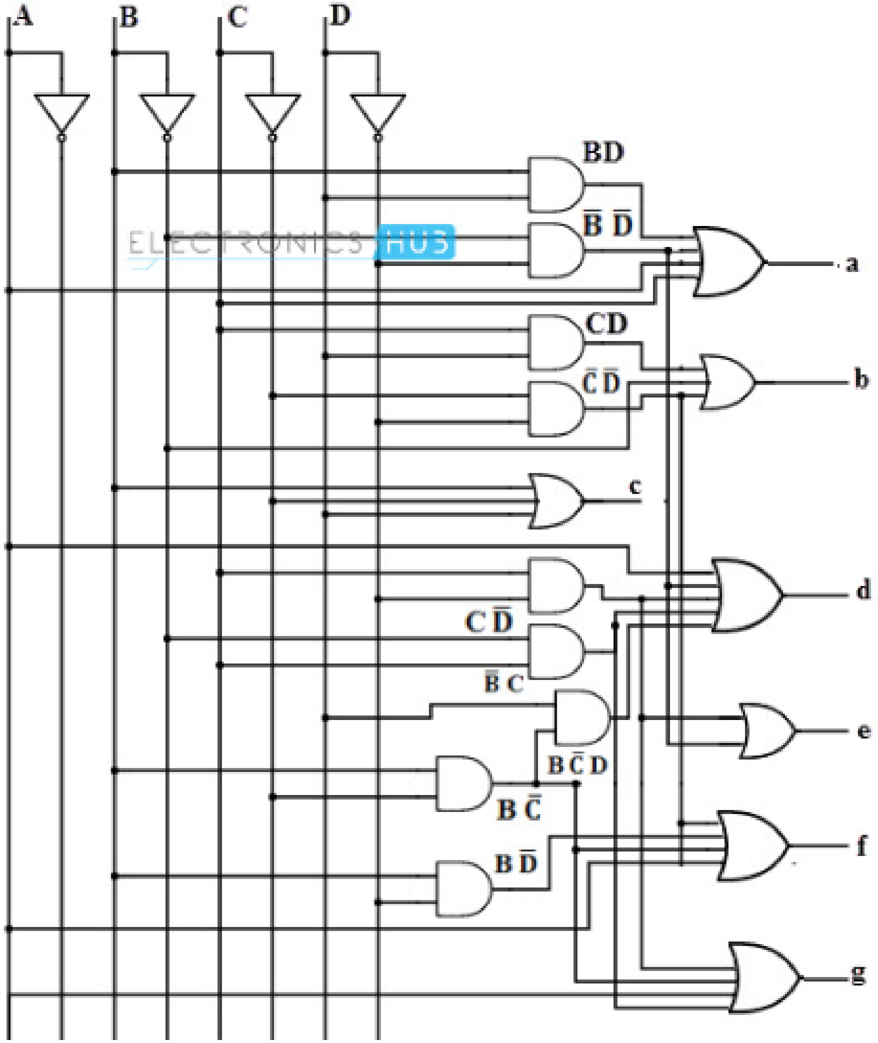
$e = \bar{B}\,\bar{D} + C\bar{D}$

$f = A + \bar{C}\,\bar{D} + B\bar{C} + B\bar{D}$

$g = A + B\bar{C} + \bar{B}C + C\bar{D}$

Design Procedure

Step 4 Technology Mapping (Logic Diagram)


A
B
C
D
BD
$\bar{B}\,\bar{D}$
a
CD
$\bar{C}\,\bar{D}$
b
c
d
$C\,\bar{D}$
$\bar{B}\,C$
e
$B\,\bar{C}\,D$
$B\,\bar{C}$
f
$B\,\bar{D}$
g