JTAG TAP Controller Implementation

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Introduction

JTAG TAP controller is an interface between external testers, debuggers and the embedded circuits of a chip. It is used to facilitate debugging, testing, and programming of embedded circuits. By using JTAG to perform boundary scan testing, we can expose previously hidden aspects of the embedded circuits.

JTAG ports

| Port | width | Input/Output | description |
| --- | --- | --- | --- |
| trst\_n | 1 | input | reset pin(active low) |
| tms | 1 | input | Input select(fsm control) |
| tdi | 1 | input | Test data input |
| tck | 1 | input | Test clock |
| sw | 1 | input | switch(for debugging) |
| tdo | 1 | output | Test data output |
| led | 16 | output | leds(visuals) |

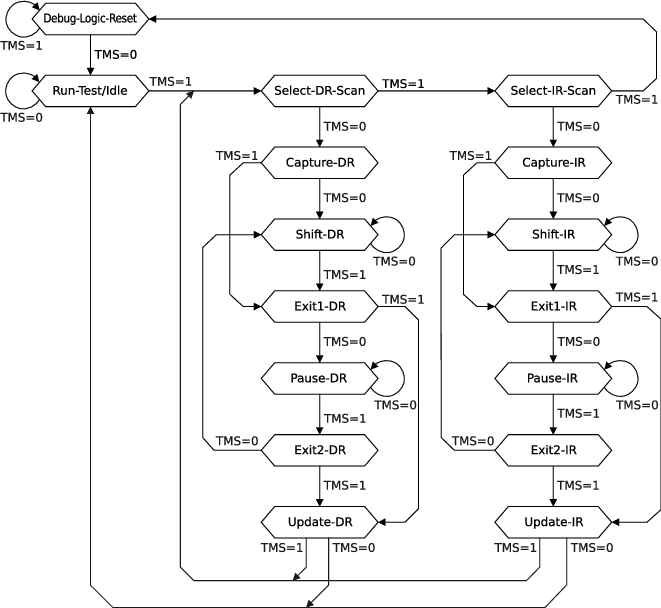
Registers

| name | width | r/w access | description |
| --- | --- | --- | --- |
| tk\_tdr | 8 | read/write | Test data register |
| IDCODE | 32 | read | ID code register(32’hA8B967EE) |

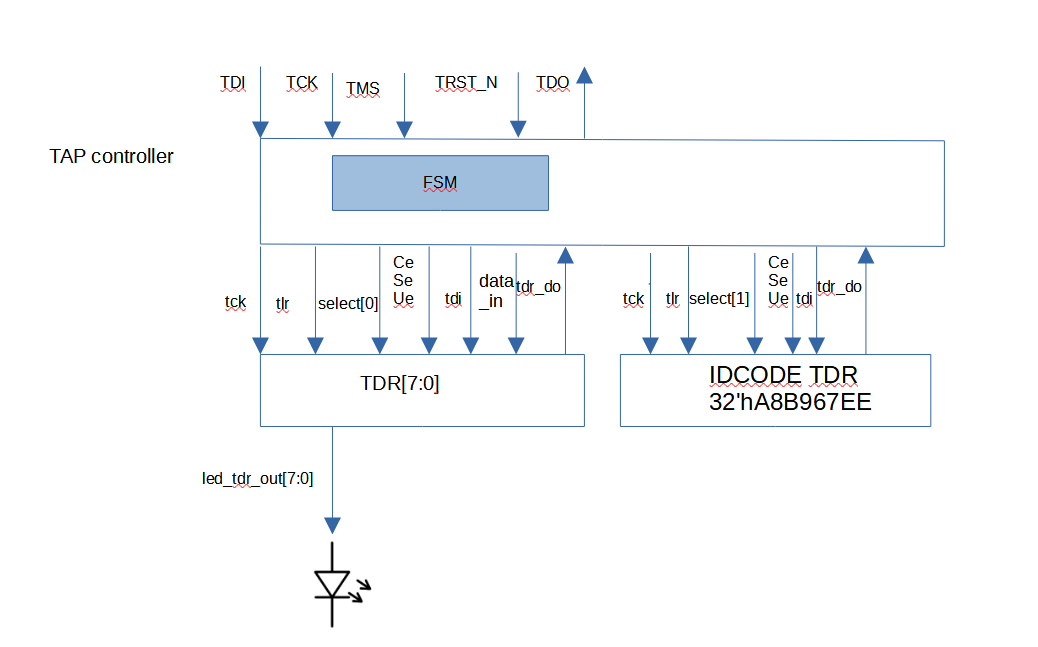
Instructions

| Name | code | description |
| --- | --- | --- |
| CLAMP | 000000 | Forces outputs to certain values |
| EXTEST | 000001 | Tests external logic between chips |
| EXTEST\_PULSE | 000010 | Similar to EXTEST, generates output transitions |
| EXTEST\_TRAIN | 000011 | Same as EXTEST\_PULSE but continuously toggles output on falling tck edge on RUN\_TEST/IDLE state |
| INTEST | 000100 | Internal testing. Loads data from boundary scan register to device core logic. |
| SAMPLE\_PRELOAD | 000101 | Sample data entering and leaving device and preload data into boundary scan register |
| HIGHZ | 000110 | Sets all ports to high impedance. |
| HOSTIJTAG | 000111 | IEEE 1687 IJTAG extension |
| BYPASS | 111111 | Bypasses chip |
| USERDEFINED |  | User defined functions |

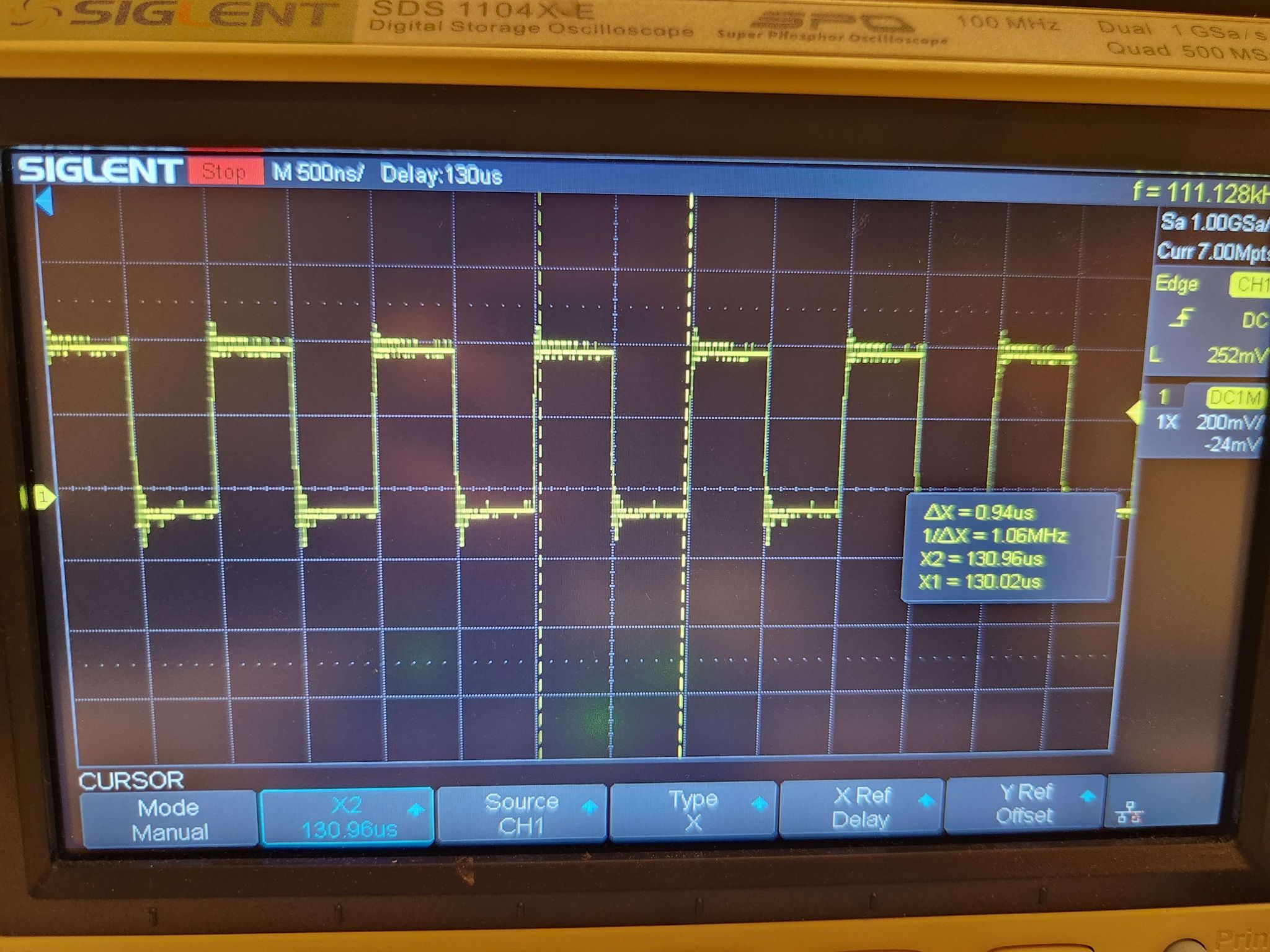
Tap controller



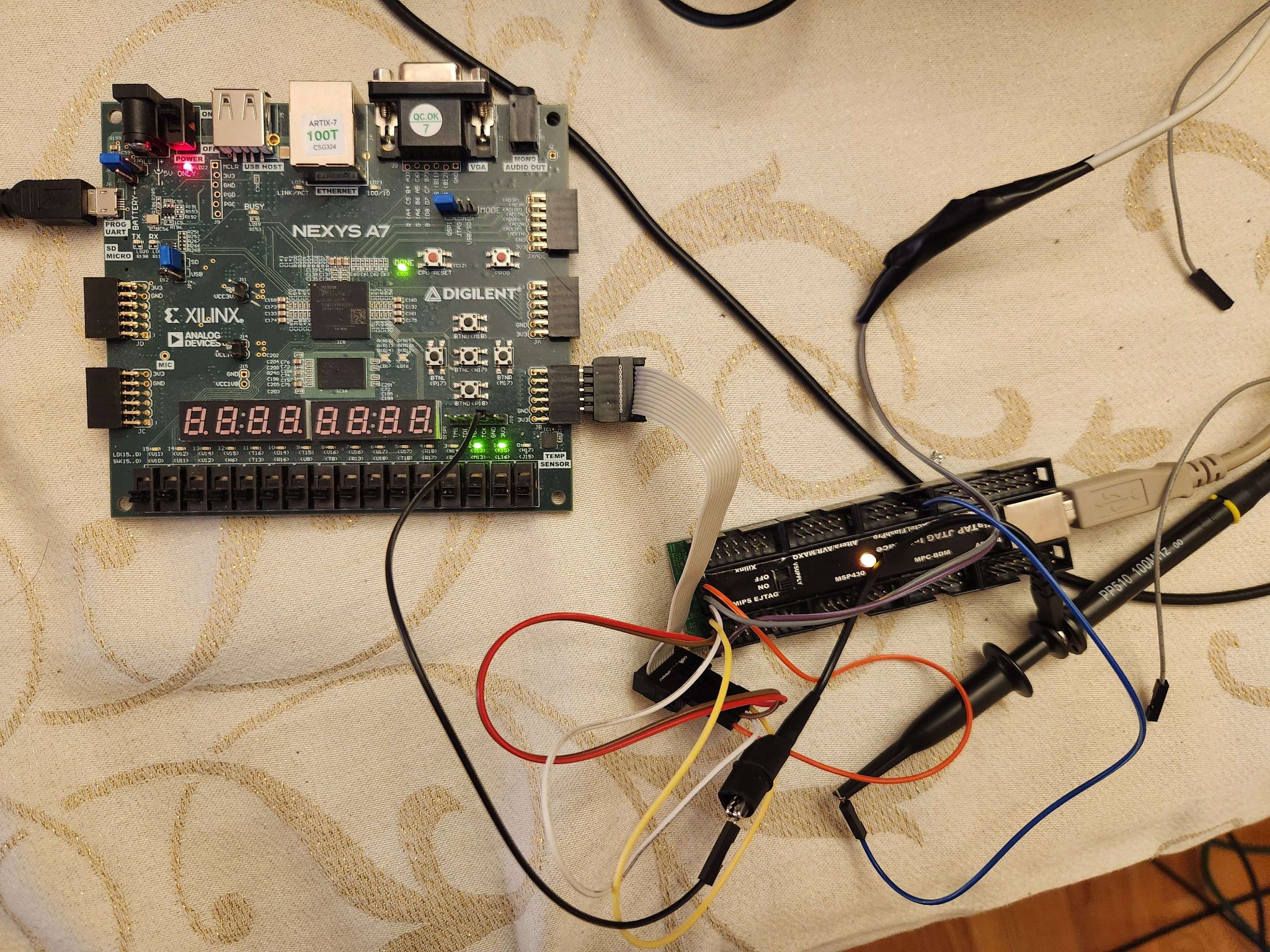
This is the state machine for the TAP controller. It is controlled by the TMS input pin. These states represent what the TAP controller needs to do to read and write from data and instruction registers. For example, test logic reset state is when the test logic is disabled and normal operation of the integrated chip is enabled. In run test idle state, test logic is only active if certain instructions are running. Both Select DR scan and Select IR scan states control whether or not to enter the data path/ instruction path or not. Capture IR and capture DR both shift in values into the register.



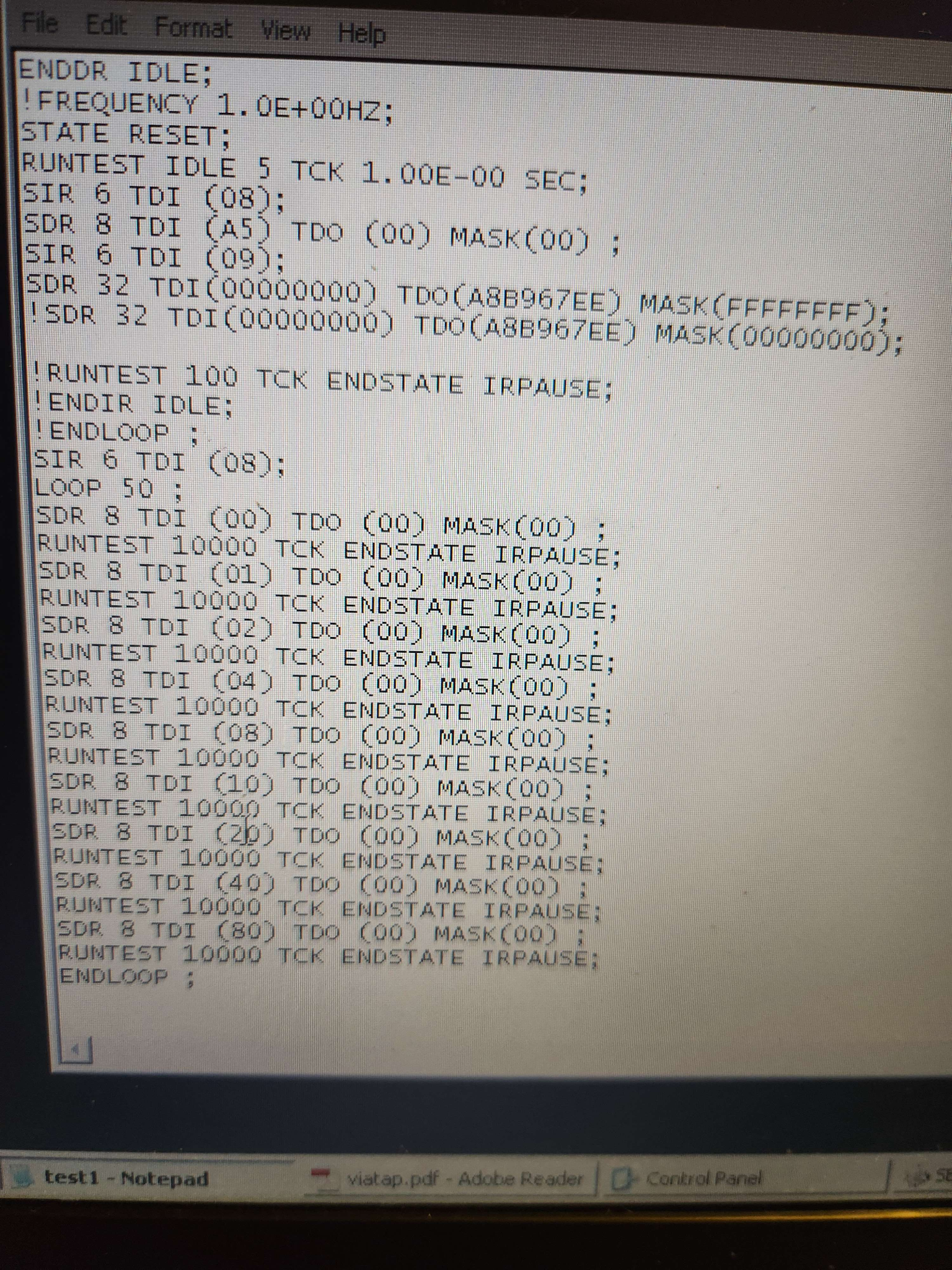
We implemented a JTAG TAP controller linked with an IDCODE register and a normal TDR that drives 8 leds. The TAP controller is controlled by 4 inputs, the data input, the clock, the state machine control input, and the test reset. The TAP controller also outputs data on TDO for the computer to read.



This is the TDI input signal.



The JTAG TAP controller was programmed onto an Diligent A7 100t FPGA board. The computer communicates with the fpga board via an USB to PMOD header adaptor.



This is an example of the SVF file that controls the inputs into the fpga. It is telling the TAP controller to set the data in the TDR so that the leds can pick that data up and display it. We are alternating which of the 8 leds is lit up. This shows how we can control the behavior of any combinational circuit connected to the TAP controller. Instead of this simple example of an array of leds, we can control various other circuits by making the registers in the internal circuit visible to be read and written from an external device.