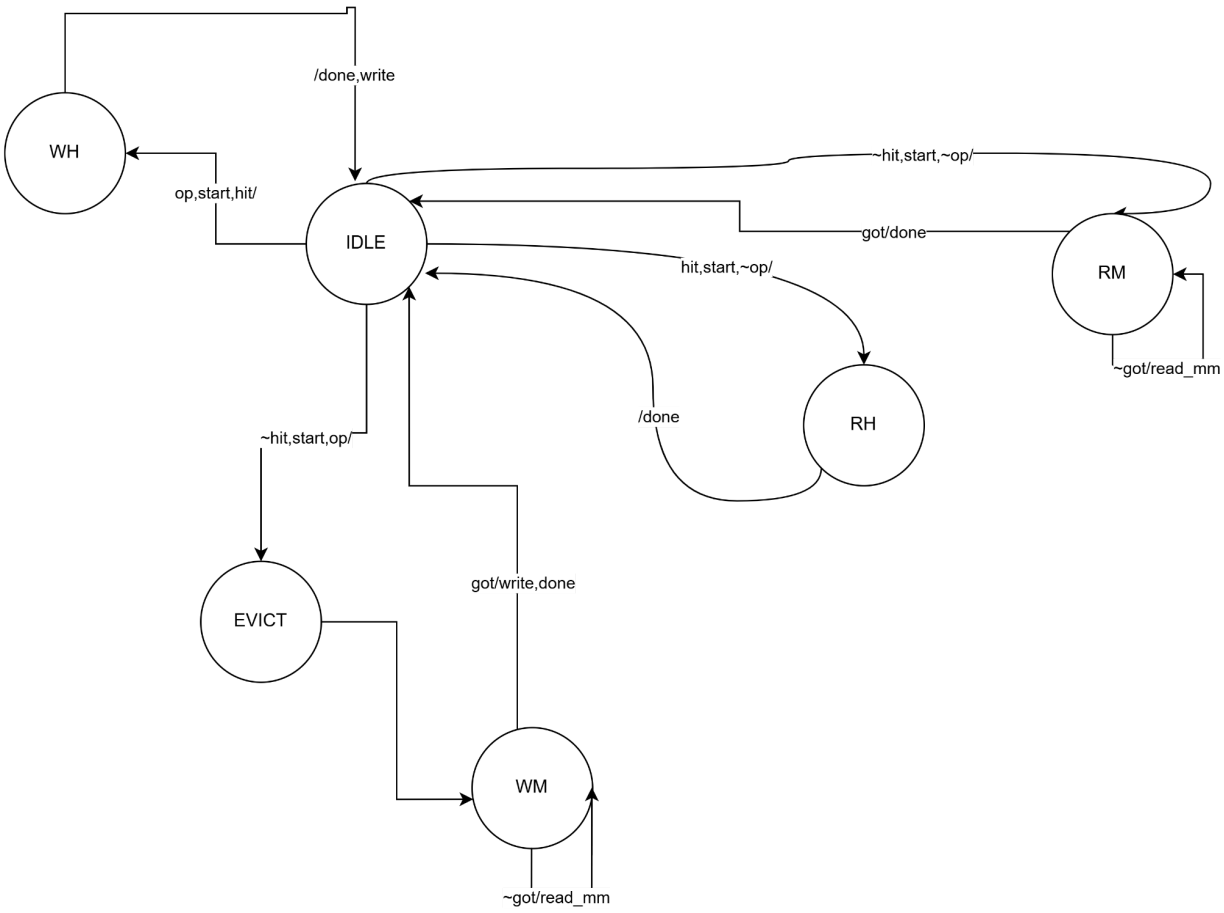
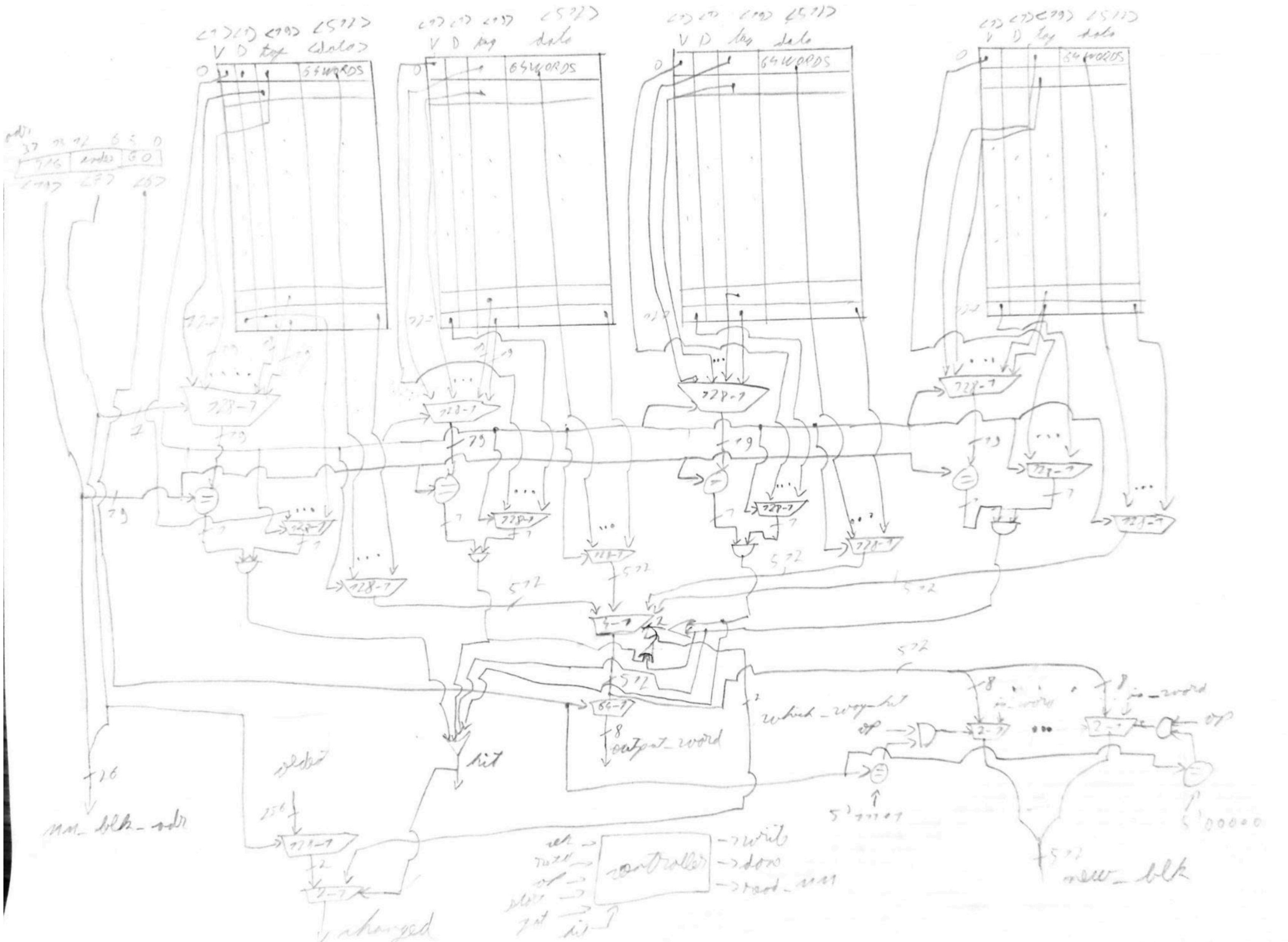
Cache

Brebu Iasmin

FSM diagram

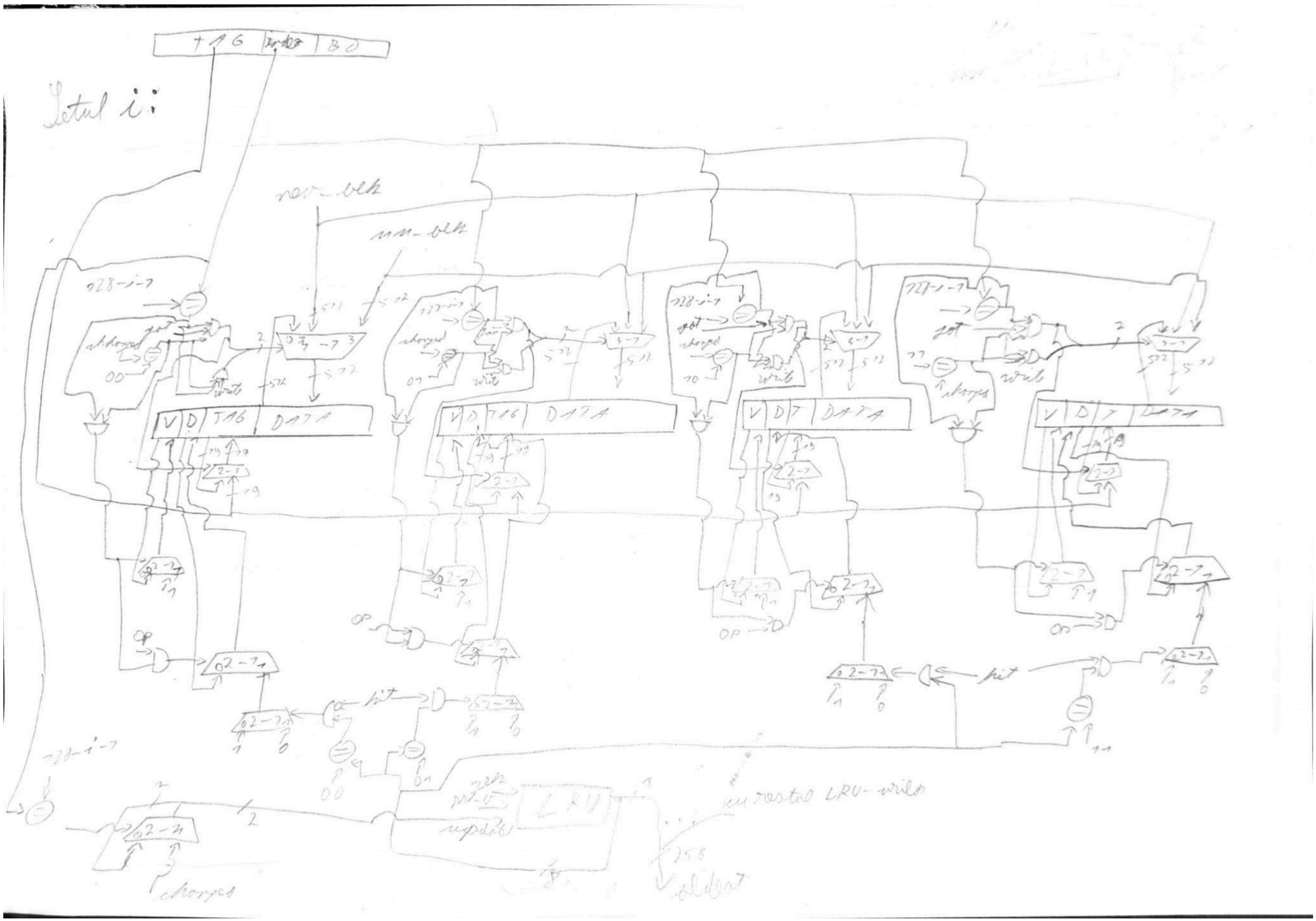


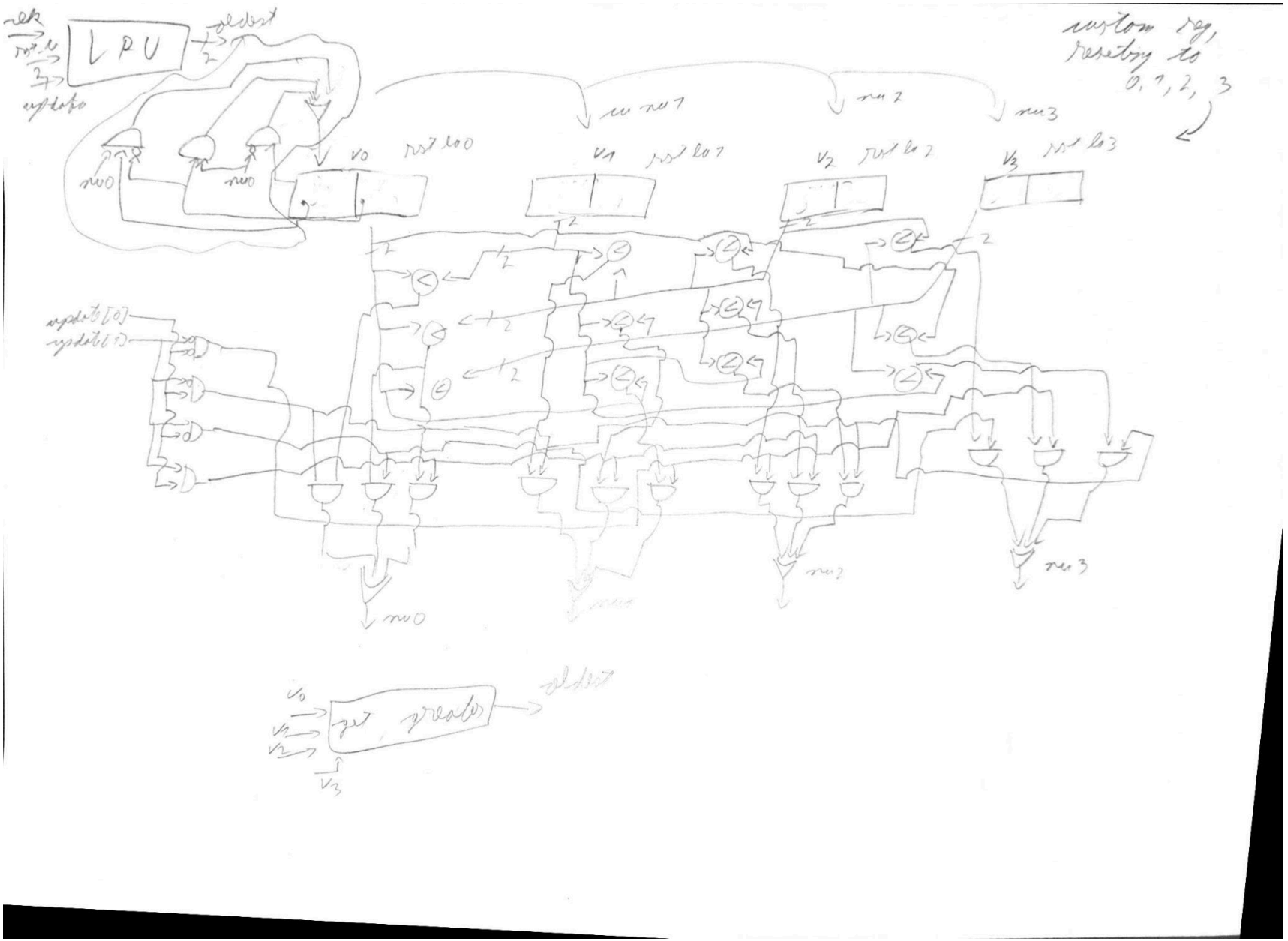
Block Diagram



V D tag data
64WORDS
128-1
hit
output_word
controller
new_blk
changed

Setul i:




LPU
custom reg, resetting to 0, 1, 2, 3
update[0]
update[1]

Why Verilog

Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction.

Chosen due to my familiarity with the language.