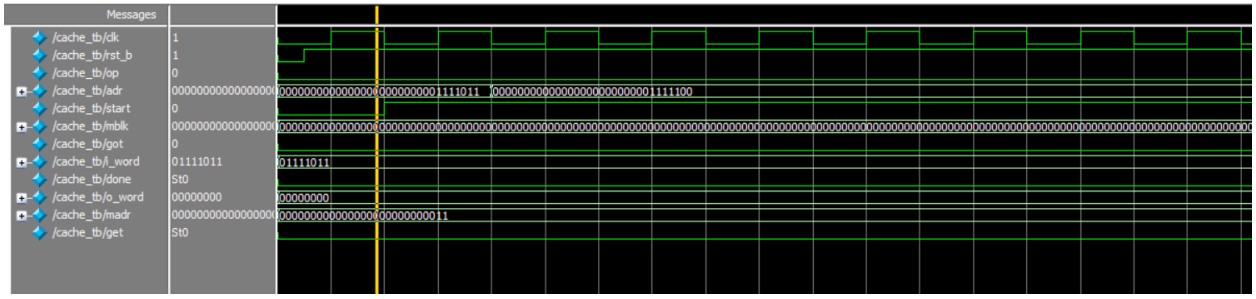
Testing and metrics

Test plan

The test plan was as follows: simulate in the test bench the main memory, having a delay before giving to the cache the signal that the data can be retrieved.

The tests includes, read hits, read misses, write hits, and write misses, the misses having variable length until the block is received from the main memory.

Observed Waveform



Performance Metrics

In theory, access time in case of a hit should be 2 cc, increasing by around 50 cc depending on the performance of the main memory.

We can calculate the HR assuming mostly sequential memory accesses. Since a block has 64 words, the miss rate should be 1/64. If we assume non sequential memory accesses, then this metric will worsen, expecting it to degrade to somewhere around 1/40.