64.CSE1003-Digital Logic and Design Lab

Duration: 9.00 AM to 10.50 AM **Max.Marks = 50**

Distribution of 50 Marks							
Grade Element	**Objective**	**Theory&/ Tables/Model graphs**	**Schematic/ Circuit/ Logicdiagrams/ Relevant Equations**	**Execution**	**Result/ Discussion/ Conclusion**	**Viva**	**Total**
Max. Marks	2	10	18	5	10	5	50
Marks Earned							

(Q) Design a 5-bit odd parity generator. Odd parity bit means that the number of 1's in the code including the parity bit is an odd number. A 5-bit code in which four of the bits (A, B, C, D) represents the information to be sent and fifth bit (x), represents the parity bit.

Viva Questions:

3. Explain the differences among a truth table, a state table, a characteristic table, and an excitation table.

4. Also, explain the difference among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation.

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Digital Logic Design (CSE 1003)

Q). Design a 5 bit parity (odd) generator.

Ans:-

Objective:-

To Design a 5 bit odd parity generator preferably using Multiplexers.

Here, odd parity refers that the total number of '1's including the parity bit is odd number.

Apparatus Used:-

- IC 7404 HEX Inverter
- IC 74151 8 to 1 Multiplexer.
- Logic Toggle
- Logic Probe
- LED
- Common GND Terminal
- Digital pulsed Clock as Input bits.

Softwares Used:-

- Logic Works 5.

Theory:-

Multiplexers

A multiplexer is a special type of combinational circuit in which there are multiple input lines and one output line. The input from any one inputs ($I_0, I_1, I_2 \ldots I_n$) will be redirected to the output with the help of selection inputs.

For 'n' selection inputs, there can be maximum 2^n input lines while the output is always only one.

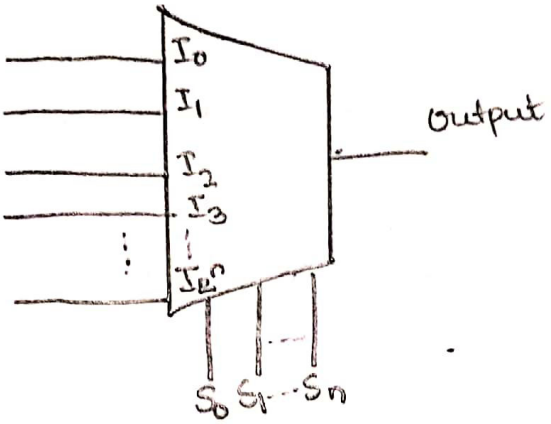

Fig:- 2^n to 1 Multiplexer.

Odd parity

Odd parity is a method for error checking during the transmission of data. It means that the total number of '1's should be odd including the parity bit which is added as redundant bit.

Eg:- Following shows some Odd parity bits :-

A	B	C	D	parity bit
0	0	1	0	0
0	1	1	0	1

Following is the table that demonstrates the corresponding parity bit along with all the possible combination of the input 4 bits.

Inputs				Output (parity bit)
A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Since we are using Multiplexer, we can use the 'A' bit to input data in the input pins of the multiplexer. 'B', 'C' and 'D' can be used as select pins to select one out of 8 input pins from I_0 to I_7.

Following table shows the connection of A or A' to the input pins:-

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A=0 (A')	1	0	0	1	0	1	1	0
A'=1 (A)	0	1	1	0	1	0	0	1
	A'	A	A	A'	A	A'	A'	A

Hence, here,

$I_0, I_3, I_5, I_6 = A'$

$I_1, I_2, I_4, I_7 = A$

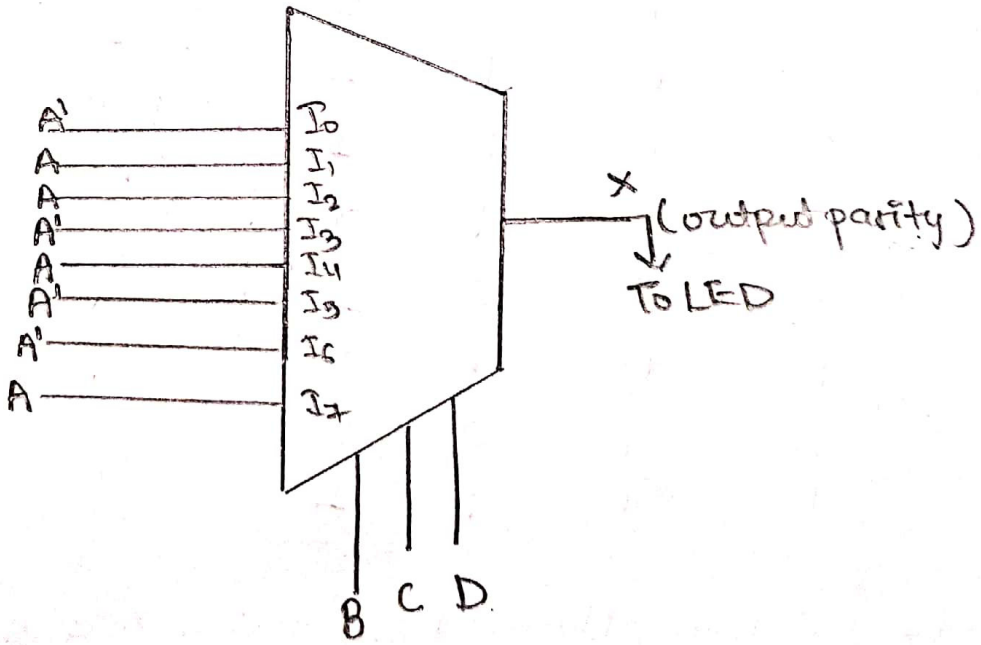

Fig:- General Schematic for odd parity generation using Multiplexer (8:1).

Here, the relevant equations are:-

~~$I_0 = \bar{S}_0\bar{S}_1\bar{S}_2$~~

~~I_7~~

$$X = \bar{S}_0\bar{S}_1\bar{S}_2 I_0 + \bar{S}_0\bar{S}_1 S_2 I_1 + \bar{S}_0 S_1\bar{S}_2 I_2 + \bar{S}_0 S_1 S_2 I_3 + S_0\bar{S}_1\bar{S}_2 I_4 + S_0\bar{S}_1 S_2 I_5 + S_0 S_1\bar{S}_2 I_6 + S_0 S_1 S_2 I_7$$

Take $S_0 = B$, $S_1 = C$, $S_2 = D$ and $(I_0 - I_7)$ as specified above

$$X = \bar{B}\bar{C}\bar{D}\bar{A} + \bar{B}\bar{C}DA + \bar{B}C\bar{D}A + \bar{B}CD\bar{A} + B\bar{C}\bar{D}A + BC\bar{D}\bar{A} + BCDA$$

Now, the required circuit is assembled using Logicworks 5 software and corresponding results are attached with the simulation diagram.

Interpretation of Observed Result from Software:-

We can see that the output sequence follows the pattern

[0 1 1 0 1 0 0 1 0 1 1 0 1 0 0 1] 0 1 1 0 1 ....

↑ required parity bits are obtained.

↑ Same sequence Repeats.

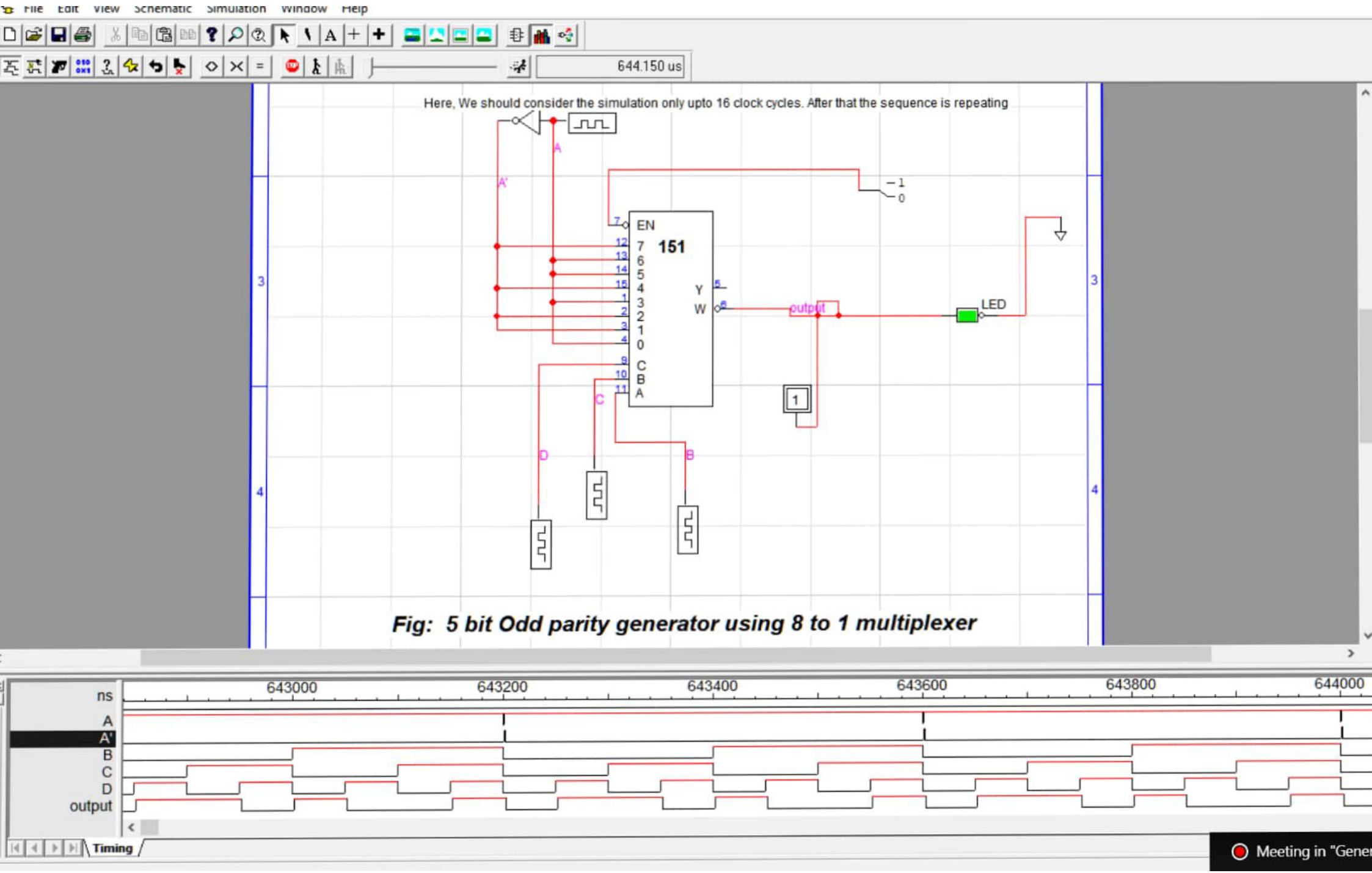

Fig: 5 bit Odd parity generator using 8 to 1 multiplexer

Hence,

In this way, the 5 bit odd parity generator can be made using 8:1 multiplexer.

Viva Questions :-

3). Explain the differences betn truth table, State table, Characteristic Table and excitation table.

Ans :-

Truth Tables

- Truth Tables explain the functionality of given circuit by specifying output for every possible input combination
- Truth table depicts the relation of output with respect to it's inputs.
- It helps relate and study circuit behaviour for both combinational and sequential circuits.

State Table :-

- It is only applicable for sequential circuits.
- It shows the transition from one state to another by mentioning present ~~input~~ State and next state.

Characteristics Table :-

- It gives us information about the inputs of the logic circuits, the present state as well as next state.
- It is also applicable only for sequential circuits.
- It's a bit more detailed than State table.

Excitation Table:-

- This is also only applicable for sequential circuits.
- Excitation refers to inputs, it gives information about what inputs cause state change in a sequential circuit.

4.) Explain the differences among Boolean Equation, State Equation, characteristic Equation and flip-flop input equation.

↳ Ans:-

Boolean Equation:-

- It is the equation applicable for both sequential and combinational circuits.
- It defines the logic circuits and generates logical output true/false for certain set of input combinations.

Eg:- $Y = W'X + W + X$

State Equation:-

- It is the way to describe the behavior of the Sequential Circuit.
- It describes the state of sequential circuit as function of it's state variables.

Eg:- $Q^t = Q + \bar{Q}K$

Characteristic Equation:-

- It is applicable for sequential circuits only.
- It describes the next state as a function of inputs and present state.

Eg:- $Q^+ = X \cdot J_A + J_B Y$

Flip-flop input functions:-

- It is applicable only for flip-flops. Eg:- $J_A = K + X J_B$
- It shows the input of flip-flops as a function of the inputs, present state and other combinational logic.