DIGITAL LOGIC DESIGN EXPERIMENT #8

CLOCKED SEQUENTIAL CIRCUITS AND COUNTERS

OBJECTIVE:

- To design, build and test synchronous sequential circuits.
- To design, build, and test synchronous counters
- To design, build and test asynchronous counters

APPARATUS:

- IC type 7476 dual JK master-slave flip-flops
- IC type 7400 quad 2-input NAND gates

Softwares Used:

- Cadence Capture CIS Lite

PROCEDURE:

1. *SYNCHRONOUS SEQUENTIAL CIRCUITS:*

a) *Design, construct and test a sequential circuit whose state is shown in Fig.1. Use JK flip-flops in the design.*
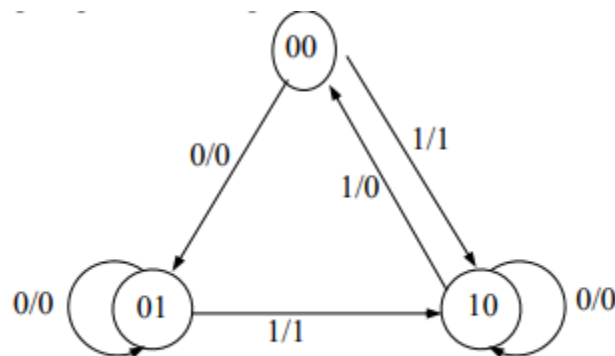

Fig. 1

The circuit has two flip-flops A, B, one input x and one output y. The circuit is to be designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting. If not suggest a solution.

b) *Complete the excitation table shown in Table 1*

Table 1.

Present state		Input	Next state		Output	Flip-flop input function			
A	B	X	A	B	Y	JA	KA	JB	KB
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0	0	1	0	0	X	X	0
0	1	1	1	0	1	1	X	X	1
1	0	0	1	0	0	X	0	0	X
1	0	1	0	0	0	X	1	0	X
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X

*c)*Using Karnaugh maps obtain minimal expressions for the flip-flop input functions JA, KA, JB, KB.

JA　B,X

	00	01	11	10
A 0	0	1	1	0
1	-	-	-	-

KA　B,X

	00	01	11	10
A 0	-	-	-	-
1	0	1	-	-

JB　B,X

	00	01	11	10
A 0	1	0	-	-
1	0	0	-	-

KB　B,X

	00	01	11	10
A 0	-	-	1	0
1	-	-	-	-

Y　B,X

	00	01	11	10
A 0	0	1	1	0
1	0	0	-	-

From the above Kmap, Input functions are:

JA = X

KA = X

JB = A'X'

KB = X

Output function is:

Y=A'X

d. Simulate the circuit using LogicWorks. LogicWorks does not have the JK master-slave flip-flop IC 7476. Use instead the generic JK flip-flop as you did in experiment 9. In the Lab, build the circuit and check the output to verify the state table values.
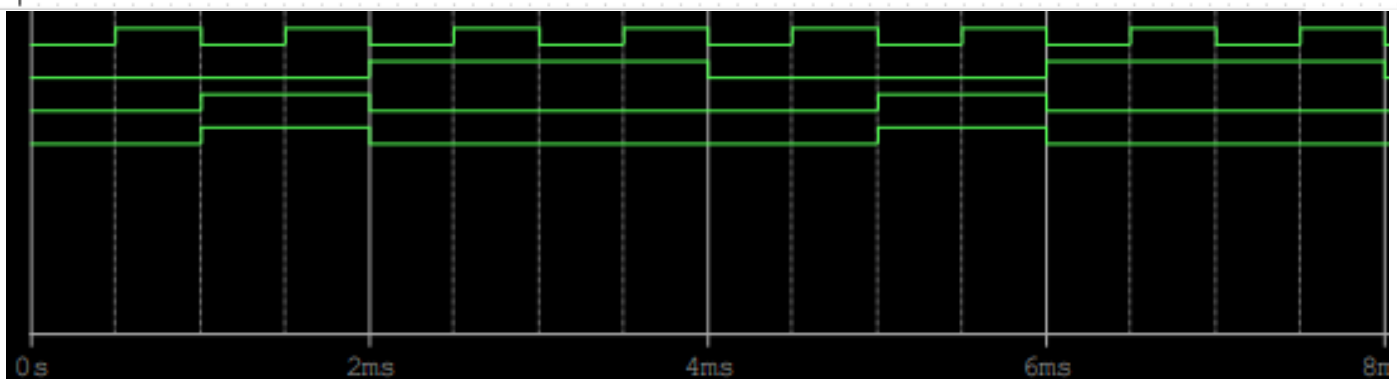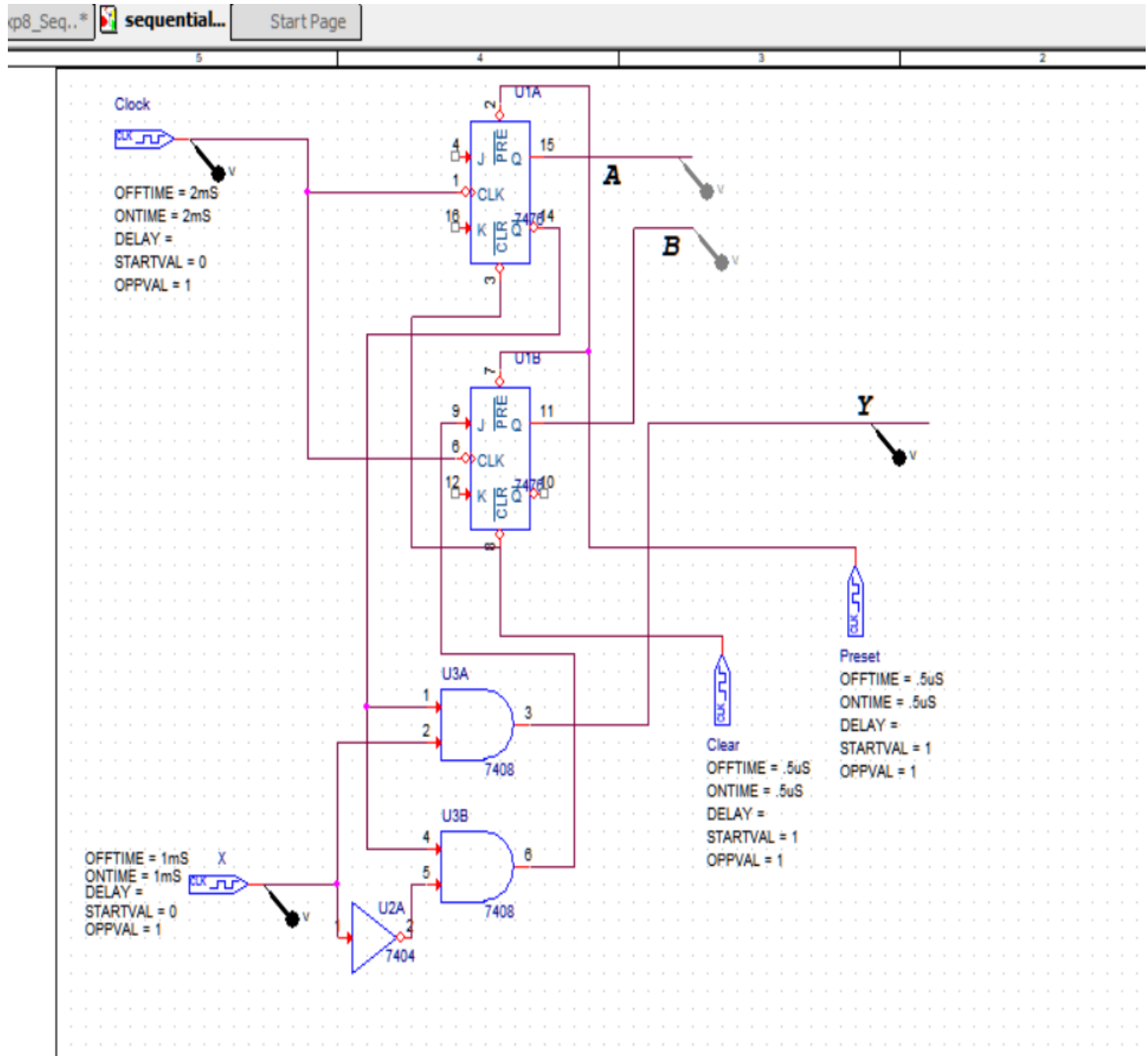
2. # *Synchronous Counters*

Synchronous counters have all clock lines tied to a common clock causing all flip-flops to change at the same time. The count sequence of a counter can be analyzed by placing the counter into every possible number in the sequence and determining the next number in the sequence state diagram is developed as the analysis proceeds. (A state diagram is an illustration of the transitions that occur after each clock pulse).

a) *In the pre-lab using LogicWorks and then in the lab using hardware chips, design a 2-bit gray code counter using JK flip-flops. The required sequence is the binary equivalent of (0-1-3-2-0). A state diagram for this counter is given in Fig. 2.*
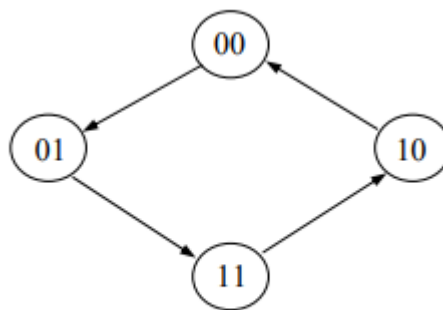

Fig. 2

b) *Complete the excitation table (Table 2) for the counter and obtain logic expression for the JK flip-flop input functions.*

Present_State		Next state		Flip Flop input functions			
A	B	A	B	JA	JB	KA	KB
0	0	0	1	0	X	X	X
0	1	1	1	X	X	X	0
1	0	0	0	0	1	1	X
1	1	1	0	X	0	0	1

The respective KMaps of JA, JB, KA, KB are:

Flip-flop input functions are:

JA=B   **KA=B'**
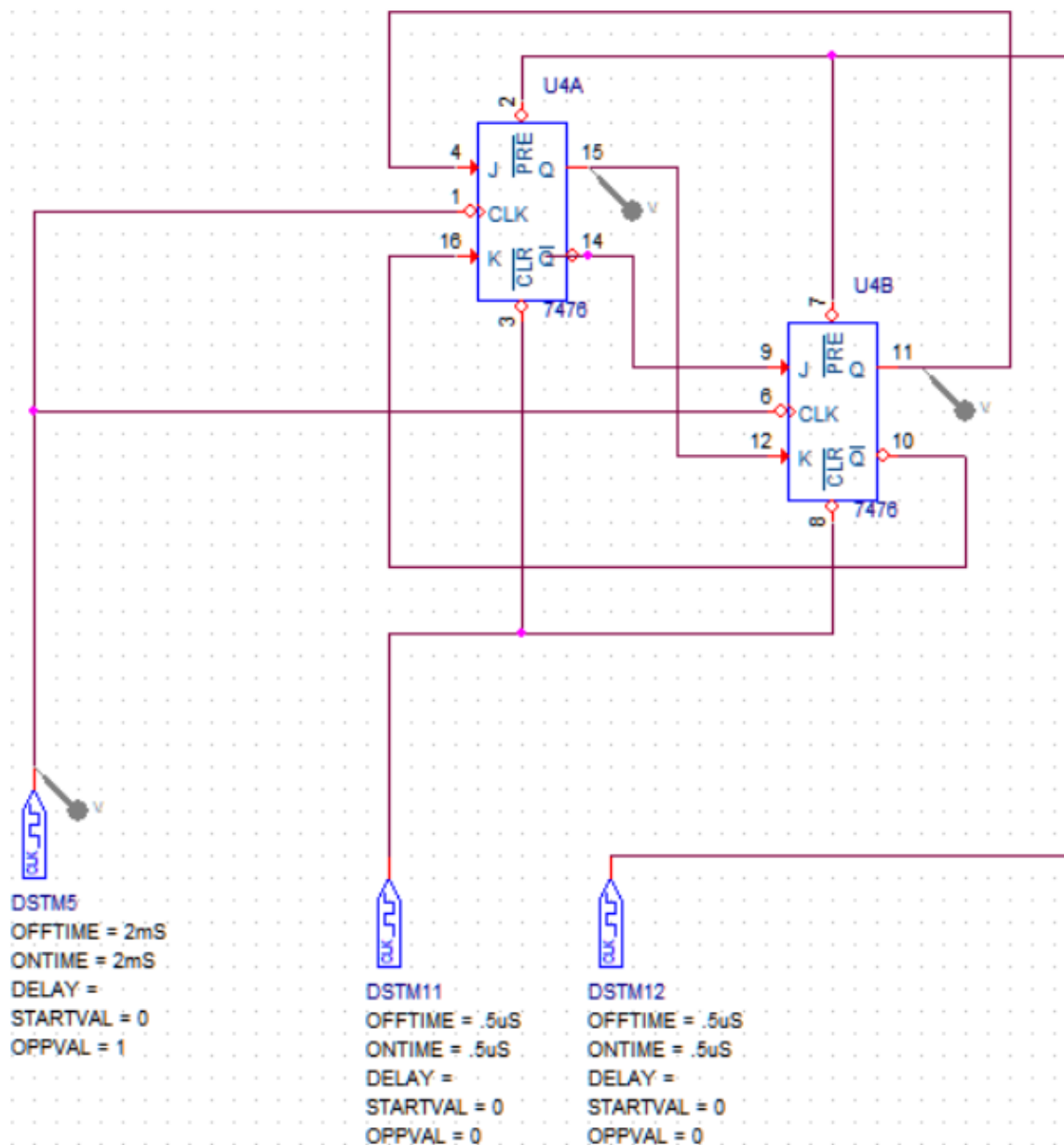
JB=A'   **KB=A**

c) In the lab, build the circuit and test it by pulsing it from the PB-503. Check that the output is the designed sequence.

U4A

J   PRE   Q   15
4
1
CLK
16
K   CLR   Q̄   14
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U4B

J   PRE   Q   11
9
6
CLK
12
K   CLR   Q̄   10
7476

DSTM5
OFFTIME = 2mS
ONTIME = 2mS
DELAY =
STARTVAL = 0
OPPVAL = 1

DSTM11
OFFTIME = .5uS
ONTIME = .5uS
DELAY =
STARTVAL = 0
OPPVAL = 0

DSTM12
OFFTIME = .5uS
ONTIME = .5uS
DELAY =
STARTVAL = 0
OPPVAL = 0

3. # *Asynchronous Counters*

Asynchronous counters are a series of flip-flops each clocked by the previous state, one after the other. Since all the stages of the counter are not clocked together, a ripple effect propagates as various flip-flops are clocked. For this reason they are called ripple counters. The modulus of a counter is the number of different output states the counter may take (i.e. Mod 4 means the counter has four output states).

a) *In the pre-lab construct a 4-bit asynchronous counter shown in Fig.3. (It is also called binary ripple counter). Use four generic JK flip-flops. Connect four Binary Probes to Q outputs. Connect all R and S inputs to Logic 1 and connect a switch to the CP input.*
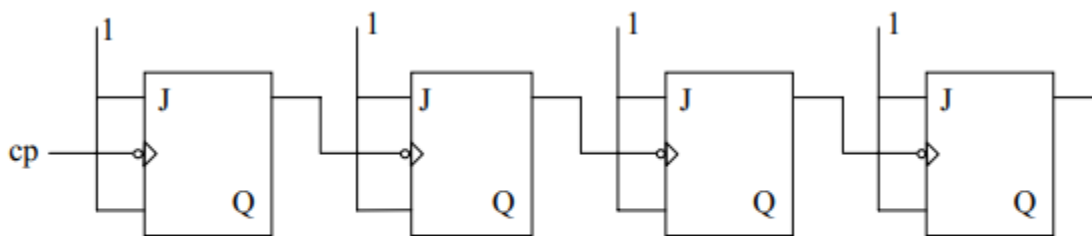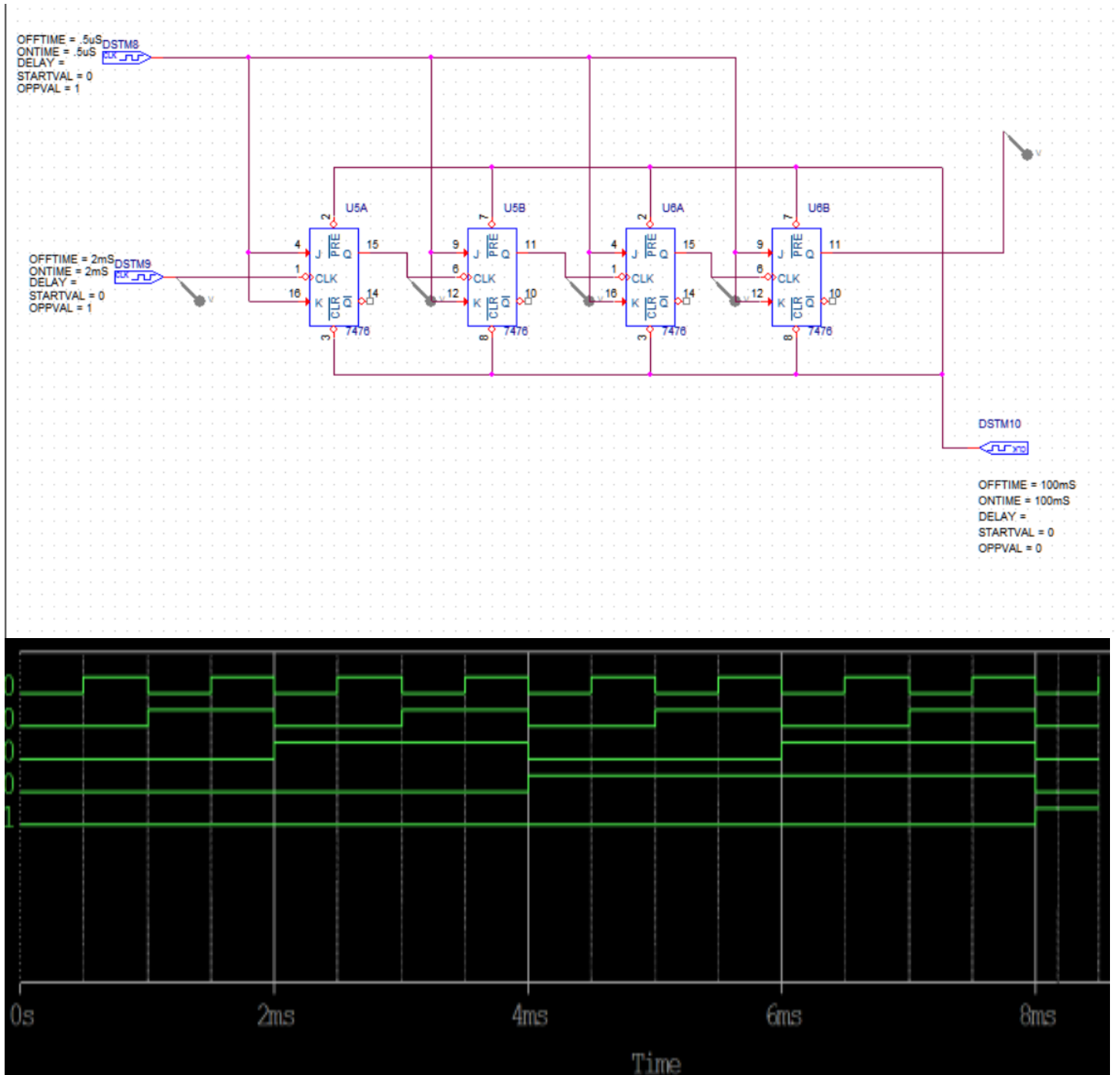

Fig. 3 4-bit ripple counter

b) In the Lab use two 7476 ICs to implement the design. Connect Q outputs of flip-flops to indicator lamps of the PB-503. Connect all clear (CLR) and preset (PRE) inputs to logic 1. Connect the CP input to the pulse output of the PB-503 and check the counter for proper operation.

c) Write down the count sequence in Table 3. Identify this count sequence (up or down). Comment on what happens after the application of 15 pulses to CP input.

Table 3. Count sequence for the 4-bit ripple counter.

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	`1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

The above given is up counter.

After the counter reaches upto 16, it resets to 0000 and the cycle again continues.