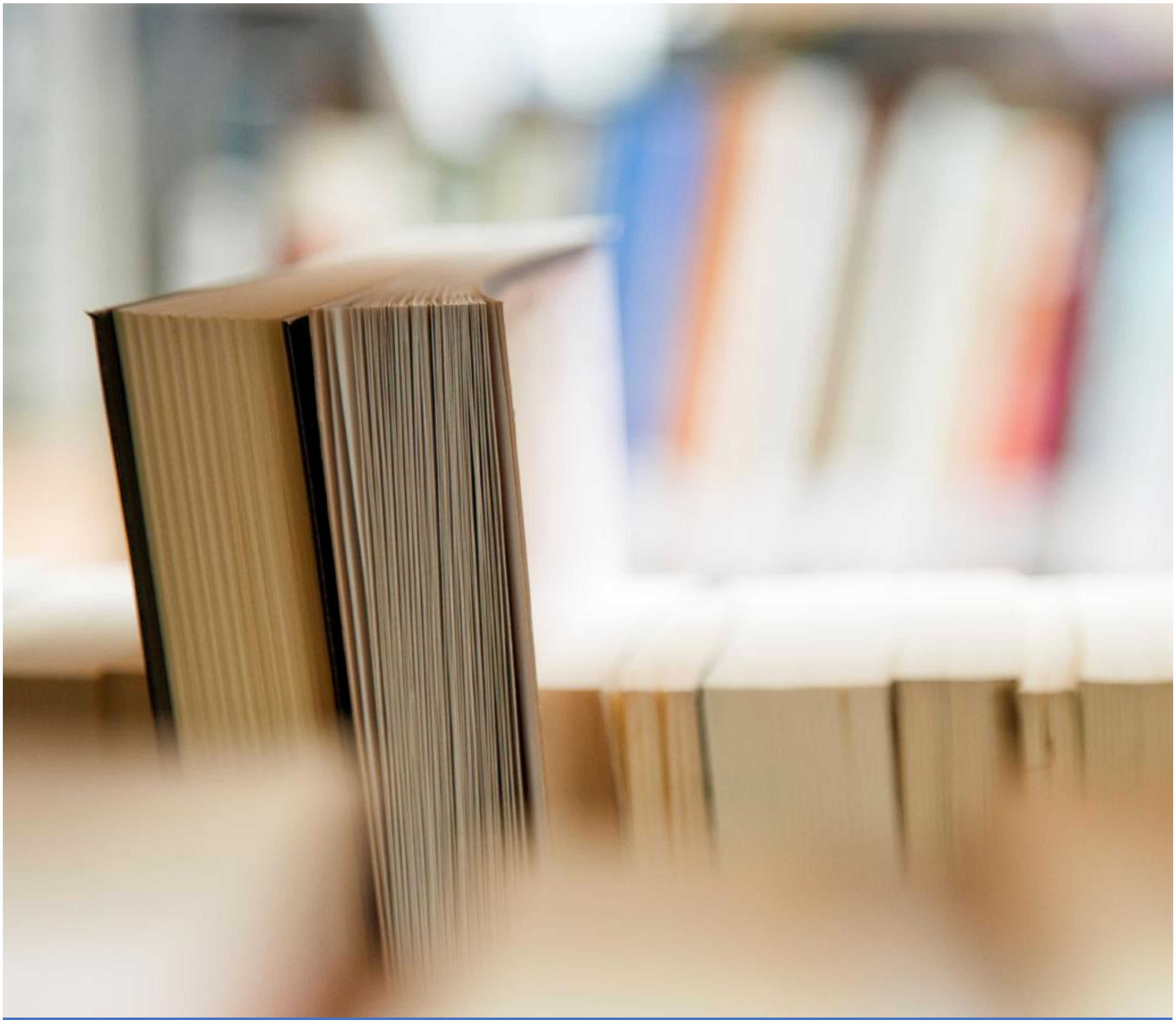


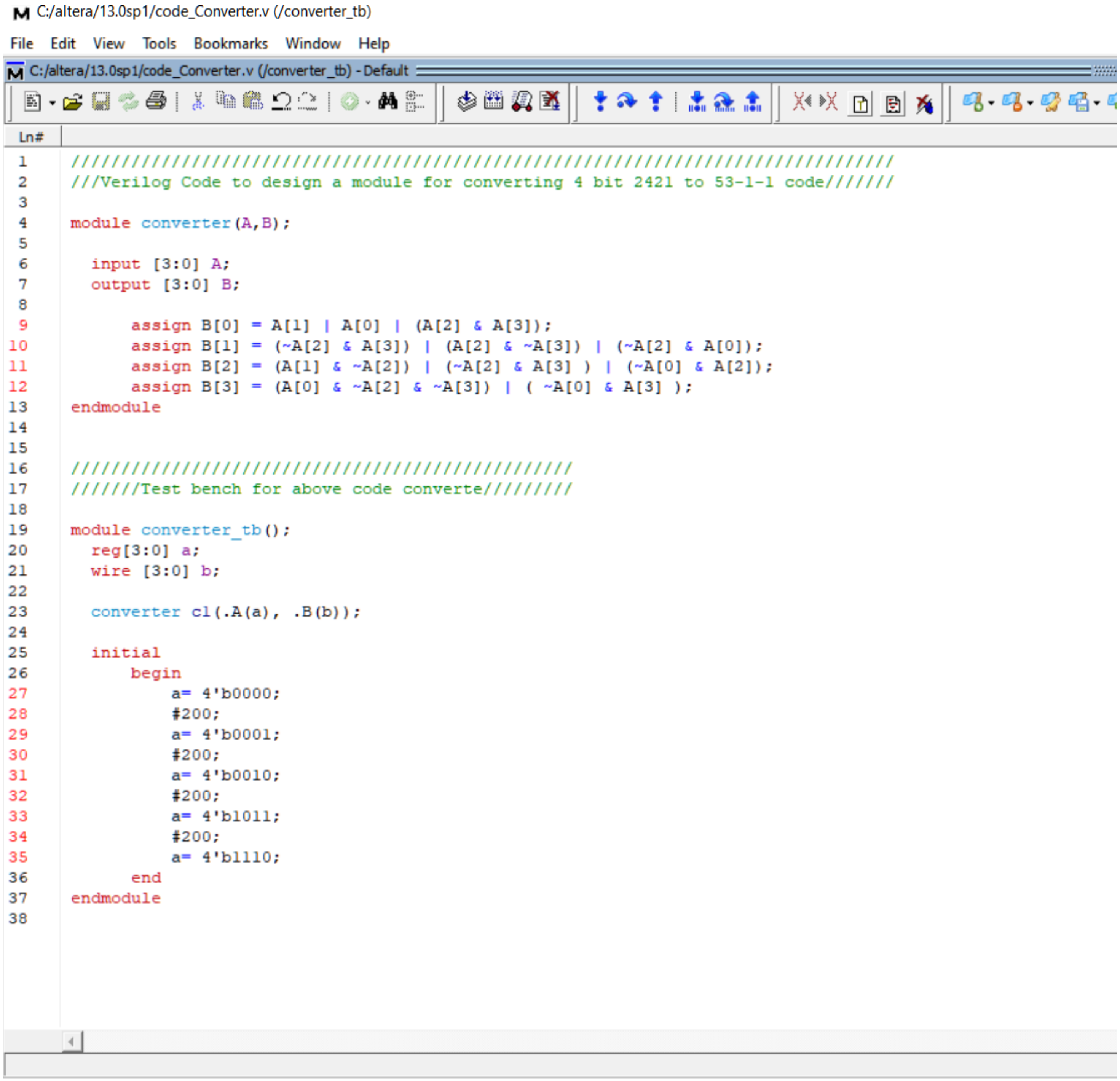
Digital Simulation Using Verilog in Modelsim

Experiment 9

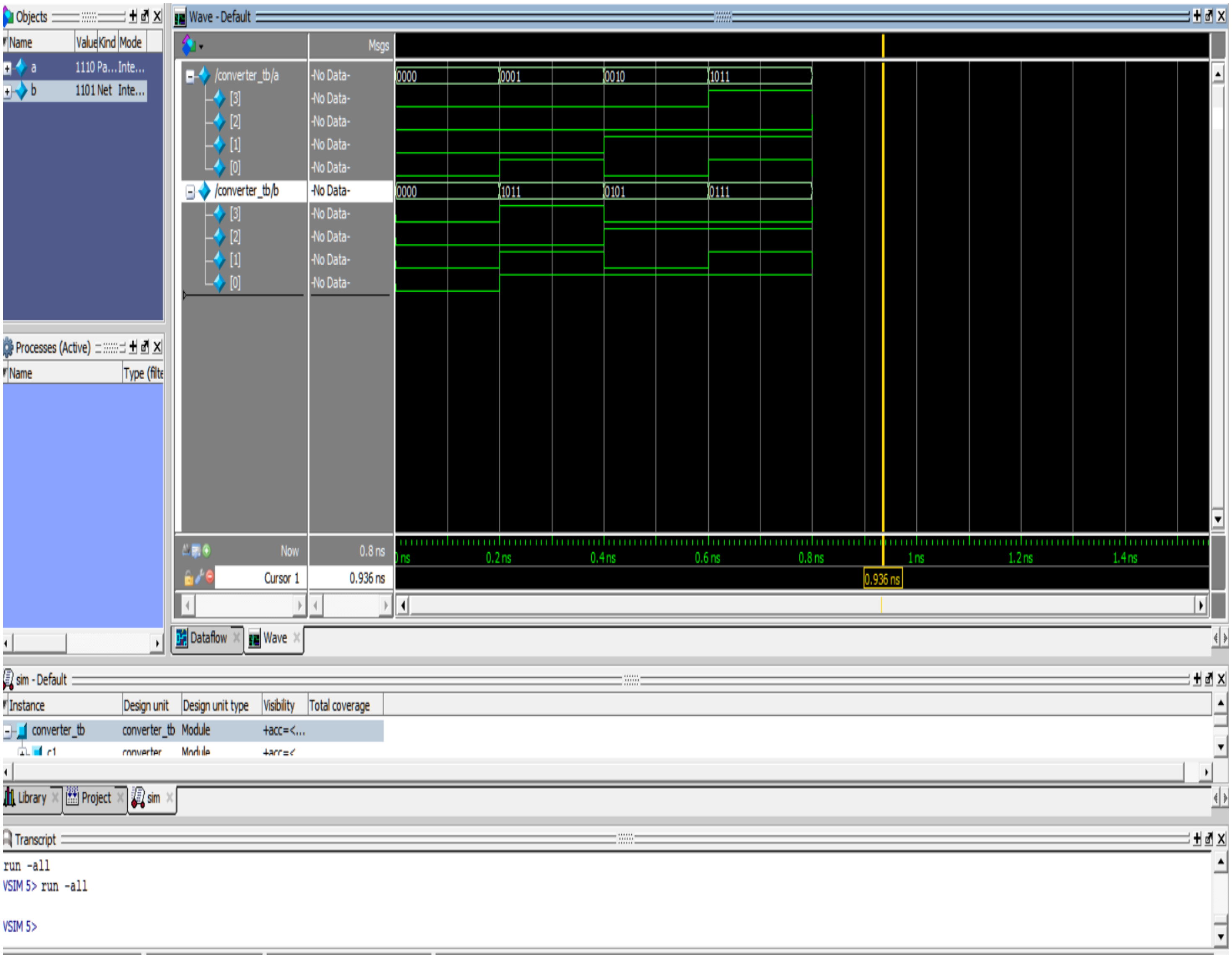
BIMAL PARAJULI (20BDS0405) 7/18/21 CSE – 1003 (LAB)

Bimal parajuli (20BDS0405)

Verilog Simulation of 2421 to 53-1-1 Code Converter ($_{DA_2}$).


C:/altera/13.0sp1/code_Converter.v (/converter_tb)
File Edit View Tools Bookmarks Window Help
C:/altera/13.0sp1/code_Converter.v (/converter_tb) - Default
Ln#

```
//////////////////////////////////////////////////////////////////////////////////
///Verilog Code to design a module for converting 4 bit 2421 to 53-1-1 code///////

module converter(A,B);

  input [3:0] A;
  output [3:0] B;

      assign B[0] = A[1] | A[0] | (A[2] & A[3]);
      assign B[1] = (~A[2] & A[3]) | (A[2] & ~A[3]) | (~A[2] & A[0]);
      assign B[2] = (A[1] & ~A[2]) | (~A[2] & A[3] ) | (~A[0] & A[2]);
      assign B[3] = (A[0] & ~A[2] & ~A[3]) | ( ~A[0] & A[3] );
endmodule


//////////////////////////////////////////////////
///////Test bench for above code converte/////////

module converter_tb();
  reg[3:0] a;
  wire [3:0] b;

  converter c1(.A(a), .B(b));

  initial
      begin
          a= 4'b0000;
          #200;
          a= 4'b0001;
          #200;
          a= 4'b0010;
          #200;
          a= 4'b1011;
          #200;
          a= 4'b1110;
      end
endmodule
```



Name	Value	Kind	Mode
a	1110	Pa...	Inte...
b	1101	Net	Inte...

	Msgs				
/converter_tb/a	-No Data-	0000	0001	0010	1011
[3]	-No Data-				
[2]	-No Data-				
[1]	-No Data-				
[0]	-No Data-				
/converter_tb/b	-No Data-	0000	1011	0101	0111
[3]	-No Data-				
[2]	-No Data-				
[1]	-No Data-				
[0]	-No Data-				

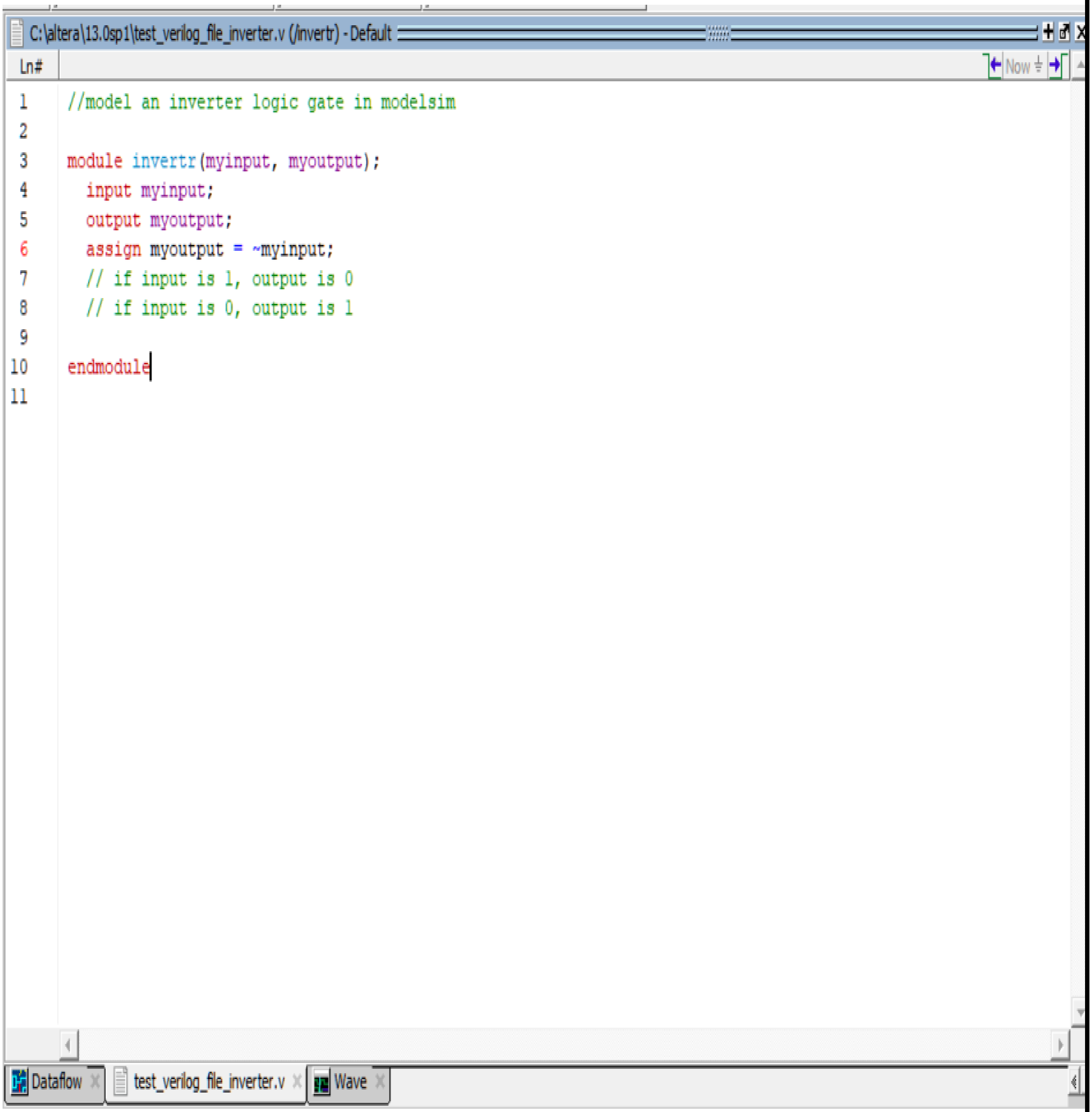
Now	0.8 ns
Cursor 1	0.936 ns

Instance	Design unit	Design unit type	Visibility	Total coverage
converter_tb	converter_tb	Module	+acc=<...	
c1	converter	Module	+acc=<	

```
run -all
VSIM 5> run -all

VSIM 5>
```

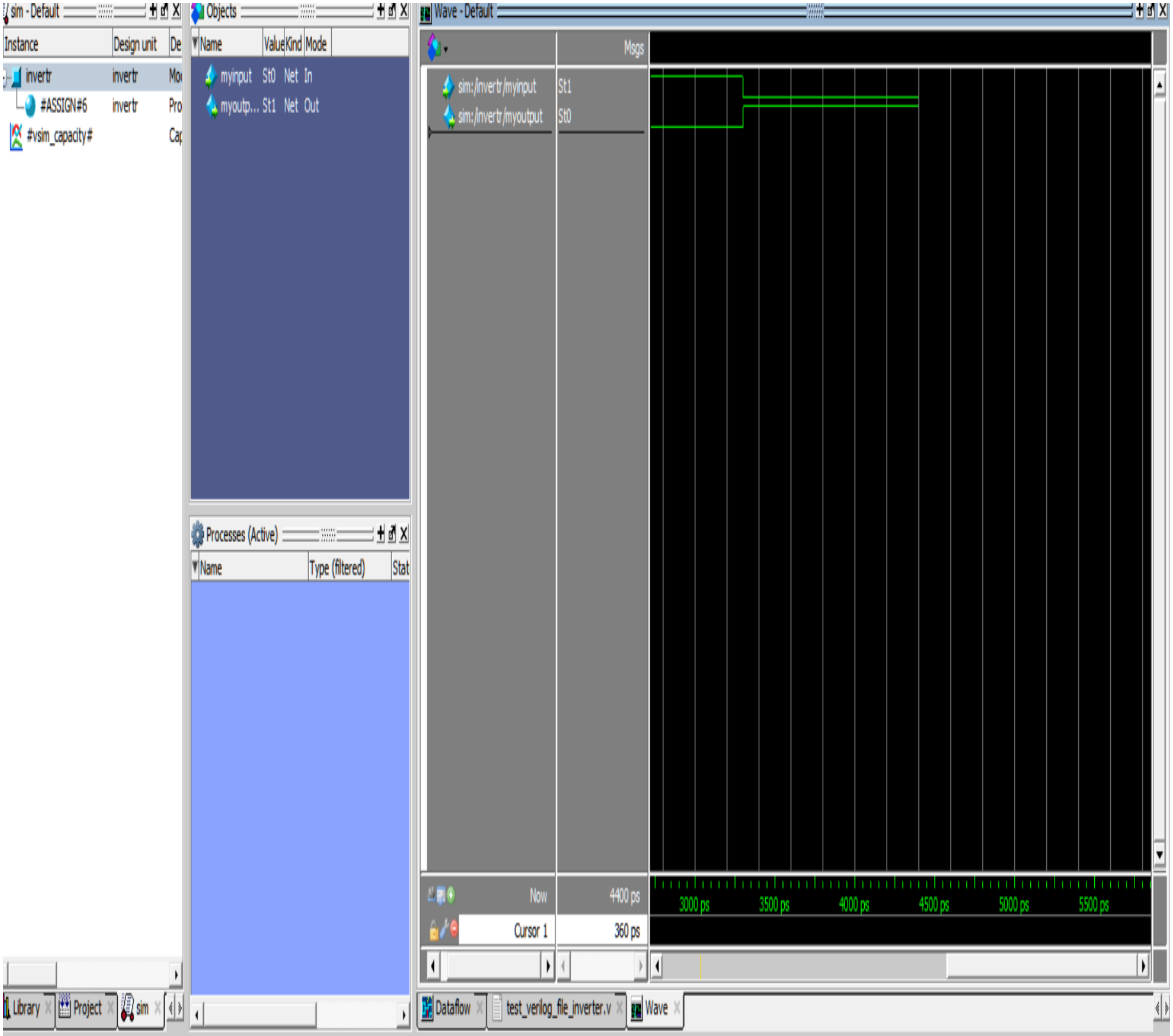
Bimal parajuli (20BDS0405)

Verilog Simulation of a basic Inverter:


C:\altera\13.0sp1\test_verilog_file_inverter.v (/invertr) - Default
Ln#
Now
Dataflow
test_verilog_file_inverter.v
Wave

```verilog
//model an inverter logic gate in modelsim

module invertr(myinput, myoutput);
  input myinput;
  output myoutput;
  assign myoutput = ~myinput;
  // if input is 1, output is 0
  // if input is 0, output is 1

endmodule

```

Bimal parajuli (20BDS0405)



Instance	Design unit	De
invertr	invertr	Mo
#ASSIGN#6	invertr	Pro
#vsim_capacity#		Ca

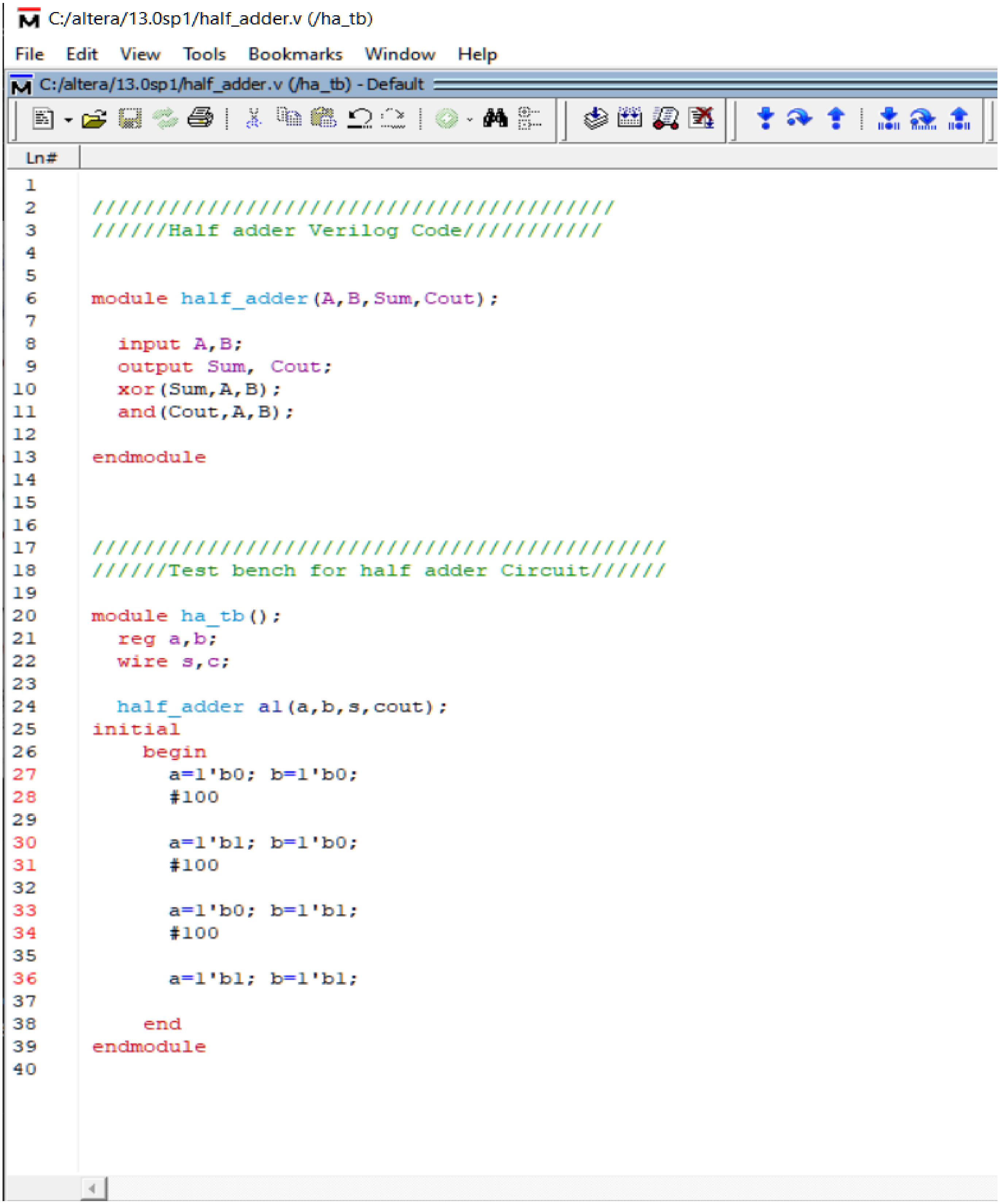
Name	Value	Kind	Mode
myinput	St0	Net	In
myoutp...	St1	Net	Out

Name	Type (filtered)	Stat

	Msgs
sim:/invertr/myinput	St1
sim:/invertr/myoutput	St0
Now	4400 ps
Cursor 1	360 ps

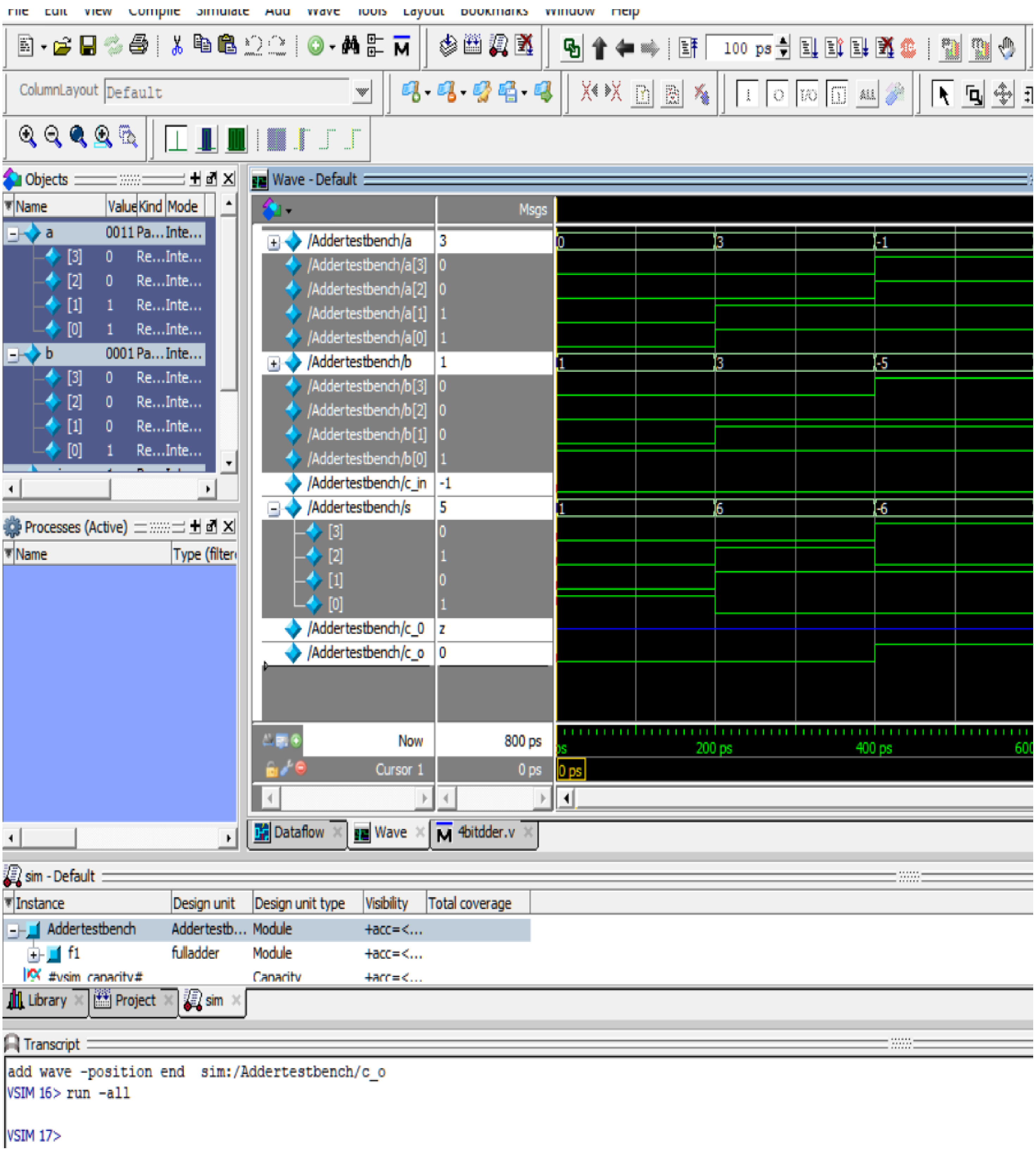
Bimal parajuli (20BDS0405)

Verilog Simulation of a half Adder:


C:/altera/13.0sp1/half_adder.v (/ha_tb)
File Edit View Tools Bookmarks Window Help
C:/altera/13.0sp1/half_adder.v (/ha_tb) - Default
Ln#

```

/////////////////////////////////////////
//////Half adder Verilog Code///////////


module half_adder(A,B,Sum,Cout);

  input A,B;
  output Sum, Cout;
  xor(Sum,A,B);
  and(Cout,A,B);

endmodule



/////////////////////////////////////////////
//////Test bench for half adder Circuit//////

module ha_tb();
  reg a,b;
  wire s,c;

  half_adder a1(a,b,s,cout);
initial
    begin
      a=1'b0; b=1'b0;
      #100

      a=1'b1; b=1'b0;
      #100

      a=1'b0; b=1'b1;
      #100

      a=1'b1; b=1'b1;

    end
endmodule

```

Bimal parajuli (20BDS0405)



Name	Value	Kind	Mode
a	0011	Pa...	Inte...
[3]	0	Re...	Inte...
[2]	0	Re...	Inte...
[1]	1	Re...	Inte...
[0]	1	Re...	Inte...
b	0001	Pa...	Inte...
[3]	0	Re...	Inte...
[2]	0	Re...	Inte...
[1]	0	Re...	Inte...
[0]	1	Re...	Inte...

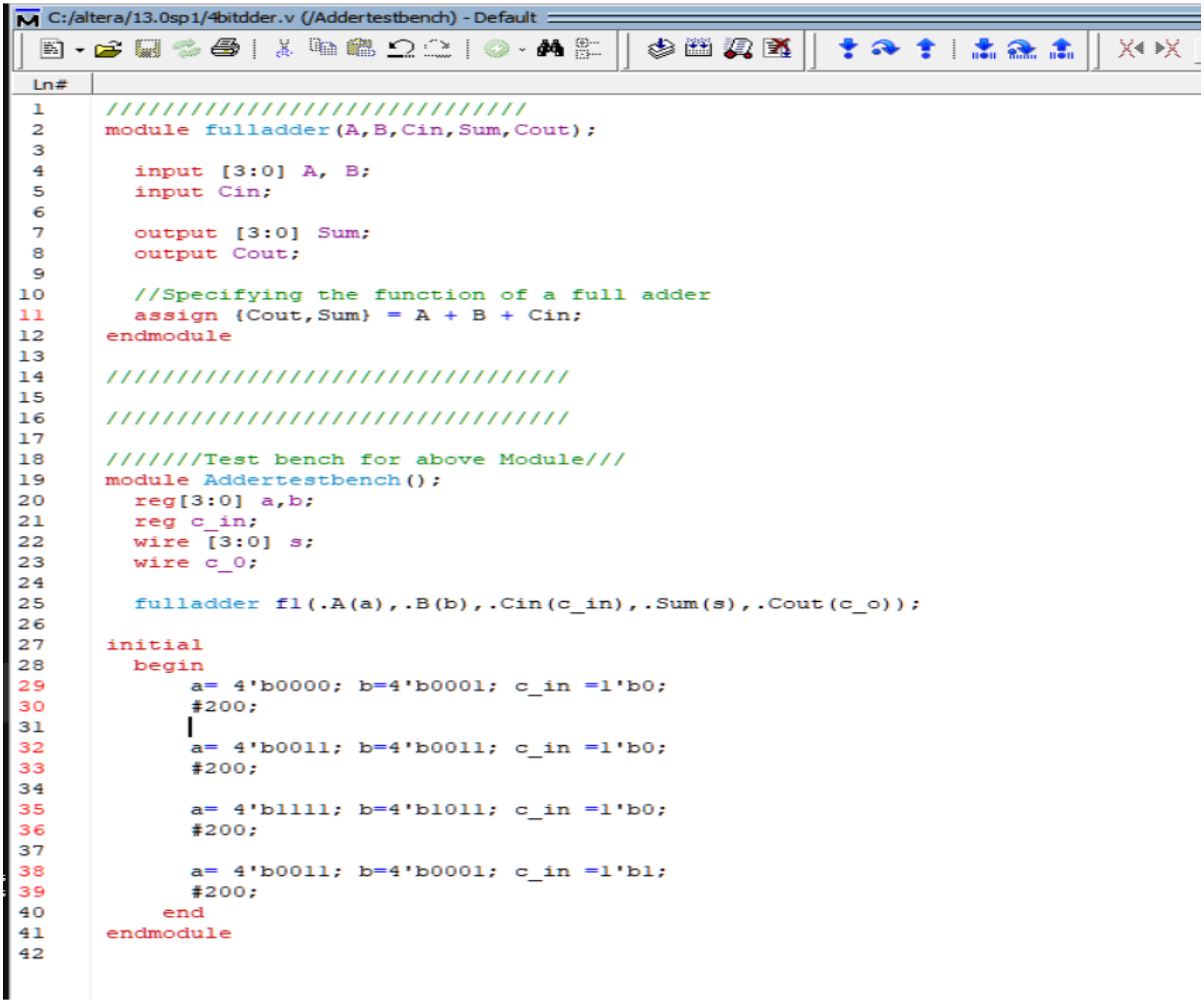
	Msgs
/Addertestbench/a	3
/Addertestbench/a[3]	0
/Addertestbench/a[2]	0
/Addertestbench/a[1]	1
/Addertestbench/a[0]	1
/Addertestbench/b	1
/Addertestbench/b[3]	0
/Addertestbench/b[2]	0
/Addertestbench/b[1]	0
/Addertestbench/b[0]	1
/Addertestbench/c_in	-1
/Addertestbench/s	5
[3]	0
[2]	1
[1]	0
[0]	1
/Addertestbench/c_0	z
/Addertestbench/c_o	0
Now	800 ps
Cursor 1	0 ps

Instance	Design unit	Design unit type	Visibility	Total coverage
Addertestbench	Addertestb...	Module	+acc=<...	
f1	fulladder	Module	+acc=<...	
#vsim_capacity#		Capacity	+acc=<...	

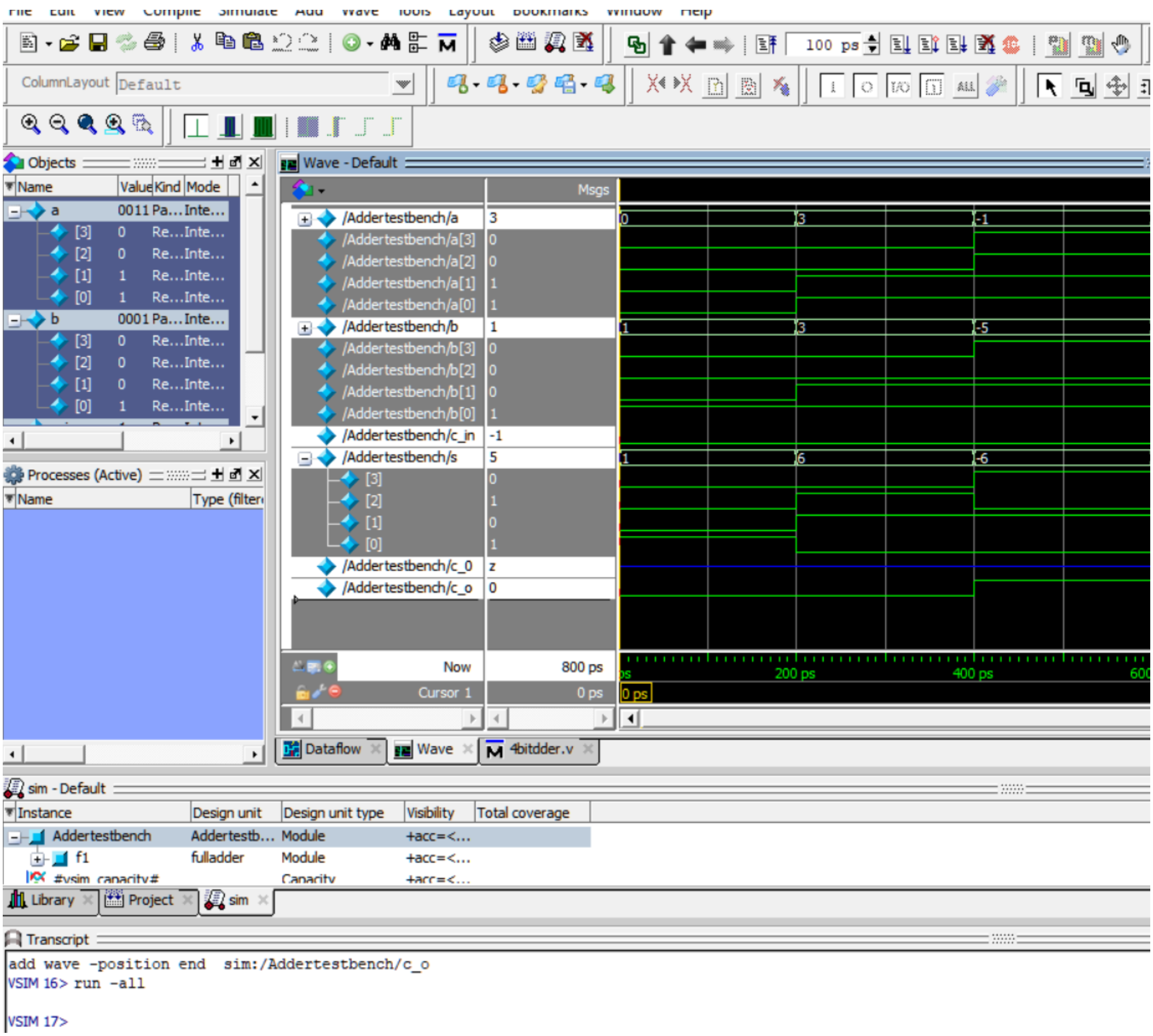
```
add wave -position end  sim:/Addertestbench/c_o
VSIM 16> run -all

VSIM 17>
```

Bimal parajuli (20BDS0405)

Verilog Simulation of a Full Adder:



```verilog
//////////////////////////////
module fulladder(A,B,Cin,Sum,Cout);

  input [3:0] A, B;
  input Cin;

  output [3:0] Sum;
  output Cout;

  //Specifying the function of a full adder
  assign {Cout,Sum} = A + B + Cin;
endmodule

/////////////////////////////////

/////////////////////////////////

///////Test bench for above Module///
module Addertestbench();
  reg[3:0] a,b;
  reg c_in;
  wire [3:0] s;
  wire c_0;

  fulladder f1(.A(a),.B(b),.Cin(c_in),.Sum(s),.Cout(c_o));

initial
  begin
      a= 4'b0000; b=4'b0001; c_in =1'b0;
      #200;

      a= 4'b0011; b=4'b0011; c_in =1'b0;
      #200;

      a= 4'b1111; b=4'b1011; c_in =1'b0;
      #200;

      a= 4'b0011; b=4'b0001; c_in =1'b1;
      #200;
    end
endmodule

```



Name	Value	Kind	Mode
a	0011	Pa...	Inte...
[3]	0	Re...	Inte...
[2]	0	Re...	Inte...
[1]	1	Re...	Inte...
[0]	1	Re...	Inte...
b	0001	Pa...	Inte...
[3]	0	Re...	Inte...
[2]	0	Re...	Inte...
[1]	0	Re...	Inte...
[0]	1	Re...	Inte...

Name	Type (filter

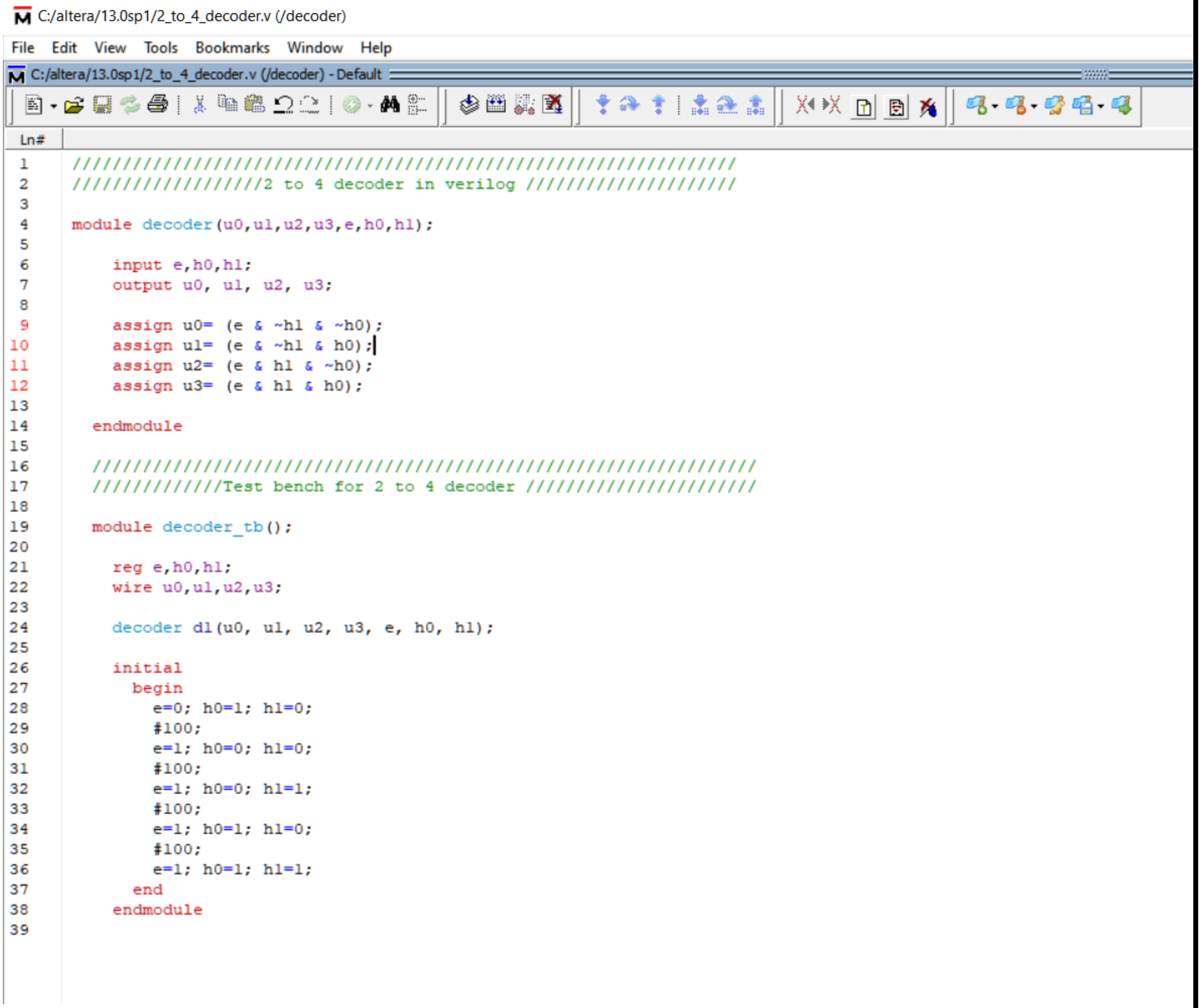
	Msgs
/Addertestbench/a	3
/Addertestbench/a[3]	0
/Addertestbench/a[2]	0
/Addertestbench/a[1]	1
/Addertestbench/a[0]	1
/Addertestbench/b	1
/Addertestbench/b[3]	0
/Addertestbench/b[2]	0
/Addertestbench/b[1]	0
/Addertestbench/b[0]	1
/Addertestbench/c_in	-1
/Addertestbench/s	5
[3]	0
[2]	1
[1]	0
[0]	1
/Addertestbench/c_0	z
/Addertestbench/c_o	0
Now	800 ps
Cursor 1	0 ps

Instance	Design unit	Design unit type	Visibility	Total coverage
Addertestbench	Addertestb...	Module	+acc=<...	
f1	fulladder	Module	+acc=<...	
#vsim_capacity#		Capacity	+acc=<...	

```
add wave -position end  sim:/Addertestbench/c_o
VSIM 16> run -all

VSIM 17>
```

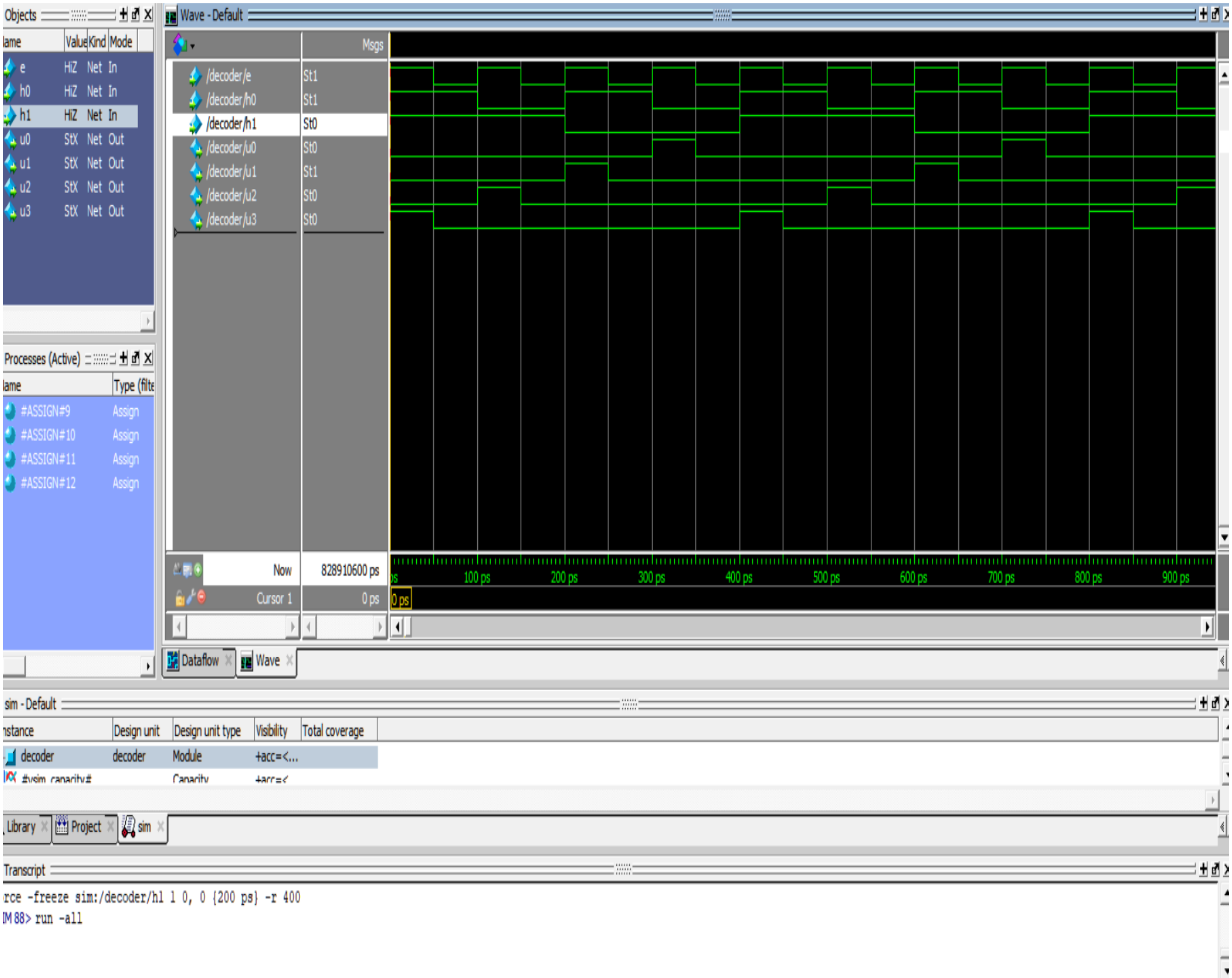
Bimal parajuli (20BDS0405)

Verilog Simulation of a 2 to 4 decoder:


C:/altera/13.0sp1/2_to_4_decoder.v (/decoder)
File Edit View Tools Bookmarks Window Help
C:/altera/13.0sp1/2_to_4_decoder.v (/decoder) - Default
Ln#

```
/////////////////////////////////////////////////////////////////////
///////////////////2 to 4 decoder in verilog ////////////////////

module decoder(u0,u1,u2,u3,e,h0,h1);

    input e,h0,h1;
    output u0, u1, u2, u3;

    assign u0= (e & ~h1 & ~h0);
    assign u1= (e & ~h1 & h0);
    assign u2= (e & h1 & ~h0);
    assign u3= (e & h1 & h0);

  endmodule

  /////////////////////////////////////////////////////////////////////
  /////////////Test bench for 2 to 4 decoder //////////////////////

  module decoder_tb();

    reg e,h0,h1;
    wire u0,u1,u2,u3;

    decoder d1(u0, u1, u2, u3, e, h0, h1);

    initial
      begin
        e=0; h0=1; h1=0;
        #100;
        e=1; h0=0; h1=0;
        #100;
        e=1; h0=0; h1=1;
        #100;
        e=1; h0=1; h1=0;
        #100;
        e=1; h0=1; h1=1;
      end
    endmodule
```

Bimal parajuli (20BDS0405)



lame	Value	Kind	Mode
e	HiZ	Net	In
h0	HiZ	Net	In
h1	HiZ	Net	In
u0	StX	Net	Out
u1	StX	Net	Out
u2	StX	Net	Out
u3	StX	Net	Out

lame	Type (filte
#ASSIGN#9	Assign
#ASSIGN#10	Assign
#ASSIGN#11	Assign
#ASSIGN#12	Assign

	Msgs
/decoder/e	St1
/decoder/h0	St1
/decoder/h1	St0
/decoder/u0	St0
/decoder/u1	St1
/decoder/u2	St0
/decoder/u3	St0
Now	828910600 ps
Cursor 1	0 ps

nstance	Design unit	Design unit type	Visibility	Total coverage
decoder	decoder	Module	+acc=<...	
#vsim_capacity#		Capacity	+acc=<	

```
rce -freeze sim:/decoder/h1 1 0, 0 {200 ps} -r 400
IM 88> run -all
```