



# Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

## Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
- Computational Fluid Dynamics

# PCB Design and Analysis Learning Map

Beginner

Advanced




Beginner



Advanced

## Logic Design



Allegro® Design Entry HDL Front-to-Back Flow   



Allegro Design Entry HDL Basics  

Allegro System Capture   


Allegro System Architect  




Allegro Design Reuse  



Allegro AMS Simulator  



Allegro AMS Simulator Advanced Analysis  

Allegro Design Entry Using OrCAD® Capture  



OrCAD CIS 

OrCAD Capture Constraint Manager PCB Flow   




Allegro EDM Design Entry HDL Front-to-Back Flow  

Allegro Team Design Authoring  



Analog Simulation with PSpice®  

Analog Simulation with PSpice Advanced Analysis  




## PCB Design




Allegro PCB Editor Basic Techniques   

Allegro PCB Editor Intermediate Techniques   

Allegro PCB Router Basics  


Allegro PCB Editor Advanced Methodologies   


Allegro High-Speed Constraint Management   



Allegro Update Training   



Advanced Design Verification with the RAVEL Programming Language  



## SI/PI Analysis





Essential High-Speed PCB Design for Signal Integrity 



PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials 



Allegro Sigrity™ SI Foundations  




Allegro Sigrity PI  



Sigrity PowerDC™ and OptimizePI™  

Sigrity Aurora    



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis  




Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM  



Clarity 3D Solver   




Celsius Thermal Solver  

## Library Development

Allegro PCB Librarian   

Allegro EDM PCB Librarian   

Allegro Design Entry HDL SKILL® Programming Language  

Allegro PCB Editor SKILL Programming Language   

# IC Package Design and Analysis Learning Map

Beginner



Advanced

## IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language **NEW**



Allegro Package Designer Plus **NEW**



## SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Clarity 3D Solver **NEW**



Celsius Thermal Solver **NEW**



Beginner



Advanced



New Course



Number of days for instructor-led course

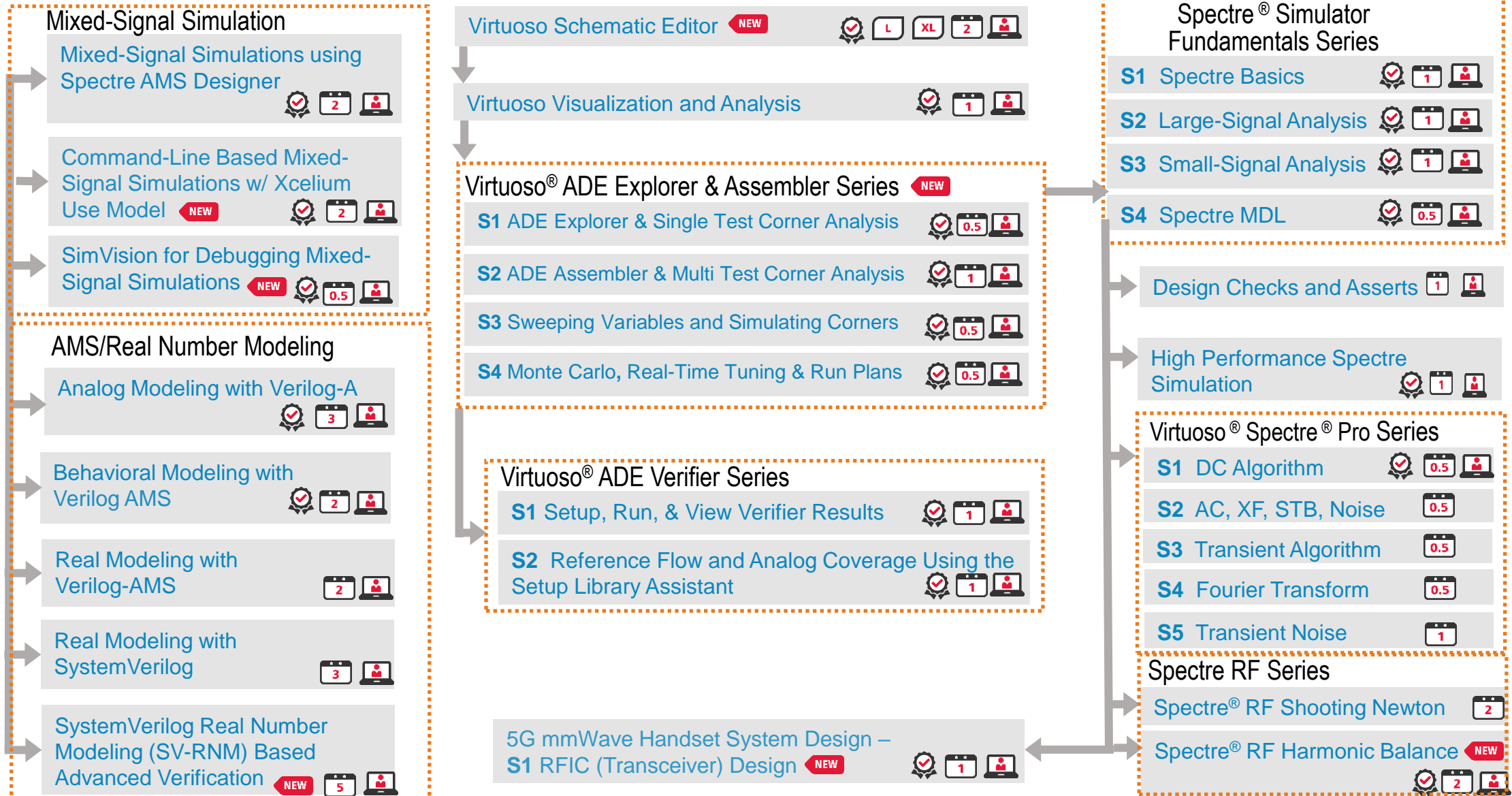


Tiers of Cadence products used in course



Online Course Available

## Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

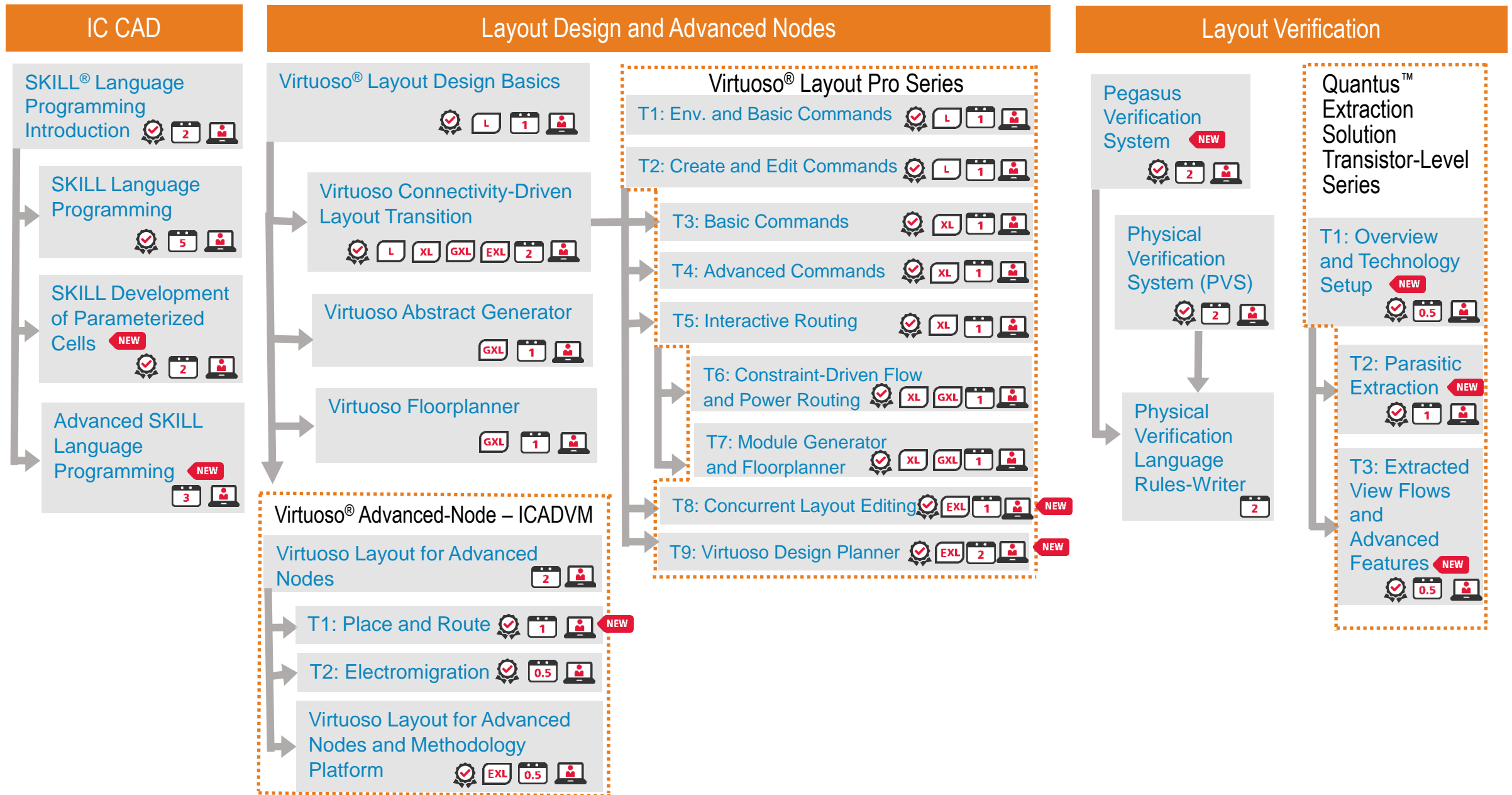


Beginner

Advanced

Beginner

Advanced



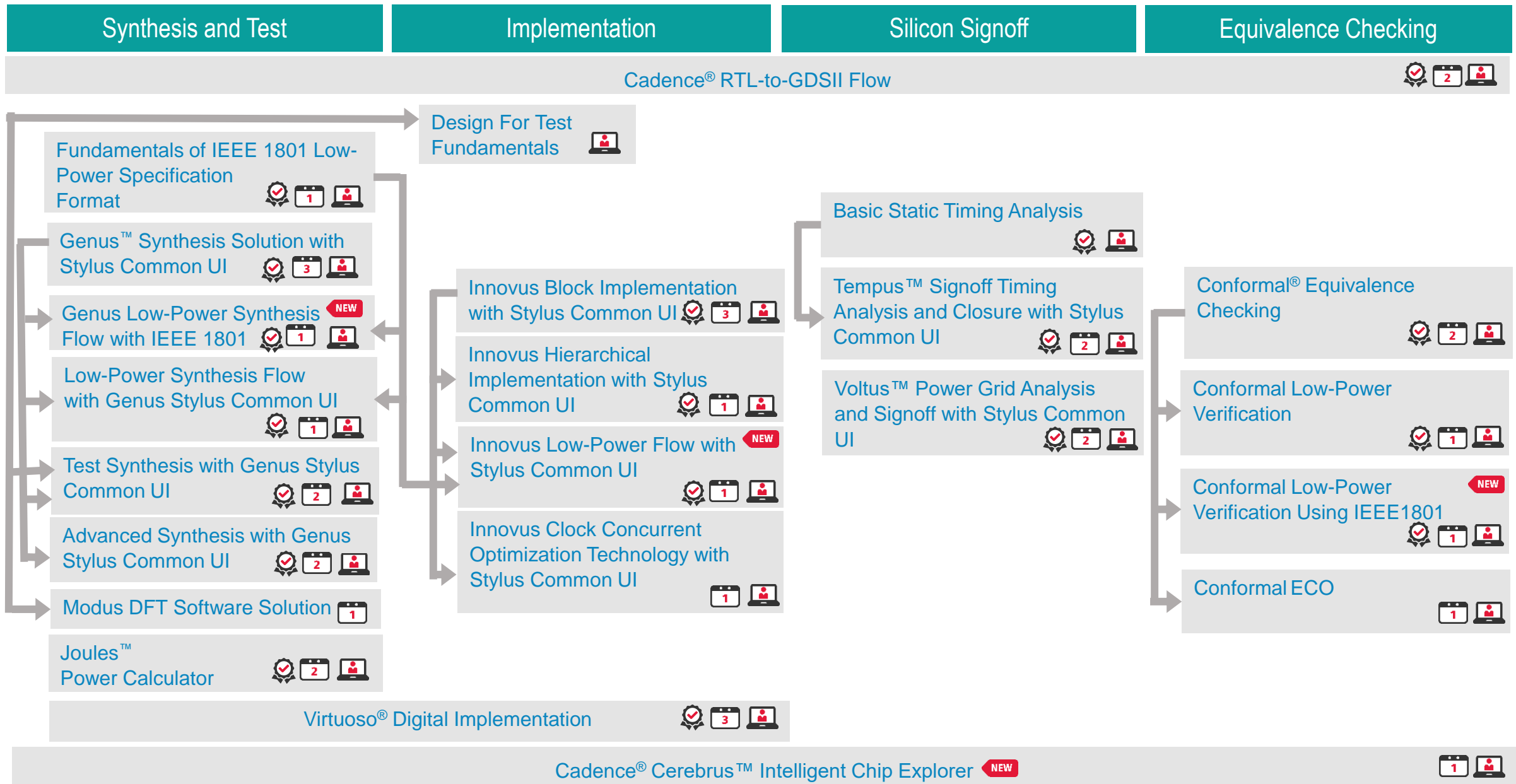
# Digital Design and Signoff Learning Map

Beginner

Advanced

Beginner

Advanced



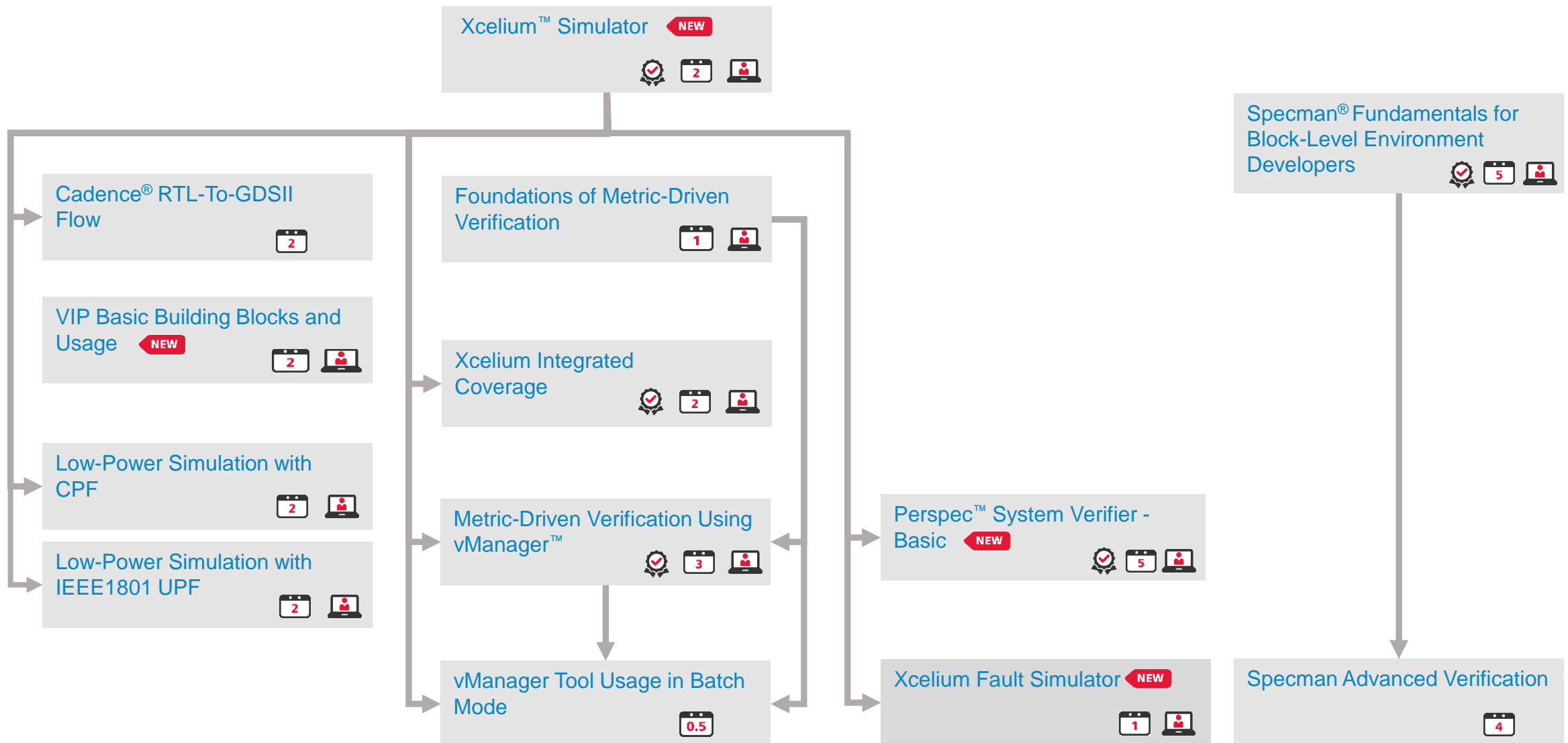


# System Design and Verification Learning Map

Beginner

Advanced

## Simulation, Coverage and Debug



Beginner

Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available



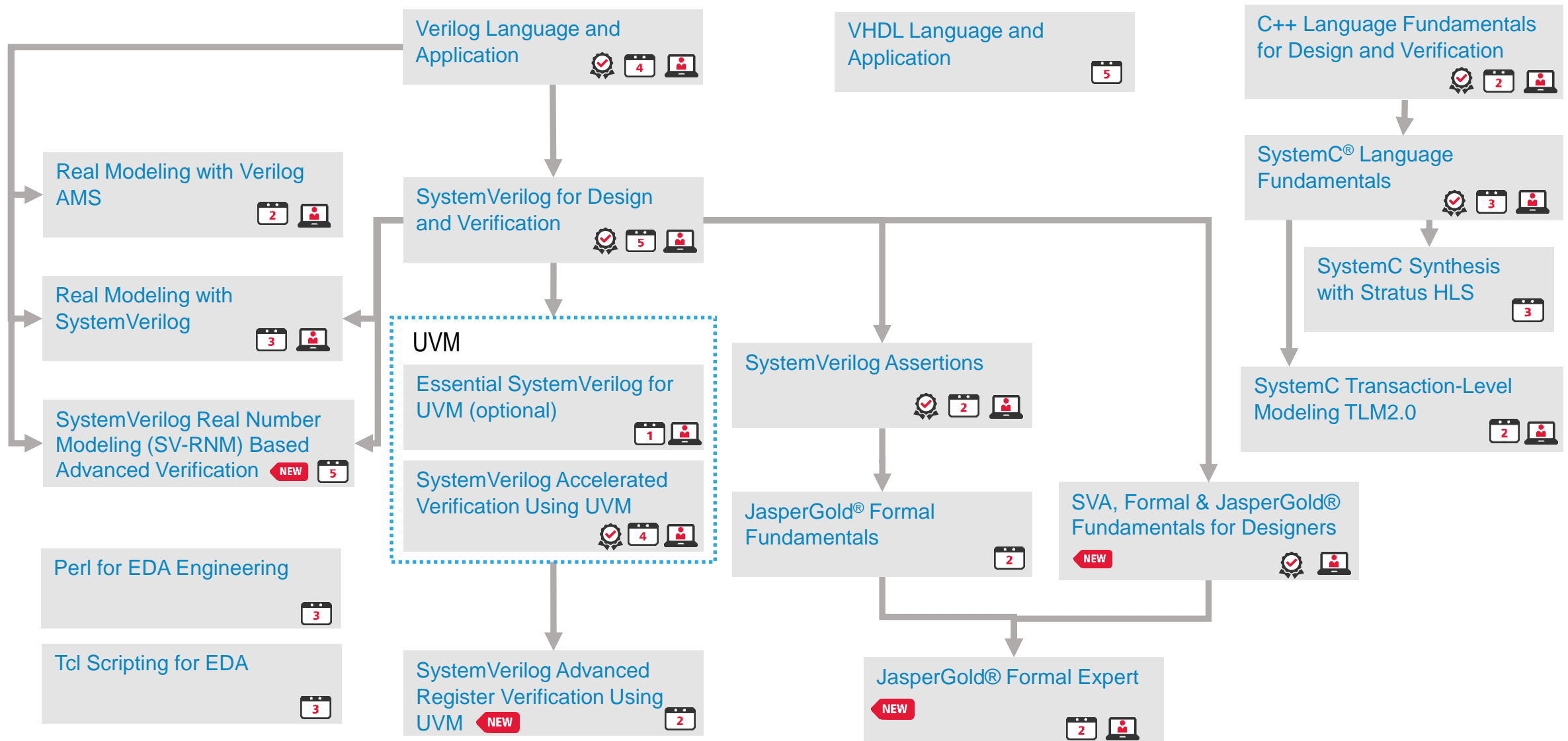
Digital Badge Available

© 2020 Cadence Design Systems, Inc.

# System Design and Verification Learning Map

Beginner

## Design and Verification Languages



Beginner

Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available



Digital Badge Available

© 2020 Cadence Design Systems, Inc.



# Tensilica Processor IP Learning Map

1 of 2 – see next page



## Tensilica Xtensa LX

[Tensilica® Xtensa® LX Processor Fundamentals](#)



## ConnX DSP

[Tensilica ConnX BBE16EP Baseband Engine](#)



[Tensilica ConnX BBE32EP Baseband Engine](#)



[Tensilica ConnX BBE64EP Baseband Engine](#)



[Tensilica ConnX 110 and 120 DSP Family](#)



## Fusion & FloatingPoint DSP

[Tensilica Fusion F1 DSP](#)



[Tensilica Fusion G3 DSP](#)



[Tensilica Fusion G6 DSP](#)



[Tensilica FloatingPoint DSP Family](#)



## HiFi Audio DSP

[Tensilica Audio Codec API](#)



[Tensilica HiFi 2/EP/Mini Audio Engine ISA](#)



[Tensilica HiFi 3 Audio Engine ISA](#)



[Tensilica HiFi 4 DSP](#)



[Tensilica HiFi 5 DSP](#)



[Tensilica Xtensa Audio Framework](#)



## Vision DSP

[Tensilica Vision DSP Family](#)



[Tensilica Xtensa Neural Network Compiler v2](#)



[Tensilica DNA 100 Architecture and Programming](#)



New Course



Number of days for instructor-led course



Online Course Available

## Tensilica Xtensa NX

## ConnX DSP

## Vision DSP

[Tensilica® Xtensa® NX  
Processor Fundamentals](#)



[Tensilica Xtensa NX  
Processor Interfaces](#)



[Tensilica Xtensa NX  
Hardware Verification and  
EDA](#)



[Tensilica Instruction  
Extension Language and  
Design](#)



[Tensilica System  
Modeling using XTSC](#)



[Tensilica ConnX B10  
DSP](#)

NEW



[Tensilica ConnX B20  
DSP](#)

NEW



[Tensilica Vision DSP Family](#)

NEW



[Tensilica Xtensa Neural  
Network Compiler v2](#)

NEW



# Computational Fluid Dynamics

Beginner

Advanced

Fidelity		
Turbomachinery	Meshing	Auto Aero

Fine
Marine

Fidelity Turbo: Introduction

3

Fidelity Automesh for  
Unstructured Meshing

1.5

Fidelity Flow

1.5

Fine Marine for Beginners

2.5

Fine Marine for Advanced Users

1.75

Beginner

Advanced

NEW

New Course



Number of days for instructor-led course

L

XL

GXL

Tiers of Cadence products used in course



Online Course Available

© 2020 Cadence Design Systems, Inc.



# cādence®

© 2020 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at [www.cadence.com/go/trademarks](http://www.cadence.com/go/trademarks) are trademarks or registered trademarks of Cadence Design Systems, Inc. Accellera and SystemC are trademarks of Accellera Systems Initiative Inc. All Arm products are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All MIPI specifications are registered trademarks or service marks owned by MIPI Alliance. All PCI-SIG specifications are registered trademarks or trademarks of PCI-SIG. All other trademarks are the property of their respective owners.