Department of Electronic and Telecommunication Engineering

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EN4603 - Digital IC Design

Laboratory Experiment 3
Place & Route

Laboratory Report

Submitted by

Submitted by

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Note:
All the materials related to the report can also be found at https://github.com/bimalka98/Digital-IC-Design

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List of Abbreviations

ASIC Application Specific Integrated Circuit

ATPG Automatic Test Pattern Generation

DEF Design Exchange Format

DFT Design For Testability

GPDK Generic Process Design Kit

HDL Hardware Description Language

IC Integrated Circuit

RTL Register-Transfer Level

RX Receiver

TCL Tool Command Language

TX Transmitter

UART Universal Asynchronous Receiver Transmitter

1 Introduction

1.1 Practical

In this practical, you will be using *Cadence Innovus* to place and route the design you synthesized in Laboratory Experiment 2. As inputs to Innovus, you will provide,

1. Source Verilog files
2. Technology libraries provided by the fabrication plant (here, 45 *nm* educational Generic Process Design Kit (GPDK) given by Cadence) : `(.lib, .lef, .tch)`
    - Library Timing (.lib) files specify timing (cell delay, cell transition time, setup and hold time requirement) and power characteristics of standard cells. Slow and fast libraries characterize standard cells with maximum and minimum signal delays, which could occur from process variations.
    - Tch files are binary files that accurately characterize library elements, that include capacitance and resistance.
    - Library Exchange Format (LEF) specify design rules, metal capacitances, layer information. . . etc.
3. Multi Mode Multi Corner file (.view)
4. Constraints file (.sdc)
5. Scan DEF file (.scandef)

and will obtain the GDSII file as output, which is an industry standard format for exchanging Integrated Circuit (IC) layout data. You will then analyze, compare, and comment on the placement, cell count, congestion etc. of the design at various stages of the place and route design flow.

1.2 Place & Route

Place & route is the final step in the IC design flow before fabrication. As the name implies, this step comprises of two main tasks – placement and routing.

In placement, the IC designer decides where to place all the elements of the design. In addition to placing cells, this step involves making initial decisions about the aspect ratio and utilization factors (core utilization / cell utilization).

Then, in the routing step, the designer makes the physical interconnects between the placed elements. This step comprises of three main stages: (1) Power Routing: routing of VDD and GND nets, (2) Clock Tree Synthesis: re-synthesizing of clock nets based on cell placement in order to balance clock skew throughout the design and minimize insertion delay, and (3) Signal Routing: routing of all other nets.

The general design flow for place & Route, which we will be following in this laboratory experiment, is shown in Figure 1.

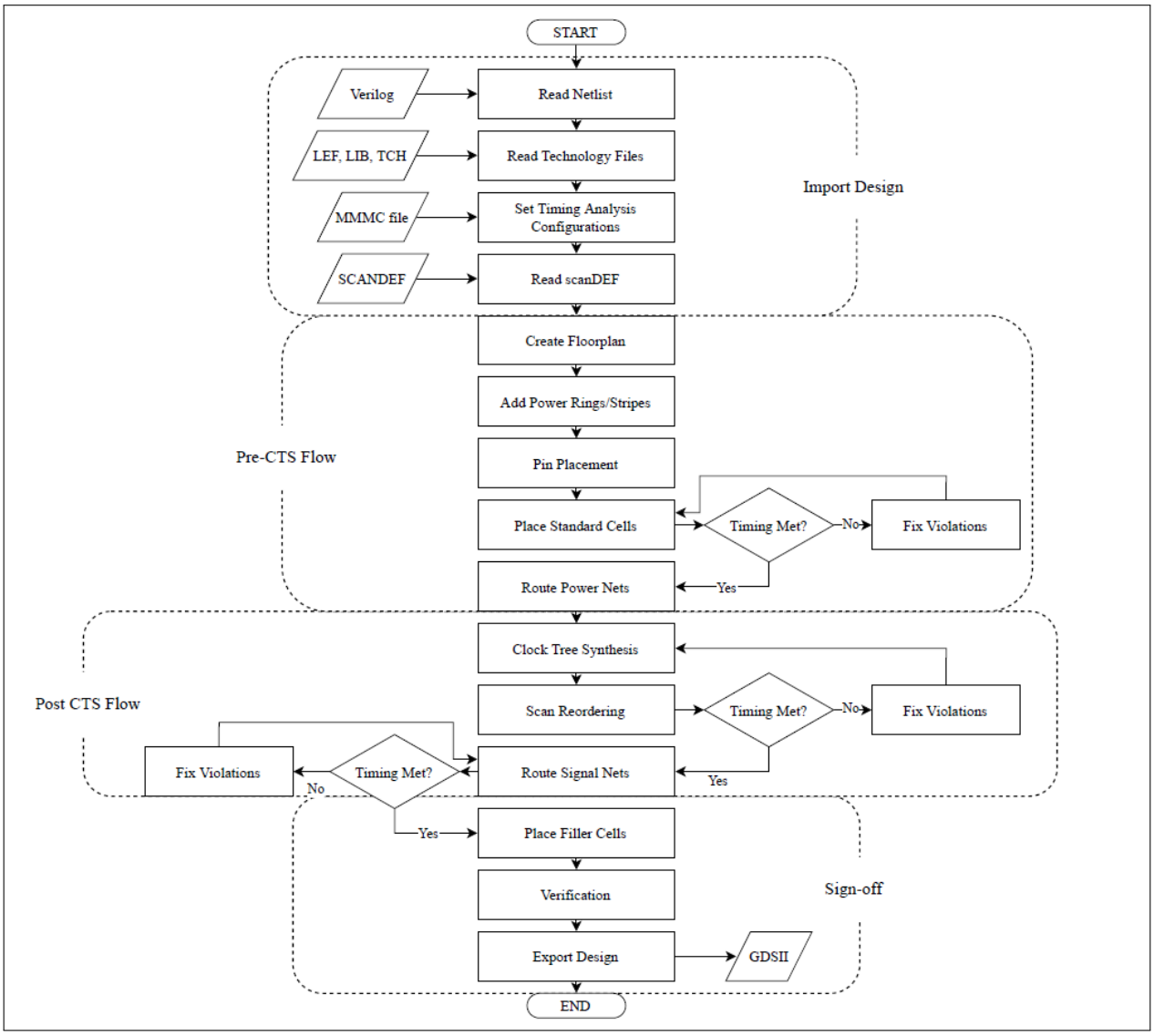

Figure 1: The general design flow for place & Route

2 Using Innovus for Place and Route

This section demonstrates the steps carried out at the 'Step 3' in the Laboratory guide, with necessary illustrations.

1.) Import the Design: this step loads the design according to the netlist, technology libraries, labels for power nets and the timing analysis configurations. Once the design is loaded an empty core in the design area of Innovus can be observed as shown in the Figure 2, and it displays "In Memory" in the bottom right corner of Innovus.

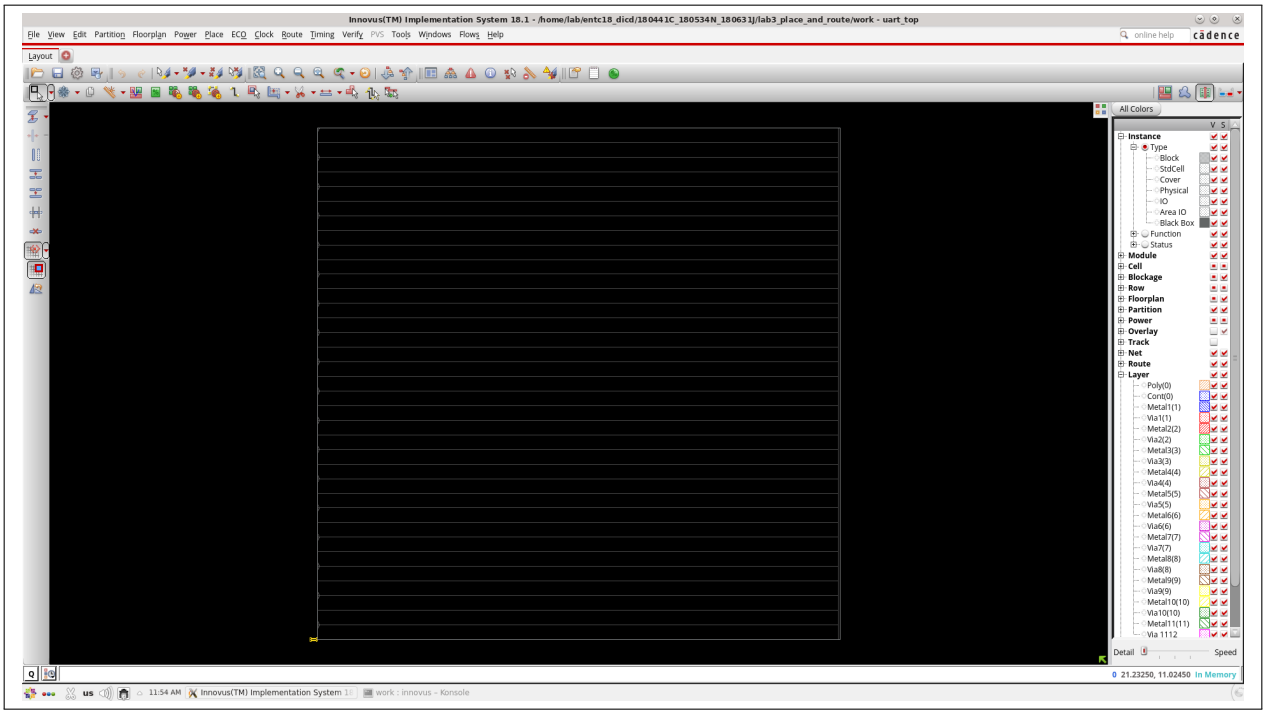

Figure 2: Empty core in the design area of Innovus, when the design is loaded

2.) Read the scanDEF file: this file specifies the scan chains available in the design and to perform scan reordering later.

```
<CMD> defIn ../input/uart_top_2_scanDEF.scandef
Reading DEF file '../input/uart_top_2_scanDEF.scandef', current time is Thu Jan 19 11:55:00 2023 ...
--- CASESENSITIVE ON
--- DIVIDERCHAR '/'
DEF file '../input/uart_top_2_scanDEF.scandef' is parsed, current time is Thu Jan 19 11:55:00 2023.
```

Figure 3: Innovus log for reading the scanDEF file

3.) Set the design mode to 45nm process

```
<CMD> setDesignMode -process 45
Applying the recommended capacitance filtering threshold values for 45nm process node: total_c_th=0, relative_c_th=1 and coupling_c_th=0.1.
        These values will be used by all post-route extraction engines, including TQuantus, IQuantus and Quantus QRC extraction.
        Capacitance filtering mode(-capFilterMode option of the setExtractRCMode) is 'relAndCoup' for all engines.
        The accuracy mode for postRoute effortLevel low extraction will be set to 'high'.
        Default value for EffortLevel(-effortLevel option of the setExtractRCMode) in postRoute extraction mode is 'medium'.
Updating process node dependent CCOpt properties for the 45nm process node.
```

Figure 4: Innovus log for setting the design mode to 45nm process

Bibliography