Department of Electronic and Telecommunication Engineering

University of Moratuwa, Sri Lanka

EN4603 - Digital IC Design

Laboratory Experiment 3
Place & Route

Laboratory Report

Submitted by

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Note:
All the materials related to the report can also be found at https://github.com/bimalka98/Digital-IC-Design

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List of Abbreviations

ASIC Application Specific Integrated Circuit

ATPG Automatic Test Pattern Generation

DEF Design Exchange Format

DFT Design For Testability

GPDK Generic Process Design Kit

HDL Hardware Description Language

IC Integrated Circuit

RTL Register-Transfer Level

RX Receiver

TCL Tool Command Language

TX Transmitter

UART Universal Asynchronous Receiver Transmitter

1 Introduction

1.1 Practical

In this practical, you will be using *Cadence Innovus* to place and route the design you synthesized in Laboratory Experiment 2. As inputs to Innovus, you will provide,

1. Source Verilog files
2. Technology libraries provided by the fabrication plant (here, 45 *nm* educational Generic Process Design Kit (GPDK) given by Cadence) : `(.lib, .lef, .tch)`
    - Library Timing (.lib) files specify timing (cell delay, cell transition time, setup and hold time requirement) and power characteristics of standard cells. Slow and fast libraries characterize standard cells with maximum and minimum signal delays, which could occur from process variations.
    - Tch files are binary files that accurately characterize library elements, that include capacitance and resistance.
    - Library Exchange Format (LEF) specify design rules, metal capacitances, layer information. . . etc.
3. Multi Mode Multi Corner file (.view)
4. Constraints file (.sdc)
5. Scan Design Exchange Format (DEF) file (.scandef)

and will obtain the GDSII file as output, which is an industry standard format for exchanging Integrated Circuit (IC) layout data. You will then analyze, compare, and comment on the placement, cell count, congestion etc. of the design at various stages of the place and route design flow.

Bibliography