Department of Electronic & Telecommunication Engineering
University of Moratuwa

B.Sc. Eng. Semester 7

EN 4603 – Digital IC Design

Laboratory Experiment 3: Place & Route

Objectives:

a) To understand and follow the place & route design flow
b) To familiarize with Cadence Innovus for place & route

Software Required: Cadence Innovus - Ver. 18.10

In this practical, you will be using Cadence Innovus to place and route the design you synthesized in Laboratory Experiment 2. As inputs to Innovus, you will provide

1. Source Verilog files (.v)
2. Technology libraries provided by the fabrication plant – here, 45 nm educational GPDK given by cadence (.lib, .lef, .tch)
3. Multi Mode Multi Corner file (.view)
4. Constraints file (.sdc)
5. ScanDEF file (.scandef)

and will obtain the GDSII file as output, which is an industry standard format for exchanging IC layout data. You will then analyze, compare, and comment on the placement, cell count, congestion etc. of the design at various stages of the place and route design flow.

Note: Unix commands are given as **`unix:`** and Innovus commands are given as **`Innovus:`**

Lab report:

You need to submit a small report, answering the questions in the exercise with screenshots and explanations. The format of the report is not a concern. You need to demonstrate that you understand every step of the process. Ask the junior staff for any clarifications.

Place & Route

Place & route is the final step in the IC design flow before fabrication. As the name implies, this step comprises of two main tasks – placement and routing.

In placement, the IC designer decides where to place all the elements of the design. In addition to placing cells, this step involves making initial decisions about the aspect ratio and utilization factors (core utilization / cell utilization).

Then, in the routing step, the designer makes the physical interconnects between the placed elements. This step comprises of three main stages – (1) Power Routing: routing of VDD and GND nets, (2) Clock Tree Synthesis: resynthesizing of clock nets based on cell placement in order to balance clock skew throughout the design and minimize insertion delay, and (3) Signal Routing: routing of all other nets.

The general design flow for place & route, which we will be following in this laboratory experiment, is shown in figure 1.

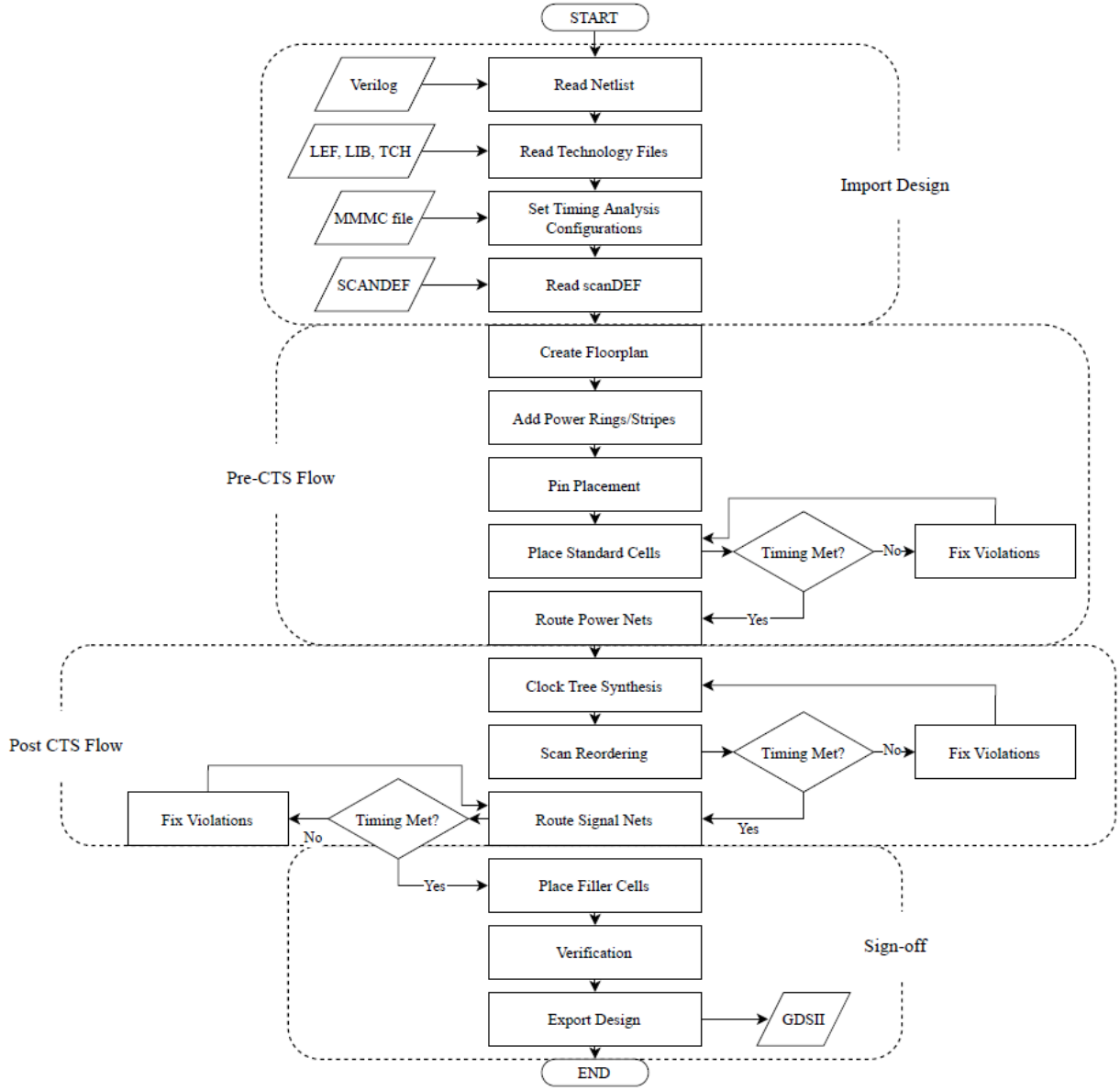

Figure 1: Place & route design flow

Step 1: Setup the Project Directories

1. Launch Terminal: In the start menu (application launcher) search and open: *Konsole*

2. Check if you are in the right directory:
   ```
   unix: pwd
   ```
   You should get **/home/student/**
3. Navigate to your directory:
   ```
   unix: cd entc17_dicd/<index_no>
   ```

4. Copy the lab files & examine the folder structure
   ```
   unix: cp -r ../../dicd_labs/lab3_place_and_route ./
   unix: cd lab3_place_and_route
   ```

lab3_place_and_route:

|--input/	# Contains input files (.v, .sdc,.scandef, .view)
|--libs/	# Contains technology libraries (45nm GPDK)
|--log/	# Stores generated log files
|--output/	# Output files
|--report/	# Generated reports
|--pre_CTS	
|--post_CTS	
|--post_Route	
|**--work/**	# This is the working directory of the project

5. Change directory to **`work`**

NOTE: Follow the instructions in **xlaunch_guide.pdf** and setup your xlaunch configuration file before proceeding any further.

Step 3: Using Innovus for Place and Route

1. Start Innovus by double-clicking **`innovus.xlaunch.`** This will open the Innovus window and terminal on your local desktop.

2. Import the Design – Go to **`File > Import Design`** and you will be presented a window as shown in figure 2. to specify the netlist, technology libraries, floorplan (if available), labels for power nets and the analysis configuration.

   - Netlist:
     - Select Verilog option
     - Browse and select **`../input/uart_top_2.v`** as the Verilog file
     - Set Top Cell to auto assign

   - Technology Libraries
     - Select LEF Files option
     - Browse and select the LEF files in **`../input/libs/gsclib045/lef/`** and add them in the following order (see figure 3):
       `1) *_tech.lef`
       `2) *_multibitsDFF.lef`
       `3) *_macro.lef`

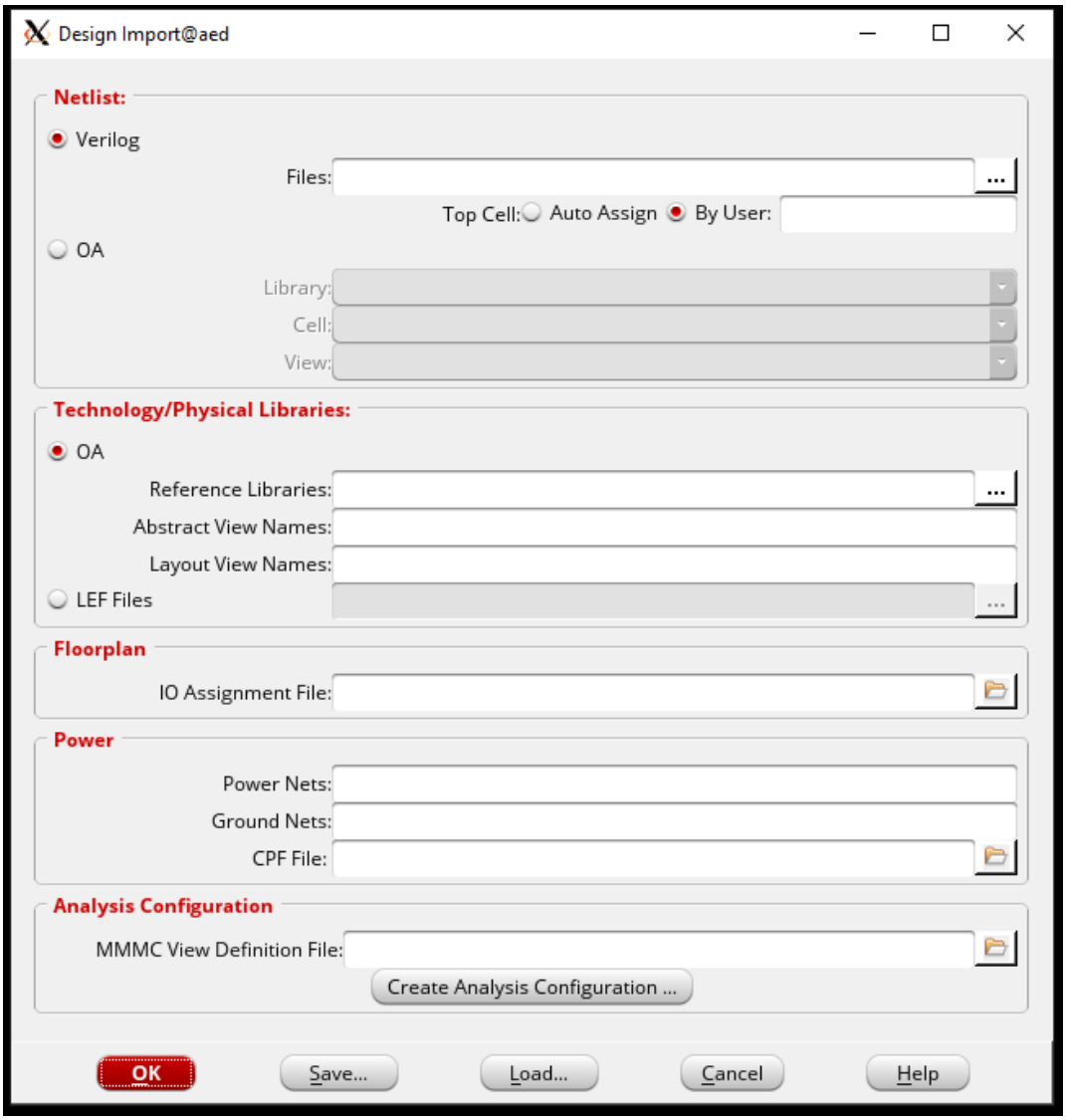

Figure 2: Import Design window

Figure 3: Adding LEF files in the correct order

- Floorplan
  - We will not be specifying a floorplan as we do not have a floorplan when we initially begin the layout design

- Power
  - Specify the label for power nets as **`VDD`**
  - Specify the label for ground nets as **`GND`**
  - Leave the CPF field empty

  Note: Common Power Format (CPF) files are used to specify power saving techniques in the design such as clock gating, multi-voltage logic and dynamic power management.

- Analysis Configuration
  - Browse and select **`../input/uart_top.view`** as the MMMC view definition file. The view definition file contains timing analysis configurations (SDC file of the design, slow/fast cell libraries, delay corners) for clock tree synthesis, setup time analysis and hold time analysis.

- Click Save to save the import configuration so that it can be easily loaded back later (if necessary)
- Click OK to load the design according to the given configuration. You should now see the empty core in the design area of Innovus and it should display "In Memory" in the bottom right corner of Innovus.

3. Read the scanDEF file. We will need this file to specify the scan chains available in the design and to perform scan reordering later.
   `Innovus: defIn ../input/uart_top_2_scanDEF.scandef`

4. Set the design mode to 45nm process
   `Innovus: setDesignMode -process 45`

5. Specify floorplan – Go to **`Floorplan > Specify Floorplan`**
   - Select specify by size
   - Select Core Size
   - Select Aspect Ratio
   - Set the aspect ratio as **1.0** (this will adjust to the closest workable value)
   - Set Core Utilization as **0.4** (this will adjust to the closest workable value)

     Note: The core utilization value determines the percentage of core area available for standard cell and macro placement. Here we set core utilization factor to 0.4 because we need to reduce routing congestions and reserve area for additional cell placements which may occur during clock tree synthesis and design optimization.
   - Set core margins by core to IO boundary. Set a margin of **5 Microns to all sides** from the core. (this will adjust to the closest workable value)
   - Leave the rest of the parameters to their default values and click OK

   You should now see a floorplan similar to figure 4 on the Innovus design area.

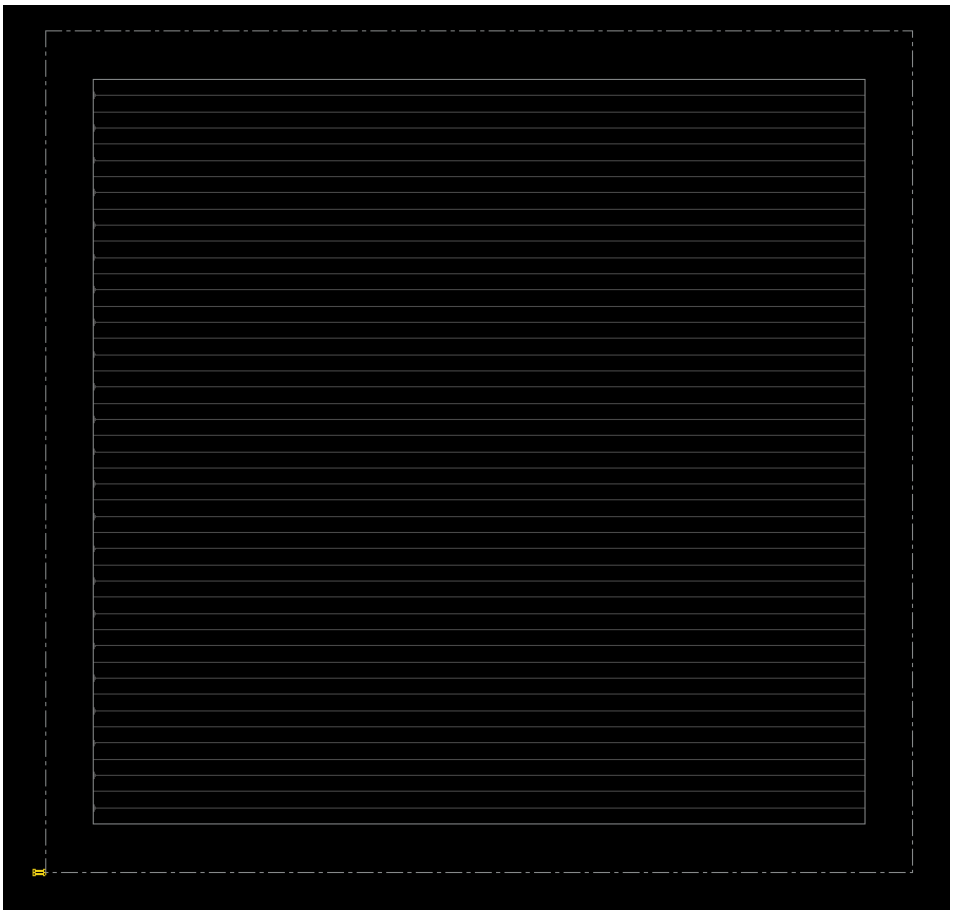

Figure 4: Floorplan

Tip: To zoom into an area of the design, select the interested area by clicking and holding the right mouse button and release. To re-fit the design in the design area, go to **`View > Fit`** or press F.

6. Add power rings and power stripes

Note: We will use Metal 7 for horizontal power rings/stripes and Metal 8 for vertical power rings/stripes

- Power Rings – Go to **`Power Planning > add Rings`**
  - In the Net(s) field enter: **`VDD GND`**
  - Set the Ring Type as Core rings contouring around the core boundary
  - Ring Configuration
    - Width: **1.0**
    - Spacing (spacing between rings): **0.8**
    - Offset (offset from core boundary): **0.8**
  - Click OK

  You should now see the power rings placed on your design

- Power Stripes – Go to **`Power Planning > add Stripes`**
  Adding horizontal stripes
  - In the Net(s) field enter: **`VDD GND`**

- Layer: **Metal 7**
- Direction: **Horizontal**
- Width: **1.0**
- Spacing: **0.8**
- In Set Pattern, select **Number of sets** and set it to **3**
- Set strip boundary to **core ring**
- Set the starting point of the first stipe and the ending point of the last stipe in First/Last Stripe section as follows
    - Select start from bottom
    - Relative from core or selected area
        - Start: **15**
        - End: **15**
- Click OK.

You should now see the horizontal power stripes placed on your design

- Similarly, add the **vertical** power stripes in the **Metal 8** layer

Your design should now look similar to figure 5 after adding the powering rings and stripes.

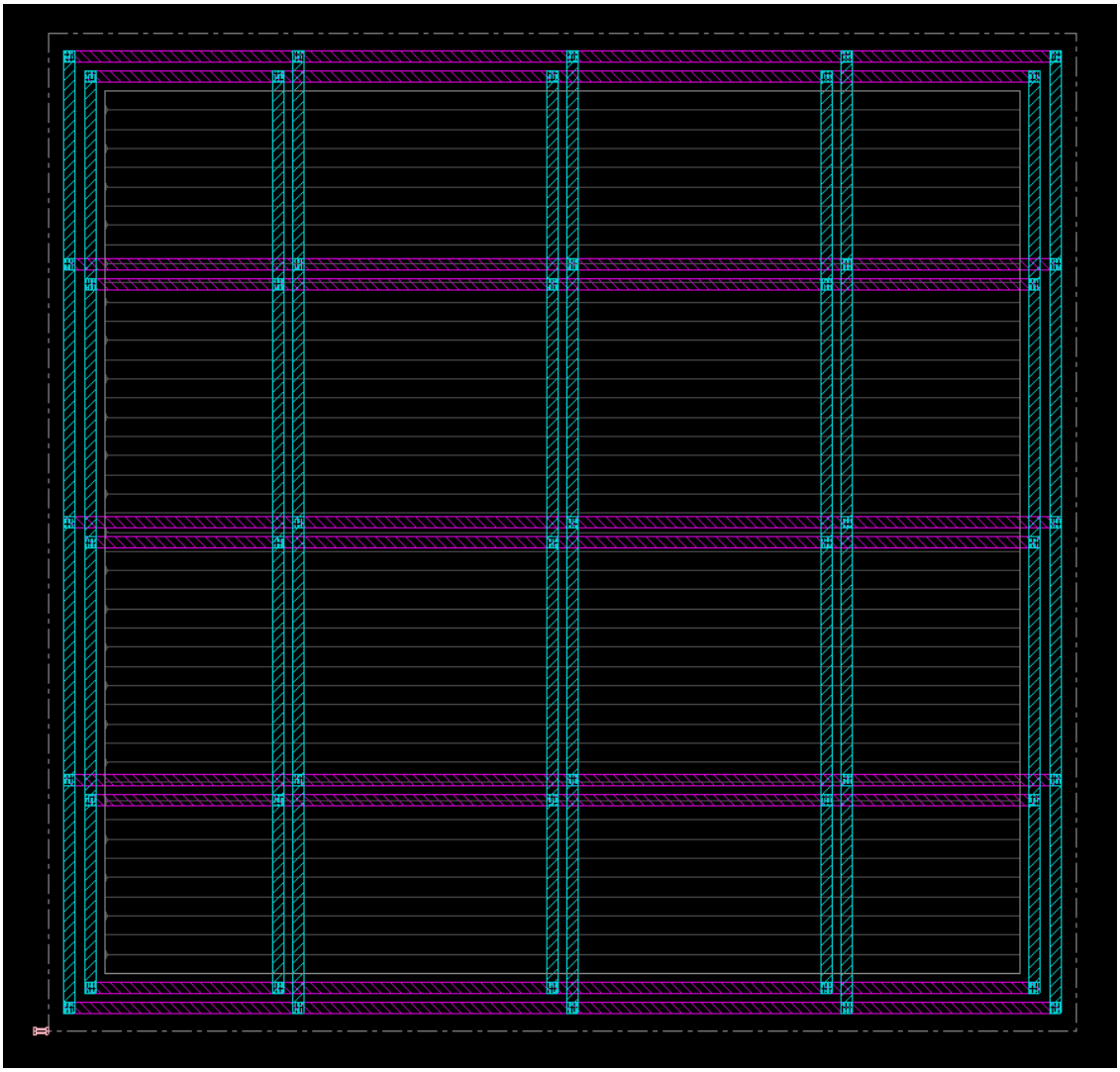

Figure 5: After the addition of power ring and power stripes

7. Pin Placement – Go to **`Edit > Pin Editor`**. Here you should see all the pins (unassigned a location at the moment) in the Pin Group section. Follow the below steps to assign a set of pin to the top IO boundary.
    - Select all the pins from **`clk_a`** to **`rx_full_b`** (using shift key + left click)
    - In the location section select Spread and set the spread type to From Center
    - Select the Side/Edge as **Top**
    - Set spacing as **5.0 Microns** (This will adjust to the closest workable value)
    - Leave the other parameters to the default values
    - Click Apply and you should see that the pins are now assigned to the top boundary.
- Notice that selected set of pins were set as SIGNAL pins. However, we should change this attribute for the clock pins **`clk_a`** and **`clk_b`**.
    - Select **`clk_a`** and **`clk_b`** from the pin group
    - Under Location, select Update attribute. This will grey-out the options to edit the pin location.
    - At the bottom of the pin attributes, change use: SIGNAL to use: CLOCK

- Similarly, assign the remainder of pins as follows:

Pins	Side/Edge	Spacing
`rx_parallel_data_out_a[]` **`rx_parallel_data_out_b[]`**	**Left**	**5 Microns**
`rx_parity_error_a` **`rx_parity_error_b`** **`rx_stop_bit_error_a`** **`rx_stop_bit_error_b`** **`scan_in_a`** **`scan_in_b`** **`scan_out_a`** **`scan_out_b`** **`SE`** **`tx_busy_out_a`** **`tx_busy_out_b`** **`tx_data_wr_enable_in_a`** **`tx_data_wr_enable_in_b`**	**Bottom**	**5 Microns**
`tx_parallel_data_in_a[]` **`tx_parallel_data_in_b[]`**	**Right**	**5 Microns**

8. Save the design in its current status.
    - Go to **`File > Save Design`**.
    - Select data type as **Innovus** and set the file name as *uart_top_prePlacement*.
    - Click OK to save the design

We can now load the design after the pin placement step by going to **`File > Restore Design`**. You will have to load the design at different stages to answer the questions in the exercise section. Feel free to save the design at various checkpoints throughout the experiment.

9. Place standard cells – Go to **`Place > Place Standard Cell`**. You will be presented with the placement configuration window.
    - Select **Run Full Placement**
    - Under optimization options select Include **Pre-Place Optimization**
    - Click Mode…
        - Make sure place IO pins is NOT selected in the placement mode as we have already placed the IO pins
        - Leave the other parameters to the default values and click OK
    - Click OK to perform placement of standard cells

Tip: By selecting items in the control window of Innovus, you can control what Innovus displays on the design area. For example, to hide all nets, deselect Net in the control window as shown in figure 6 and you will the shown the design without the nets as shown in figure 7.

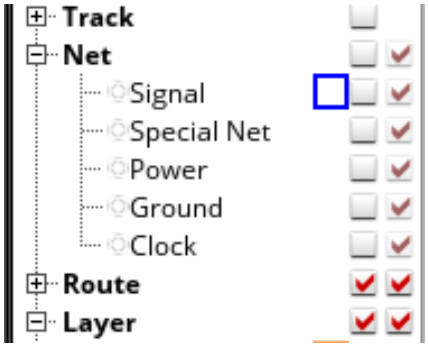

Figure 6: Hide all nets using the control window

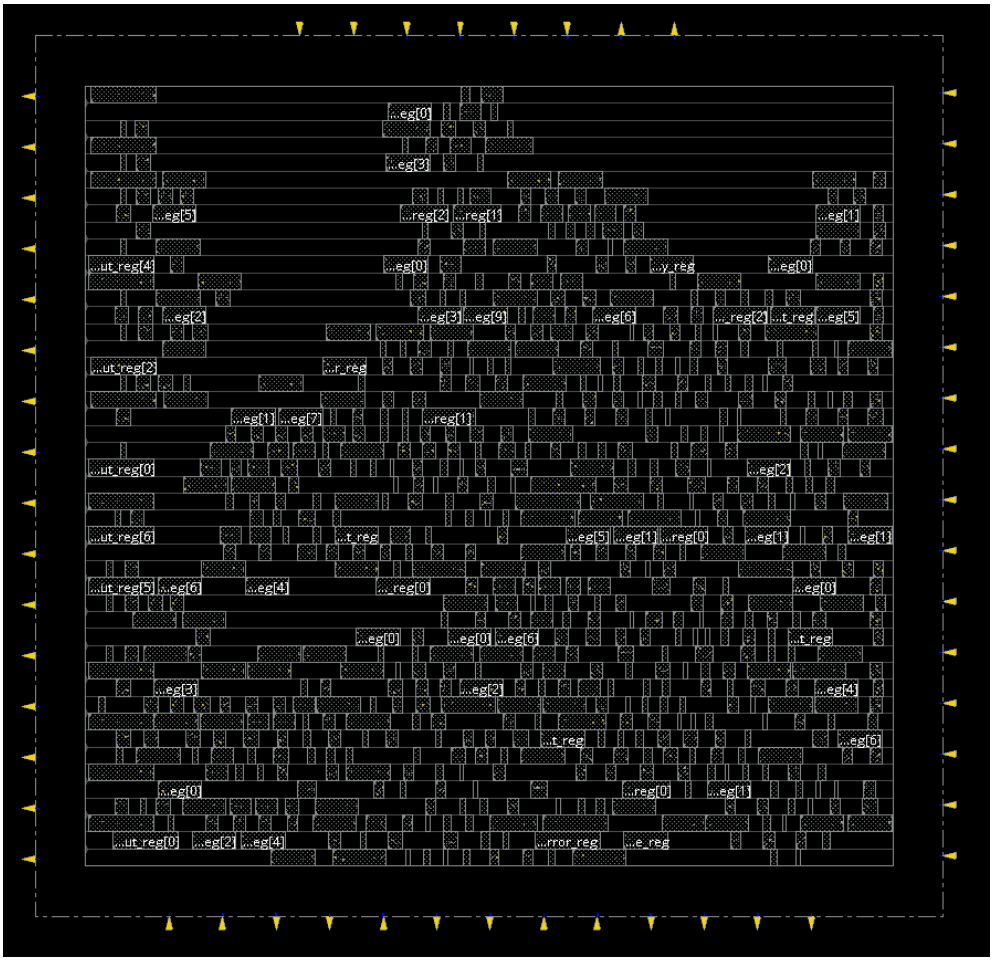

Figure 7: Design after placement with all nets hidden

- Take a screenshot of the design without any nets
- Take a screenshot of the design with the clock net

10. Report gate count and area – Go to **`File > Report > Gate Count`** and save the report as *uart_top_optPlace.gateCount* in the report folder.

11. Pre-CTS setup time analysis – Go to **`Timing > Report Timing`** and you will be presented with the timing analysis window.
    - Select **Pre-CTS** as the design stage
    - Select **Setup** as the analysis type
    - Provide a suitable prefix for the report files
    - Set the **`../report/pre_CTS`** folder as the output directory
    - Click OK to generate the timing reports

    According to the given constraints, you should not see any violations at this stage.

12. Route power nets – Go to **`Route > Special Route`** and you will be presented with the special route configuration window
    - In the Net(s) field enter: **`VDD GND`**
    - Leave the remaining parameters to their default values and click OK

    You should now see horizontal power routes spanning across the core area

13. Clock tree synthesis (CTS)– Use the following command to perform clock tree synthesis

    `Innovus: ccopt_design`

    This command will resynthesize the clock net and add buffers or change wire lengths of clock nets to balance clock skew throughout the design.

    - Take a screenshot of the design without any nets after CTS (hide all nets using the control window options)
    - Take a screenshot of the clock nets after CTS

Now that we have synthesized the clock tree, we will now perform clock tree aware scan chain reordering, which will contribute to reduce signal routing congestion in the design.

14. Scan reorder – Go to **`Place > Scan Chain > Reorder`**
    - Select the clock tree aware option
    - Leave the remaining parameters to their default values
    - Click OK to perform scan reordering

15. Post CTS timing analysis – Go to **`Timing > Report Timing`** and you will be presented with the timing analysis window.
    - Select **Post-CTS** as the design stage
    - Select **Hold** as the analysis type
    - Provide a suitable prefix for the report files
    - Set the **`../report/post_CTS`** folder as the output directory
    - Click OK to generate the timing reports

    According to the given constraints, you should not see any violations at this stage.

However, if you were to see that there are timing violations, you may execute the following command to optimize the design and fix the hold time violations

Innovus: optDesign -postCTS -hold

16. Signal Route – Go to **Route > NanoRoute > Route** and you will be presented with the NanoRoute configuration window which we will use to route signal nets.
    - Leave the parameters to their default values
    - Click OK to perform routing of signal nets

17. Post-Route Timing analysis – Now that we have fully placed and routed the functional design, we may perform post route timing analysis to ensure that all timing constraints are still met. For post route timing analysis, before generating the timing reports, we should change the analysis type to On-Chip Variation (OCV). Execute the following command to change the analysis type;

    Innovus: setAnalysisMode -analysisType onChipVariation

    - Now go to **Timing > Report Timing** and make verify that there are no timing violations

18. Place filler cells – To ensure that there is n-well continuity and to avoid sagging of layers after fabrication, we need fill the empty spaces in the core area with filler cells. Go to **Place > Physical Cell > Add Filler** and you will be presented with the Filler configuration window.
    - In the Cell Name(s) field, select all the cells with the "FILL" prefix
    - Set the Prefix as "FILLER"
    - Select Do DRC
    - Select Fit Gap (this will allow Innovus to use combinations of filler cells to fit empty gaps in the core area)
    - Leave the remaining parameters to their default values and click OK
    - Your design should now look similar to the design shown in figure 8.

19. Verification – Before exporting the design verify that there are no geometry violations (cell overlaps, spacing, min area etc.) and no connectivity issues (open nets, unrouted nets) in the design.
    - Geometry Verification
      - Go to **Verify > Verify Geometry**
      - Go to advanced tab and change location to **../report/uart_top.geom.rpt**
      - Click OK to generate the report
    - Connectivity Verification
      - Go to **Verify > Verify Connectivity**
      - Change location to **../report/uart_top.conn.rpt**
      - Click OK to generate the report

    You should not see any violations in these verification reports

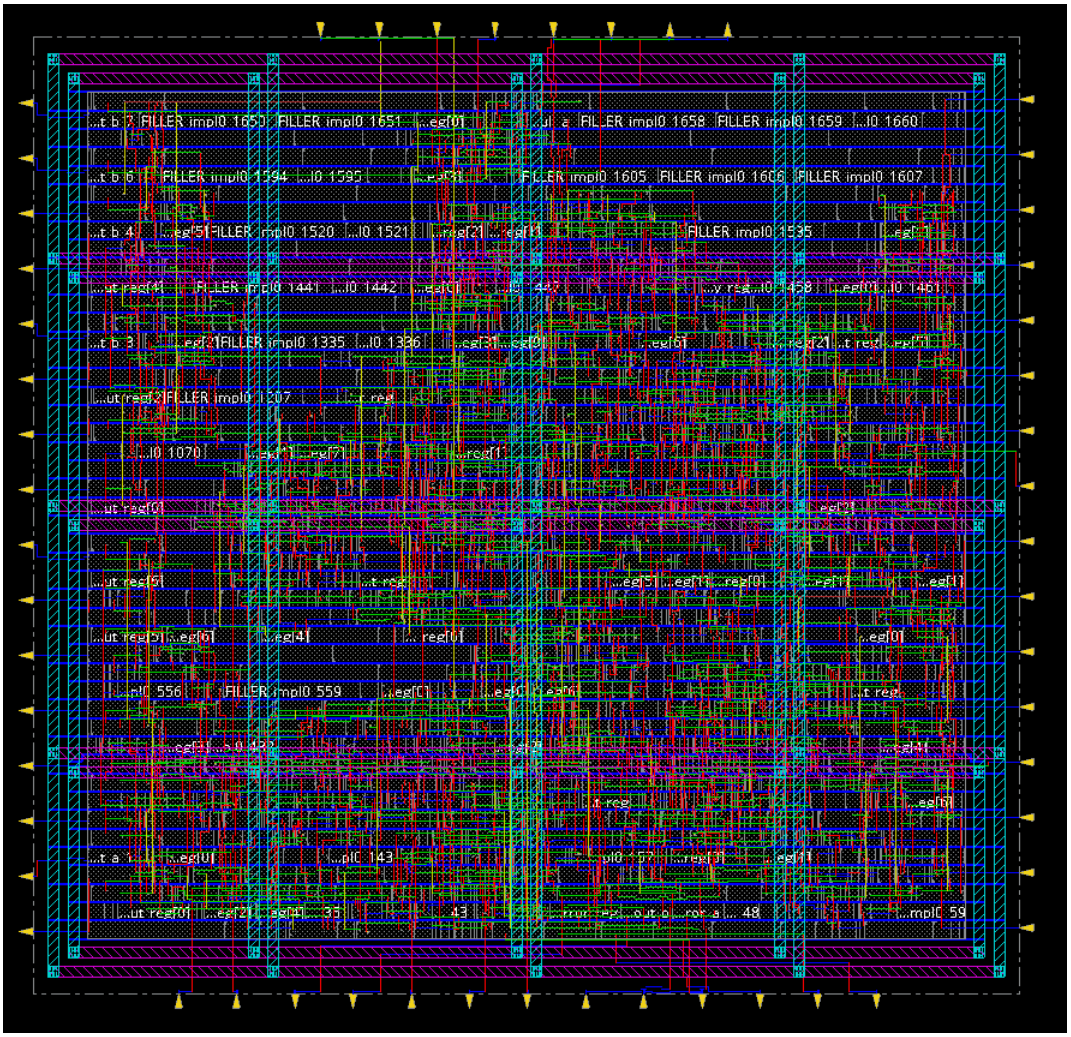

Figure 8: Design after filler cell placement

20. GDSII Export – After making sure that there are no timing violations and design rule violations in the design, the final step in the place and route process is to generate the data exchange file required by the foundries to fabricate the design. In this experiment, we will export the design to the widely accepted GDSII format. Go to **`File > Save > GDS/OASIS`** and you will be presented with the GDS/OASIS export configuration window.
    - Select GDSII/Stream as the output format
    - Set the output files as **`../output/uart_top.gds`**
    - Select the map file from the input folder (streamOut.map)
    - Change the Library name to uart_lib
    - Leave the remaining parameters to their default values
    - Click OK to generate the GDSII file for the design

Exercise

1. Restore the design you saved at part 8 of step 3 (*uart_top_prePlacement*), perform placement of standard cells **without** pre-place optimization and report the gate count & area. Compare and comment on the gate count & area with and without pre-place optimization.

2. Note that we did only setup time analysis in pre-CTS timing analysis. There is little purpose in performing hold time analysis at the pre-CTS stage. What is the reason for this?

3. Compare and comment on the cell count and the routing of the clock net before and after CTS. (show screenshots of the design to support your answer)

4. What is the reason for changing the analysis mode to on-chip variation at the post-Route timing analysis stage?

5. In some designs, in addition to the placement of filler cells, a metal fill is added as well. Describe the difference between filler cell placement and metal fill.