Department of Electronic and Telecommunication Engineering

University of Moratuwa, Sri Lanka

EN4603 - Digital IC Design

Laboratory Experiment 3
Place & Route

Laboratory Report

Submitted by

Submitted by

C.S.Pallikkonda	180441C
R.M.A.S.Rathnayake	180534N
B.P.Thalagala	180631J

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Contents

Note:
All the materials related to the report can also be found at https://github.com/bimalka98/Digital-IC-Design

List of Figures

List of Tables

List of Abbreviations

ASIC Application Specific Integrated Circuit

ATPG Automatic Test Pattern Generation

CTS Clock Tree Synthesis

DEF Design Exchange Format

DFT Design For Testability

GPDK Generic Process Design Kit

HDL Hardware Description Language

IC Integrated Circuit

IO Input Output

RTL Register-Transfer Level

RX Receiver

TCL Tool Command Language

TX Transmitter

UART Universal Asynchronous Receiver Transmitter

1 Introduction

1.1 Practical

In this practical, you will be using *Cadence Innovus* to place and route the design you synthesized in Laboratory Experiment 2. As inputs to Innovus, you will provide,

1. Source Verilog files
2. Technology libraries provided by the fabrication plant (here, 45 *nm* educational Generic Process Design Kit (GPDK) given by Cadence) : `(.lib, .lef, .tch)`
    - Library Timing (.lib) files specify timing (cell delay, cell transition time, setup and hold time requirement) and power characteristics of standard cells. Slow and fast libraries characterize standard cells with maximum and minimum signal delays, which could occur from process variations.
    - Tch files are binary files that accurately characterize library elements, that include capacitance and resistance.
    - Library Exchange Format (LEF) specify design rules, metal capacitances, layer information. . . etc.
3. Multi Mode Multi Corner file (.view)
4. Constraints file (.sdc)
5. Scan DEF file (.scandef)

and will obtain the GDSII file as output, which is an industry standard format for exchanging Integrated Circuit (IC) layout data. You will then analyze, compare, and comment on the placement, cell count, congestion etc. of the design at various stages of the place and route design flow.

1.2 Place & Route

Place & route is the final step in the IC design flow before fabrication. As the name implies, this step comprises of two main tasks – placement and routing.

In placement, the IC designer decides where to place all the elements of the design. In addition to placing cells, this step involves making initial decisions about the aspect ratio and utilization factors (core utilization / cell utilization).

Then, in the routing step, the designer makes the physical interconnects between the placed elements. This step comprises of three main stages: (1) Power Routing: routing of VDD and GND nets, (2) Clock Tree Synthesis: re-synthesizing of clock nets based on cell placement in order to balance clock skew throughout the design and minimize insertion delay, and (3) Signal Routing: routing of all other nets.

The general design flow for place & Route, which we will be following in this laboratory experiment, is shown in Figure 1.

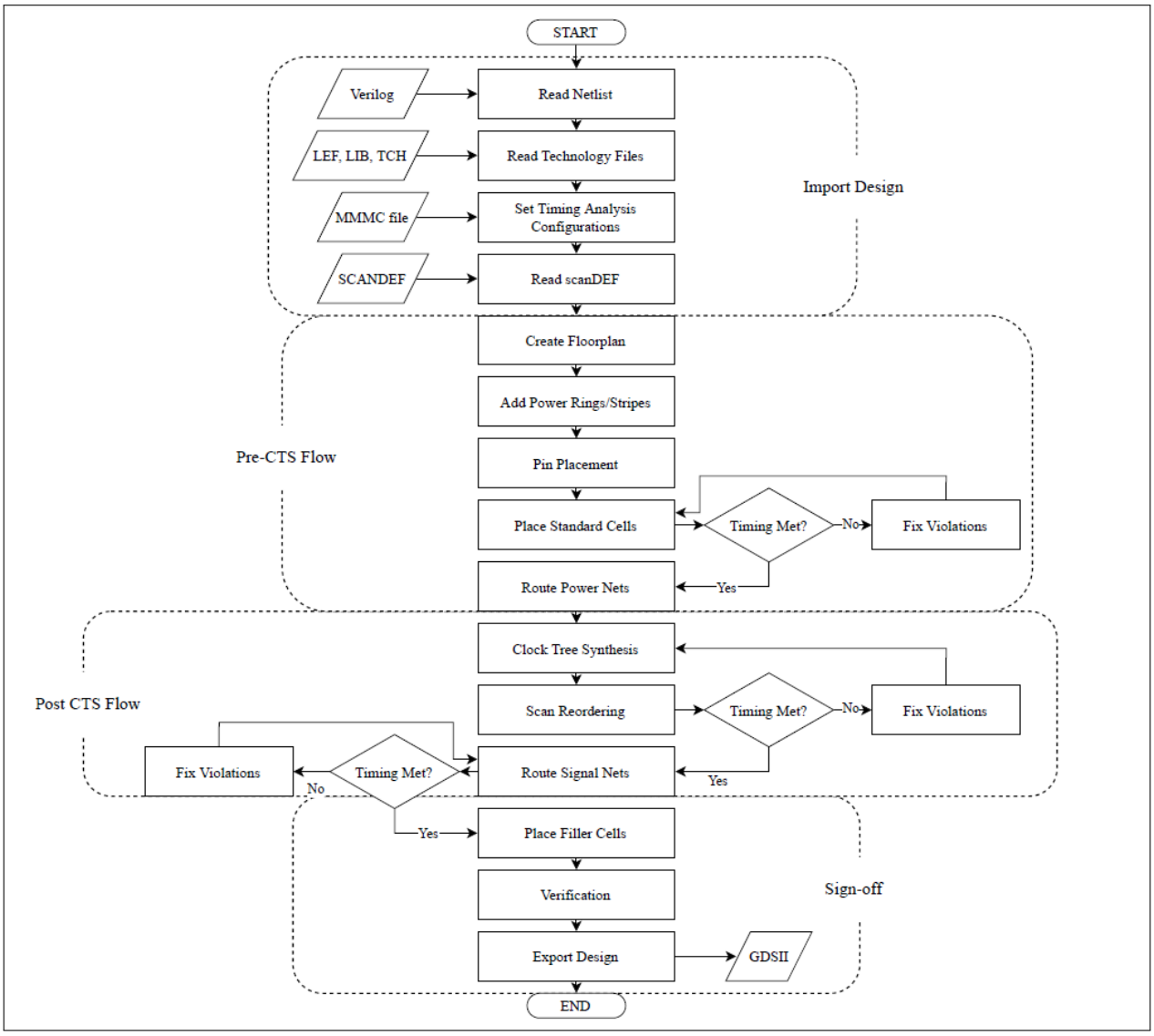

Figure 1: The general design flow for place & Route

2 Using Innovus for Place and Route

This section demonstrates the steps carried out at the 'Step 3' in the Laboratory guide, with necessary illustrations.

1.) Import the Design: this step loads the design according to the netlist, technology libraries, labels for power nets and the timing analysis configurations. Once the design is loaded an empty core in the design area of Innovus can be observed as shown in the Figure 2, and it displays "In Memory" in the bottom right corner of Innovus.

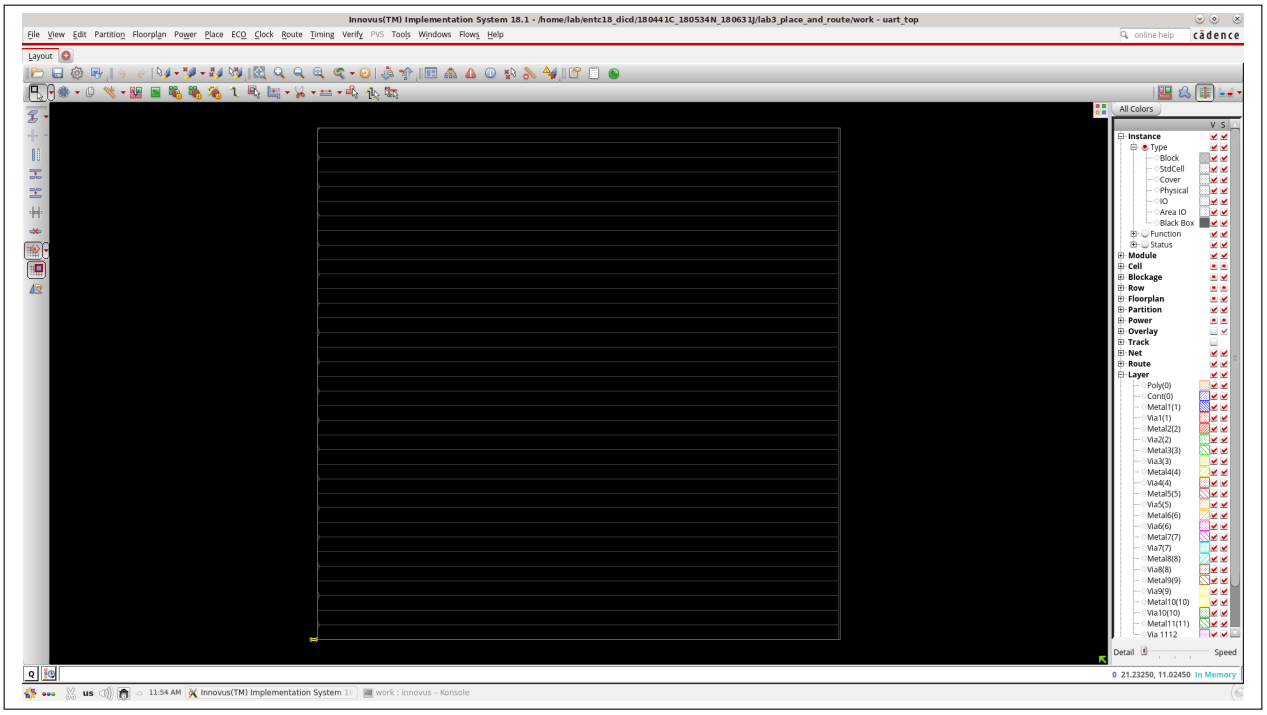

Figure 2: Empty core in the design area of Innovus, when the design is loaded

2.) Read the scanDEF file: this file specifies the scan chains available in the design and to perform scan reordering later.

```
<CMD> defIn ../input/uart_top_2_scanDEF.scandef
Reading DEF file '../input/uart_top_2_scanDEF.scandef', current time is Thu Jan 19 11:55:00 2023 ...
--- CASESENSITIVE ON
--- DIVIDERCHAR '/'
DEF file '../input/uart_top_2_scanDEF.scandef' is parsed, current time is Thu Jan 19 11:55:00 2023.
```

Figure 3: Innovus log for reading the scanDEF file

3.) Set the design mode to 45nm process

```
<CMD> setDesignMode -process 45
Applying the recommended capacitance filtering threshold values for 45nm process node: total_c_th=0, relative_c_th=1 and coupling_c_th=0.1.
        These values will be used by all post-route extraction engines, including TQuantus, IQuantus and Quantus QRC extraction.
        Capacitance filtering mode(-capFilterMode option of the setExtractRCMode) is 'relAndCoup' for all engines.
        The accuracy mode for postRoute effortLevel low extraction will be set to 'high'.
        Default value for EffortLevel(-effortLevel option of the setExtractRCMode) in postRoute extraction mode is 'medium'.
Updating process node dependent CCOpt properties for the 45nm process node.
```

Figure 4: Innovus log for setting the design mode to 45nm process

4.) Specify floorplan: Set the *Aspect Ratio* as 1.0 and *Core Utilization* as 0.4. Set core margins by core to IO boundary. Set a margin of 5 Microns to all sides from the core. This resulted in a floor plan shown in the Figure 5.

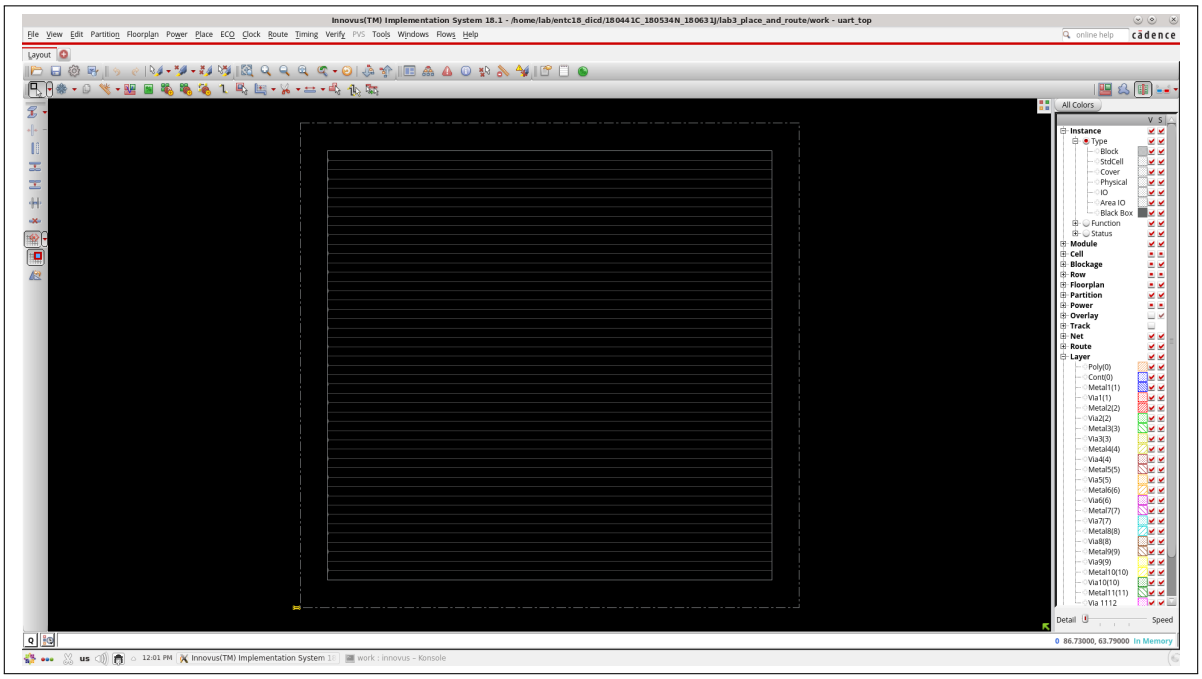

Figure 5: Specified floorplan

5.) Add power rings and power stripes:Metal 7 layer is used for for horizontal power rings/stripes, while Metal 8 layer for vertical power rings/stripes.

a. Power rings

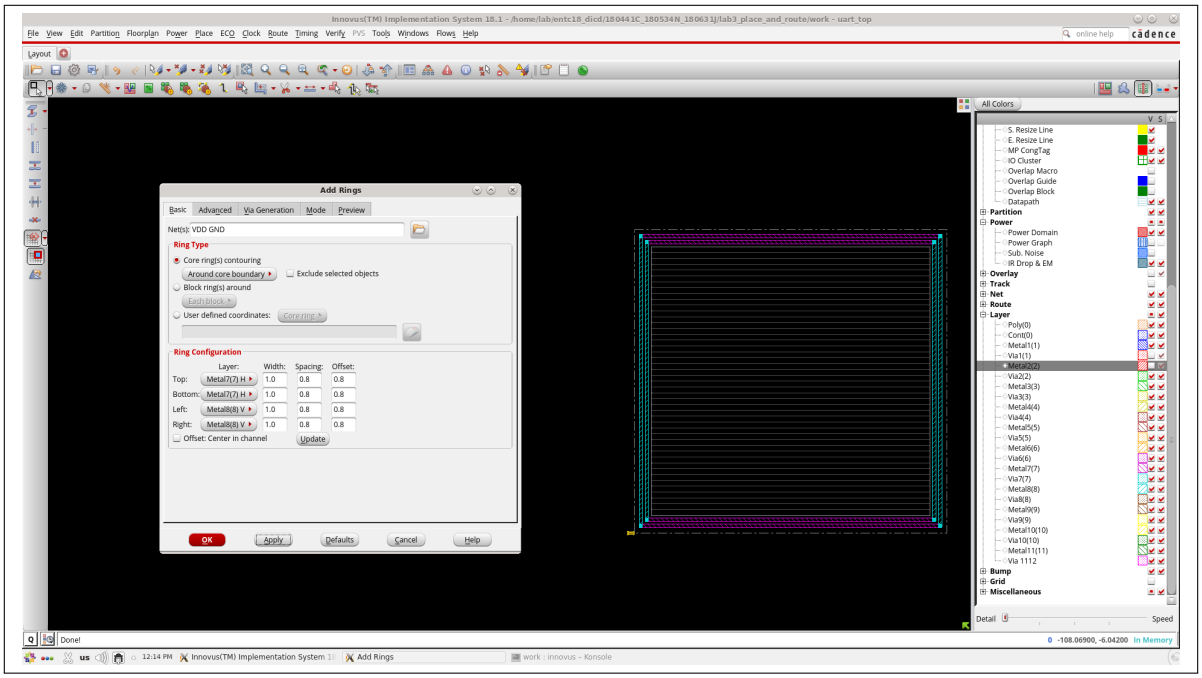

Figure 6: Adding power rings

b. Horizontal power strips

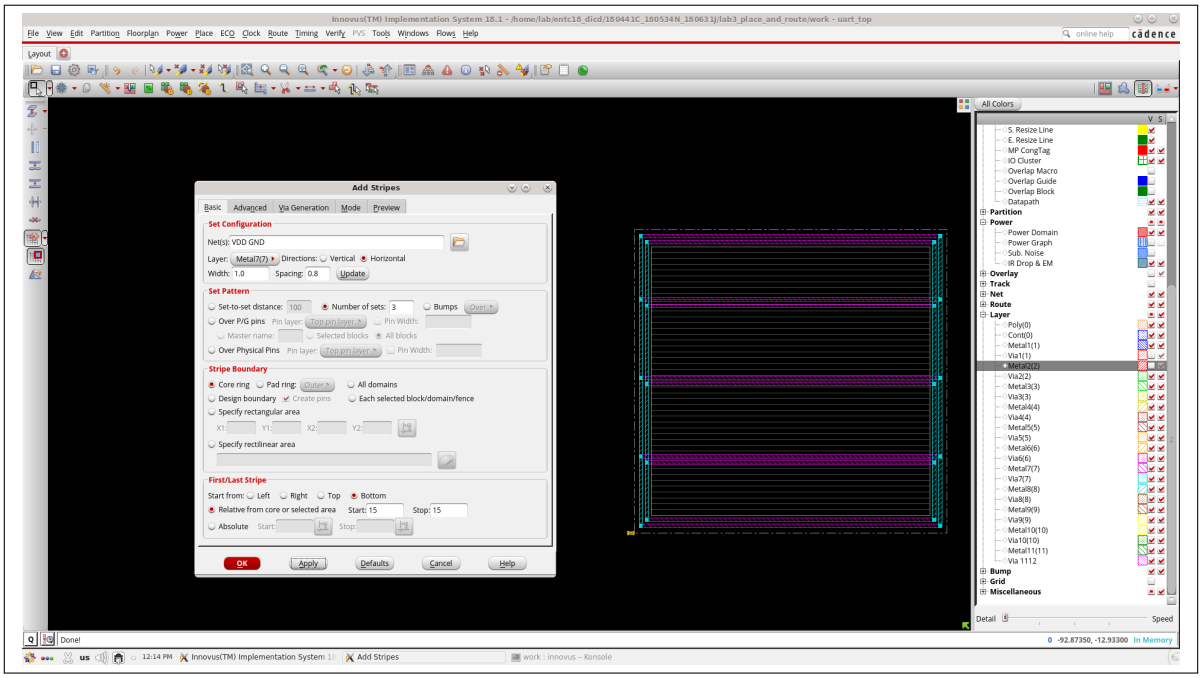

Figure 7: Adding horizontal power strips

c. Vertical power strips

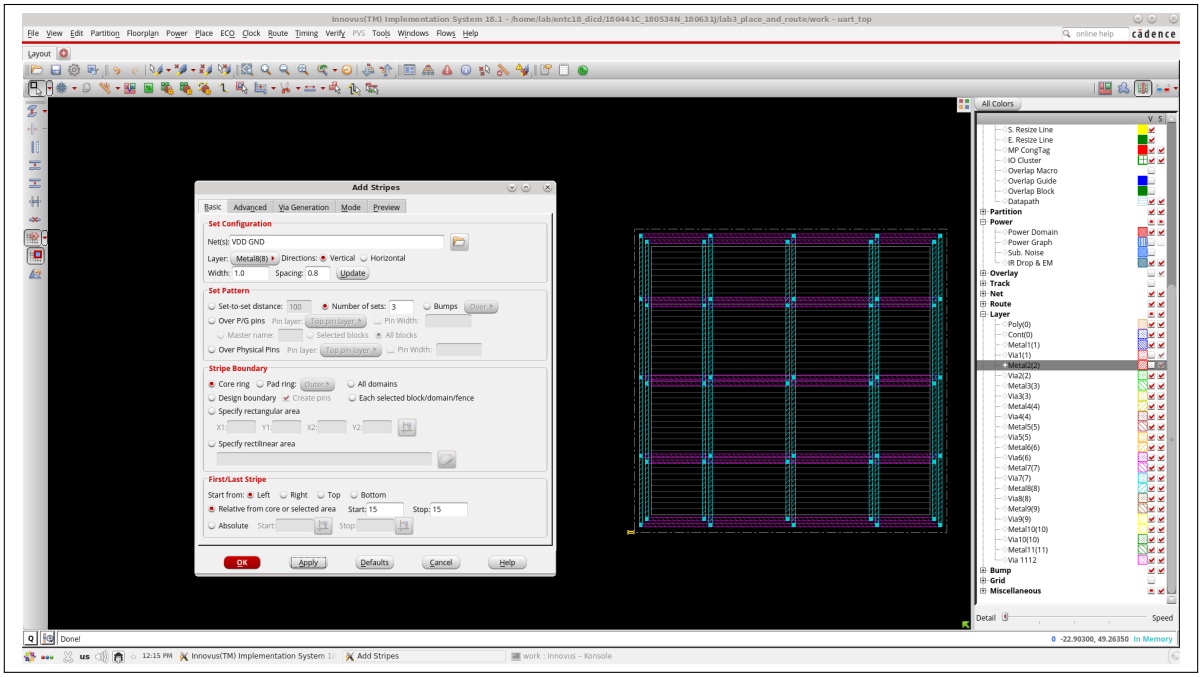

Figure 8: Adding vertical power strips

6.) Pin Placement: assigns a set of pin to the IO boundary. By default the pins are set as *SIGNAL* pins. However, we should change this attribute for the clock pins `clk_a` and `clk_b` to *CLOCK*. Figure 10 illustrated the view of the floorplan after all the pins are assigned.

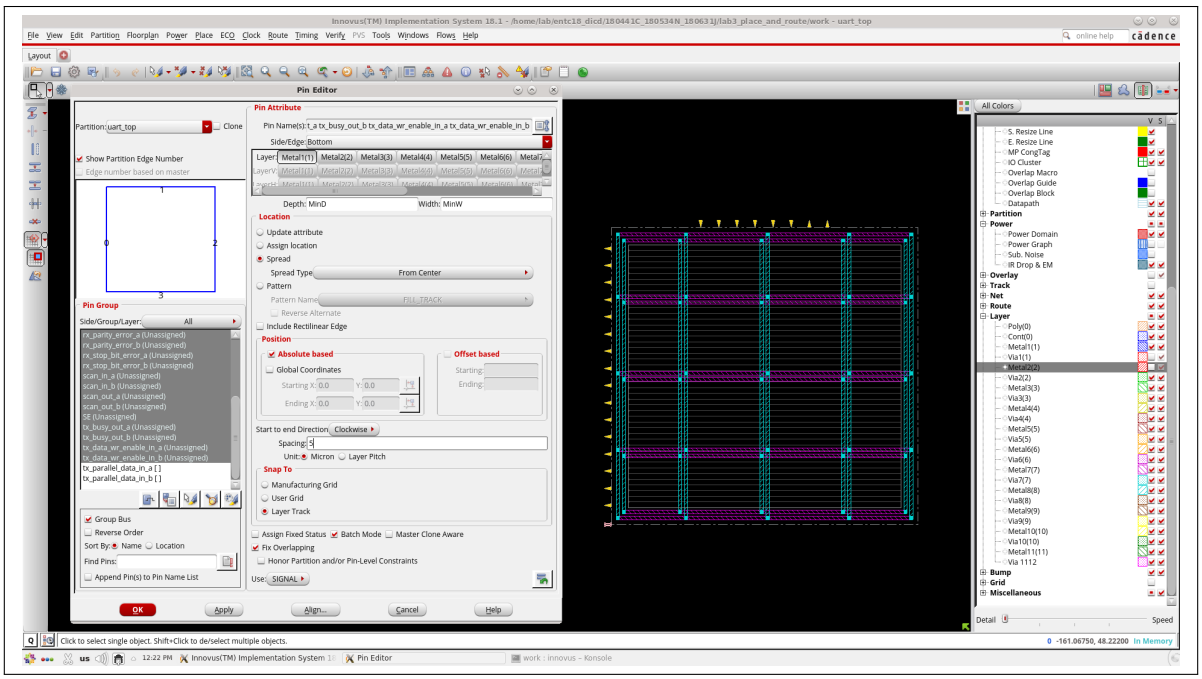

Figure 9: Assigning the pins to the IO boundary

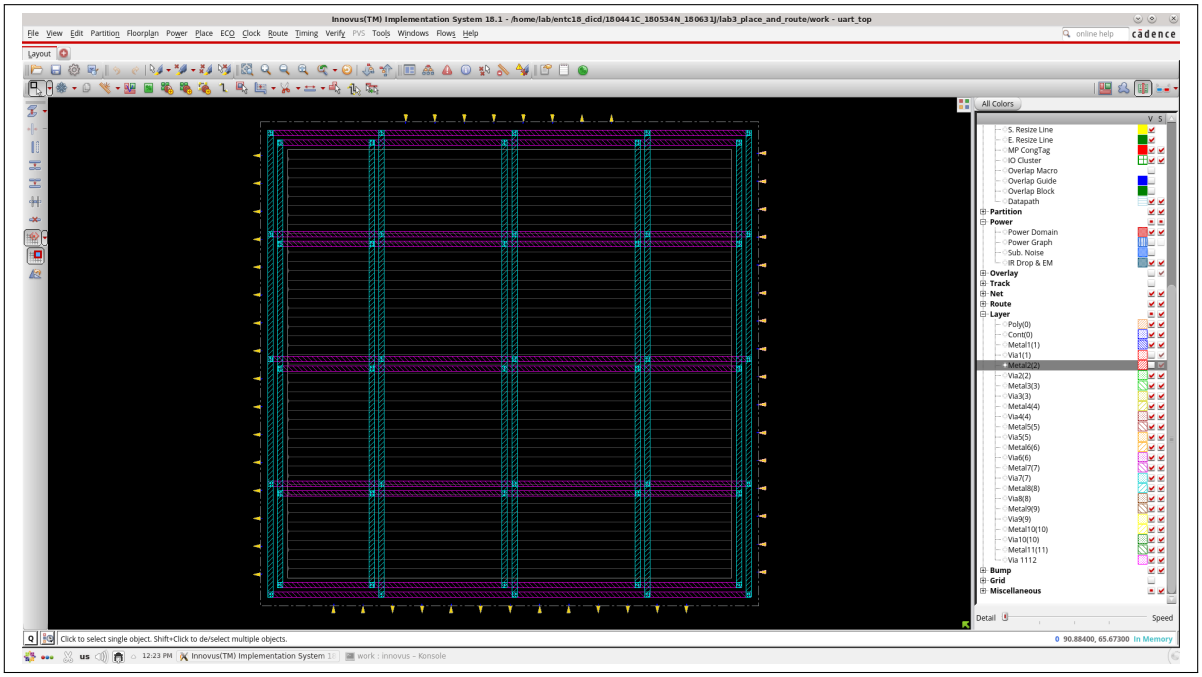

Figure 10: View of the floorplan after the pins are assigned

7.) Standard cell placement: this step runs a full placement with pre-place optimization as shown in the dialog box of the Figure 11.

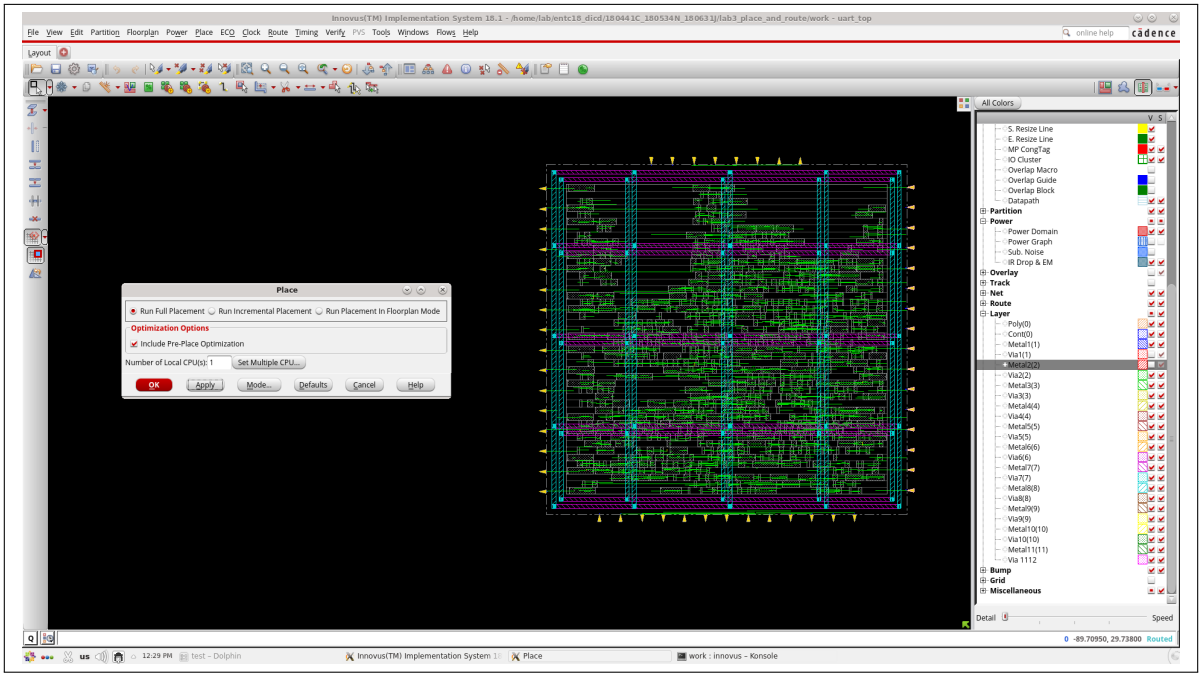

Figure 11: 'Run Full Placement' with 'Pre-Place Optimization'

a. A screenshot of the design without any nets

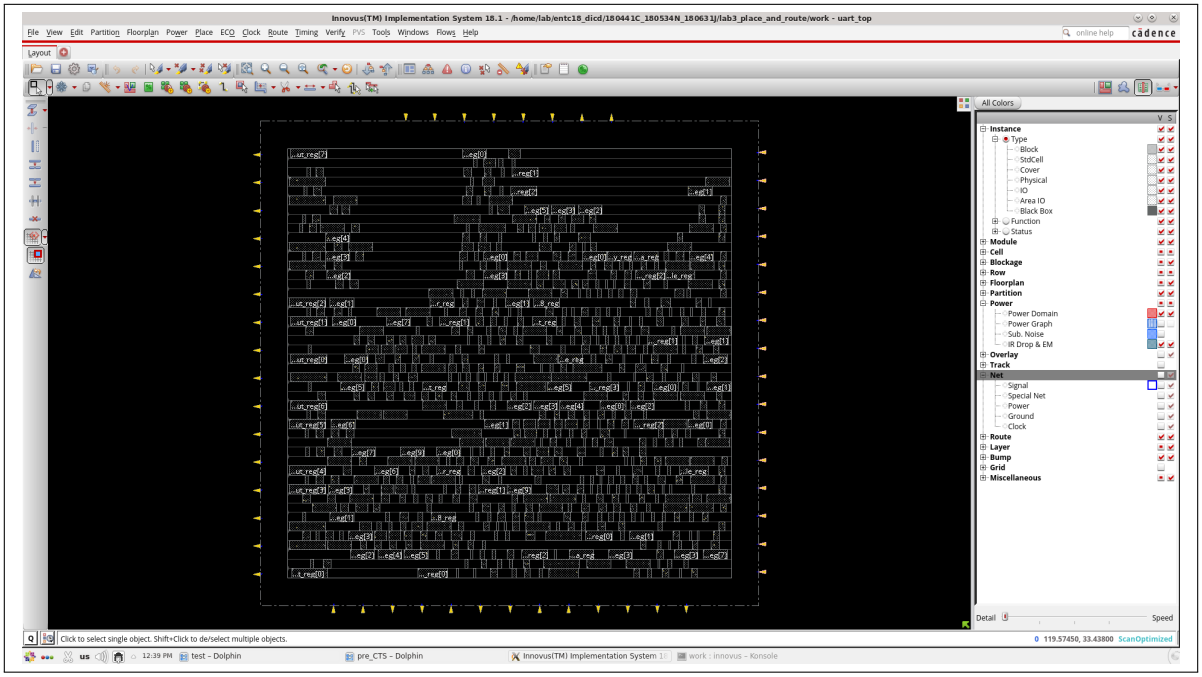

Figure 12: Screenshot of the design without any nets

b. A screenshot of the design with the clock net

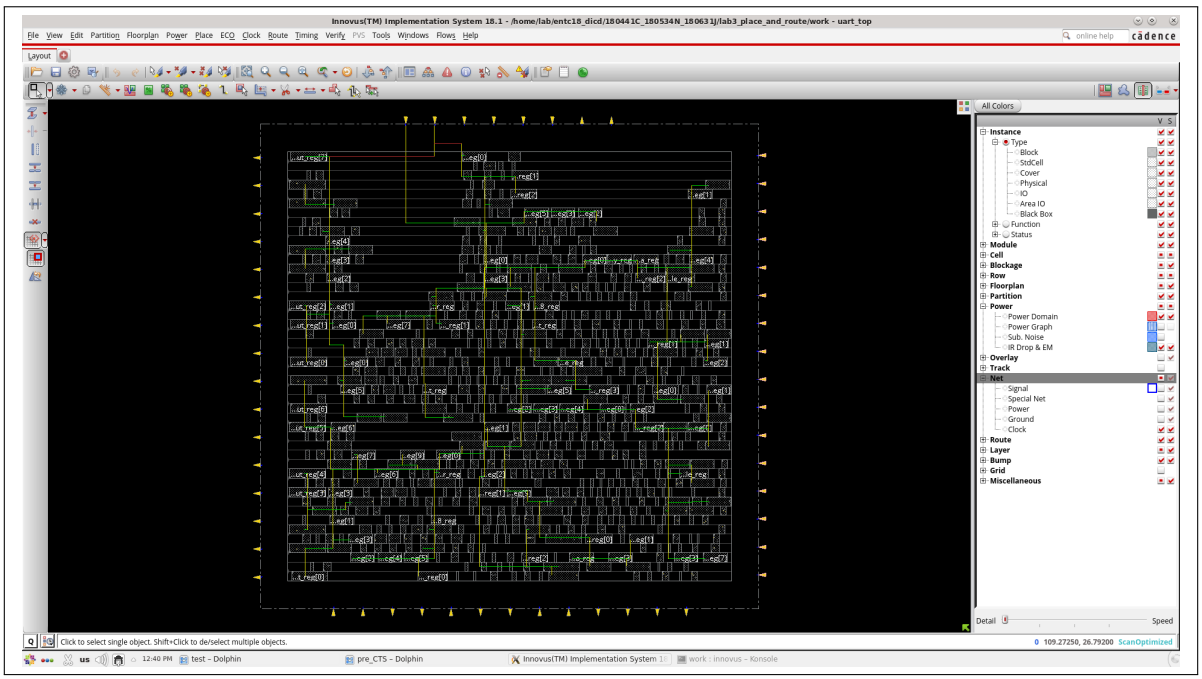

Figure 13: Screenshot of the design with the clock net

8.) Report gate count and area

```
Gate area 1.0260 um^2
Level 0 Module uart_top                                Gates=      2300 Cells=     738 Area=    2359.8 um^2
Level 1 Module ins_uart_transceiver_A                  Gates=1151       Cells=369       Area=    1181.3 um^2
Level 2 Module ins_uart_transceiver_A/ins_rx_wrapper   Gates=606        Cells=179       Area=     621.8 um^2
Level 2 Module ins_uart_transceiver_A/ins_tx_wrapper   Gates=545        Cells=190       Area=     559.5 um^2
Level 1 Module ins_uart_transceiver_B                  Gates=1148       Cells=369       Area=    1178.5 um^2
Level 2 Module ins_uart_transceiver_B/ins_rx_wrapper   Gates=607        Cells=179       Area=     623.5 um^2
Level 2 Module ins_uart_transceiver_B/ins_tx_wrapper   Gates=541        Cells=190       Area=     555.1 um^2
```

Figure 14: Gate count and the area report

9.) Pre-CTS setup time analysis: according to the given constraints, there will be no violations at this stage. Summary of this is shown in the Figure 15.

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 view_slow

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  3.052  |  8.028  |  3.052  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   514   |   324   |   352   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |     24 (68)      |   -1.057   |     24 (68)      |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 36.765%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

Figure 15: Summary of the Pre-CTS setup time analysis

10.) Route power nets: observe the horizontal power routes spanning across the core area shown in the Figure 16.

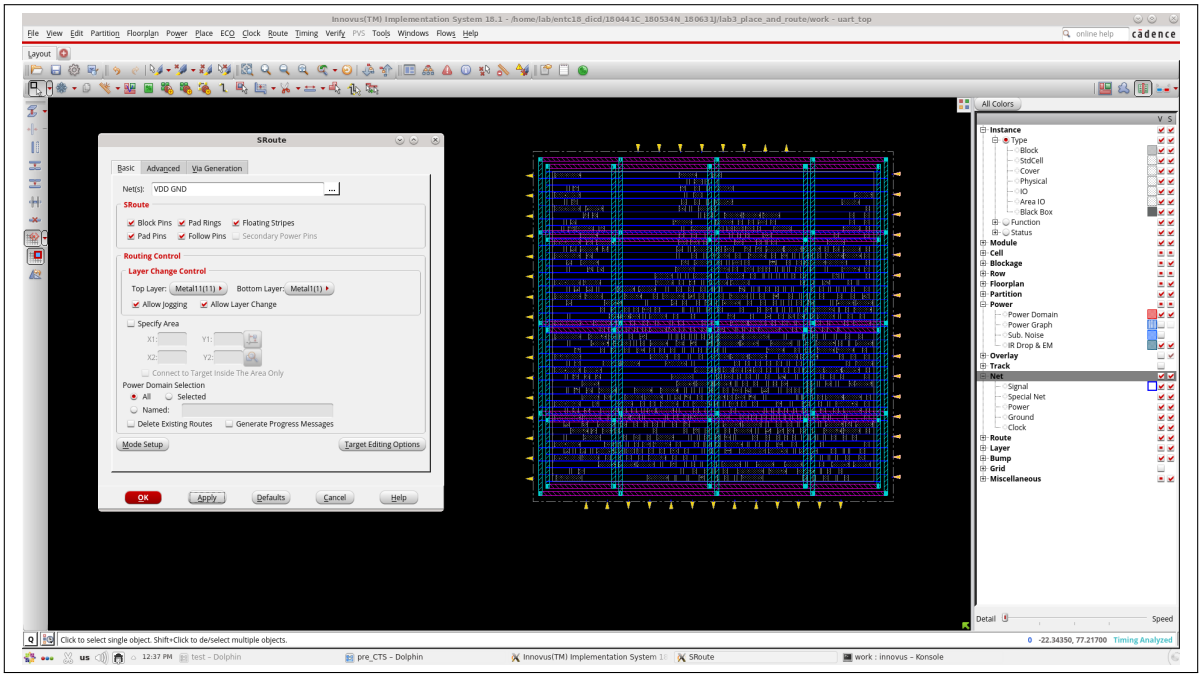

Figure 16: Horizontal power routes spanning across the core area

11.) CTS using `ccopt_design` command: resynthesize the clock net and add buffers or change wire lengths of clock nets to balance clock skew throughout the design.

a. A screenshot of the design without any nets after CTS

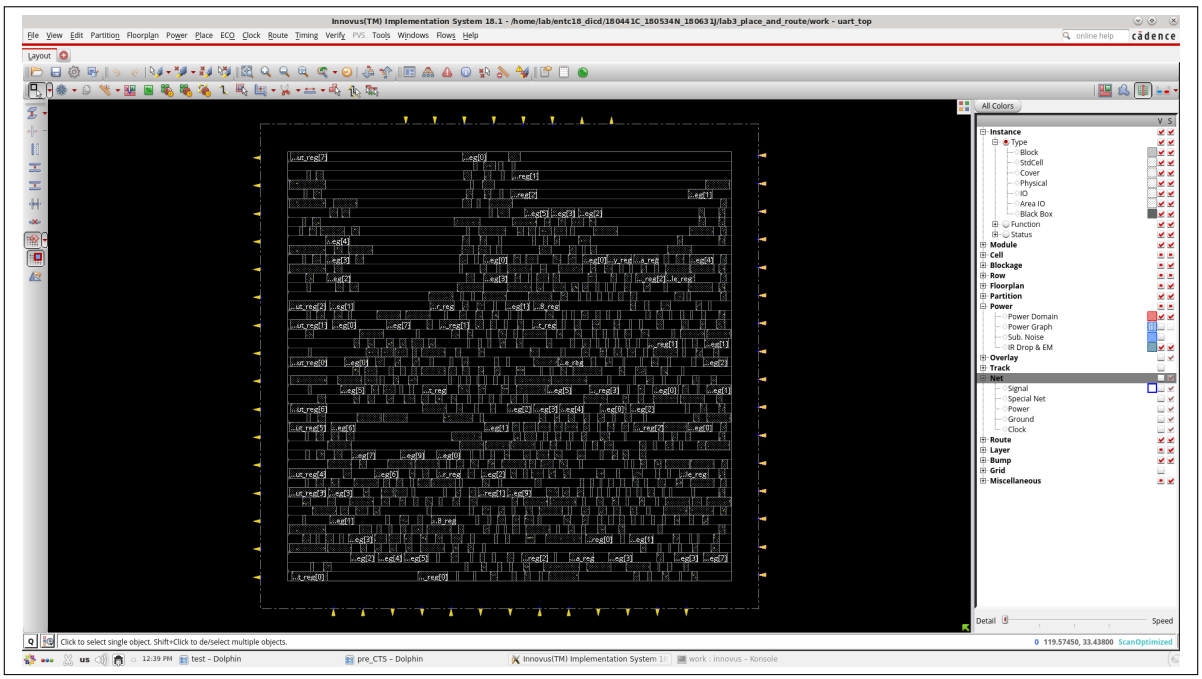

Figure 17: Screenshot of the design without any nets after CTS

b. A screenshot of the design with the clock net after CTS

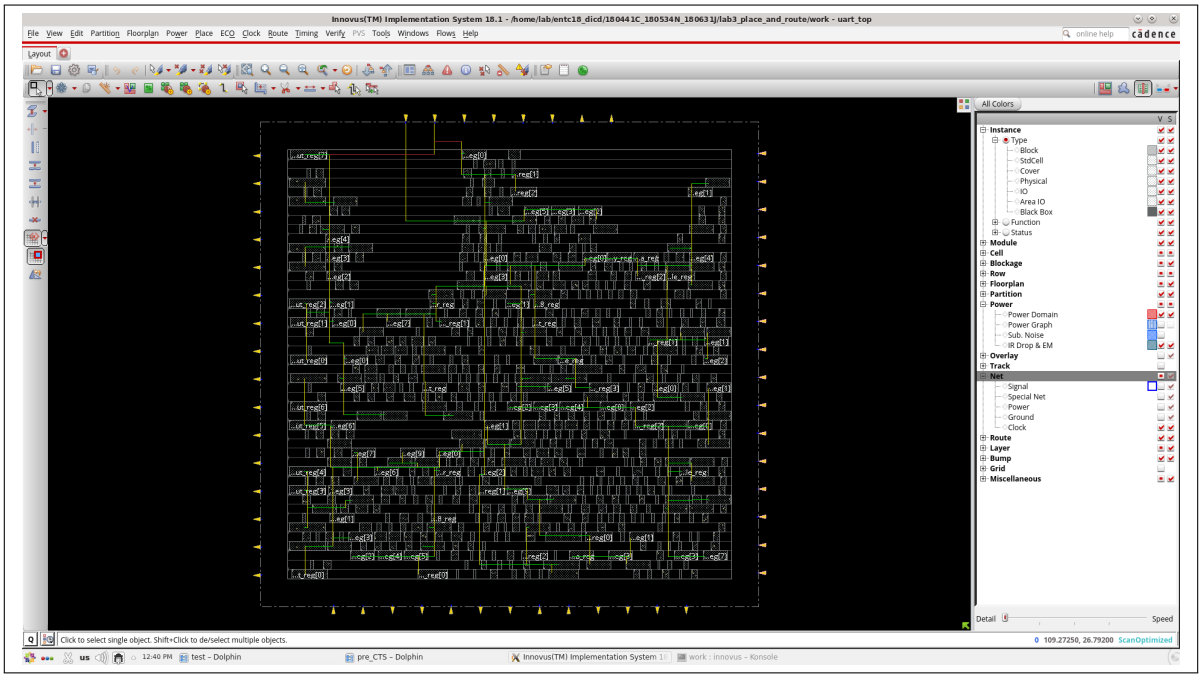

Figure 18: Screenshot of the design with the clock net after CTS

Bibliography