Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
- Computational Fluid Dynamics

cadence®

PCB Design and Analysis Learning Map

Beginner → Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow — 3 days
- Allegro Design Entry HDL Basics — 1 day
- Allegro System Capture — NEW — 2.5 days
- Allegro System Architect — 2 days
- Allegro Design Reuse — 1 day
- Allegro AMS Simulator — 3 days
  - Allegro AMS Simulator Advanced Analysis — 1 day
- Allegro Design Entry Using OrCAD® Capture — 2 days
- OrCAD CIS — 1 day
- OrCAD Capture Constraint Manager PCB Flow — NEW — 1 day
- Allegro EDM Design Entry HDL Front-to-Back Flow — 3 days
- Allegro Team Design Authoring — 1 day
- Analog Simulation with PSpice® — 3 days
  - Analog Simulation with PSpice Advanced Analysis — 1 day

PCB Design

- Allegro PCB Editor Basic Techniques — 3 days
  - Allegro PCB Editor Intermediate Techniques — 2 days
  - Allegro PCB Router Basics — 2 days
  - Allegro PCB Editor Advanced Methodologies — 1 day
- Allegro High-Speed Constraint Management — 2 days
- Allegro Update Training — NEW — 1 day
- Advanced Design Verification with the RAVEL Programming Language — 2 days

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity — 3 days
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials — 2 days
- Allegro Sigrity™ SI Foundations — 2 days
- Allegro Sigrity PI — 1 day
- Sigrity PowerDC™ and OptimizePI™ — 1 day
- Sigrity Aurora — NEW — 3 days
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis — 3 days
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM — 3 days
- Clarity 3D Solver — NEW — 2 days
- Celsius Thermal Solver — 1 day

Library Development

- Allegro PCB Librarian — 2 days
- Allegro EDM PCB Librarian — NEW — 2 days
- Allegro Design Entry HDL SKILL® Programming Language — 3 days
- Allegro PCB Editor SKILL Programming Language — 3 days

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout
- Allegro® Package Designer
- Allegro FPGA System Planner
- Allegro Sigrity Package Assessment and Model Extraction
- OrbitIO™ System Planner
- Advanced Design Verification with the RAVEL Programming Language NEW
- Allegro Package Designer Plus NEW

SI/PI Analysis

- Allegro Sigrity™ SI Foundations
- Allegro Sigrity PI
- Sigrity PowerDC™ and OptimizePI™
- TopXplorer SystemSI for Parallel Bus and Serial Link Analysis
- Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM
- Clarity 3D Solver NEW
- Celsius Thermal Solver NEW

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Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Mixed-Signal Simulation

- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model NEW
- SimVision for Debugging Mixed-Signal Simulations NEW

AMS/Real Number Modeling

- Analog Modeling with Verilog-A
- Behavioral Modeling with Verilog AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification NEW

- Virtuoso Schematic Editor NEW
- Virtuoso Visualization and Analysis

Virtuoso® ADE Explorer & Assembler Series NEW

- **S1** ADE Explorer & Single Test Corner Analysis
- **S2** ADE Assembler & Multi Test Corner Analysis
- **S3** Sweeping Variables and Simulating Corners
- **S4** Monte Carlo, Real-Time Tuning & Run Plans

Virtuoso® ADE Verifier Series

- **S1** Setup, Run, & View Verifier Results
- **S2** Reference Flow and Analog Coverage Using the Setup Library Assistant

- 5G mmWave Handset System Design – **S1** RFIC (Transceiver) Design NEW

Spectre® Simulator Fundamentals Series

- **S1** Spectre Basics
- **S2** Large-Signal Analysis
- **S3** Small-Signal Analysis
- **S4** Spectre MDL

- Design Checks and Asserts
- High Performance Spectre Simulation

Virtuoso® Spectre® Pro Series

- **S1** DC Algorithm
- **S2** AC, XF, STB, Noise
- **S3** Transient Algorithm
- **S4** Fourier Transform
- **S5** Transient Noise

Spectre RF Series

- Spectre® RF Shooting Newton
- Spectre® RF Harmonic Balance NEW

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Custom IC, Analog and RF Design Learning Map

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Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — NEW — 2
- Advanced SKILL Language Programming — NEW — 3

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L — 1
- Virtuoso Connectivity-Driven Layout Transition — L XL GXL EXL — 2
- Virtuoso Abstract Generator — GXL — 1
- Virtuoso Floorplanner — GXL — 1

Virtuoso® Advanced-Node – ICADVM

- Virtuoso Layout for Advanced Nodes — 2
  - T1: Place and Route — 1 — NEW
  - T2: Electromigration — 0.5
  - Virtuoso Layout for Advanced Nodes and Methodology Platform — EXL — 0.5

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L — 1
- T2: Create and Edit Commands — L — 1
- T3: Basic Commands — XL — 1
- T4: Advanced Commands — XL — 1
- T5: Interactive Routing — XL — 1
- T6: Constraint-Driven Flow and Power Routing — XL GXL — 1
- T7: Module Generator and Floorplanner — XL GXL — 1
- T8: Concurrent Layout Editing — EXL — 1 — NEW
- T9: Virtuoso Design Planner — EXL — 2 — NEW

Layout Verification

- Pegasus Verification System — NEW — 2
  - Physical Verification System (PVS) — 2
    - Physical Verification Language Rules-Writer — 2

Quantus™ Extraction Solution Transistor-Level Series

- T1: Overview and Technology Setup — NEW — 0.5
- T2: Parasitic Extraction — NEW — 1
- T3: Extracted View Flows and Advanced Features — NEW — 0.5

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test

- Fundamentals of IEEE 1801 Low-Power Specification Format — 1
- Genus™ Synthesis Solution with Stylus Common UI — 3
- Genus Low-Power Synthesis Flow with IEEE 1801 — NEW — 1
- Low-Power Synthesis Flow with Genus Stylus Common UI — 1
- Test Synthesis with Genus Stylus Common UI — 2
- Advanced Synthesis with Genus Stylus Common UI — 2
- Modus DFT Software Solution — 1
- Joules™ Power Calculator — 2

Implementation

- Design For Test Fundamentals
- Innovus Block Implementation with Stylus Common UI — 3
- Innovus Hierarchical Implementation with Stylus Common UI — 1
- Innovus Low-Power Flow with Stylus Common UI — NEW — 1
- Innovus Clock Concurrent Optimization Technology with Stylus Common UI — 1
- Virtuoso® Digital Implementation — 3

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure with Stylus Common UI — 2
- Voltus™ Power Grid Analysis and Signoff with Stylus Common UI — 2

Equivalence Checking

- Conformal® Equivalence Checking — 2
- Conformal Low-Power Verification — 1
- Conformal Low-Power Verification Using IEEE1801 — NEW — 1
- Conformal ECO — 1

Cadence® RTL-to-GDSII Flow — 2

Cadence® Cerebrus™ Intelligent Chip Explorer — NEW — 1

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug

- Xcelium™ Simulator NEW — 2
- Cadence® RTL-To-GDSII Flow — 2
- VIP Basic Building Blocks and Usage NEW — 2
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage — 2
- Metric-Driven Verification Using vManager™ — 3
- vManager Tool Usage in Batch Mode — 0.5
- Perspec™ System Verifier - Basic NEW — 5
- Xcelium Fault Simulator NEW — 1
- Specman® Fundamentals for Block-Level Environment Developers — 5
- Specman Advanced Verification — 4

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application
- VHDL Language and Application
- C++ Language Fundamentals for Design and Verification
- Real Modeling with Verilog AMS
- SystemVerilog for Design and Verification
- SystemC® Language Fundamentals
- Real Modeling with SystemVerilog
- SystemC Synthesis with Stratus HLS
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification NEW
- UVM
  - Essential SystemVerilog for UVM (optional)
  - SystemVerilog Accelerated Verification Using UVM
- SystemVerilog Assertions
- SystemC Transaction-Level Modeling TLM2.0
- Perl for EDA Engineering
- JasperGold® Formal Fundamentals
- SVA, Formal & JasperGold® Fundamentals for Designers NEW
- Tcl Scripting for EDA
- SystemVerilog Advanced Register Verification Using UVM NEW
- JasperGold® Formal Expert NEW

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Tensilica Processor IP Learning Map

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Tensilica Xtensa LX

- Tensilica® Xtensa® LX Processor Fundamentals
- Tensilica Xtensa LX Processor Interfaces
- Tensilica Xtensa LX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design
- Tensilica System Modeling using XTSC

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine (2)
- Tensilica ConnX BBE32EP Baseband Engine
- Tensilica ConnX BBE64EP Baseband Engine (2)
- Tensilica ConnX 110 and 120 DSP Family NEW (2)

Fusion & FloatingPoint DSP

- Tensilica Fusion F1 DSP
- Tensilica Fusion G3 DSP
- Tensilica Fusion G6 DSP (2)
- Tensilica FloatingPoint DSP Family NEW

HiFi Audio DSP

- Tensilica Audio Codec API
- Tensilica HiFi 2/EP/Mini Audio Engine ISA
- Tensilica HiFi 3 Audio Engine ISA
- Tensilica HiFi 4 DSP
- Tensilica HiFi 5 DSP
- Tensilica Xtensa Audio Framework NEW

Vision DSP

- Tensilica Vision DSP Family NEW
- Tensilica Xtensa Neural Network Compiler v2 NEW
- Tensilica DNA 100 Architecture and Programming

NEW New Course | # Number of days for instructor-led course | Online Course Available

Tensilica Processor IP Learning Map

Tensilica Xtensa NX

- Tensilica® Xtensa® NX Processor Fundamentals
- Tensilica Xtensa NX Processor Interfaces
- Tensilica Xtensa NX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design
- Tensilica System Modeling using XTSC

ConnX DSP

- Tensilica ConnX B10 DSP (NEW)
- Tensilica ConnX B20 DSP (NEW) (2)

Vision DSP

- Tensilica Vision DSP Family (NEW)
- Tensilica Xtensa Neural Network Compiler v2 (NEW)

NEW New Course | # Number of days for instructor-led course | Online Course Available

Computational Fluid Dynamics

Beginner

Advanced

Fidelity

Turbomachinery

Fidelity Turbo: Introduction — 3

Meshing

Fidelity Automesh for Unstructured Meshing — 1.5

Auto Aero

Fidelity Flow — 1.5

Fine

Marine

Fine Marine for Beginners — 2.5

Fine Marine for Advanced Users — 1.75

Beginner

Advanced

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available