Control Store Summary							ALU (4 bits)				C Bus WRITE Enable											Memory Signals			Incremetation		B bus mux			
Memory address	**Instruction**	**Microinstruction**	**Break down of microinstruction**	**Next address**	**Next address in binary**	**Jump**	**3**	**2**	**1**	**0**	**MAR**	**MDR**	**PC**	**MBRU**	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**	**R9**	**Accumulator**	**FETCH**	**READ**	**WRITE**	**PC**	**Accumulator**	**3**	**2**	**1**	**0**
0	FETCH	FETCH1	MBRU ← IRAM[PC]; FETCH	1	b00000001	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1		FETCH2	PC←PC+1	xxxxxxxxxxxx	xxxxxxxxxx	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
3	NOOP		IDLE	0	b00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	CLAC		AC←0,Z=1	0	b00000000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5	LDAC	LDAC 1	AR ← AC; READ	6	b00000110	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
6		LDAC 2	IDLE	7	b00000111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7		LDAC 3	DR ← M(AC)	8	b00001000	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8		LDAC 4	AC ← DR	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
9	LDX1R1	LDX1R1 1	AR ← MBRU; READ	10	b00001010	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
10		LDX1R1 2	IDLE	11	b00001011	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11		LDX1R1 3	DR ← M(X1)	12	b00001100	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12		LDX1R1 4	AC ← DR	13	b00001101	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
13		LDX1R1 5	R1 ← AC	0	b00000000	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	LDX2R2	LDX2R2 1	AR ← MBRU; READ	15	b00001111	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
15		LDX2R2 2	IDLE	16	b00010000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16		LDX2R2 3	DR ← M(X2)	17	b00010001	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17		LDX2R2 4	AC ← DR	18	b00010010	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
18		LDX2R2 5	R2 ← AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	LDX3R3	LDX3R3 1	AR ← MBRU; READ	20	b00010100	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
20		LDX3R3 2	IDLE	21	b00010101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21		LDX3R3 3	DR ← M(X2)	22	b00010110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22		LDX3R3 4	AC ← DR	23	b00010111	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
23		LDX3R3 5	R3 ← AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	LDXXR9	LDX12R9 1	AR ← MBRU; READ	25	b00011001	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
25		LDX12R9 2	IDLE	26	b00011010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26		LDX12R9 3	DR ← M(X12)	27	b00011011	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
27		LDX12R9 4	AC ← DR	28	b00011100	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
28		LDX12R9 5	R9 ← AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
29	LDX4R6	LDX4R6 1	AR ← MBRU;READ	30	b00011110	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
30		LDX4R6 2	IDLE	31	b00011111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31		LDX4R6 3	DR ← M(X4)	32	b00100000	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32		LDX4R6 4	AC ← DR	33	b00100001	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
33		LDX4R6 5	R6 ← AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
34	SWX5R3	SWX5R3 1	AC←R3	36	b00100100	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
35	SWX12R2	SWX12R2 1	AC←R2	36	b00100100	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
36	SWXXAC	SWX5AC 1	AR← MBRU	37	b00100101	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
37		SWX5AC 2	DR ← AC ;WRITE	0	b00000000	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
38	STAC		DR ← AC ; WRITE	0	b00000000	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
39	MOVACR1		R1←AC	0	b00000000	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	MOVACR2		R2←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
41	MOVACR3		R3←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
42	MOVACR4		R4←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
43	MOVACR5		R5←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
44	MOVACR6		R6←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Control Store Summary							ALU (4 bits)				C Bus WRITE Enable											Memory Signals			Incremetation		B bus mux			
Memory address	Instruction	Microinstruction	Break down of microinstruction	Next address	Next address in binary	Jump	3	2	1	0	MAR	MDR	PC	MBRU	R1	R2	R3	R4	R5	R6	R7	R8	R9	Accumulator	FETCH	READ	WRITE	PC	Accumulator	3	2	1	0
45	MOVACR7		R7←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
46	MOVACR8		R8←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
47	MOVACR9		R9←AC	0	b00000000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
48	MOVR1AC		AC←R1	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
49	MOVR2AC		AC←R2	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
50	MOVR3AC		AC←R3	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
51	MOVR4AC		AC←R4	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1
52	MOVR5AC		AC←R5	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
53	MOVR6AC		AC←R6	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
54	MOVR7AC		AC←R7	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
55	MOVR8AC		AC←R8	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1
56	MOVR9AC		AC←R9	0	b00000000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0
57	MOVACMAR		MAR←AC	0	b00000000	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
58	MOVACMDR		MDR ←AC ; WRITE	0	b00000000	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
59	ADDR1		AC←AC+R1	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
60	ADDR2		AC←AC+R2	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
61	ADDR4		AC←AC+R4	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1
62	ADDR5		AC←AC+R5	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
63	ADDR6		AC←AC+R6	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
64	ADDR7		AC←AC+R7	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
65	LSHIFT1		AC ← AC<<1	0	b00000000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
66	RSHIFT1		AC ← AC>>1	0	b00000000	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
67	LSHIFT8		AC ← AC<<8	0	b00000000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
68	INCREMENTPC		PC←PC+1	0	b00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
69	INCREMENTAC		AC←AC+1	0	b00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
70	DECREMENTAC		AC←AC-1	0	b00000000	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
71	JUMP	JUMP1	AC← MBRU	72	b01001000	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1
72		JUMP2	PC←AC	0	b00000000	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	JMPZ	JUMPZ1		XXXXXXXX	xxxxxxxxxx	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
73		JMPZN1 (Z = 0)	NOOP	0	b00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
74		JMPZY1 (Z = 1)	AC ← MBRU	75	b01001011	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
75		JMPZY2 (Z = 1)	PC← AC	0	b00000000	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	JMPNZ	JMPNZ1		XXXXXXXX	xxxxxxxxxx	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
76		JMPNZY1 (Z = 1)	NOOP	0	b00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
77		JMPNZN1 (Z = 0)	AC ← MBRU	78	b01001110	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
78		JMPNZN2 (Z = 0)	PC← AC	0	b00000000	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0