

DEPARTMENT OF ELECTRONIC AND TELECOMMUNICATION  
UNIVERSITY OF MORATUWA  
EN3030: CIRCUITS AND SYSTEMS DESIGN



**INSTRUCTION SET ARCHITECTURE**

Mendis N. P. A.	180398A
Kumarasinge H. A. N. H.	180337M
Nagasinghe K.R.Y	180411K
Thalagala B. P.	180631J

Date of submission: 15<sup>th</sup> December 2021

# 1. INSTRUCTION SET

## 1.1. PROGRAM CONTROL

### START/ INITIALIZE

1.  $PC \leftarrow 0$
2.  $IR \leftarrow 0$

### FETCH

1.  $AR \leftarrow PC$
2.  $DR \leftarrow M, PC \leftarrow PC+1$
3.  $IR \leftarrow DR, AR \leftarrow PC$

### NOP

IDLE processor

### CLAC

1.  $AC \leftarrow 0, Z=1$

### ENDOP

End all operations

## JUMP INSTRUCTIONS

### JUMP

1. READ
2.  $AC \leftarrow IM(\tau)$
3.  $PC \leftarrow AC$

3.  $PC \leftarrow AC$
4.  $PC \leftarrow PC+1$
5. READ

### JMPZ

1. READ
2.  $AC \leftarrow IM(\tau)$

### JMPNZ

1.  $AC \leftarrow IM(\tau)$
2.  $PC \leftarrow AC$
3.  $PC \leftarrow PC+1$

## 1.2. LOAD AND STORE INSTRUCTIONS

### LDIAC

1. MEM READ
2.  $AC \leftarrow IM(\tau)$
3.  $PC \leftarrow PC+1$

3.  $DR \leftarrow M(\tau)$
4.  $AC \leftarrow DR$

### LDAC

1.  $AC \leftarrow AC$
2. READ



### STAC

1. READ AC to bus
2.  $AR \leftarrow AC$
3.  $M \leftarrow AC$

## 1.3. MOVE INSTRUCTIONS

### MOVR

1.  $R \leftarrow AC$

### MOVACR1

1.  $R1 \leftarrow AC$



### MOVACR2

1.  $R2 \leftarrow AC$

### MOVACR3

1.  $R3 \leftarrow AC$

### MOVACR4

1.  $R4 \leftarrow AC$

#### MOVACR5

1.  $R5 \leftarrow AC$

#### MOVRAC

1.  $AC \leftarrow R$

#### MOVR1AC

1.  $AC \leftarrow R1$

#### MOVR2AC

1.  $AC \leftarrow R2$

#### MOVR3AC

1.  $AC \leftarrow R3$

#### MOVR4AC

1.  $AC \leftarrow R4$

#### MOVR5AC

1.  $AC \leftarrow R5$

#### MOVAC

1.  $PC \leftarrow AC$
2.  $AR \leftarrow PC$

### 1.4. ARITHMETIC AND LOGICAL OPERATIONS

#### ALU BASED

##### ADD

1.  $AC \leftarrow AC + R$

##### SUB

1.  $AC \leftarrow AC - R$

##### MULTIPLY

1.  $AC \leftarrow AC * R$

##### DIVIDE

1.  $AC \leftarrow AC / R$

##### AND

1.  $AC \leftarrow AC \& R$

##### XOR

1.  $AC \leftarrow AC \text{ XOR } R$

##### OR

1.  $AC \leftarrow AC | R$

##### NOT

1.  $AC \leftarrow \overline{AC}$

##### LSHIFT

1.  $AC \leftarrow AC \ll R$

##### RSHIFT

1.  $AC \leftarrow AC \gg R$

#### DEDICATED ADDER BASED

##### INCREMENT PC

1.  $PC \leftarrow PC + 1$

##### INCREMENT AC

1.  $AC \leftarrow AC + 1$



##### INCREMENT R

1.  $PC \leftarrow PC + 1$

##### INCREMENT R1

1.  $R1 \leftarrow R1 + 1$

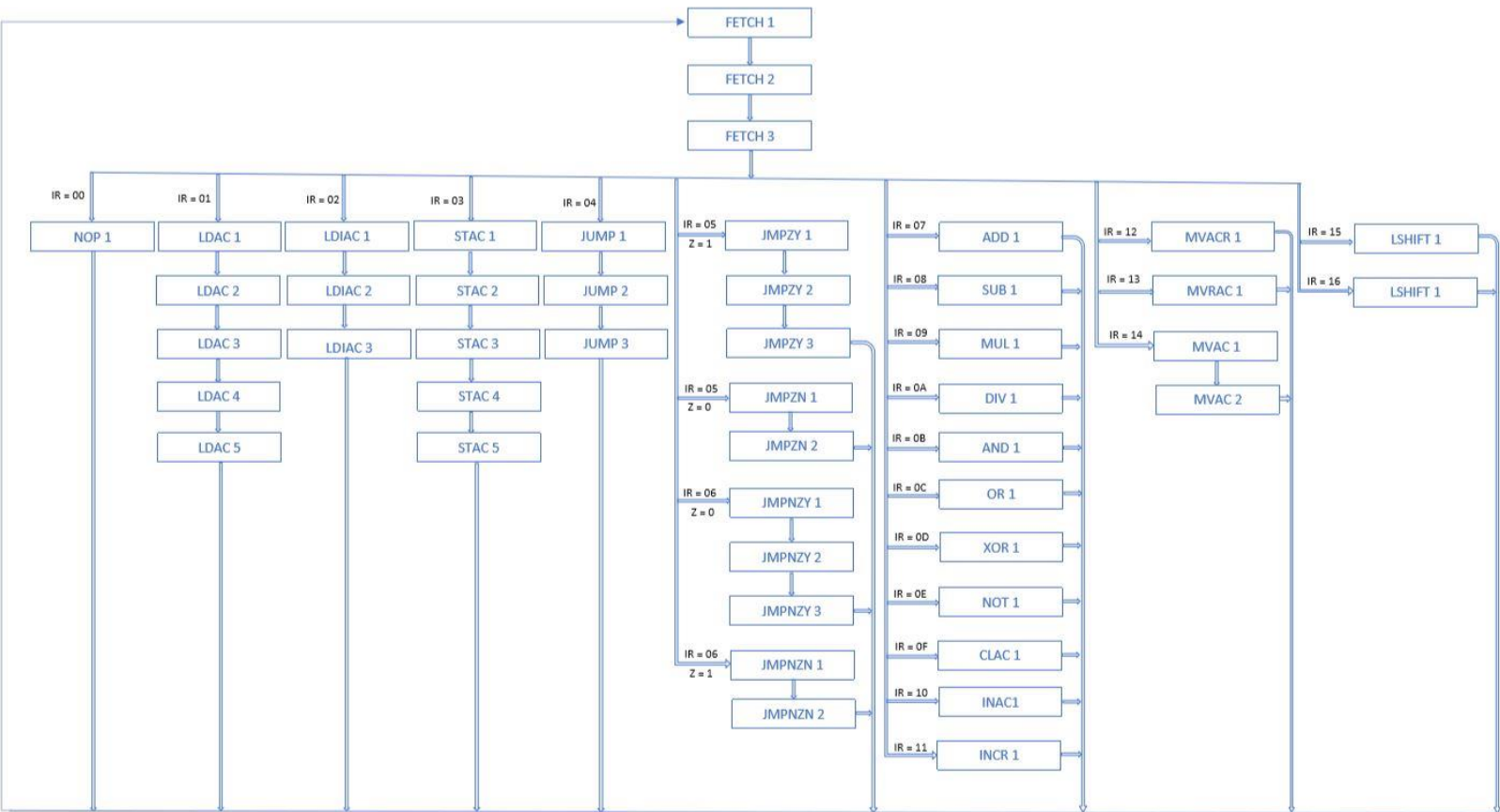
##### INCREMENT R2

1.  $R2 \leftarrow R2 + 1$

##### INCREMENT R3

1.  $R3 \leftarrow R3 + 1$

## 2. STATE DIAGRAM



### 3. DATA PATH

