

DEPARTMENT OF ELECTRONIC AND TELECOMMUNICATION
UNIVERSITY OF MORATUWA
EN3030: CIRCUITS AND SYSTEMS DESIGN



INSTRUCTION SET ARCHITECTURE

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1. INSTRUCTION SET

1.1. PROGRAM CONTROL

START/INITIALIZE

1. $PC \leftarrow 0$
2. $IR \leftarrow 0$

FETCH

1. $AR \leftarrow PC$
2. $DR \leftarrow M, PC \leftarrow PC+1$
3. $IR \leftarrow DR, AR \leftarrow PC$

NOP

IDLE processor

CLAC

1. $AC \leftarrow 0, Z=1$

ENDOP

End all operations

JUMP INSTRUCTIONS

JUMP

1. READ
2. $AC \leftarrow IM(\tau)$
3. $PC \leftarrow AC$

3. $PC \leftarrow AC$

4. $PC \leftarrow PC+1$

5. READ

JMPZ

1. READ
2. $AC \leftarrow IM(\tau)$

JMPNZ

1. $AC \leftarrow IM(\tau)$

2. $PC \leftarrow AC$

3. $PC \leftarrow PC+1$

1.2. LOAD AND STORE INSTRUCTIONS

LDIAC

1. MEM READ
2. $AC \leftarrow IM(\tau)$
3. $PC \leftarrow PC+1$

3. $DR \leftarrow M(\tau)$

4. $AC \leftarrow DR$

LDAC

1. $AC \leftarrow AC$
2. READ

STAC

1. READ AC to bus
2. $AR \leftarrow AC$
3. $M \leftarrow AC$

1.3. MOVE INSTRUCTIONS

MOV R

1. $R \leftarrow AC$

MOVACR2

1. $R2 \leftarrow AC$

MOVACR1

1. $R1 \leftarrow AC$

MOVACR3

1. $R3 \leftarrow AC$

MOVACR4

1. $R4 \leftarrow AC$

MOVACR5

1. $AC \leftarrow R5$

MOVRA

1. $AC \leftarrow R$

MOVR1AC

1. $AC \leftarrow R1$

MOVR2AC

1. $AC \leftarrow R2$

MOVR3AC

1. $AC \leftarrow R3$

MOVR4AC

1. $AC \leftarrow R4$

MOVR5AC

1. $AC \leftarrow R5$

MOVAC

1. $PC \leftarrow AC$
2. $AR \leftarrow PC$

1.4. ARITHMETIC AND LOGICAL OPERATIONS

ALU BASED**ADD**

1. $AC \leftarrow AC + R$

SUB

1. $AC \leftarrow AC - R$

MULTIPLY

1. $AC \leftarrow AC * R$

DIVIDE

1. $AC \leftarrow AC / R$

AND

1. $AC \leftarrow AC \& R$

XOR

1. $AC \leftarrow AC \text{ XOR } R$

OR

1. $AC \leftarrow AC | R$

NOT

1. $AC \leftarrow \overline{AC}$

LSHIFT

1. $AC \leftarrow AC << R$

RSHIFT

1. $AC \leftarrow AC >> R$

DEDICATED ADDER BASED**INCREMENT PC**

1. $PC \leftarrow PC + 1$

INCREMENT AC

1. $AC \leftarrow AC + 1$

INCREMENT R

1. $PC \leftarrow PC + 1$

INCREMENT R1

1. $R1 \leftarrow R1 + 1$

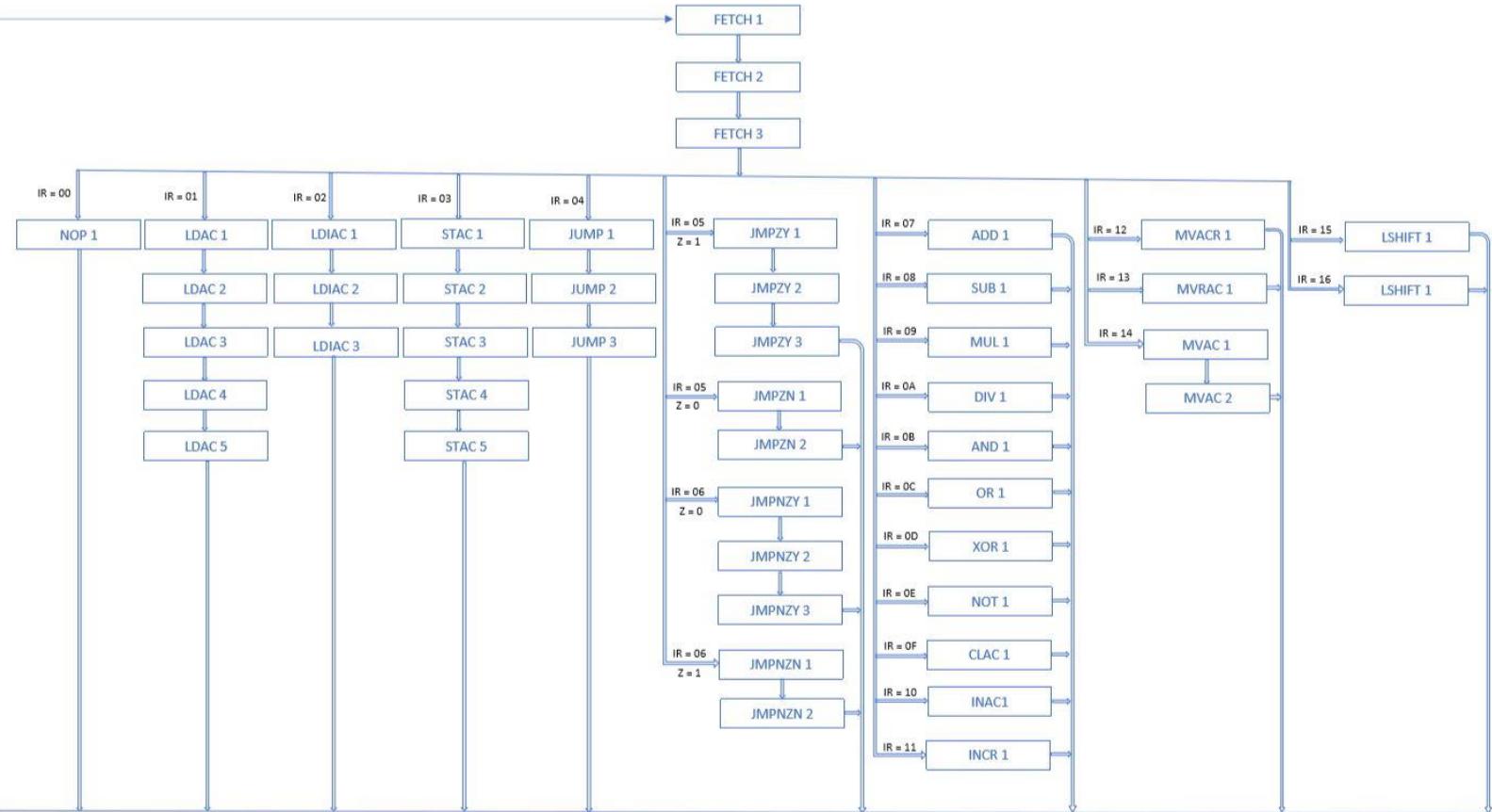
INCREMENT R2

1. $R2 \leftarrow R2 + 1$

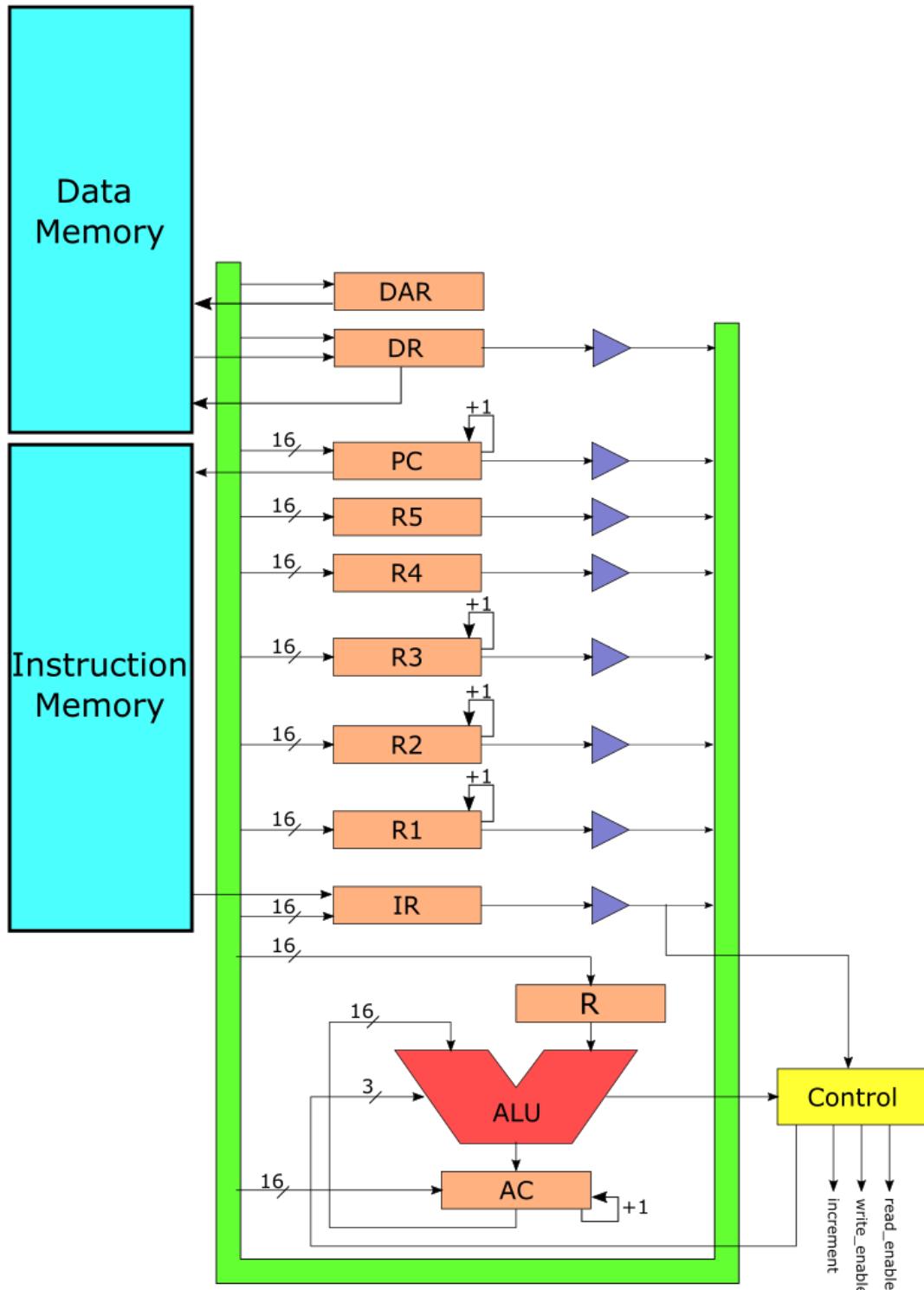
INCREMENT R3

1. $R3 \leftarrow R3 + 1$

2. STATE DIAGRAM



3. DATA PATH



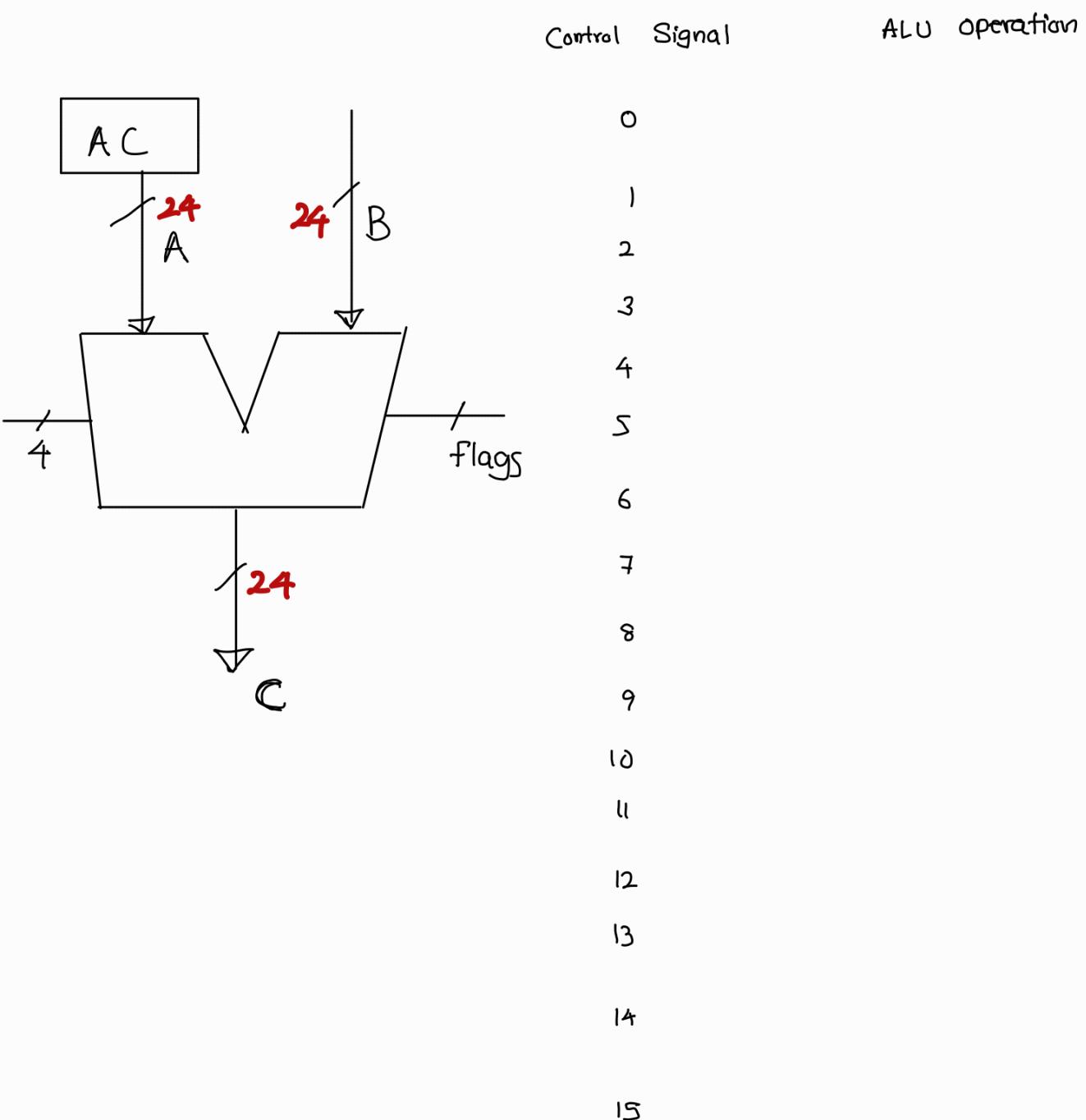
Architecture

- Data Memory \rightarrow Pixel Value 0 - 255 (8 bits)
 $256 \times 256 = 65536 (2^{16})$
- Instruction Memory \rightarrow ROM block
8 by 256 256 instructions
8 bits wide

Registers

- Program Counter \rightarrow 8 bits $2^8 = 256$ instructions
- Memory Address Register (MAR) \rightarrow 16 bits 2^{16}
Hold addresses of data memory
- Memory Buffer Register Unit \rightarrow 8 bits
hold the fetched instruction
- Accumulator \rightarrow 24 bits (check width)
(AC) Direct connection to the ALU
- L, C1, C2, C3, T, E Registers } General Purpose Registers
R1, R2, R3, R4, R5, R6 } 24 bits wide
9 registers

• ALU → control bits = number of operations
 4 bits , $2^4 = 16$ operations.

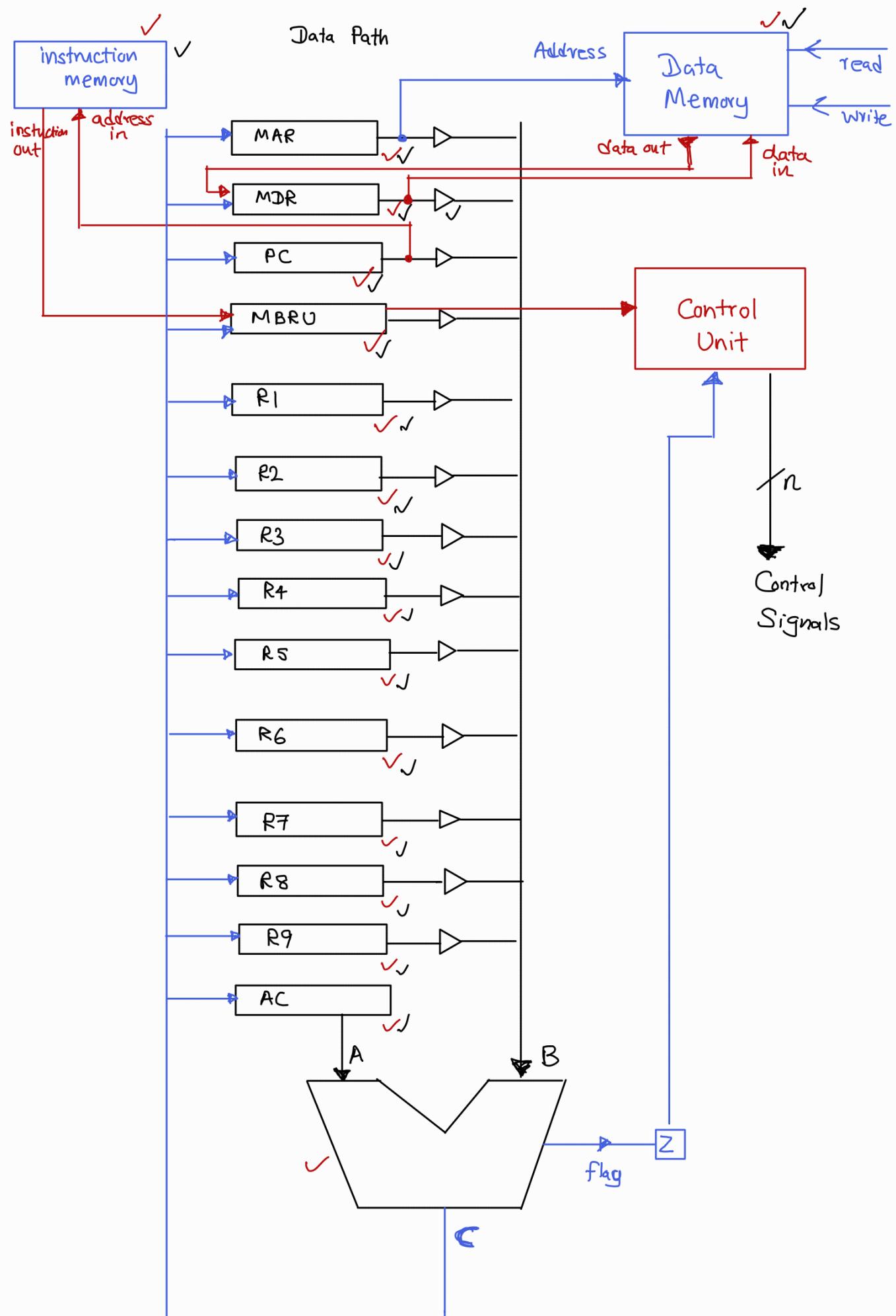


Data Bus **24 bits**

A - direct connected to AC

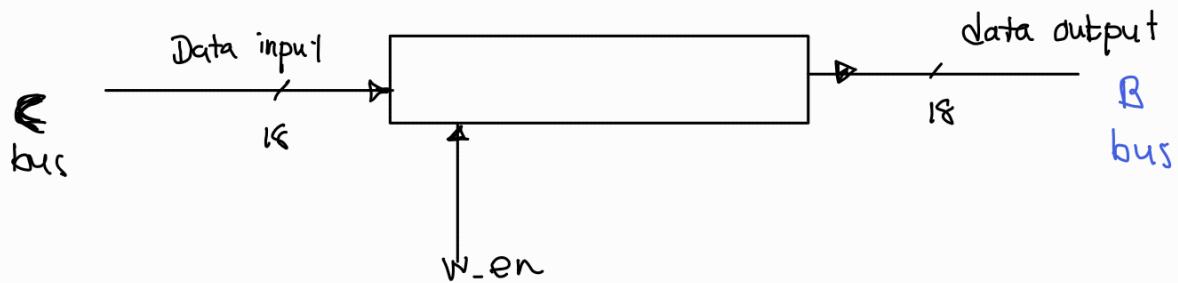
B - Multiple Register Access

C - Output Bus

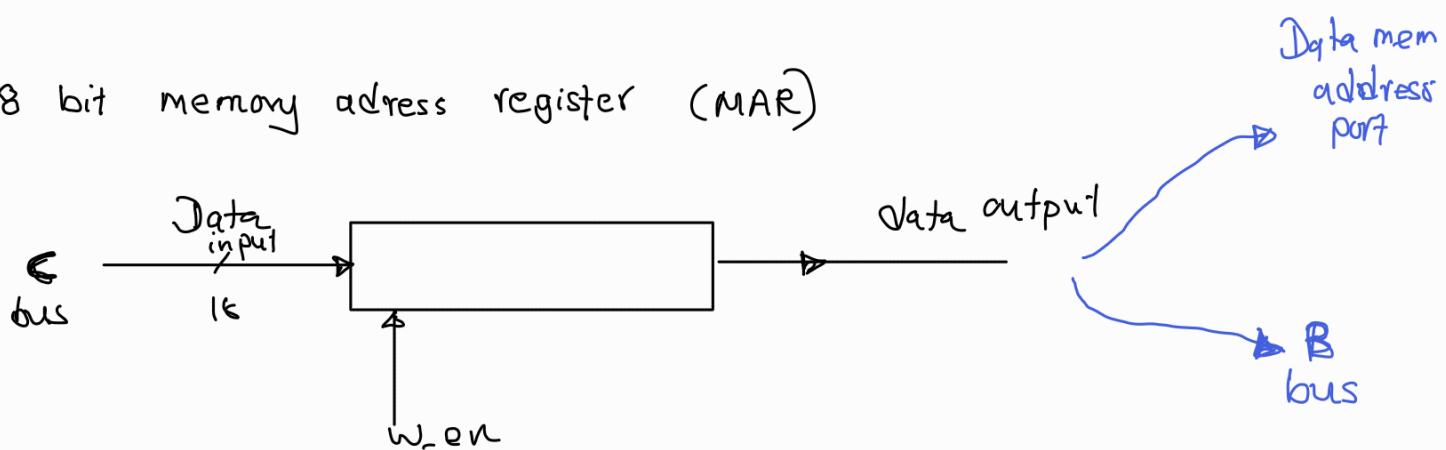


Modules

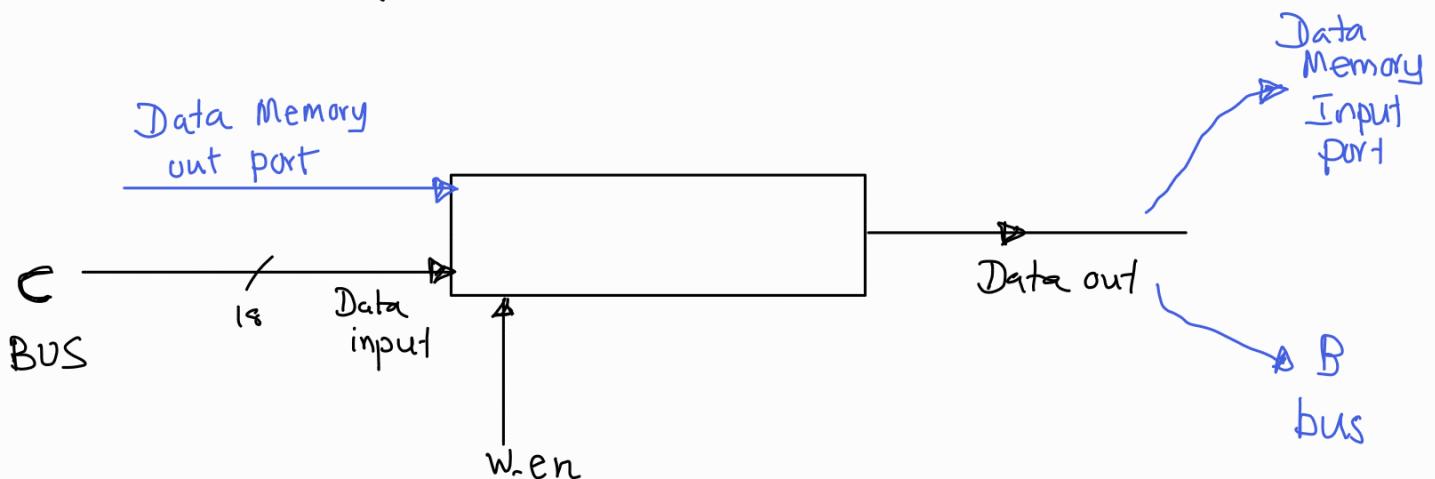
18 bit general purpose register



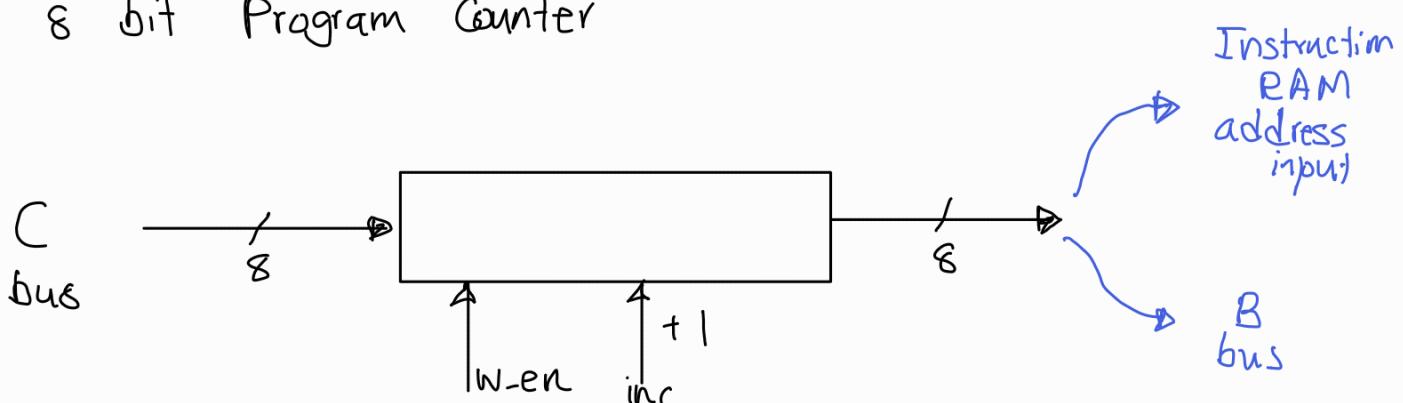
18 bit memory address register (MAR)



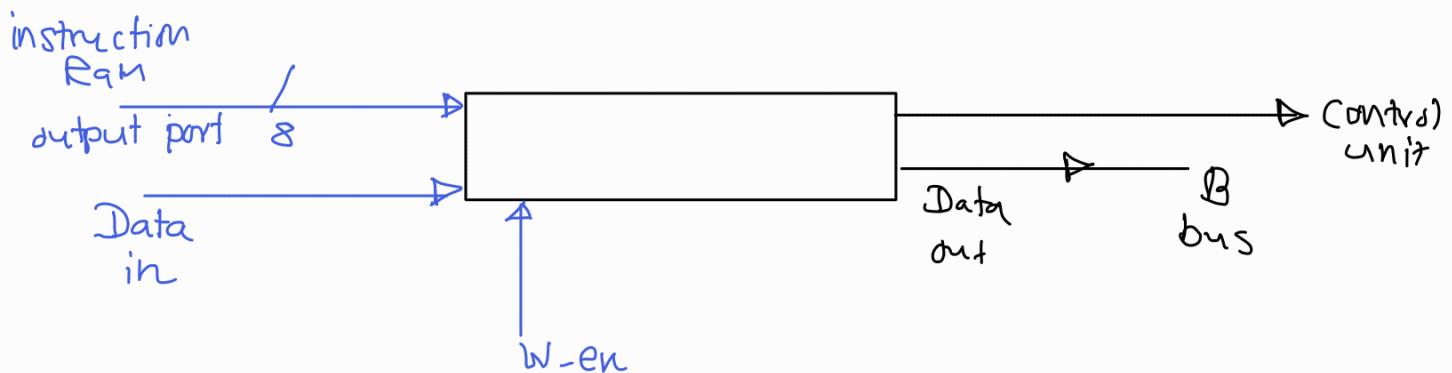
18 bit memory address register (MDR)



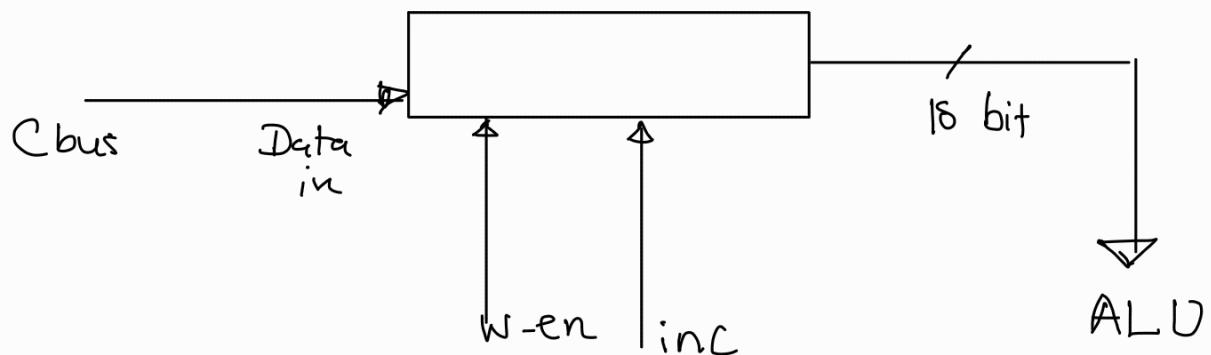
8 bit Program Counter



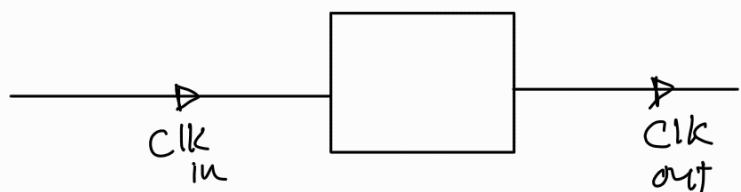
8 Memory Buffer Register unit (MBRU)



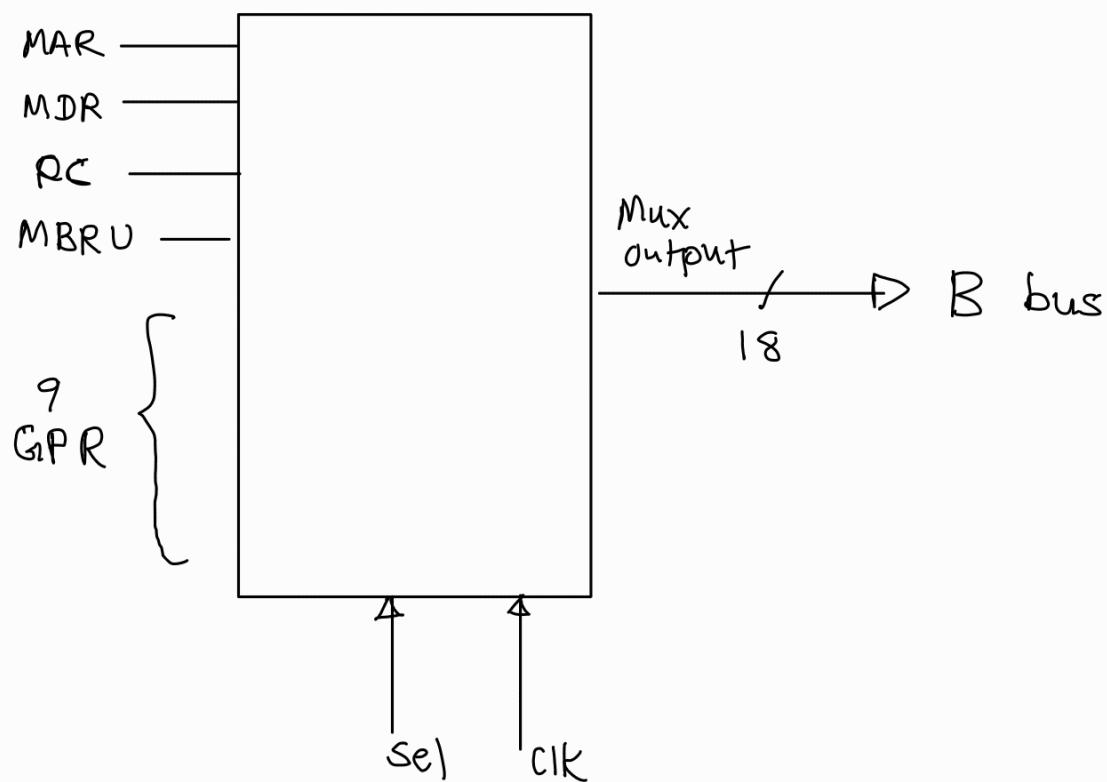
18 bit accumulator



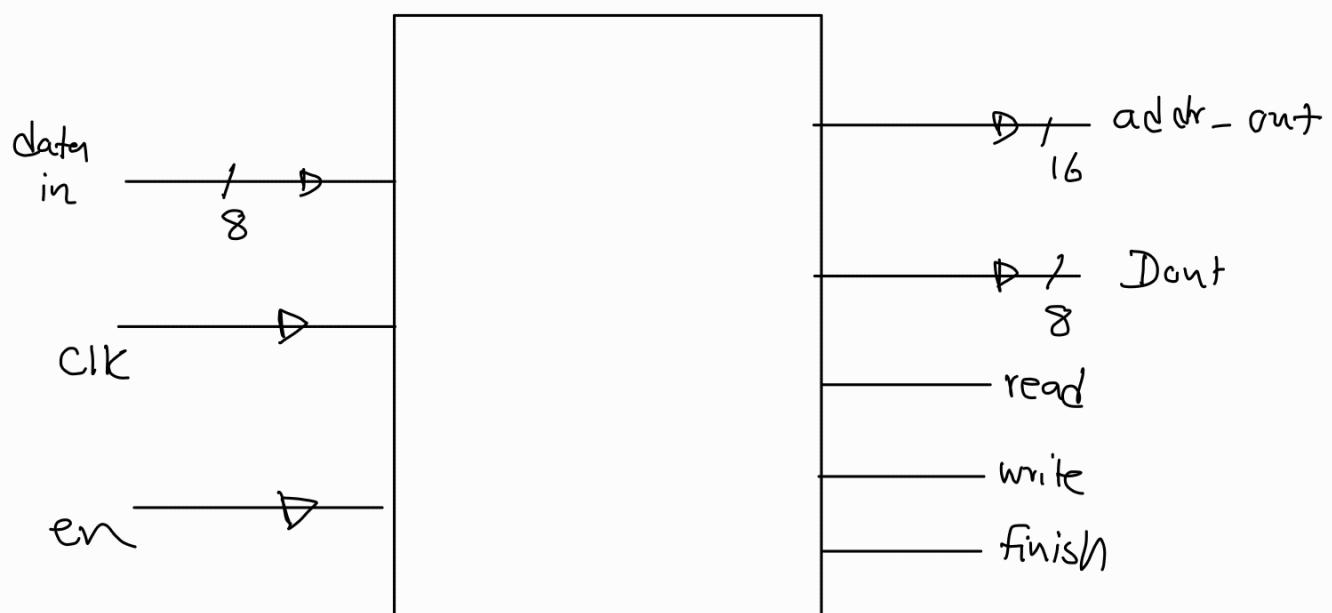
Clock Divider circuit



B bus MUX



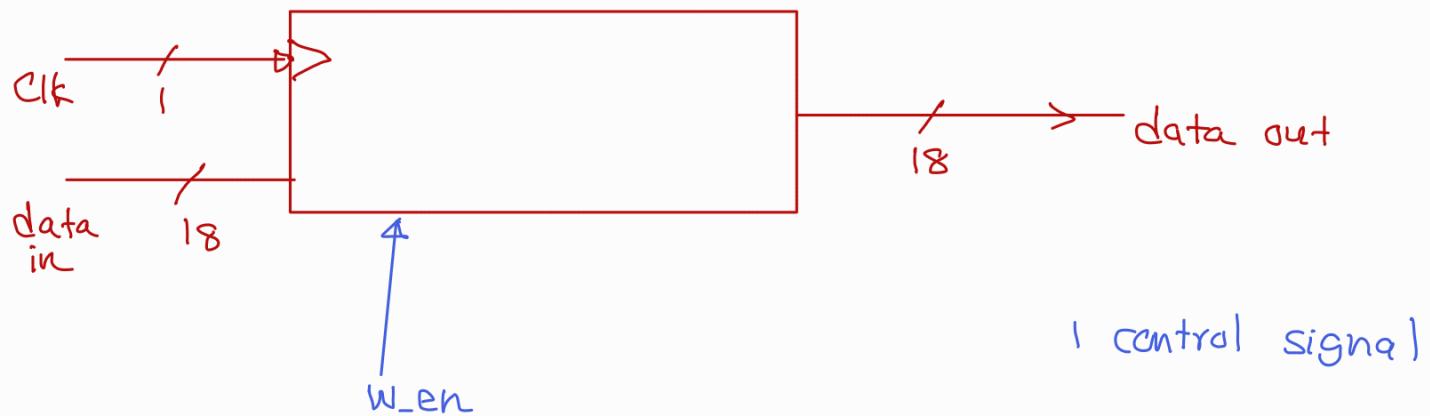
Processor



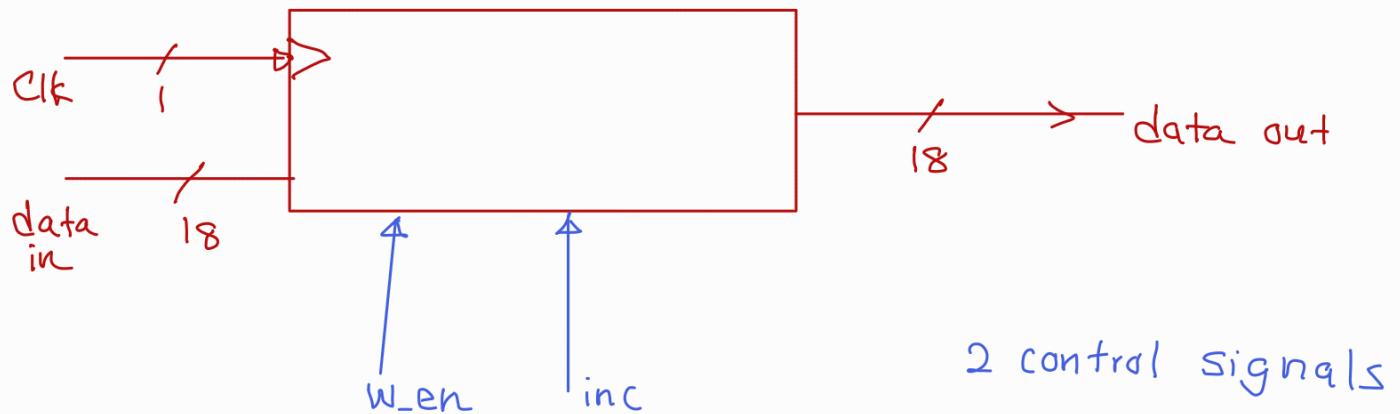
Communication

Implemented blocks

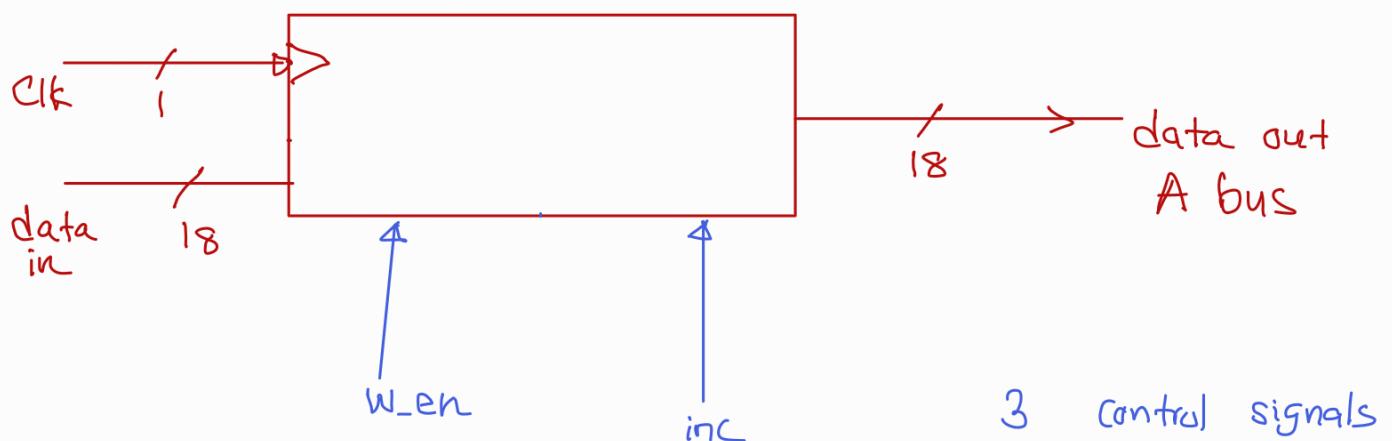
Register R1, R2, R3, R4, R5, R6, R7, R8, R9



Register With increment.

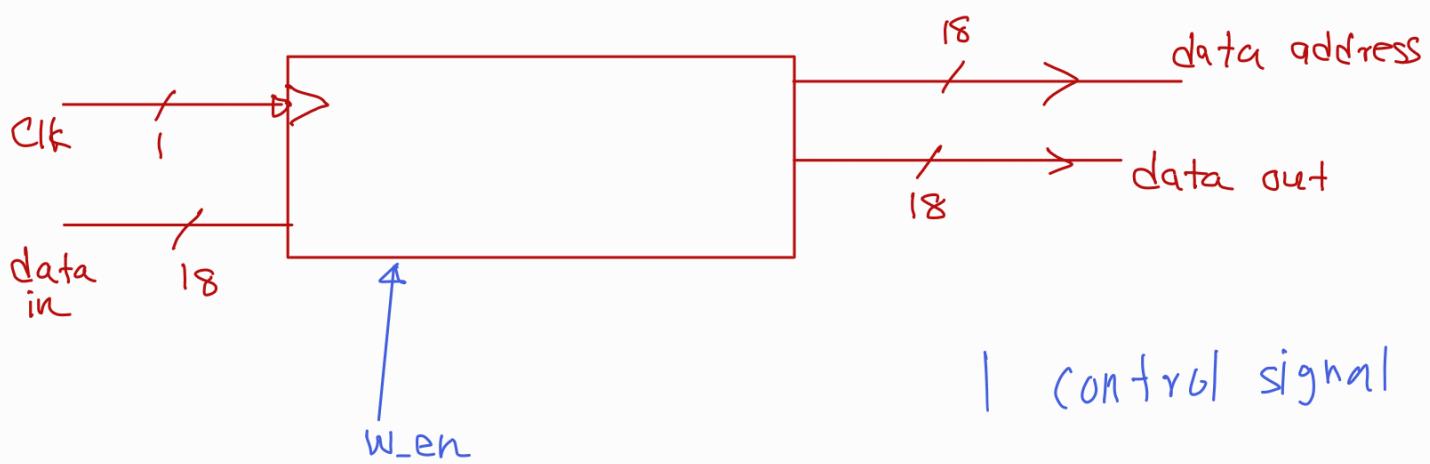


Accumulator.



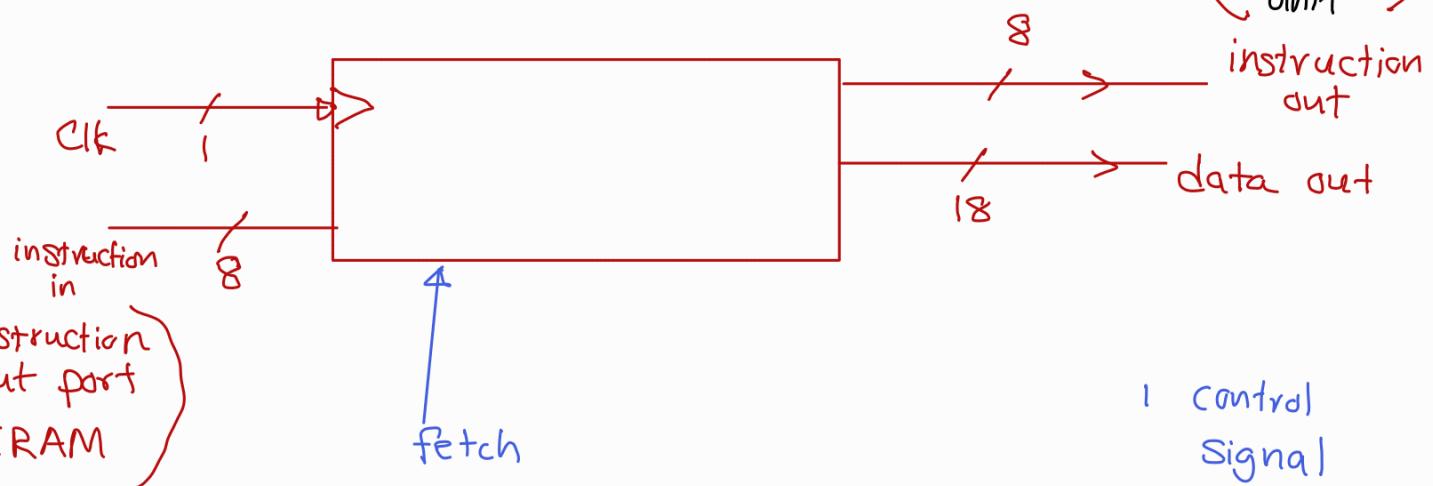
MAR

Data Ram
address part



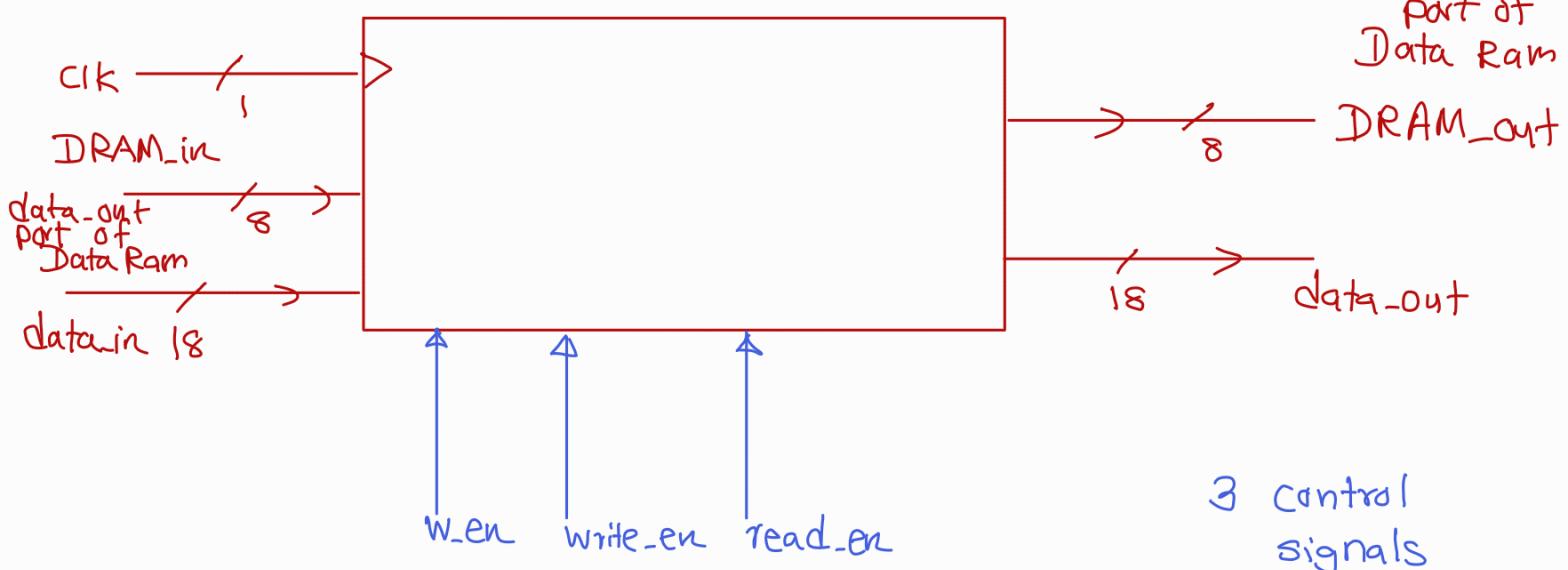
MBRU

(instr_in
part of
Control
unit)

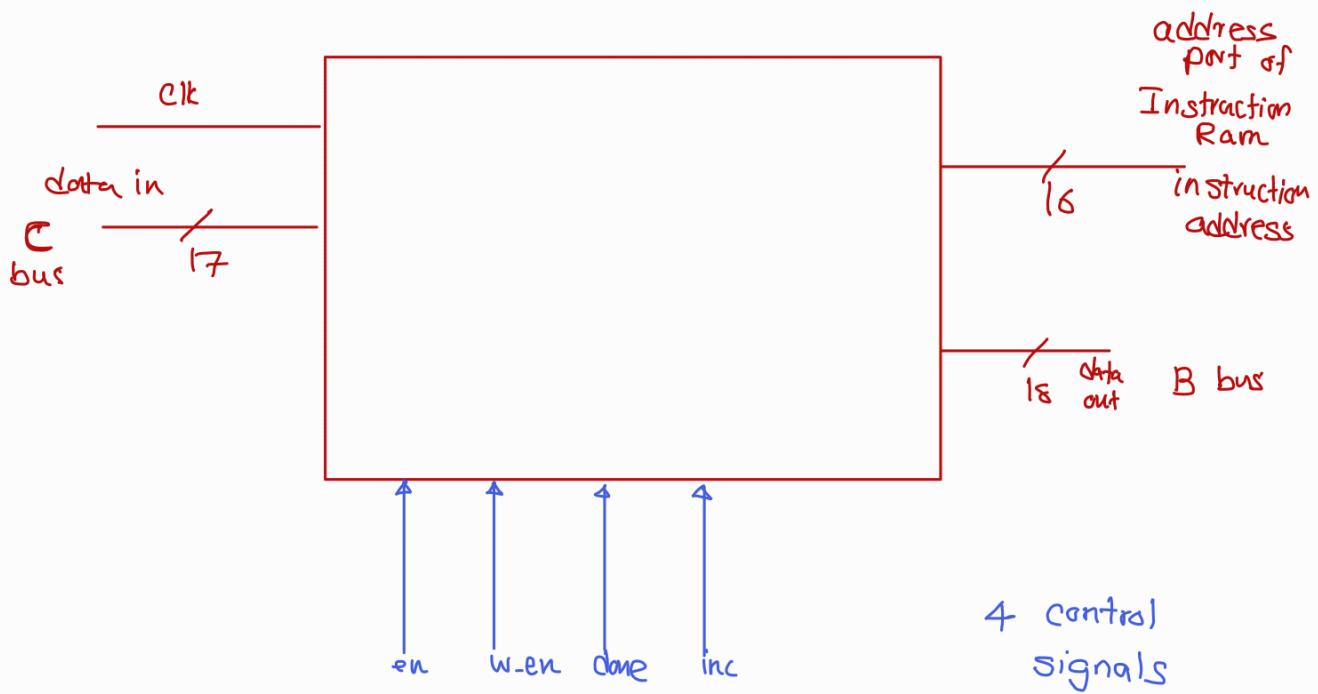


MDR connected to data memory

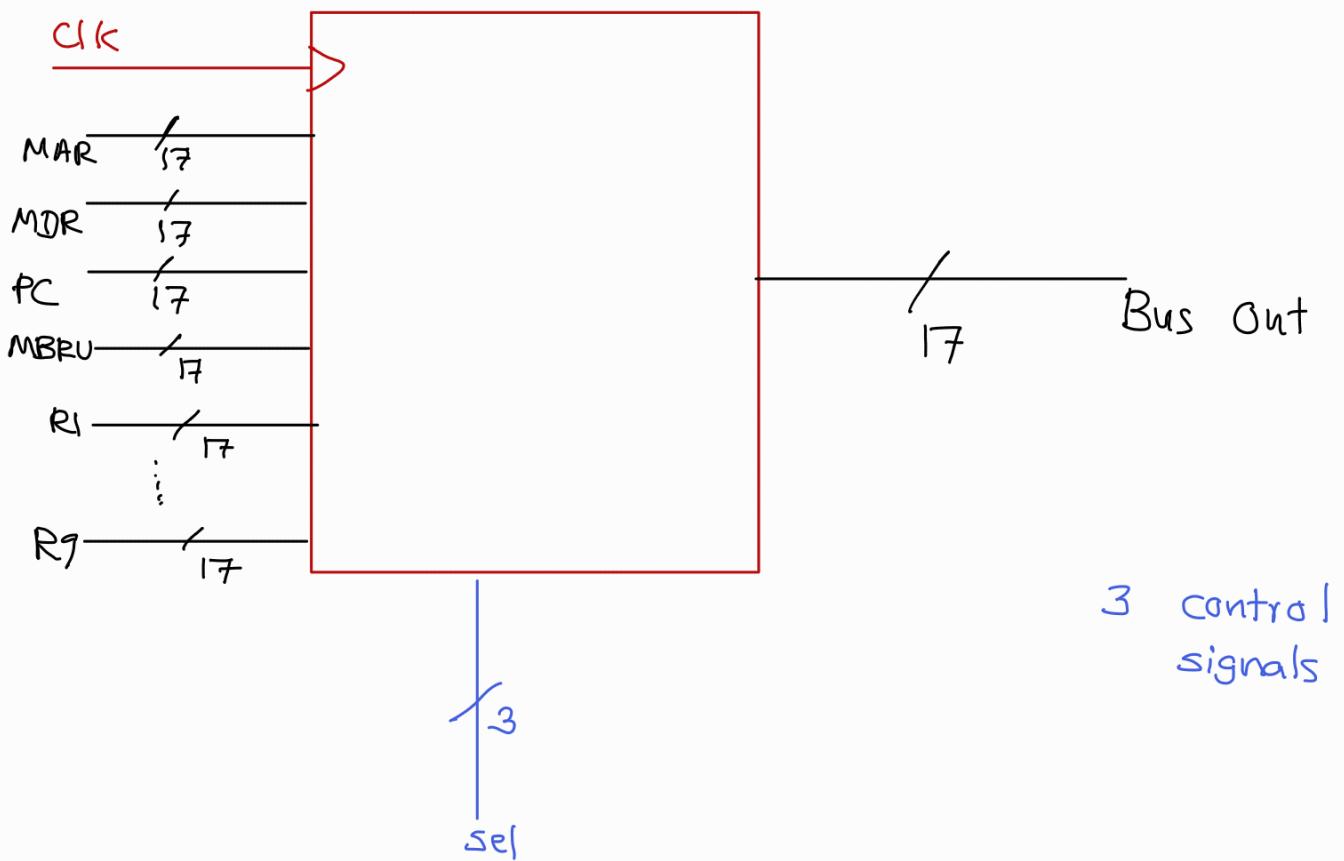
data_in
part of
Data Ram



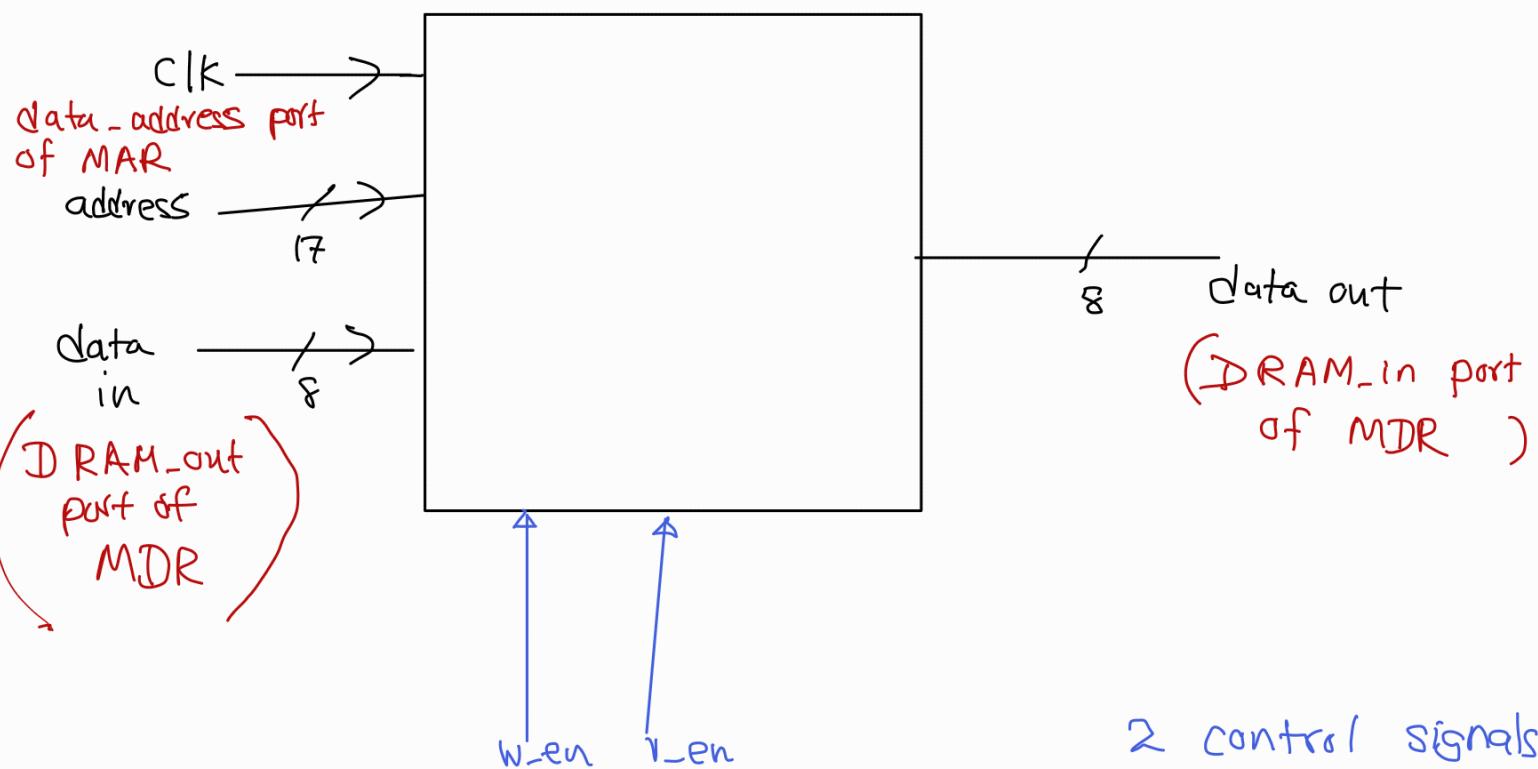
Program Counter



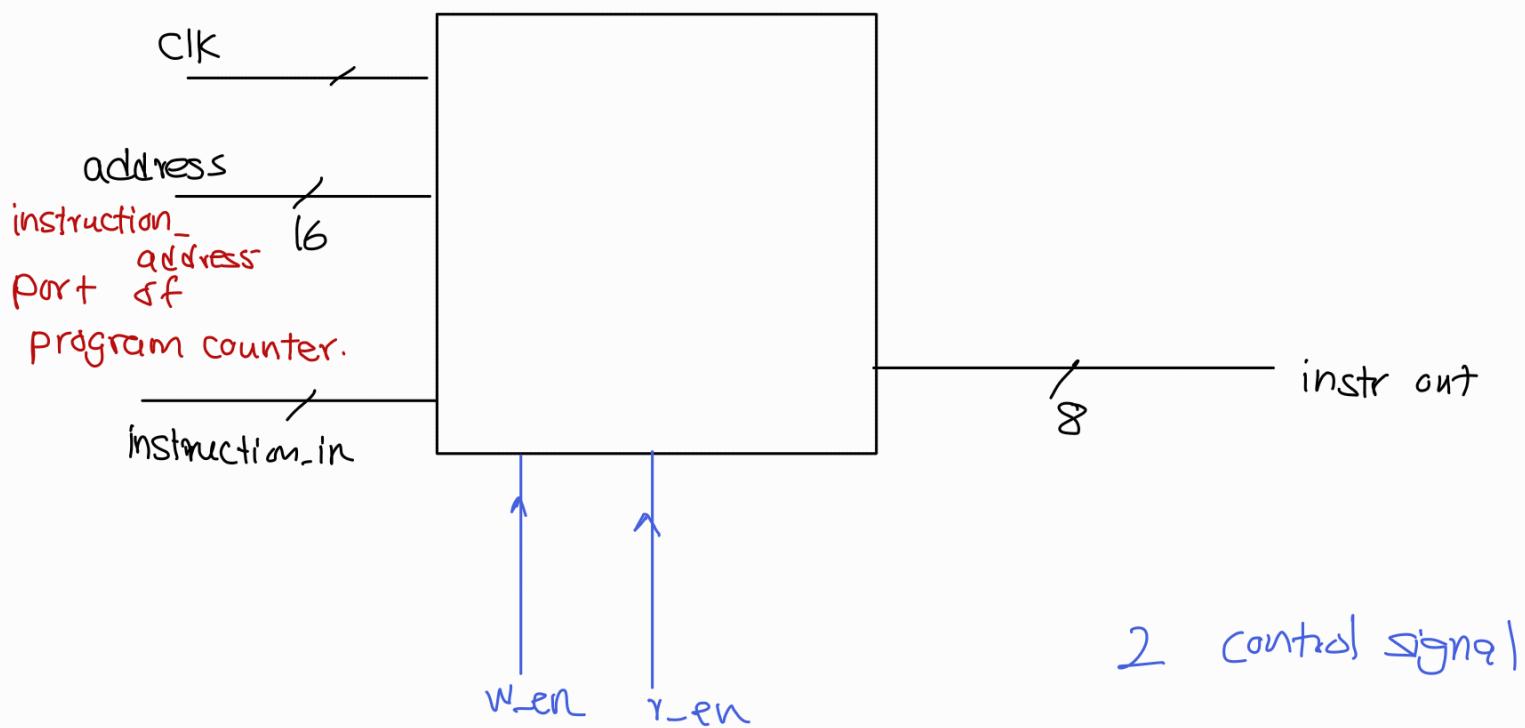
B bus Mux



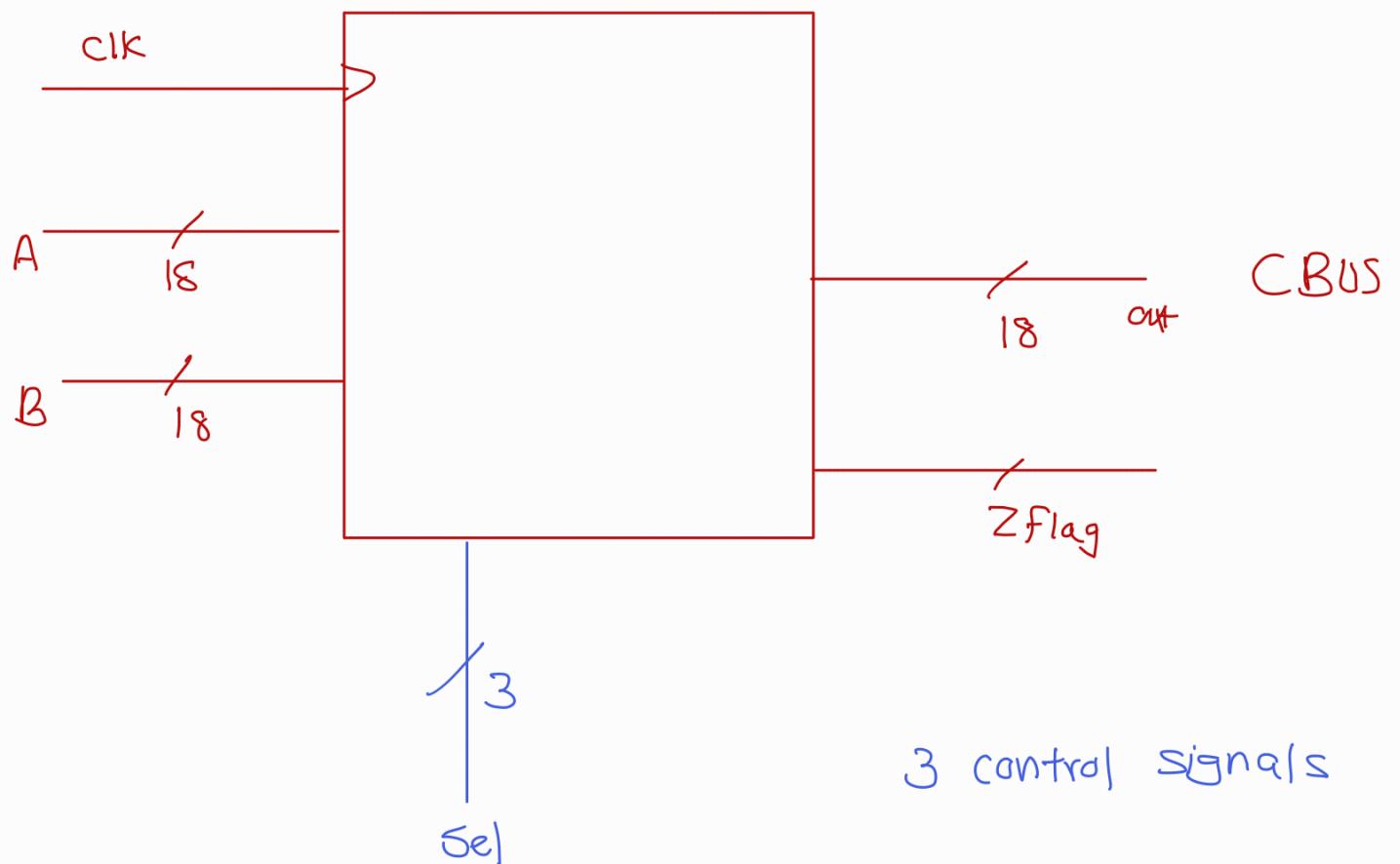
Data RAM



Instruction RAM



ALU



Control bits

18 bit general purpose
registers

R1	w_en ✓
R2	w_en ✓
R3	w_en ✓
R4	w_en ✓
R5	w_en ✓
R6	w_en ✓
R7	w_en ✓
R8	w_en ✓
R9	w_en ✓

Accumulator w_en ✓
 inc ✓

MAR w_en ✓

MDR w_en ✓

PC w_en ✓
 inc ✓

MBRU w_en ✓

ALU

4 bit selection ✓

B bus MUX

4 bit selection

output from B bus

1 MAR

2 MDR

3 PC

4 MBRU

5 R1

6 R2

7 R3

8 R4

9 R5

10 R6

11 R7

12 R8

13 R9

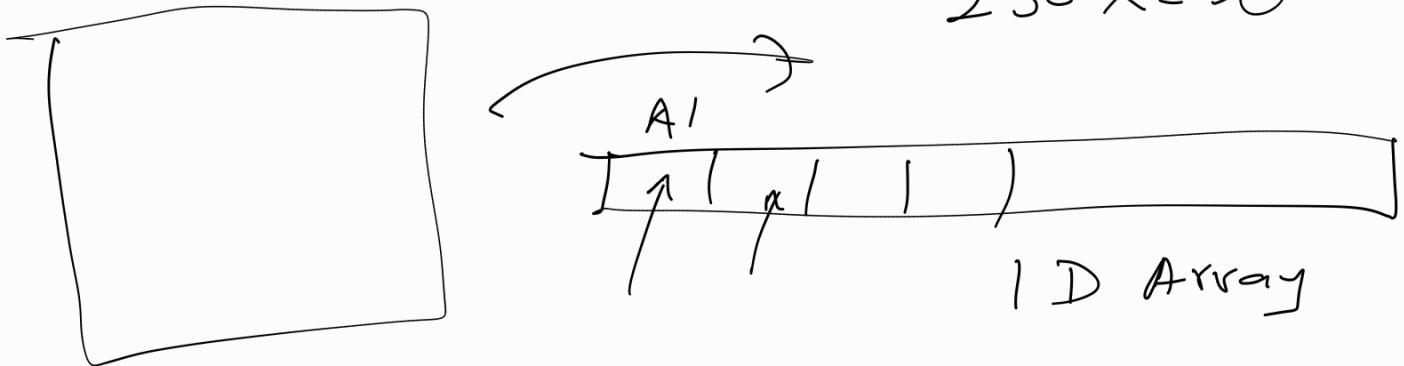
14

15

16

	x Jump 1 bit		
	x x x x ALU operation 4bits	x MAP MDR PC MBRU R1 R2 R3 R4 R5 R6 R7 R8 R9 Accumulator	C bus write enable. 14 bits
		x PC Accumulator	Incrementation 2bits
		x x x x 4bits	B bus mux

256×256



$\text{ram}[\sigma] = A_1$

$\text{ram}[\tau] = A_2$