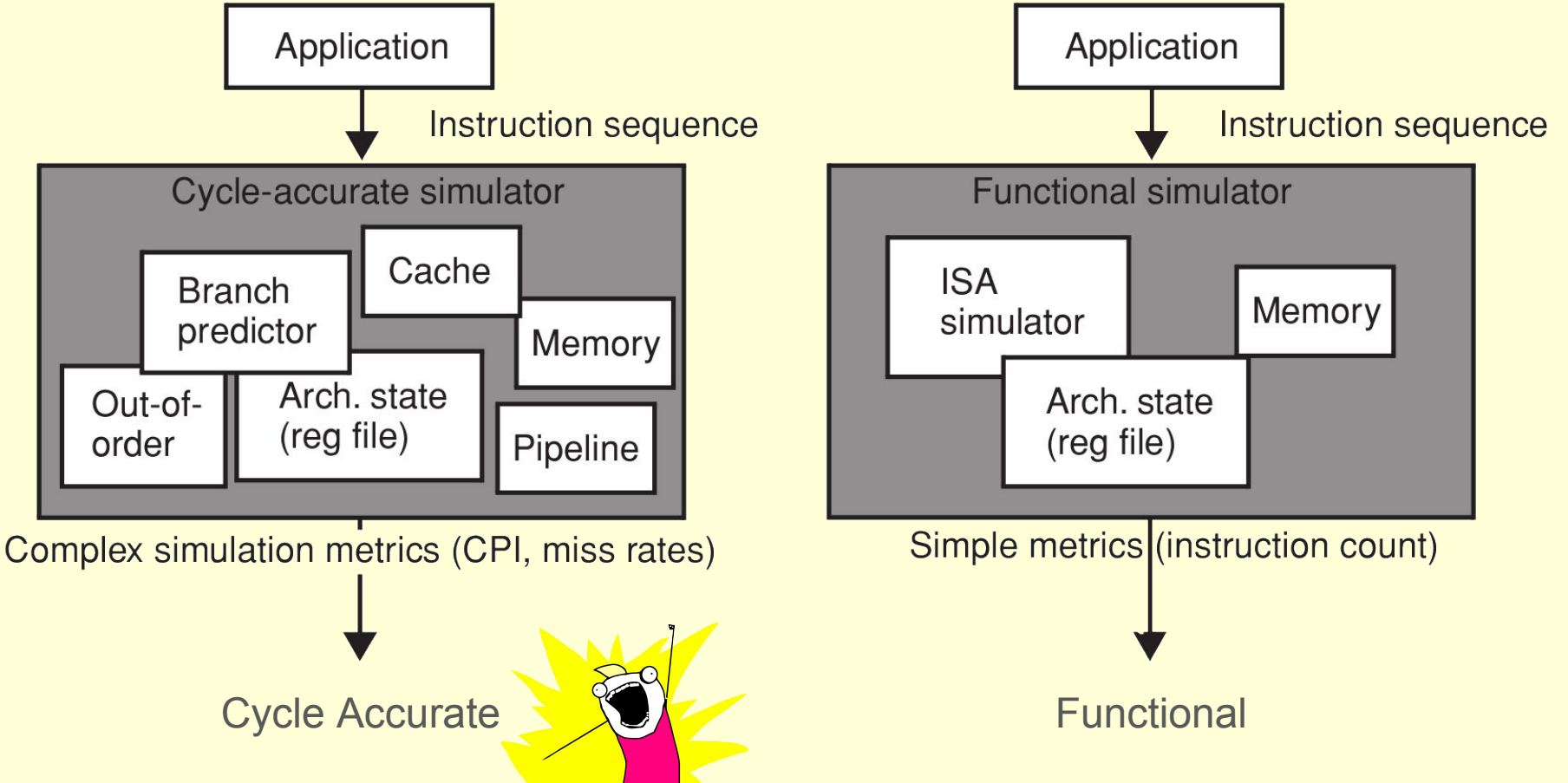
# Cycle Accurate versus Functional



# Cycle Accurate versus Functional

**Functional - no/limited model of the micro architecture**

- An (add) instruction of the target can be translated to an (add) instruction on the host, and be simulated that way.
- Example 1: Simple Scalar sim-fast
- Example 2: QEMU, Full-system emulator using dynamic translation

**Cycle Accurate - includes model of the micro architecture**

- Block resources in the pipeline when instruction executes
- Use target branch predictor scheme
- Out-of-order execution
- Example: Simple Scalar sim-outorder