Government of Karnataka
Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title: Fundamentals of Digital Electronics		Course Code:15MC21T
Mode (L:T:P) : 4:0:0	Credits:4	Core/ Elective: Core
Type of Course: Lectures & Student Activities		Total Contact Hours: 52
CIE= 25 Marks		SEE= 100 Marks

Prerequisites: Knowledge of Mathematics, Basic Electrical and Electronics Engineering

Course objective: Understand the integrated approach to mechatronics system and basics of Digital system

Course Outcomes: At the end of the course, the students will be able to

1. Understand interdisciplinary & integrated approach to Mechatronics engineering and differentiate analog/digital signals
2. Understand number system concepts, conversion rules, and different codes and apply the same to perform arithmetic operations on numbers.
3. Apply different Boolean laws, rules and K-map to simplify Boolean expressions and Implement the logic gates to perform a specific logic function.
4. Implement various combinational circuits
5. Implement Synchronous and Asynchronous sequential circuits
6. Implement programmable logic devices

Course Outcome		Cognitive level	Linked with PO	Teaching Hours
CO1	Understand interdisciplinary & integrated approach to Mechatronics engineering and differentiate analog/digital signals	*U*	1,2	4
CO2	Understand number system concepts, conversion rules, and different codes and apply the same to perform arithmetic operations on numbers	*U/A*	1,2	8
CO3	Apply different Boolean laws, rules and K-map to simplify Boolean expressions and Implement the logic gates to perform a specific logic function	*R/U/A*	1,2	10
CO4	Implement various combinational circuits	*U/A*	1,2	12
C05	Implement Synchronous and Asynchronous sequential circuits	*U/A*	1,2	13
C06	Implement programmable logic devices	*U/A*	1,2	5
		Total sessions		**52**

Legend: R; Remember, U: Understand A: Application

Mapping of Course Outcomes with Program Outcomes

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Fundamentals Of Digital Electronics	**3**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.
If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3
If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2
If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1
If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Content and Weightage For SEE

Unit No	Unit Name	CO	Hour	Marks allocated for different Cognitive level Questions			Marks weightage (%)
				R	U	A	
1	Introduction to Mechatronics and Digital principles	**1**	**4**	**-**	**15**	**-**	**10.34**
2	Number System	**2**	**8**	**-**	**05**	**15**	**13.79**
3	Logic gates & Boolean algebra	**3**	**10**	**05**	**-**	**25**	**20.68**
4	Combinational Logic Circuits	**4**	**12**	**-**	**05**	**25**	**20.68**
5	Sequential Logic Circuits	**5**	**13**	**-**	**15**	**20**	**24.13**
6	Programmable Logic Devices	**6**	**5**	**-**	**05**	**10**	**10.34**
	Total		**52**	**145 Marks**			**100**

Contents

Unit-I

Introduction to Mechatronics and Digital principles

Introduction to Mechatronics – Definition, Mechatronics system, building block, domains, constituents, key elements, applications, merits & demerits. Introduction to Digital system – Definition of analog and digital signals, examples, Comparisons, Advantages of digital technology, Digital system design stages.

4 Hours

Unit-II

Number System

Review of Binary, Octal & Hexadecimal number systems , Conversion of numbers from one radix to another radix , Binary arithmetic operations , Representation of signed numbers , Subtraction of numbers using 1's and 2's complement arithmetic , Numeric codes - BCD, Excess-3, Gray code , Alphanumeric codes - ASCII , EBCDIC.

8 Hours

Unit-III

Logic gates & Boolean algebra

Logic gates – AND , OR , NOT , NAND , NOR , EX-OR and EX-NOR , Implementation of logic functions using gates , Universal gates , Characteristics of logic gates-Boolean postulates and laws , Demorgan's theorems, Boolean expressions minimization using Boolean laws , Karnaugh map minimization.

10 Hours

Unit-IV

Combinational Logic Circuits

Design procedure – Half adder , Full adder , Half Subtractor , Full Subtractor, Binary Ripple carry adder , Multiplexer – 2:1 Mux, 4.1 Mux & 8.1 Mux, De-multiplexer – 1: 4 De-mux & 1:8 De-mux, Encoder – DECIMAL to BCD, Decoder – 3 to 8 line & BCD to DECIMAL Decoders , Magnitude Comparator - 1-bit Comparator, Parity generators-4 bit Parity generator.

12Hours

Unit-V

Sequential Logic Circuits

Introduction, comparison with combinational circuits, Flip-Flops - Types of triggering , Edge triggered S-R, D , J-K, T, J-K Master slave Flip-Flop's, Race around condition, Applications , Shift Registers, Types – SISO, SIPO, PISO, PIPO, Bidirectional shift register , Applications , Counters – Classification, comparisons , Asynchronous Ripple counters (4-bit up ,4-bit down), 3-bit Asynchronous Up/Down counter, Modulo-N Ripple Counters - Mod-5 & Mod-10 (up counters), Mod-3 Synchronous up counter , Applications.

13 Hours

Unit-VI

Programmable Logic Devices

Introduction, Basic structure of PLD'S – PAL, PLA, PROM, Implementation of simple combinational logic circuits and Boolean expressions using PLD's, Advantages, Comparisons. **5 Hours**

Reference:

1. Mechatronics – M D Singh , J G Joshi.---PHI Publication
2. Fundamentals of Digital circuits – A.Anand Kumar , 3rd edition , PHI publication.
3. Digital Fundamentals - Thomas L. Floyd, Pearson Education.
4. Digital Fundamentals- Basavaraju
5. Mechatronics –K P Ramachandran , G K Vijayaragavan , M S Balasundaram---WILEY Publication
6. Logic and computer design fundamentals – M.Moris Mano,Charles.R.Kime
7. Digital Electronics – By Tokchim , Tata McGraw-Hill Edition

e-Reference:

1. www.sriengg.com
2. www.ssit.edu.in
3. http://www.wiziq.com/tutorial/567997-digitalelectronicslecture/introduction
4. www.authorstream.com/presentation/psureshvenugopal-1137243-digitalelectronicsbasics

Student Activity

Activity No	Description of the Activity
1	Write a chart to represent decimal numbers from 0 to 50 in binary, octal and hexadecimal number systems.
2	Collect the information about any three digital systems and highlight the difference between analog and digital systems.
3	Collect the information on signed and unsigned binary numbers. Prepare a chart to represent the decimal numbers from -20 to +20 in 8-bit format in signed and signed-magnitude representation.
4	Perform binary multiplication and division with examples.
5	List the features of BCD, ASCII excess-3 codes with examples.
6	Simulate a realistic digital circuit containing at least six logic gates
7	Collect the catalogues and specification sheets or a chart displaying various logic ICs (At least 10)

Note:

1. Each student should do above activity or any other similar activity related to the course COs and get it approved from concerned Teacher and HOD.
2. No student should have activity repeated or similar
3. Teacher should ensure activities by group must cover all COs
4. Teacher should asses every student by using suitable **Rubrics** approved by HOD

Rubrics

Dimension	Exemplary	Accomplished	Developing	Beginning	Roll No. of the Student				
	5/4	3	2	1	1	2	3	4	5
Organization	Information presented in logical, interesting sequence	Information in logical sequence	Difficult to follow presentation--student jumps around	Cannot understand presentation--no sequence of information	Ex: 2				
Subject Knowledge	Demonstrates full knowledge by answering all class questions with explanations and elaborations	At ease with expected answers to questions but does not elaborate	Uncomfortable with information and is able to answer only rudimentary questions	Does not have a grasp of the information. Cannot answer questions about subject	3				

Graphics	Explain and reinforce screen text and presentation	Relate to text and presentation	Occasionally uses graphics that rarely support text and presentation	Uses superfluous graphics or no graphics	4				
Oral Presentation	Maintains eye contact and pronounces all terms precisely. All audience members can hear	Maintains eye contact most of the time and pronounces most words correctly. Most audience members can hear presentation	Occasionally uses eye contact, mostly reading presentation, and incorrectly pronounces terms. Audience members have difficulty hearing	Reads with no eye contact and incorrectly pronounces terms. Speaks too quietly	5				
Total Score=2+3+4+5=14/4=3.5=4									

Course Assessment Pattern

Particulars			**Max Marks**	**Evidence**	**Course outcomes**
Direct Assessment	**CIE**	Three test (Average of three tests)	20	Blue books	1,2,3,4,5,6
		Student Activity	05	Student Activity Sheets	1,2,3,4,5,6
	SEE	End of the course	100	Answer scripts at BTE	1,2,3,4,5,6
Indirect Assessment	**Student Feedback on course**	Middle of the course		Feedback forms	1, 2&3
		End of the course		Feedback forms	1,2,3, 4, 5&6

Note: I.A. test shall be conducted for 20 marks. Average marks of three tests shall be rounded off to the next higher digit.

FORMAT OF I A TEST QUESTION PAPER (CIE)

Test/Date and Time	Semester/year	Course/Course Code	Max Marks
Ex: I test/6 th weak of sem 10-11 Am	I/II SEM		20
	Year:		

Name of Course coordinator : Units:__

CO's:____

Question no	Question	MARKS	CL	CO	PO
1					
2					
3					
4					

Note: Internal Choice may be given in each CO at the same cognitive level (CL).

Model Question Paper (CIE)

Date and Time	Semester	Course	Max Marks
2Test(10 th weak of sem) 10-11 Am	II SEM	Fundamentals Of Digital Electronics	20
	Year: 2015-16	Course code:15MC21T	

Name of Course coordinator : **Units:3,4 Co: 3,4**

All questions carries equal marks

Question No	Question	CL	CO	PO
1	Explain the operation of the basic gates with truth table, logic symbol & logic expression OR Explain the following with respect to logic gate. i) Fan- out ii) Propagation delay .	U	3	1,2
2	Explain Boolean constants, variables & function with example OR Show that ABC+B+BD+ABD+AC=B+C	U	3	1,2
3	Realize Half-Adder circuit using basic gates & write the output expression OR Explain the operation of BCD to Decimal Decoder using truth table & logic diagram.	A	4	1,2

4	Explain the operation of 4 to 1 multiplexer with logic symbol, truth table & logic diagram. OR Explain the operation of 3 to 8 line Decoder using truth table & logic diagram.	A	4	1,2

Model Question Paper
II Semester Diploma in Mechatronics Engineering
Fundamentals of Digital Electronics

Instructions: Answer any six questions from part A and Seven full questions from part B

PART-A

Answer any six questions. **5X6=30 marks**

1. Explain the constituents of Mechatronics system.
2. Explain 8421 Binary code
3. Subtract 16 from 46 using 2's compliment method.
4. State Demorgan's theorems.
5. Realize EX-OR & EX-NOR gates using NAND and NOR gates.
6. Realize Half-Adder circuit using basic gates & write the output expression.
7, Realize Half-Subtractor circuit using basic gates & write the output expression.
8. Explain the significance of PRESET and CLEAR inputs in the flip-flop
9. Compare the three combinational PLD's (PROM, PAL, and PLA)..

PART- B

Answer any seven full questions. **10X7=70marks**

1. Describe the building blocks of Mechatronic system with the help of block diagram. **10m**
2. Perform the following operations.
   i) 11101_2 Binary to decimal number.
   ii) $1101.101_{(2)} + 111.011_{(2)}$.
   iii) $100110011_{(2)}$ convert in to gray code.
   iv) $5BC_{16}$ Hexadecimal to decimal number. **2x5=10m**
   v) Find 1's of $110011001_{(2)}$

3. a) Solve $Y = (A + B)(A + B + \mathbf{C}) + \mathbf{AB}$ using Boolean algebra. **5m**
   b) Show that ABC+B+BD+ABD+AC=B+C **5m**

4. a) Realize AND & OR gates using NOR gate. **5m**
   b) Solve the following function using K-map.

$F(X, Y, Z) = \sum m\ (0, 2, 4, 6)$ **5m**

5. Explain the operation of Full-Subtractor circuit using truth table, output expression and logic diagram. **10m**

6. Explain the operation of 4 to 1 multiplexer with logic symbol, truth table & logic diagram. **10m**

7. a) Determine the number of flip-flops in each of the Counters.
   i) mod-3 ii) mod-8 iii) mod-25 **05m**
   b) Compare asynchronous and synchronous counters **05m**

8. Explain the operation of mod -3 synchronous up counter with the help of logic diagram (use T- ff), Truth table and timing diagram **10m**

9. Explain the operation of 4-bit SISO shift register with the help of logic diagram (Use D-ff) and truth table.

10. Implement the following Boolean functions using PLA.

$f1\ (A, B, C) = \bar{A}\ B\ C + A\ \bar{C} + \bar{A}\ B\ C$

$f2\ (A, B, C) = \bar{A}\ \bar{B}\ \bar{C} + BC$ **10m**

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Model Question Bank
II Semester Diploma in Mechatronics Engineering
Fundamentals of Digital Electronics

Unit -1

Introduction to Mechatronics and Digital principles

Cognitive level- Understanding

1. Explain Mechatronic system with example.
2. Explain the domain of Mechatronics.
3. Explain the constituents of Mechatronics system.
4. Justify the multidisciplinary approach in Mechatronics.
5. Explain the merits of Mechatronics system.
6. Discuss the general applications of Mechatronics.
7. Explain the scope of Mechatronics.
8. Explain analog signal. Give two examples.
9. Explain digital signal. Give two examples.
10. Distinguish between analog & digital signal.
11. Discus the advantages of digital technology.
12. Discuss the limitations of digital technology and Name the three stages of digital system design and explain.
13. Describe building blocks of Mechatronics system with the help of block diagram

Unit -II

Number System

Cognitive level- Understanding

1. Explain Number system. Write its classification.
2. Explain positional weighted codes. Give examples.
3. Explain 8421 Binary code.
4. Describe the procedure to convert Binary to Decimal with an example.
5. Discuss Binary Coded Decimal system
6. Describe the procedure to convert octal number to Binary with an example
7. Discuss the procedure to convert Binary number to octal number with an example

8. Discuss the procedure to convert octal number to Decimal with an example
9. Discuss the procedure to convert Binary number to Hexa Decimal number
10. Discuss the procedure to convert Hexadecimal to binary number
11. Discuss the procedure to convert Decimal to Hexadecimal
12. Describe the sign magnitude representation of signed numbers with an example
13. Describe how signed numbers are represented in 2's complement form with an example.
14. Describe how signed numbers are represented in 1's complement form with an example
15. Discuss the steps to perform subtraction using 1's complement method
16. . Discuss the steps to perform subtraction using 2's complement method
17. Discuss the properties of gray code.
18. Discuss the properties of BCD code.
19. Discuss the properties of Excess-3 code
20. Discuss the procedure to convert Binary to Gray code with an example
21. Discuss the procedure to convert Gray to Binary code with an example
22. Discuss the importance of ASCII code
23. Discuss the importance of EBCDIC code.

Cognitive level- Application

1Convert the following Binary number to Decimal.

i)$10101_{(2)}$ ii) $101011.101_{(2)}$

2 Describe the procedure to convert Decimal to Binary with an example (repeated division by 2 method)

3 Convert the following to Binary.

i) $121_{(10)}$ iii) $49_{(10)}$

4. Convert the following to Binary.

i) $123.6875_{(10)}$ ii) $32.625_{(10)}$

5 Convert the following decimal to BCD

i) $345_{(10)}$ ii) $9990_{(10)}$

6 perform theBinary addition for the following.

i) $1101.101_{(2)} + 111.011_{(2)}$ ii) $110011_{(2)} + 111111_{(2)}$

7 Perform the Binary subtraction for the following.

i) $1111.101_{(2)} - 111.011_{(2)}$ ii) $110011_{(2)} - 1011_{(2)}$

8 Perform the Binary multiplication for the following.

i) Multiply $1101_{(2)}$ by $110_{(2)}$

ii) Multiply $1011.101_{(2)}$ by $101.01_{(2)}$

9. Convert the following to binary number.

i) $367.527_{(8)}$ ii) $123.564_{(8)}$

10 Convert the following to octal number.

i) $111011.111010_{(2)}$ ii)$10101111001.0111_{(2)}$

11 Convert the following to Decimal number

i) $4057.06_{(8)}$ ii)$123.456_{(8)}$

12 Convert the following to Hexadecimal.

i) $1011011011_{(2)}$ ii) $111100001010_{(2)}$

13 Convert the following to Hexadecimal number.

i) $577_{(8)}$ ii) $145_{(8)}$

14 Convert the following to octal number

i) $AB3_{(H)}$ ii) $BCD7_{(H)}$

15 Convert the following to base 2.

i) $5C7_{(H)}$ ii) $A8F1_{(H)}$

16 Convert the following to Hexadecimal.

i) $25.675_{(10)}$ ii) $496_{(10)}$

17 Represent the following signed numbers in sign-magnitude, 2's complement & 1's compliment form.

i) +31 ii) -51.

18 Subtract 16 from 46 using 8 bit 2's compliment method.

19 Subtract 23 from 15 using 8 bit 2's compliment method.

20 Subtract 49 from 76 using 8 bit 1's compliment method.

21 Subtract 56 from 20 using 8 bit 1's compliment method.

22 Find the 1's complement of the following.

i) -99 ii) -77.25

23 Find the 2's complement of the following.

i) -47 ii) -23.25

24 Convert the following to gray code.

i) $100110011_{(2)}$ ii) 3A7 (H) iii) $527_{(8)}$

25 Convert the 10110010 Gray number in to

i) Hex ii) Binary iii) Decimal.

26 Convert the Decimal number 597 to excess-3.

27 Perform the following operations.

i) 11101_2 Binary to decimal number.

ii) $1101.101_{(2)} + 111.011_{(2)}$.

iii) $100110011_{(2)}$ convert in to gray code.

iv) $5BC_{16}$ Hexadecimal to decimal number.

v) Find 1's of $110011001_{(2)}$

28 a) Subtract 49 from 76 using 8 bit 1's compliment method.

b) Convert the following to base 2.

i) $5C7_{(H)}$ ii) $A8F1_{(H)}$

Unit -III

Logic gates & Boolean Algebra.

Cognitive level- Remembering

1. Define a logic gate
2. Define Universal gate .Give examples
3. Define the following with respect to logic gate. i) Fan- out ii) Propagation delay iii) Fan-in iv) Noise margin v) Power dissipation
4. Define Boolean constants, variables & function with example
5. Define K Map

Cognitive level- Understanding

1. Describe the concepts of positive and negative logic
2. Explain the operation of the basic gates with truth table, logic symbol & logic expression
3. Write the truth table. Logic symbol, logic expression of EX-OR and EX-NOR gates.
4. Write the truth table and logic diagram for the following expression Y = AB+BC
5. List the rules and laws of Boolean algebra.
6. prove Demorgan's theorem
7. Write rules of K-MAP& Prepare **K**-MAP for 2, 3, and 4 Variables

Cognitive level- Application

1. Realize all Basic gates using NAND gate.
2. Realize all Basic gates using NOR gate.
3. Realize EX-OR & EX-NOR gates using NAND and NOR gates
4. Simplify the following Boolean function using the laws of Boolean algebra & implement the same using logic gates

   $Y=AB+ABC+BC$

5. Show that $ABC+B+BD+ABD+AC=B+C$
6. Solve the following expression using K-MAP to obtain minimal expression & write logic diagram. $F(x, y, z) = \sum m(0, 2, 4, 6)$
7. Solve the following expression using K-MAP to obtain minimal expression & write logic diagram. $f(x, y, z) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$
8. Simplify the following Boolean function using the laws of Boolean algebra & implement the same using logic gates

   $Y=AB+ABC+BC$

9. Solve the given expression to obtain the minimal SOP expression and implement it in NAND logic.

   $Y=\sum m(2,3,5,7,9,11,12,13,14,15)$

10. Simplify $Y= (A+B)(A+B+C)+AB$

Unit -IV

Combinational Logic Circuits

Cognitive level- Understanding

1. Distinguish between combinational circuits and sequential circuits
2. Explain the concept of delay in a digital circuit with an example
3. Explain the operation of 4-bit parallel Adder

Cognitive level- Application

1. Realize Half-Adder circuit using basic gates & write the output expression
2. Realize a Full-Adder circuit using two Half-Adder circuit
3. Realize Half-Subtractor circuit using basic gates & write the output expression
4. Explain the operation of 4 to 1 multiplexer with logic symbol, truth table & logic diagram
5. Explain the operation of Full-Subtractor circuit using truth table, output expression and logic diagram
6. Explain the operation of Full-Adder circuit using truth table, output expression. And logic diagram
7. Explain the operation of 8 to 1 multiplexer with logic symbol, truth table & logic diagram
8. Explain the operation of 1to 4 De- multiplexer with logic symbol truth table &logic diagram
9. Explain the operation of Decimal to Binary Encoder using truth table & logic diagram.
10. Explain the operation of 1 to 8 De-Multiplexer with logic symbol, truth table & logic diagram
11. Explain the operation of 3 to 8 line Decoder using truth table & logic diagram
12. Explain the operation of BCD to Decimal Decoder using truth table & logic diagram
13. Explain 1-bit magnitude Comparator using truth table & logic diagram
14. Explain the operation of 4-bit odd Parity generator using Logic diagram & truth table.
15. Explain the operation of 4-bit Even Parity generator using Logic diagram & truth table.

Unit -V

Sequential Logic Circuits

Cognitive level- Understanding

1. Explain the Flip-Flop and write its applications
2. What is meant by clocked Flip-Flop? How it is different from a Latch
3. What are the different types of triggering? Explain
4. Explain the significance of PRESET and CLEAR inputs in the flip-flop

5. What is shift register and write its applications
6. What is a counter and write its applications
7. Explain the two basic types of counters
8. Compare asynchronous and synchronous counters
9. What is meant by race around condition? How it is eliminated in Master-Slave JK flip-flop.

Cognitive level- Application

1. Determine the number of flip-flops in each of the Counters. i) mod-3 ii) mod-8 iii) mod-25
2. What is the maximum modulus of a counter with eachof the following number of FF's? i) 2 ii) 8 iii) 10
3. Draw the schematic circuit of an edge triggered SR flip-flop using NAND gates and explain its operation with the help of a truth table.
4. Explain the operation of an edge triggered D-flip-flop with the help of truth table & Logic diagram
5. Draw the schematic circuit of an edge triggered JK flip-flop using NAND gates and explain its operation with the help of a truth table
6. Draw the schematic circuit of an edge triggered JK flip-flop using NAND gates and explain its operation with the help of a truth table.
7. Draw the schematic circuit of an edge triggered T flip-flop using NAND gates and explain its operation with the help of a truth table
8. Draw the schematic circuit of pulse triggered Master-Slave JK flip-flop using NAND gates and explain its operation with the help of a truth table.
9. Explain the operation of 4-bit SISO shift register with the help of logic diagram (Use D-ff) and truth table.
10. Explain the operation of 4-bit SIPO shift register with the help of logic diagram (Use D-ff) and truth table
11. Explain the operation of 4-bit SIPO shift register with the help of logic diagram (Use D-ff) and truth table.
12. Explain the operation of 4-bit PIPO shift register with the help of logic diagram (Use D-ff) and truth table.
13. Explain the operation of 4-bit bidirectional shift register with the help of logic diagram (use D-ff) and truth table.

14. Explain the operation of 3-bit Binary asynchronous (Ripple) Up counter with the help of logic diagram (use T- ff) ,Truth table and timing diagram
15. Explain the operation of 3-bit Binary asynchronous (ripple) down counter with the help of logic diagram (use T- ff), Truth table and timing diagram
16. Explain the operation of 3-bit Binary asynchronous (ripple) up/down counter with the help of logic diagram (use T- ff) &Truth table
17. Explain the operation of mod -5 ripple up counter with the help of logic diagram (Use T- ff), truth table and timing diagram
18. Explain the operation of mod -10 (decade) ripple up counter with the help of logic diagram (use T- ff), Truth table and timing diagram
19. Explain the operation of mod -3 synchronous up counter with the help of logic diagram (use T- ff), Truth table and timing diagram.

Unit VI

Programmable Logic Devices

Cognitive level- Understanding

1. What is a PLD? List the advantages of PLD's over fixed array logic
2. Compare the three combinational PLD's (PROM, PAL, and PLA).
3. Explain the features of PLA
4. Explain the features of PAL
5. Explain the features of PROM

Cognitive level- Application

1. Implement Full-adder using PAL with Boolean expression for o/p's
2. Implement Full-Subtractor using PAL with Boolean expression for o/p
3. Implement Half-Subtractor using PAL with Boolean expression for o/p.
4. Implement half-adder using PAL with Boolean expression for o/p.
5. Prove that $A+\bar{A}B=1$
6. Implement logic gates to perform the 2:1 multiplexer
7. Implement the following Boolean functions using PLA

   f1 (A, B, C) =A B C+A C + A B C