Government of Karnataka

DEPARTMENT OF COLLEGIATE AND TECHNICAL EDUCATION

Programme	Electronics and Communication	**Semester**	III
Course Code	20EC32P	**Type of Course**	Program Core
Course Name	Logic Design using Verilog	**Contact Hours**	8 hours/week 104 hours/semester
Teaching Scheme	L:T:P :: 3:1:4	**Credits**	6
CIE Marks	60	**SEE Marks**	40

1. Rationale

Digital Electronics is a field of electronics involving the study of digital signals and engineering of devices that use or produce them. It is very important in today's life because if digital circuits are used instead of analog circuits the signals can be transmitted without degradation due to noise. Also in a digital system information stored is easier than that of analog systems. The functionality of digital circuits can be changed easily with the help of software without changing the actual circuit. Verilog, a Hardware Description Language, is used for describing digital electronic circuits and systems. It is used for verification of digital circuits through simulation, for timing analysis, for test analysis and for logic synthesis.

2. Course Outcomes: On successful completion of the course, the students will be able to:

CO-01	List the types of Verilog modeling and the use of each model for specific application
CO-02	Design and construct a sequential circuit for a given application and test the circuit to obtain the desired result/output.
CO-03	Compare and contrast combinational and sequential circuits and simulate a given circuit using Verilog descriptions to test to obtain the desired result/output
CO-04	List the various types of A to D, D to A converters along with memory and for a given application select the appropriate converters and/or memory types to be used to obtain the given result/output.

3. Course Content

Week	CO	PO	Lecture (Knowledge Criteria)	Tutorial (Activity Criteria)	Practice (Performance Criteria)
			3 hours/week	1 hour/week	4 hours/week (2 hours/batch twice in a week)
1	1	1,4,5, 6,7	1. VLSI - Introduction, Importance & Need. HDL- Introduction, Importance, Need & Types. 2. Introduction to Verilog HDL, Types of modeling- Switch level, Structural, Data flow and Behavioral. 3. Basic Concepts- Lexical conventions, comments, keywords, identifiers, strings.	Refer Table 1	1. Familiarization of Xilinx software. 2. Familiarization of FPGA/CPLD KIT.

2	1	1,2,4	1. Data types -Value Set, Wires, Nets, Registers, Vectors, Integers, Real, Time, Parameters, Arrays, Strings. 2. Operators- Arithmetic, Logical, Relational, Bit-wise. 3. Reduction, Shift, Concatenation, Replication, Conditional operators. Operator Precedence.	Refer Table 1	1. Demonstrate and Practice simple examples using different data types. 2. Compute the output for expressions having different operators using simple programs.
3	1,3	1,2,3, 6	1. Program structure- Module declaration, port declaration, port connection. 2. Gate level modeling for basic gates. 3. Gate level Verilog description for half adder, full adder.	Refer Table 1	Write the verilog code, simulate and download to FPGA/CPLD kit for the following 1. 2 input basic gates using gate level modelling. 2. Full adder and full subtractor using gate level modelling.
4	1,3	1,2,3, 4,6	1. Data flow modeling- Continuous assignment, Module instantiations, net declaration, delays, expressions. 2. Data flow Verilog description of multiplexer and demultiplexer. 3. Data flow Verilog description for 4-bit comparator	Refer Table 1	Write the verilog code, simulate and download to FPGA/CPLD kit for the following. 1. 4:1 Mux and 1:4 Demux using data flow modeling. 2. Comparator using data flow modeling.
5	1,3	2,3,4, 6	1. System tasks-display, strobe, monitor, reset, stop, finish. Compiler directives- include, define. Behavioral modeling- Always and Initial statements. 2. Procedural Assignments- Blocking and non-blocking assignments. Timing Control-Delay, Event 3. Conditional statements-if, if-else, Case, Loops- While, For, Repeat, Forever.	Refer Table 1	1a.Write and execute simple programs to illustrate conditional statements. 1b. Write and execute simple programs to illustrate loops. 2. Write the verilog code, simulate and download to FPGA/CPLD kit for a 4-bit ALU with any 2 arithmetic and logical operations.
6	1,3	1,2,3, 4,6	1. Behavioral Verilog description for BCD to seven segment decoder for common anode display using if-else, Case. 2. Traffic light controller using Behavioral description. 3. Test bench- Need, Importance, testbench for half adder.	Refer Table 1	1. Write the verilog code, simulate and download to FPGA/CPLD kit for a BCD to seven segment decoder using case statement. 2. Write and simulate a Test bench for half adder.

7	2	1,2,3, 4,6,7	1. Sequential circuits - Introduction. Flip flops- types, SR flip flop- Gate level circuit using NAND gates, truth table, working, timing diagram. 2. JK, JK-MS flip flops-Logic circuit, truth table, working, timing diagram. 3. D, T flip flops-Logic circuit, truth table, working, timing diagram. Relevance of Asynchronous inputs to flip-flops.	Refer Table 1	1. Construct and test clocked SR Flip flop using NAND gates in digital trainer kit. 2. Implement D and T Flip flops using JK flip flop in digital trainer kit and observe the timing diagram.
8	2,3	1,2,3, 4	1. Verilog description of SR flip flops using data flow modeling. 2. Verilog description of JK flip flop using behavioral modeling. 3. Registers- Classification of registers, realization of simple (3 or 4 bit) SISO using flip-flops.	Refer Table 1	Write the verilog code, simulate and download to FPGA/CPLD kit for the following. 1. SR, JK flip flops using data flow modeling 2.D, T flip flops using behavioral modeling
9	2,3	1,2,3, 4,6,7	1. Realization of SIPO, PISO and PIPO using flip flops. 2. Concept of universal shift-register. Ring counter and Johnson's counter (3 bit). 3. Verilog description of any one shift register using any modeling.	Refer Table 1	Construct and verify the working of the following using suitable IC in digital trainer kit 1. SISO, SIPO, PISO and PIPO(4-bit) shift registers. 2. Ring and Johnson counter(4-bit).
10	3	1,3,4, 6,7	1. Counters - definition, classification, modulus. Working and realization of asynchronous (3 bit/4 bit) counters using flip-flops. 2. Working and realization of synchronous (3-bit/ 4-bit) counters and their comparison. 3. Realization of partial mod (mod n) counters-asynchronous, synchronous.	Refer Table 1	Construct and verify the working of the following using digital trainer kit 1. 3 bit ripple counter using IC 7476. 2. 4 bit counter as a frequency divider.
11	3,4	1,2,6, 7	1. Realization of higher-mod counters using lower-mod counters. Concept of up/ down counters. 2. Verilog description of any one counter using any modeling. 3. Data converters- Need for DAC and ADC, DAC specifications, types, working of Weighted resistor type.	Refer Table 1	1. Write the verilog code, simulate and download to FPGA/CPLD kit for an up/down counter using behavioral modeling. 2. Construct/Simulate and verify the working of R-2R DAC.
12	4	1,2,3, 4,6,7	1. ADC specifications. types, working of Flash ADC.	Refer Table 1	1. Construct/Simulate and verify the working of Flash ADC.

			2. Working of Successive approximation and dual slope ADCs. 3. Memory devices- Introduction, classification based on different criteria, read and write operations.		2. Illustrate the storing and retrieving of data in RAM using suitable IC.
13	4	1,2,3, 4,7	1. Introduction to PLDs- PAL, PLA, CPLD, FPGA, ASIC. IC Design Verification – Types & Stages. 2. PAL- Architecture, Implementation of a Boolean expressions using PAL. 3. PLA-Architecture, Implementation of a Boolean expressions using PLA.	Refer Table 1	1. Implementation of Boolean expressions using PAL. 2. Implementation of Boolean expressions using PLA.
Total in hours			**39**	**13**	**52**

Note: 1) In Practice sessions Video demonstration should be followed by MCQs/Quiz/Subjective questions and the evaluation has to be documented.

2) In Practice sessions, all circuits should be simulated using suitable software before its construction and verification.

TABLE 1: Suggested activities for tutorials

The list is shared as an example and not inclusive of all possible activities of the course.

The list of activities for one week can be shared among teams in a batch of students.

Week No.	Suggested activities for tutorials
01	1. Explain the typical design flow for VLSI IC Circuits. 2. Give a presentation on comparison of different types of HDLs. 3. Give a presentation on comparison of different types of modeling in Verilog.
02	1. Prepare a report on declaration and initialization of variables of different data types in Verilog. 2. Prepare a report on hierarchy of operators.
03	1. Explain basic components of a module? Which components are mandatory? 2. Prepare a report on Hierarchical names for variables. 3. Write and explain a Verilog code for 4:1 mux and 1:4 demux using gate level modeling.

04	1. Write and explain the Verilog code for full adder using data flow modeling. 2 Write and explain the Verilog code for 8:1 mux using data flow modeling.
05	1.Give a presentation on the differences between tasks and functions 2. Illustrate the use of system tasks with examples. 3. Illustrate the use of gate delays to model timing for a simple logic equation.
06	1. Compare if-else and case statements with the help of examples. 2. Compare all loops with the help of examples. 3. Write and explain the verilog code for full subtractor and 1:8 demux using behavioral modeling. 4. Explain the Verilog Test bench with an example to verify the HDL designs.
07	1. Prepare a report on differences between Combinational and Sequential circuits with examples. 2. Give a presentation on application of flip flop as bounce elimination switch. 3. Demonstrate the working of flip flop as a one bit memory element.
08	1. Prepare a report on flip flop ICs and their features. 2. Give a presentation on eliminating race -around condition in JK flip flop. 3. Compare the advantages and disadvantages of all flip flops.
09	1. Prepare a report on shift register ICs and their features. 2. Give a presentation on applications of shift registers in real life. 3. Demonstrate the working of IC 7495 as shift register.
10	1. Prepare a report on differences between asynchronous and synchronous counters. 2. Give a presentation on how counters can be used in a simple car parking system. 3. Give a presentation on implementation of footfall counter for various purposes
11	1. Prepare a report & explain the specifications of DAC and ADC ICs. 2. Give a presentation on any application of DAC in real life. 3. Give a presentation on any application of ADC in real life.

12	1. Prepare a report & explain the types of RAM and ROM. 2. Give a presentation on usage of RAM and ROM in different digital devices.
13	1. Study the latest technological changes in this course and present the impact of these changes on industry. 2. Prepare a report on CPLD, FPGA and ASIC and its applications. 3. Give a presentation on importance or scope of Design Verification in Integrated circuit designs.

LINKS.

1. https://verilogguide.readthedocs.io/en/latest/verilog/testbench.html
2. https://youtu.be/XES0QUi8ttY(week 11, exp 2)
3. https://www.youtube.com/watch?v=krmXg-WTbIU (week 12, exp 1)
4. http://www.asicguru.com/verilog/tutorial/system-tasks-and-functions/68/.
5. https://youtu.be/vHlg_QLGIQ (week 7,exp 3)
6. https://youtu.be/AtX5x53FcLI (week 9,exp 3)
7. https://youtu.be/Bx_4rsUAGoM
8. https://www.irisys.net/people-counting.

4. CIE and SEE Assessment Methodologies

Sl. No	Assessment	Test Week	Duration In minutes	Max marks	Conversion
1.	CIE-1 Written Test	5	80	30	Average of three tests 30
2.	CIE-2 Written Test	9	80	30	
3	CIE-3 Written Test	13	80	30	
4.	CIE-4 Skill Test-Practice	6	180	100	Average of two skill tests 20
5	CIE-5 Skill Test-Practice	12	180	100	
6	CIE-6 Portfolio continuous evaluation of Activity through Rubrics	1-13		10	10
				Total CIE Marks	60
	Semester End Examination (Practice)		180	100	40
				Total Marks	**100**

5. Format for CIE (1,2,3) Written Test

Course Name	**Logic Design Using Verilog**	Test	I/II/III	Sem	III/IV
Course Code	**20EC32P**	Duration	80 Min	Marks	30
Note: Answer any one full question from each section. Each full question carries 10 marks.					
Section	Assessment Questions		Cognitive Levels	Course Outcome	Marks
I	1				

	2			
II	3			
	4			
III	5			
	6			
Note for the Course coordinator: Each question may have one, two or three subdivisions. Optional questions in each section carry the same weightage of marks, Cognitive level and course outcomes.				

5. (a) Format for CIE-4 Skill Test -Practice.

SL. No.	COs	Particulars/Dimension	Marks
1	1	List the types of Verilog modelling and the use of each model for specific application.	20
2	3	Write two Verilog programs on combinational circuits for a given application -40 Marks Simulation - 20 Marks Download to FPGA kit - 10 Marks	70
3	1,3	PortFolio evaluation of Practice sessions through rubrics	10
		Total Marks	**100**

5. (b) Format for CIE-5 Skill Test - Practice.

SL. No.	COs	Particulars/Dimension	Marks
1	2	Write a Sequential circuit for a given application -20 Marks Conduction using DTK -20 Marks Output -10 Marks	50
2	3	Write a Verilog program on Sequential circuits for a given application - 10 Marks Simulation -5 Marks Output - 5 Marks	20
3	4	Identify various types of A to D, D to A converters/ memory for a given application & select the appropriate converters/ memory types needed to obtain the required output.	20
4	2,3,4	Portfolio evaluation of Practice sessions through rubrics.	10
		Total Marks	**100**

6. Rubrics for Assessment of Activity (Qualitative Assessment)

Sl. No.	Dimension	Beginner	Intermediate	Good	Advanced	Expert	Students Score
		2	4	6	8	10	
1		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	8
2		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	6
3		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	2
4		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	2
					Average Marks= (8+6+2+2)/4=4.5		**5**

Note: Dimension and Descriptor shall be defined by the respective course coordinator as per the activities

7. Reference:

Sl. No.	Description
1	Fundamentals of Digital Logic with Verilog Design by Stephen Brown and Zvonko Vranesic
2	Verilog HDL by Samir Palnikar
3	Introduction to Verilog-Peter M Nyasulu
4	Verilog Tutorial-Deepak Kumar Tala

8. SEE Scheme of Evaluation

SL. No.	COs	Particulars/Dimension	Marks
1	1	List the types of Verilog modelling and the use of each model for specific application	10
2	3	Write a Sequential circuit for a given application -10 Marks Conduction using DTK -10 Marks Output -10 Marks	30
3	2	Write a Verilog program for a given application - 10 Marks Simulation - 10 Marks Download to FPGA kit- - 10 Marks	30
4	4	Identify various types of A to D, D to A converters and memory and for a given application & select the appropriate converters and/or memory types needed to obtain the given output.	10
5	1,2, 3,4	Viva-Voce	20
		Total Marks	**100**

9. Equipment/software list with Specification for a batch of 20 students

Sl. No.	Particulars	Specification	Quantity
1	Computers	Intel Core i5 11th gen/8GB RAM/1 TB HDD/256GB SSD/ Graphics 2 GB	20
2	Xilinx software		
3	Digital trainer kits		20
4	Verilog kits		20
5	Dual trace oscilloscope	20-30MHz	10
6	Digital multimeters		05
7	Patch cards	different length	250
8	Digital IC Tester		02
9	ICs 7400,7402,7404,7408,7432,7486,7442, 7445,7446,7474,7476,7427,7489,7490, 7494,7495,74141,74148,74153,74157, 74155,74193,74194,DAC0808,ADC-0800,741		10 each