ABACUS

Advanced **B**oard for **A**ctive **C**ontrol
of **U**niversitary **S**atellites

User Manual

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Introduction

ABACUS is an on-board computer suitable for nano- and micro-satellites based on a fault-tolerant design and a reliability-enhancing architecture. ABACUS implements hardware redundancy, provided by a microcontroller and an FPGA, distributed in two independent but cooperative sections: technology diversity grants common mode fault tolerance. The microcontroller ensures low power operation and gives a simple access to buses, memories and peripherals. The FPGA offers all the advantages of the RTL coding for implementing fast error detection and correction techniques, data coding, state-machines or extra communication interfaces, supporting specific satellite operations. Alternatively the FPGA can be used to develop an entire application using e.g. third part IP cores, like microprocessors and microcontrollers. The microcontroller and the FPGA sections are powered from the common 5V power bus but with independent power regulation that can be switched off independently in order to limit power consumption and introduce overheat protection. The two sections share the same I2C system bus and several general purpose I/O (GPIO) lines for data exchange and synchronization. Each section has its own memory system for data storage. Several on-board sensors give housekeeping and health monitoring. Two sensors measure both FPGA and microcontroller temperature; a current shunt amplifier returns the overall current consumption. One magnetometer, one gyroscope and one accelerometer, provide information about satellite attitude. The board has a PC104 form factor and its pinout is compatible with the cubesat standard.

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Bla bla bla

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Connector Hardware needed

ABACUS CUBESAT PC104 HEADER PINOUT

H1

H1_1	**GND**
H1_3	UART1_TXD
H1_5	UART1_RXD
H1_7	
H1_9	SPI_SCK
H1_11	SPI_SIMO
H1_13	GPIO_P7.1
H1_15	GPIO_P11.1
H1_17	NC
H1_19	GPIO_P10.0
H1_21	NC
H1_23	NC
H1_25	ADC11
H1_27	ADC9
H1_29	ADC7
H1_31	ADC5
H1_33	ADC3
H1_35	CTS_P3.3
H1_37	DSR_P3.0
H1_39	UART3_TXD
H1_41	SDA2
H1_43	SCK2
H1_45	NC
H1_47	NC
H1_49	NC
H1_51	NC

H1_2	**GND**
H1_4	UART2_TXD *
H1_6	UART2_RXD *
H1_8	GPIO_P2.0 **
H1_10	GPIO_P7.0
H1_12	SPI_CS
H1_14	ADC10
H1_16	ADC8
H1_18	ADC6
H1_20	ADC4
H1_22	ADC2
H1_24	NC
H1_26	NC
H1_28	VREF+/VEREF+
H1_30	VREF-
H1_32	NC
H1_34	GPIO_P11.2
H1_36	RTS_P2.7
H1_38	DTR_P2.6
H1_40	UART3_RXD
H1_42	NC
H1_44	NC
H1_46	NC
H1_48	NC
H1_50	NC
H1_52	NC

***UART2 also on side connector**
****** optional RTC_IRQ output**

H2

H2_1	GPIO EXP1 *
H2_3	GPIO EXP3 *
H2_5	GPIO EXP5 *
H2_7	GPIO EXP7 *
H2_9	GPIO EXP9 *
H2_11	GPIO EXP11 *
H2_13	GPIO EXP13 *
H2_15	GPIO EXP15 *
H2_17	GPIO EXT PWR**
H2_19	3.3V PWR OUTPUT
H2_21	NC
H2_23	NC
H2_25	**VIN_SYS**
H2_27	NC
H2_29	**GND**
H2_31	NC
H2_33	NC
H2_35	NC
H2_37	NC
H2_39	NC
H2_41	NC
H2_43	NC
H2_45	NC
H2_47	NC
H2_49	NC
H2_51	

H2_2	GPIO EXP0 *
H2_4	GPIO EXP2 *
H2_6	GPIO EXP4 *
H2_8	GPIO EXP6 *
H2_10	GPIO EXP8 *
H2_12	GPIO EXP10 *
H2_14	GPIO EXP12 *
H2_16	GPIO EXP14 *
H2_18	**GND**
H2_20	**GND**
H2_22	NC
H2_24	NC
H2_26	**VIN_SYS**
H2_28	NC
H2_30	**GND**
H2_32	**GND**
H2_34	NC
H2_36	NC
H2_38	NC
H2_40	NC
H2_42	NC
H2_44	NC
H2_46	NC
H2_48	NC
H2_50	NC
H2_52	NC

***3.3V or EXT_V (1.8V-5.0V)**
****1.8V-5.0V**

***3.3V or EXT_V (1.8V-5.0V)**

Figure 5.1: H1, H2 pinout overview

GND	GND	GPIO EXP1 *	GPIO EXP0 *
UART1_TXD	UART2_TXD *	GPIO EXP3 *	GPIO EXP2 *
UART1_RXD	UART2_RXD *	GPIO EXP5 *	GPIO EXP4 *
NC	GPIO_P2.0 **	GPIO EXP7 *	GPIO EXP6 *
SPI_SCK	GPIO_P7.0	GPIO EXP9 *	GPIO EXP8 *
SPI_SIMO	SPI_CS	GPIO EXP11 *	GPIO EXP10 *
GPIO_P7.1	ADC10	GPIO EXP13 *	GPIO EXP12 *
GPIO_P11.1	ADC8	GPIO EXP15 *	GPIO EXP14 *
NC	ADC6	GPIO EXT PWR	GND
GPIO_P10.0	ADC4	3.3V PWR OUT	GND
NC	ADC2	NC	NC
NC	NC	NC	NC
ADC11	NC	VIN_SYS	VIN_SYS
ADC9	VREF+/VEREF+	NC	NC
ADC7	VREF-	GND	GND
ADC5	NC	NC	GND
ADC3	GPIO_P11.2	NC	NC
CTS_P3.3	RTS_P2.7	NC	NC
DSR_P3.0	DTR_P2.6	NC	NC
UART3_TXD	UART3_RXD	NC	NC
SDA2	NC	NC	NC
SCK2	NC	NC	NC
NC	NC	NC	NC
NC	NC	NC	NC
NC	NC	NC	NC
NC	NC	NC	NC

Figure 5.2: H1, H2 pins

5.6 FPGA JTAG programming connector

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6.1 Custom FW development

6.1.1 Microcontroller

Details (connections, chip pinout, ref to tools etc)

6.1.2 FPGA

Details, ref to ISE etc

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