vhdl5_59 U96935703 Aluri USF EE

The design aims to perform 32x32-bit multiplication using a high-level description for simplicity and clarity in functionality.
It directly describes the multiplication process by defining inputs, outputs, and operations in a single behavioral block, abstracting low-level details.
This model is ideal for quick simulations and functional verification of the multiplier, ensuring correctness before proceeding to structural implementation.