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Homework 5

4.16.1. (a) lw $1, 40($6)

IF/ID: ① PC+4
② fetched Ins from Ins memory.

ID/EX: ① WB, MEM, EX (RegDst, ALUOp, ALUSrc//, Branch, MemRead, MemWrite//RegWrite, MemtoReg)
② PC+4
③ ~~rd~~ $rs, $rt
④ ~~Singn~~ Signed Ins[15:0]
⑤ rs, rt, rd

EX/MEM: ① WB, MEM
② PC+4+Signed extention (New PC)
③ zero
④ ALU out
⑤ Data to write to Dmem. 疑问：这个是不是 Read Reg 2？看图不是
⑥ Rt or Rd (Acording to RegDst). (Desination)

MEM/WB ① WB
② Data read from Dmem (or Random if no mem read)
③ ALU out
④ Rt or Rd (Destination to write on Reg).

4.16.2/3

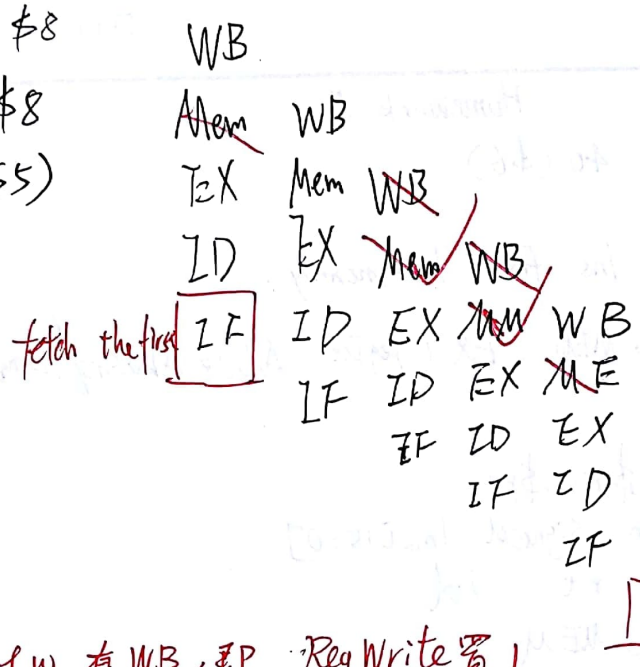
	need to be read	Actually read	EX	MEM
a.	$6	$0, $1	40+$6	load from mem
b.	$5	$5, twice	$5+$5	×

4.16.4

a. Loop

将
- 2: add $5, $5, $8
- 2: add $6, $6, $8
- 2: sw $1, 20($5)
- 2. beq

全
- 3. lw
- 3. add
- 3. add
- 3. sw
- 3. beq.



仅 add, addi, lw 有 WB, 即 RegWrite 置 1
仅 sw 有 MemWrite, 即 MEM 有用
仅 lw 有 MemRead & MemtoReg 这两命令一定相同, 也有 Mem.
至于 beq: Branch & zero → PCSrc 在比较

14.16.5

如图. only $\frac{1}{5}$ clock cycles

4.16.6

PC+4,
Ins word for previous beq.

4.17_3

use data Mem: lw, sw,

4.18_1

for add: EX = { RegDst = 1, ALUOP = 10, ALUSrc = 0 }

要写入 Reg 时为 1: (R型, lw)

仅在用 sign-extention 为 1 (lw, sw, addi)

MEM = { Branch = 0, MemRead = 0, MemWrite = 0 }

WB = { RegWrite = 1, Mem2Reg = 1 }

4.18.3

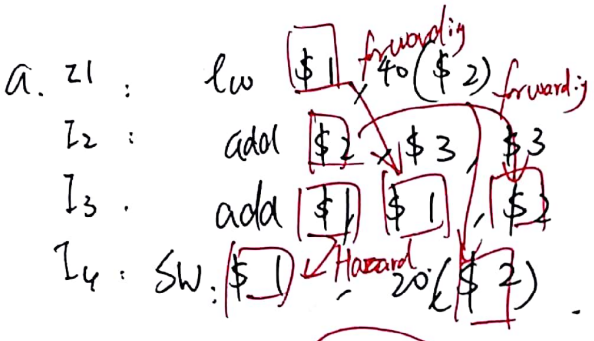
PCSrc = 0 (only J type, beq maybe 1)

In EX: faster to determin whether beq is real.

Such that can save one clock sycle for faulse.

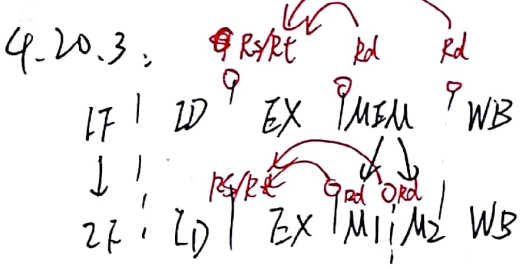
Not In Ex. May increase clock sycle time.

4.20.1



	RaferW	WaferR	WaferW
I1	$1 (I3, I4)	$2 (I2 I1)	$1 (I1, I3]
I2	$2 (I3, I2)		
I3	$1 (I3, I4)		
I4	$2 (I2, I4)		

4.20.3:



with forwarding.

($1) I1 to I3

4.20.5.

$0 = 0

$1 = 32

$2 = 2000

$3 = 1000

4.20.6

```
lw
add
nop
nop
add
nop
nop
sw.
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