

VE370

HW3

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2.21.4:

adjust location should be `addi $sp, $sp, -8` # 堆栈  
and free the stack should be `addi $sp, $sp, 8`  
Negative  
Positive

2.21.5:

$s_0 = a_2$

$v_0 = s_0 + f(a_2) +$

```
int f(a, b, c) {  
    return g(a, b) + c  
}
```

2.21.6

$$500 + C = 500 + 1000 = 1500$$

2.31-1 *tex size* *data size*

A  $0 \times 140$   $0 \times 40$

B  $0 \times 300$   $0 \times 50$

Executable File: A+B:

$$\text{Text size} = 0x140 + 0x300 = 0x440$$

$$\text{Data size} = 0x40 + 0x50 = 0x90$$

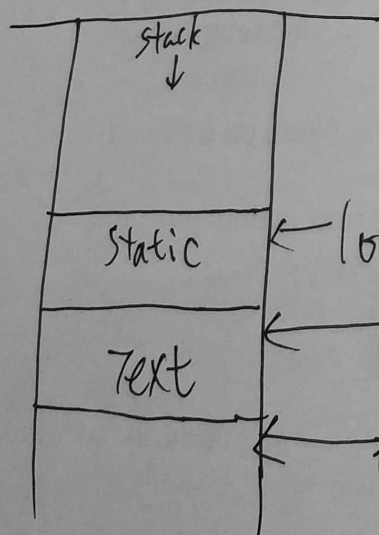
Text Segment:	Address	Instruction
Text size: $0x140$ Data size: $0x40$	A: $0x00400000$	lui \$at, 0
	$0x00400004$	ari \$a0, \$at, 0
	$0x00400008$	jal <u><math>0x00400140</math></u>

Text size:  $0x300$  B  
Data size:  $0x50$

$0x00400140$   
 $0x00400144$   
:  $140+180$   
 $0x004002c0$

static from  $0x10000000$   
sw \$a0,  $0x1000$   
jmp  $0x004002c0$   
~~jal~~ jr \$ra

2-31-2



$$\text{Data} : 10008000 - 1000 \text{ 0000} = 8000_{\text{hex}}$$

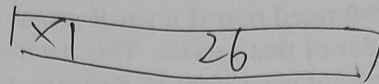
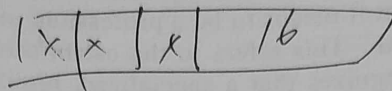
$$\text{Text} : 1000 \text{ 0000} - 0040 \text{ 0000} = 0x\text{FFC}$$

2. 31, 3:

If objects are linked too far apart,  
It's impossible to use branch & jump instr.

Branch: 16 bits,

Jump: 26 bits.



7.

```
Module mux(A,B,sel,F); input
```

```
[31:0] A;
```

```
Input [31:0] B;
```

```
input sel;
```

```
output [31:0] F; reg[31:0] F;
```

```
always @(sel or A or B) begin
```

```
if (sel == 0) F = A;
```

```
else F = B; end
```

```
endmodule
```

8.

```
module register(rdreg1,rdreg2,wrreg,wrddata,write,rddata1,rddata2); input [4:0]rdreg1;
```

```
input [4:0]rdreg2;
```

```
input [4:0]wrreg;
```

```
input [31:0]wrddata;
```

```
input write;
```

```
output[31:0]rddata1;
```

```
output[31:0]rddata2;
```

```
reg [31:0]data[0:31];
```

```
reg [31:0]rddata1;
```

```
reg [31:0]rddata2;
```

```
always @(posedge write) begin
```

```
data[wrreg]=wrddata; end
```

```
always @(rdreg1) begin
```

```
assign rddata1=data[rdreg1]; end
```

```
always @(rdreg2) begin
```

```
assign rddata2=data[rdreg2]; end
```

```
endmodule
```