JOINT INSTITUTE
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**Ve370 Introduction to Computer Organization**

# Homework 1

1. Exercise 1.3.1 ~ 1.3.3

## Exercise 1.3

Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

| | Processor | Clock Rate | CPI |
|---|---|---|---|
| a. | P1 | 3 GHz | 1.5 |
| | P2 | 2.5 GHz | 1.0 |
| | P3 | 4 GHz | 2.2 |
| b. | P1 | 2 GHz | 1.2 |
| | P2 | 3 GHz | 0.8 |
| | P3 | 4 GHz | 2.0 |

**1.3.1** [5] <1.4> Which processor has the highest performance expressed in instructions per second?

**1.3.2** [10] <1.4> If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

**1.3.3** [10] <1.4> We are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

2. Exercise 1.4.4 ~ 1.4.6

The following table shows the number of instructions for a program.

| | Arith | Store | Load | Branch | Total |
|---|---|---|---|---|---|
| a. | 650 | 100 | 600 | 50 | 1400 |
| b. | 750 | 250 | 500 | 500 | 2000 |

**1.4.4** [5] <1.4> Assuming that arith instructions take 1 cycle, load and store 5 cycles, and branches 2 cycles, what is the execution time of the program in a 2 GHz processor?

**1.4.5** [5] <1.4> Find the CPI for the program.

**1.4.6** [10] <1.4> If the number of load instructions can be reduced by one half, what is the speedup and the CPI?

3. Exercise 1.10.1 ~ 1.10.5

The table below shows the instruction type breakdown of a given application executed on 1, 2, 4, or 8 processors. Using this data, you will be exploring the speed-up of applications on parallel processors.

| | Processors | No. Instructions per Processor | | | CPI | | |
|---|---|---|---|---|---|---|---|
| | | Arithmetic | Load/Store | Branch | Arithmetic | Load/Store | Branch |
| a. | 1 | 2560 | 1280 | 256 | 1 | 4 | 2 |
| | 2 | 1280 | 640 | 128 | 1 | 5 | 2 |
| | 4 | 640 | 320 | 64 | 1 | 7 | 2 |
| | 8 | 320 | 160 | 32 | 1 | 12 | 2 |

| | Processors | No. Instructions per Processor | | | CPI | | |
|---|---|---|---|---|---|---|---|
| | | Arithmetic | Load/Store | Branch | Arithmetic | Load/Store | Branch |
| b. | 1 | 2560 | 1280 | 256 | 1 | 4 | 2 |
| | 2 | 1280 | 640 | 128 | 1 | 6 | 2 |
| | 4 | 640 | 320 | 64 | 1 | 8 | 2 |
| | 8 | 320 | 160 | 32 | 1 | 10 | 2 |

**1.10.1** [5] <1.4, 1.6> The table above shows the number of instructions required per processor to complete a program on a multiprocessor with 1, 2, 4, or 8 processors. What is the total number of instructions executed per processor? What is the aggregate number of instructions executed across all processors?

**1.10.2** [5] <1.4, 1.6> Given the CPI values on the right of the table above, find the total execution time for this program on 1, 2, 4, and 8 processors. Assume that each processor has a 2 GHz clock frequency.

**1.10.3** [10] <1.4, 1.6> If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors?

The table below shows the number of instructions per processor core on a multicore processor as well as the average CPI for executing the program on 1, 2, 4, or 8 cores. Using this data, you will be exploring the speedup of applications on multicore processors.

| | Cores per Processor | Instructions per Core | Average CPI |
|---|---|---|---|
| a. | 1 | 1.00E+10 | 1.2 |
| | 2 | 5.00E+09 | 1.4 |
| | 4 | 2.50E+09 | 1.8 |
| | 8 | 1.25E+09 | 2.6 |

| | Cores per Processor | Instructions per Core | Average CPI |
|---|---|---|---|
| b. | 1 | 1.00E+10 | 1.0 |
| | 2 | 5.00E+09 | 1.2 |
| | 4 | 2.50E+09 | 1.4 |
| | 8 | 1.25E+09 | 1.7 |

**1.10.4** [10] <1.4, 1.6> Assuming a 3 GHz clock frequency, what is the execution time of the program using 1, 2, 4, or 8 cores?

**1.10.5** [10] <1.5, 1.6> Assume that the power consumption of a processor core can be described by the following equation:

$$\text{Power} = \frac{5.0\text{mA}}{\text{MHz}} \text{Voltage}^2$$

where the operation voltage of the processor is described by the following equation:

$$\text{Voltage} = \frac{1}{5}\text{Frequency} + 0.4$$

with the frequency measured in GHz. So, at 5 GHz, the voltage would be 1.4 V. Find the power consumption of the program executing on 1, 2, 4, and 8 cores assuming that each core is operating at a 3 GHz clock frequency. Likewise, find the power consumption of the program executing on 1, 2, 4, or 8 cores assuming that each core is operating at 500 MHz.

4. Exercise 2.3.1

The following problems explore translating from C to MIPS. Assume that the variables f and g are given and could be considered 32-bit integers as declared in a C program.

| | |
|---|---|
| **a.** | `f = -g - f;` |
| **b.** | `f = g + (-f - 5);` |

**2.3.1** [5] <2.2> For the C statements above, what is the corresponding MIPS assembly code? Use a minimal number of MIPS assembly instructions.

5. Exercise 2.6.1

The following problems deal with translating from C to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 4-byte words:

| | |
|---|---|
| **a.** | `f = f + A[2];` |
| **b.** | `B[8] = A[i] + A[j];` |

**2.6.1** [10] <2.2, 2.3> For the C statements above, what is the corresponding MIPS assembly code?

6. Exercise 2.6.4

The following problems deal with translating from MIPS to C. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

| | |
|---|---|
| **a.** | `sub $s0, $s0, $s1`<br>`sub $s0, $s0, $s3`<br>`add $s0, $s0, $s1` |
| **b.** | `addi $t0, $s6, 4`<br>`add  $t1, $s6, $0`<br>`sw   $t1, 0($t0)`<br>`lw   $t0, 0($t0)`<br>`add  $s0, $t1, $t0` |

**2.6.4** [5] <2.2, 2.3> For the MIPS assembly instructions above, what is the corresponding C statement?

7. Exercise 2.10.1, 2.10.2

In the following problems, the data table contains bits that represent the opcode of an instruction. You will be asked to interpret the bits as MIPS instructions into assembly code and determine what format of MIPS instruction the bits represent.

| | |
|---|---|
| **a.** | $0000\ 0010\ 0001\ 0000\ 1000\ 0000\ 0010\ 0000_{two}$ |
| **b.** | $0000\ 0001\ 0100\ 1011\ 0100\ 1000\ 0010\ 0010_{two}$ |

**2.10.1** [5] <2.5> For the binary entries above, what instruction do they represent?

**2.10.2** [5] <2.5> What type (I-type, R-type, J-type) instruction do the binary entries above represent?

8. Exercise 2.10.4, 2.10.5

In the following problems, the data table contains MIPS instructions. You will be asked to translate the entries into the bits of the opcode and determine the MIPS instruction format.

| | |
|---|---|
| **a.** | `addi $t0, $t0, 0` |
| **b.** | `sw $t1, 32($t2)` |

**2.10.4** [5] <2.4, 2.5> For the instructions above, show the binary then hexadecimal representation of these instructions.

**2.10.5** [5] <2.5> What type (I-type, R-type, J-type) instruction do the instructions above represent?

9. Exercise 2.12.1, 2.12.2

In the following problems, the data table contains various modifications that could be made to the MIPS instruction set architecture. You will investigate the impact of these changes on the instruction format of the MIPS architecture.

| | |
|---|---|
| **a.** | 128 registers |
| **b.** | Four times as many different instructions |

**2.12.1** [5] <2.5> If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes above, show the size of the bit fields of an R-type format instruction. What is the total number of bits needed for each instruction?

**2.12.2** [5] <2.5> If the instruction set of the MIPS processor is modified, the instruction format must also be changed. For each of the suggested changes above, show the size of the bit fields of an I-type format instruction. What is the total number of bits needed for each instruction?

10. Exercise 2.13.3

In the following problems, the data table contains the values for registers `$t0` and `$t1`. You will be asked to perform several MIPS logical operations on these registers.

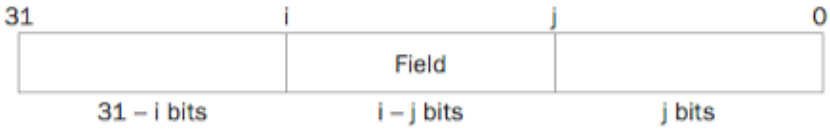
| | |
|---|---|
| **a.** | `$t0 = 0xAAAAAAAA, $t1 = 0x12345678` |
| **b.** | `$t0 = 0xF00DD00D, $t1 = 0x11111111` |

**2.13.3** [5] <2.6> For the lines above, what is the value of `$t2` for the following sequence of instructions?

```
srl $t2, $t0, 3
andi $t2, $t2, 0xFFEF
```

11. Exercise 2.14.1

The following figure shows the placement of a bit field in register `$t0`.




In the following problems, you will be asked to write MIPS instructions to extract the bits "Field" from register `$t0` and place them into register `$t1` at the location indicated in the following table.

| | |
|---|---|
| **a.** |   |
| **b.** |   |

**2.14.1** [20] <2.6> Find the shortest sequence of MIPS instructions that extracts a field from `$t0` for the constant values i = 22 and j = 5 and places the field into `$t1` in the format shown in the data table.

12. Exercise 2.16.4

For these problems, the table holds various binary values for register `$t0`. Given the value of `$t0`, you will be asked to evaluate the outcome of different branches.

| | |
|---|---|
| **a.** | 0x00101000 |
| **b.** | 0x80001000 |

**2.16.4** [5] <2.7> Suppose that register `$t0` contains a value from above. What is the value of `$t2` after the following instructions?

```
        slt  $t2, $0,   $t0
        bne  $t2, $0,   ELSE
        j    DONE
ELSE:   addi $t2, $t2,  2
DONE:
```

13. Exercise 2.17.3

For these problems, there are several instructions that are not included in the MIPS instruction set are shown.

| | |
|---|---|
| **a.** | `subi $t2, $t3, 5  # R[rt] = R[rs] - SignExtImm` |
| **b.** | `rpt  $t2, loop  # if(R[rs]>0) R[rs]=R[rs]-1, PC=PC+4+BranchAddr` |

**2.17.3** [5] <2.7> For each instruction in the table above, find the shortest sequence of MIPS instructions that performs the same operation.

14. Exercise 2.17.4

For these problems, the table holds MIPS assembly code fragments. You will be asked to evaluate each of the code fragments, familiarizing you with the different MIPS branch instructions.

| | |
|---|---|
| **a.** | `LOOP:  addi $s2, $s2, 2`<br>`       subi $t1, $t1, 1`<br>`       bne  $t1, $0,  LOOP`<br>`DONE:` |
| **b.** | `LOOP:  slt  $t2, $0,  $t1`<br>`       beq  $t2, $0,  DONE`<br>`       subi $t1, $t1, 1`<br>`       addi $s2, $s2, 2`<br>`       j    LOOP`<br>`DONE:` |

**2.17.4** [5] <2.7> For the loops written in MIPS assembly above, assume that the register `$t1` is initialized to the value 10. What is the value in register `$s2` assuming the `$s2` is initially zero?

15. Exercise 2.18.4, 2.18.5, 2.18.6

For these problems, the table holds MIPS assembly code fragments. You will be asked to evaluate each of the code fragments, familiarizing you with the different MIPS branch instructions.

**a.**

```
      addi $t1, $0, 50
LOOP: lw   $s1, 0($s0)
      add  $s2, $s2, $s1
      lw   $s1, 4($s0)
      add  $s2, $s2, $s1
      addi $s0, $s0, 8
      subi $t1, $t1, 1
      bne  $t1, $0, LOOP
```

**b.**

```
      addi $t1, $0, $0
LOOP: lw   $s1, 0($s0)
      add  $s2, $s2, $s1
      addi $s0, $s0, 4
      addi $t1, $t1, 1
      slti $t2, $t1, 100
      bne  $t2, $s0, LOOP
```

**2.18.4** [5] <2.7> What is the total number of MIPS instructions executed?

**2.18.5** [5] <2.7> Translate the loops above into C. Assume that the C-level integer `i` is held in register `$t1`, `$s2` holds the C-level integer called `result`, and `$s0` holds the base address of the integer `MemArray`.

**2.18.6** [5] <2.7> Rewrite the loop to reduce the number of MIPS instructions executed.