**Ve370 Introduction to Computer Organization Homework 3**

1. Exercise 2.21.4. (10 points)
2. Exercise 2.21.5. (10 points)
3. Exercise 2.21.6. (10 points)
4. Exercise 2.31.1. (5 points)
5. Exercise 2.31.2. (5 points)
6. Exercise 2.31.3. (5 points)
7. Describe a 32-bit 2-to-1 MUX in Verilog. Simulate your Verilog module. (10 points)

A

B

sel

F

Mux

32

32

32

0

1

1. Model the following 1-bit ALU with Verilog. Simulate your Verilog module. Note: the Overflow Detection circuit doesn’t have to be included. (20 points)



1. Model a 32 x 32-bit register file shown as following diagram using Verilog. Simulate your Verilog module with Xilinx ISE. Assume the device is not clock triggered. (25 points)

