Design1 analysed at 02/17/16 22:56:36

PLL Chip is ADF4158
Notes:
VCO is HMC509LP5E
Reference is custom

VCO Divider Inside Loop: division ratio = 2

Loop Filter designed at a VCO frequency of 7.9996GHz with a Kv of 190MHz/V

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 3.9998GHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	SDM	Filter
100	-76.20	-132.1	--	-76.20	-248.0	-133.4
1.00k	-79.94	-112.2	--	-79.95	-207.7	-113.5
10.0k	-78.49	-98.70	--	-78.56	-165.6	-100.5
100k	-114.0	-120.9	--	-115.2	-162.2	-131.1
1.00M	-141.0	-141.0	--	-172.0	-179.1	-169.3

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)
No significant spurs

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter **0.78 degrees rms**

ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = **-46.2dBc**

---- End of Frequency Domain Results ----

Transient Analysis of PLL
Frequency change from 3.96GHz to 4.04GHz
Simulation run for 1.10ms

Frequency Locking
Time to lock to 1.00kHz is 862us
Time to lock to 10.0 Hz is 980us

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 846us
Time to lock to 1.00 deg is 930us

Lock Detect Threshold
Lock Detect output did not pass 2.50 V

---- End of Time Domain Results ----