BING-YUE WU

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EDUCATION

Arizona State University

Ph.D. in Electrical Engineering

National Taiwan University of Science and Technology (Taiwan Tech)

M.S. in Electrical Engineering

National Taiwan University of Science and Technology (Taiwan Tech)

Description 2011 - 2023

Taipei, Taiwan

National Taiwan University of Science and Technology (Taiwan Tech)

Description 2016 - 2020

B.S. with major in Electrical Engineering and minor in Computer Science and Information Engineering

Taipei, Taiwan

WORK EXPERIENCE

Arizona State University

Aug. 2023 – present

Tempe, Arizona

Graduate Research Assistant

• Research the use of large language models in EDA tools.

• Conduct research on open-source EDA tools and generative AI-based EDA algorithms.

Synopsys Inc.

Oct. 2021 – June 2022

Intern (Technical-Engineering)

Taipei, Taiwan

- Researched a novel Machine Learning-based (ML) solution estimating the effective resistance of Power Delivery Networks in advanced VLSI designs to speed up the runtime and raise the accuracy of ML-driven IR analysis tools.
- Responsible for designing the data pipeline, the ML model architecture, and the entire effective resistance estimation workflow.

Research Center for Information Technology Innovation (CITI), Academia Sinica

Jul. 2020 - Nov. 2020

Full-time Research Assistant at Computational Finance and Data Analytics Lab

Taipei, Taiwan

- Researched a novel Transformer Encoder-based model to possess financial number category awareness.
- Created new pre-training and new fine-tuning tasks for the novel model.
- Developed an Online Loan Application Recommender System for E.SUN Commercial Bank, boosting performance by nearly 300% using advanced machine learning techniques.
- Designed workflow, built the model, and created Python APIs for industrial use.

SKILLS

Programming Languages: C, C++, Python, Tcl

EDA Tools: OpenROAD, OpenSTA, Innovus, Genus, ICC2, Design Compiler, HSpice, Virtuoso, Calibre

Language Ability: Mandarin (Native), English (Fluent)

PUBLICATIONS

B.-Y. Wu, U. Sharma, A. Rovinski, and V. A. Chhabria, "OpenROAD Agent: An Intelligent Self-Correcting Script Generator for OpenROAD", *Proc. ICLAD*, 2025.

V. A. Chhabria, V. Gopalakrishnan, A. B. Kahng, S. Kundu, Z. Wang, **B.-Y. Wu**, and D. Yoon, "**IEEE CEDA DATC:** Strengthening the Foundations of IC Physical Design and ML EDA Research", *Proc. ICCAD*, 2024.

V. A. Chhabria, **B.-Y. Wu**, U. Sharma, K. Kunal, A. Rovinski, and S. S. Sapatnekar, "**Generative Methods in EDA: Innovations in Dataset Generation and EDA Tool Assistants**", *Proc. ICCAD*, 2024.

B.-Y. Wu, R. Liang, G. Pradipta, A. Agnesina, H. Ren, and V. A. Chhabria, "2024 ICCAD CAD Contest Problem C: Scalable Logic Gate Sizing Using ML Techniques and GPU Acceleration", *Proc. ICCAD*, 2024.

U. Sharma*, B.-Y. Wu*, S. R. D. Kankipati, V. A. Chhabria, and A. Rovinski, "OpenROAD-Assistant: An Open-Source Large Language Model for Physical Design Tasks", *Proc. MLCAD*, 2024.

V. Gopalakrishnan, B.-Y. Wu, and V. A. Chhabria, "ML-INSIGHT: Machine Learning for Inrush Current Prediction and Power Switch Network Improvement", *Proc. ISLPED*, 2024.

B.-Y. Wu, U. Sharma, S. R. D. Kankipati, A. Yadav, B. K. George, S. R. Guntupalli, A. Rovinski, and V. A. Chhabria, "EDA Corpus: A Large Language Model Dataset for Enhanced Interaction with OpenROAD", *Proc. LAD*, 2024. (Best Paper Nominated)

V. A. Chhabria, W. Jiang, A. B. Kahng, R. Liang, H. Ren, S. S. Sapatnekar, and **B.-Y. Wu***, "**OpenROAD and CircuitOps: Infrastructure for ML EDA Research and Education**", *Proc. VTS*, 2024. (primary author)

B.-Y. Wu, S.-Y. Fang, H.-W. Chang, and P. Wei, "SpeedER: A Supervised Encoder-Decoder Driven Engine for Effective Resistance Estimation of Power Delivery Networks", *Proc. MLCAD*, 2022. (Best Paper Award)

PROJECT EXPERIENCE

OpenROAD-Agent | Python

Jan. 2025 - Mar. 2025

- Github link: https://github.com/OpenROAD-Assistant/OpenROAD-Agent
- Open-sourced the framework that integrates the script-generating LLM with the physical design tool.
- Combined prompt engineering with the physical design tool's feedback to iteratively generate the tool script.

2024 ICCAD Contest Benchmark | Verilog/Tcl/Python/C++

May. 2024 - Oct. 2024

- Github link: https://github.com/ASU-VDA-Lab/2024_ICCAD_Contest_Gate_Sizing_Benchmark
- Used C++ and SWIG to create Python APIs in OpenROAD, enabling gate sizing operations using OpenROAD's Python APIs.
- Developed Python scripts for examples and evaluations for the contest.
- Used EDA tools to synthesize netlists with the ASAP7 library and perform placement and routing.

OpenROAD-Assistant | Python

Mar. 2023 – Jun. 2024

- Github link: https://github.com/OpenROAD-Assistant/OpenROAD-Assistant
- Open-sourced the LLM for generating scripts for the physical design tools and answering questions related to the physical design tools.

EDA-Corpus | Python

Feb. 2024 - Mar. 2024

- Github link: https://github.com/OpenROAD-Assistant/EDA-Corpus
- Open-sourced the first dataset of physical design tool scripts for LLM-based physical design research.

2024 ASP-DAC Tutorial Talk | C++/Python

Oct. 2023 – Jan. 2024

- Github link: https://github.com/ASU-VDA-Lab/ASP-DAC24-Tutorial
- Developed STA-related Python API for OpenROAD to provide flexibility in ML-EDA.
- Created demos on using the OpenROAD Python Interface and using Nvidia's CircuitOps to build data pipelines for ML-based EDA research.
- Presented at 2024 ASP-DAC as a tutorial. (conference link)

CircuitOps | Tcl/Python

Oct. 2023 - Jan. 2024

- **Github link**: https://github.com/NVlabs/CircuitOps
- Developed an ML-friendly data infrastructure to generate datasets for ML-EDA applications.

Awards

MLCAD Student Travel Grant	Sept. 2024
Ferdinand A. Stanchi Fellowship	Aug. 2024
DAC Young Fellow Travel Grant	Jun. 2024
MLCAD Student Travel Grant	Sept. 2023
Fulton Fellows Fellowship	Aug. 2023
Best Paper Award at MLCAD 2022	Sept. 2022
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Professional Experience

Topic chiar of Problem C at 2024 ICCAD CAD Contest	Oct. 2024
IEEE CEDA	Newark, New Jersey
2024 ASP-DAC Tutorial Talk	Jan. 2024
ACM SIGDA	Incheon, South Korea