Stanford Research 645.lvlib:Delay Controlled Trigger.vi
C:\Users\Second Harmonic Spec\Documents\Labview Training\Data Aquisition\Stanford Research 645\Utility\Delay Controlled Trigger.vi
Last modified on 14-04-2023 at 20:21
Printed on 14-04-2023 at 20:54

Connector Pane

Stanford Research 645.lvlib:Delay Controlled Trigger.vi

Front Panel

Select Instrument
DG645 VISA resource
GPIB0::3::INSTR
Instrument Identity

Error I/O
error in (no error)
status
code
0
source
error out
status
code
0
source

Last Error
Status Byte
Status Resister
Event Status
Show Error Status Register
No
Last Error Code
Status Byte
Status Register
Event Status

Operation Modes
RESET/START TRIGG/ CLEAN STATUS/AUTO CALIBRATION/SELF TEST/REMOTE ACCESS/ FRONT ACCESS
Remote Access
5

Channel Delays, Pulse Amplitude

All Parameters Display Screen

T0 Or Zero Delay Channel
0 Delay
T0 Falling Edge Delay

Delay Channel-1 A-B
A Rising Edge Delay (2)
B Falling Edge Delay

Delay Channel-2 C-D
C Rising Edge Delay (4)
D Falling Edge Delay

Delay Channel-3 E-F
E Rising Edge Delay (6)
F Falling Edge Delay

Delay Channel-4 G-H
G Rising Edge Delay (8)
H Falling Edge Delay

Pulse Amplitude
0_T0 Pulse Amplitude
A_B Pulse Amplitude
C_D Pulse Amplitude
E_F Pulse Amplitude
G_H Pulse Amplitude

Prescale Factor
0_T0 Prescale Factor
A_B Prescale Factor
A_B Prescale Phase
C_D Prescale Factor
C_D Prescale Phase
E_F Prescale Factor
E_F Prescale Phase
G_H Prescale Factor
G_H Prescale Phase

Show Parameters
Show Parameters (Yes/No)
No

Trigger Parameters
Trigger Source
Internal Trigger Rate
Time Base for DG645
External Trig Level

Burst Parameters
Burst Count
Burst Mode
Burst Delay
T0 Status
Burst Period

Instrument Control and Input Parameters Modify

All Parameters Controls

Modify Settings
Modify Settings
No

Save Current Settings
Save (Yes/No)
No
Save to Location #
Save To 0
0

Recall Settings
Recal (Yes/No)
No
Recal From Loc #
Recal From 0
0

Burst Parameters and Trigger Source
Burst Count: 1
Burst Delay: 30e-3
Burst Period: 500e-3
Burst Mode: ENABLE 1
T0 Status: T0 ENABLED FOR ALL BURST CYLCE 0
Triggering Source and Modes: SINGLE SHOT EXT RISING EDGE 3

Channel Delay Parameters, Pulse Amplitude and Prescale Factors
0_T0 Pulse Amplitude: 2 V 3
Trig I/P Prescale Factor: 1

Delay Channel-1 A-B Or Main Shutter Control
(A Rise) Shutter Opening Delay: 0e-9
(A+B Falling Edge) Shutter Duration: 50e-3
A Rising Edge Relative to: 0 DELAY RISING EDGE 0
A_B Pulse Amplitude: 2 V 3
A_B Prescale Factor>0: 1

Delay Channel-2 C-D EMCCD Trigger Control
(C Rise) Delay to Match Pulse Phase: 0e-9
(C+D Falling Edge) EMCCD Trigg Width: 500e-6
C Rising Edge Relative to: 0 DELAY RISING EDGE 0
C_D Pulse Amplitude: 2 V 3
C_D Prescale Factor>0: 1

Delay Channel-3 E-F Gate Voltage Control
(E Rise) Gate Pulse Rising Delay: 0e-9
(E+F Falling Edge) Gate Pulse Width: 500e-6
E Rising Edge Relative to: 0 DELAY RISING EDGE 0
E_F Pulse Amplitude: 2 V 3
E_F Prescale Factor>0: 1

Delay Channel-4 G-H Drain Voltage Control
(G Rise) Drain Pulse Rising Delay: 0e-9
G+H Falling Edge Delay: 500e-6
G Rising Edge Relative to: 0 DELAY RISING EDGE 0
G_H Pulse Amplitude: 2 V 3
G_H Prescale Factor>0: 1

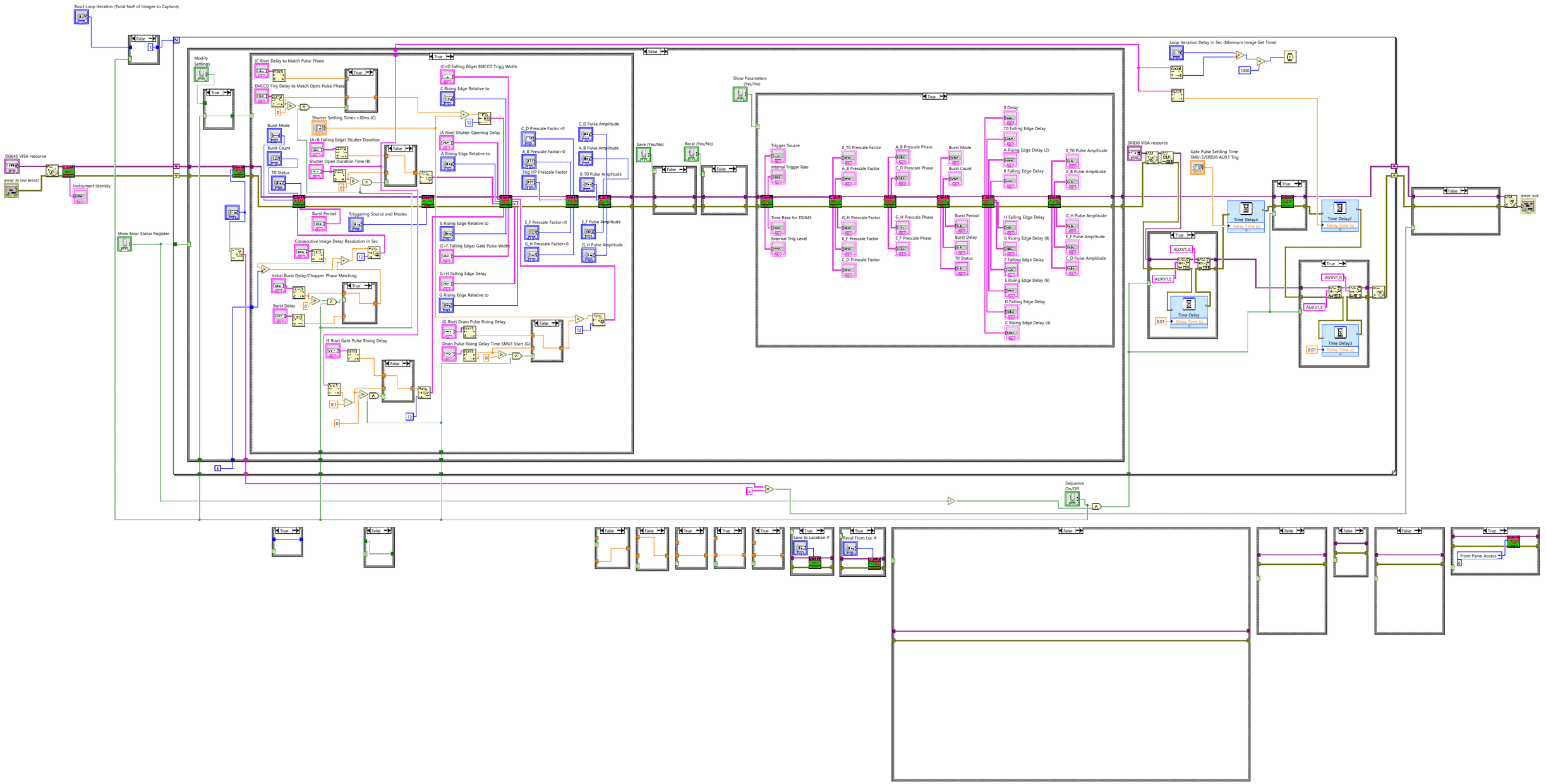
Quick Controls and Burst Delay Sequence
Initial Burst Delay/Chopper Phase Matching: 20e-3
Consecutive Image Delay Resolution in Sec: 30e-3
Shutter Open Duration Time (B): 3
Shutter Settling Time> =30ms (C): 1
EMCCD Trig Delay to Match Optic Pulse Phase (C): 10e-9
Drain Pulse Rising Delay Time SMU1 Start (G): 10e-9
Busrt Loop Iteration (Total No# of Images to Capture): 1
Loop Iteration Delay in Sec (Minimum Image Get Time): 5
Sequence On/Off
No
Sequence On/Off

Delay Control for EMCCD on DG645 Delay Generator
Designed by Binit Mallick, IIT Bombay PhD Student, EE Department (binit.mallick@gmail.com)

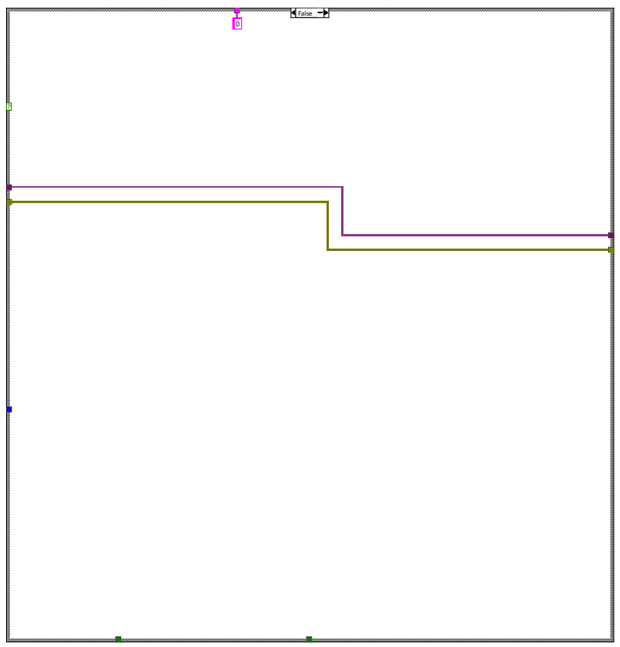
SMU-2 Trigger Control Source SR830 Lock-In AUX-1 Out
SR830 VISA resource
GPIB0::8::INSTR
Gate Pulse Settling Time SMU-2/SR830-AUX1 Trig
0.5

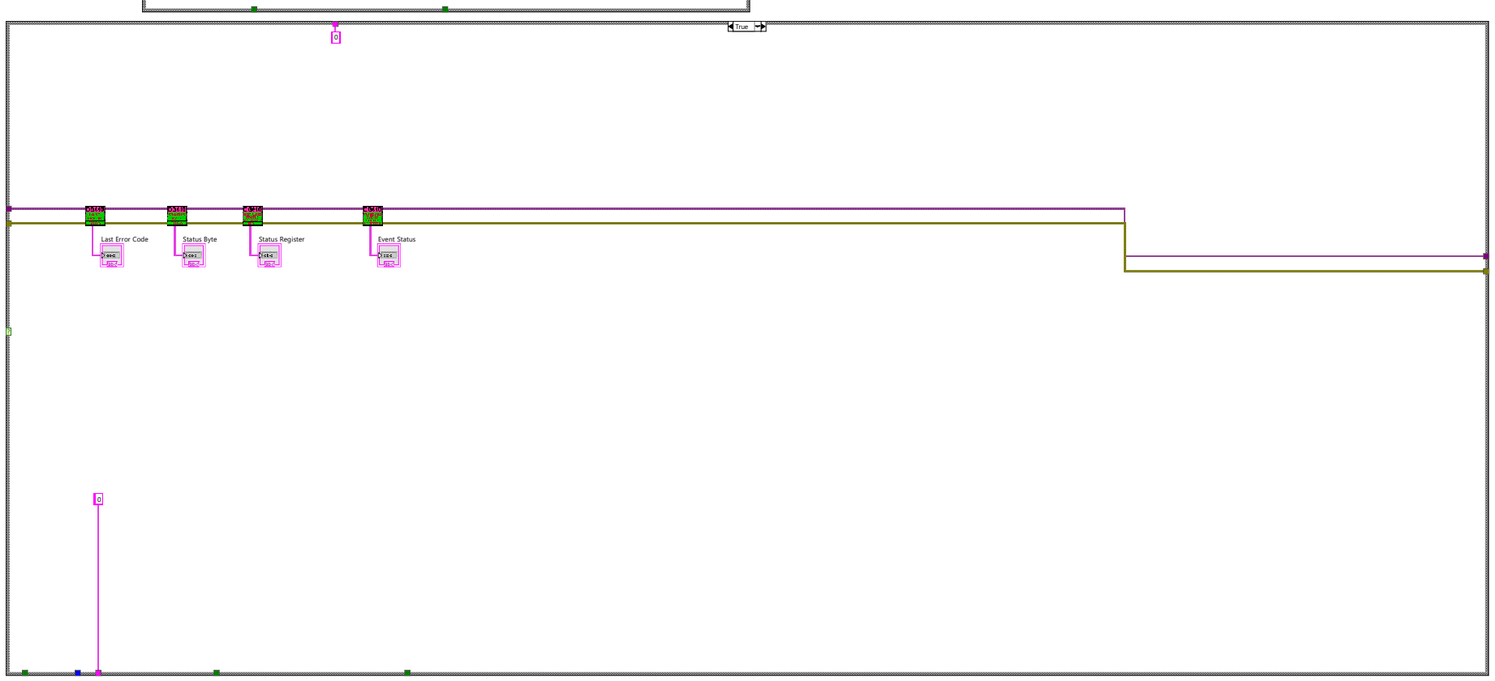
Stanford Research 645.lvlib:Delay Controlled Trigger.vi
C:\Users\Second Harmonic Spec\Documents\Labview Training\Data Aquisition\Stanford Research 645\Utility\Delay Controlled Trigger.vi
Last modified on 14-04-2023 at 20:21
Printed on 14-04-2023 at 20:54

Block Diagram



Stanford Research 645.lvlib:Delay Controlled Trigger.vi
C:\Users\Second Harmonic Spec\Documents\Labview Training\Data Aquisition\Stanford Research 645\Utility\Delay Controlled Trigger.vi
Last modified on 14-04-2023 at 20:21
Printed on 14-04-2023 at 20:54





Express VI Configuration Information