Binod Kumar
M.Tech.+Ph.D. (MicroElectronics & VLSI)

RESEARCH INTERESTS

Primary Areas: VLSI Testing Methodologies and DfT (Design for Testability) Architectures, Silicon Debugging, Application of Machine Learning in SoC Design Verification, Formal Verification

Secondary Areas: Computing Systems Security, Chip Multiprocessors (CMP) Memory Consistency & Coherency, Low Power VLSI Design, Reliability Issues in Deep Learning Systems

EDUCATION DETAILS

Master of Technology (M.Tech.) + Doctor of Philosophy (Ph.D.) in MicroElectronics & VLSI, Department of Electrical Engineering, Indian Institute of Technology Bombay (IITB), Mumbai July 2014-Sept. 2019

Thesis Title: *Effective Techniques for Post-Silicon Validation and Debug*
Thesis Advisor: *Prof. Virendra Singh*

Research: Novel techniques for some of the challenging problems during post-silicon validation and debug of integrated circuits; Self-checking methods for validation and localization of different kinds of errors; Improvements in on-chip debug infrastructure and reconfigurable visibility enhancement mechanism; Machine learning-assisted debugging methodologies for fine-grained error localization.

Bachelor of Technology (B.Tech.) in Electronics & Communication Engineering, National Institute of Technology (NIT), Silchar, Assam, India July 2009-May 2013, CPI: 9.13/10

Undergraduate Thesis Title: *Implementation of Non-Linear Effects in Designing Improved Optical Fiber Communication Systems*
Undergraduate Thesis Advisor: *Prof. Madhumita Paul*

Undergraduate Research: Applicability of non-linear effects (e.g., second harmonic generation) of novel semiconductor devices (quantum dots) for improving the performance of optical fiber communication systems; Self-Phase Modulation (SPM) effect to mitigate dispersion effects in optical transmitters.

PUBLICATION HIGHLIGHTS

Total Journal Publications: 7 (IEEE/Springer/ACM: 5, Others: 2), Book Chapters: 3
Peer-reviewed International Conferences: 19
Patents Filed: 1
Google Scholar Page: https://scholar.google.co.in/citations?user=FtNL2bwAAAAJ&hl=en
DBLP Page: https://dblp.org/pers/hd/k/Kumar_0001:Binod

TEACHING/WORK EXPERIENCE

- Research/Teaching Assistantship Experience:
  - Worked at the position of **System Administrator** in VLSI Lab, Dept. of Electrical Engineering, IIT Bombay as a part of research assistantship (RA) (July 2014-June 2017)
    - **Responsibility**: Managing various CAD tool softwares (installation and upgradation) on more than twenty-five networked Linux servers and resolving user queries related to them.
    - Developed user-oriented tutorials and effective training materials for various CAD tools.
  - Contributed to **Indo-Japanese Joint Research Laboratory Program** for the development of design and debug methodologies in ongoing project, *Architecting Intelligent Dependable Cyber-Physical System Targeting IoTs and Mobile Big Data Analysis* (July 2017-Sept. 2019)
  - Worked as Teaching Assistant (TA) (July 2017-May 2019)
    - **Responsibility**: Conducting weekly quizzes and answering doubts/assignment-related queries of students for two courses- **Testing and verification of digital circuits (PG, 60+ students)** and **Microprocessors (UG, 140+ students)**.
    - Evaluation of answer scripts, assignment and course projects.
  - Mentored 10+ students for completing Bachelor's and Master's projects (Jan. 2017- Sept. 2019)
- Industrial Work Experience:
  - Working as **Senior Engineer** at **QUALCOMM India** (Oct. 2019-Till date)
    - **Responsibility**: Handling DFT ATPG sign-off issues and silicon bring-up of different chips manufactured at cutting edge technologies (10nm and lower technology nodes).

    - Contributing to introduction of novel DFT and silicon debug techniques/tool flows.
  - Worked with **RELIANCE JIO INFOCOMM** as **Systems Engineer** (June-Nov. 2013)
    - **Responsibility**: Validating core nodes in IP Multi-media Subsystem (IMS) architecture as a part of pan-India deployment of Reliance 4G Jio network
    - Contributed to deployment of MODEMs at different sites & testing/quality assurance

MAJOR SCHOLASTIC ACHIEVEMENTS

- "Excellence in Research Award" nomination for Ph.D. thesis work
- "Excellence in Teaching Assistantship" award for undergraduate course Microprocessors at IIT Bombay.
- Honorable mention (4th prize out of 100+ teams worldwide) in ICCAD-2018 design contest challenge "Program Building for Name Mapping Suite".
- IIT Bombay EE department travel grant for attending IOLTS-2017 conference at Thessaloniki, Greece.
- Obtained **AP** grade for outstanding academic performance in Foundations of VLSI CAD course (IITB).
- National Talent Search Examination (NTSE) scholarship post-matriculation (for 6 years, 2007-13).
- North-eastern Council (NEC) regional-level scholarship (continuously for 4 years, awarded for meritorious performance during B.Tech., 2009-2013).
- Top 10% Certificate in NATIONAL STANDARD EXAM IN PHYSICS & CHEMISTRY (2008-2009).

TECHNICAL SKILLS(CAD TOOLS & PROGRAMMING)

Design Development	ModelSim, Design Compiler, VCS, IC Compiler, RTL Compiler, Xilinx ISE, NC-Sim, PrimeTime, Altera Quartus, QuestaSim, Encounter Digital Systems Implementation
Test & Verification	Tetramax, Encounter Test, JasperGold Model Checker, Incisive Formal Verifier
Languages & Scripting	Verilog, VHDL, Python, System Verilog, C/C++, Bash scripting

MAJOR RELEVANT COURSES UNDERTAKEN (M.Tech. + Ph.D.)

- Processor Design
- VLSI Design Lab
- Solid State Devices
- Foundations of VLSI CAD
- VLSI Design
- CMOS Analog VLSI Design
- Testing and Verification of VLSI Circuits
- Advanced Topics in Computer Arch.
- Current Topics in VLSI & System Design

PATENT (FILED)

- Vineesh V S, **Binod Kumar** and Virendra Singh, "A Method for Bug Localization", Mumbai, India, July 2020 (IPO Patent application number: 202021031871)

COMPLETE LIST OF PUBLICATIONS

- **Journal Articles**

($J1$) **Binod Kumar**, Masahiro Fujita, and Virendra Singh, "SAT-based Silicon Debug of Electrical Errors under Restricted Observability Enhancement", Journal on Electronic Test Theory and Applications (**JETTA**), October 2019

($J2$) **Binod Kumar**, Jay Adhaduk, Kanad Basu, Masahiro Fujita, and Virendra Singh, "A Methodology to Capture Fine-grained Internal Visibility during Multi-session Silicon Debug", IEEE Transaction on on Very Large Scale Integration Systems (**TVLSI)**, Dec. 2019

($J3$) **Binod Kumar**, Kanad Basu, Masahiro Fujita, and Virendra Singh, "Post-silicon gate-level error localization with effective & combined trace signal selection", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems (**TCAD**), Nov. 2018

($J4$) Vineesh V S, **Binod Kumar**, Rushikesh Shinde, Neelam Sharma, Masahiro Fujita and Virendra Singh, "Enhanced Design Debugging with Assistance from Guidance-based Model Checking", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Aug. 2020 (**TCAD**)

($J5$) Nandan Kumar Jha, Sparsh Mittal, **Binod Kumar** and Govardhan Mattela, "DeepPeep: Exploiting Design Ramifications to Decipher the Architecture of Compact DNNs", ACM Journal of Emerging Technologies in Computing Systems (**JETC**), 2020

($J6$) V. Kumar, K. L. Baishnab and **B. Kumar**, "A Novel Shared Active Pixel Architecture (SAPA) with Low Dark Current and High Fill-Factor (FF) for CMOS Image Sensors", Journal of Low Power Electronics (JOLPE), 2017, Pages: 490-496

($J7$) V. Kumar, A. Singh, S. Upadhyay and **B. Kumar**, "PowerDelay-Error-Efficient Approximate Adder for Error-Resilient Applications", Journal of Circuits, Systems and Computers, 2019

- **Book Chapters**

($BC1$) Saurabh Gangurde and **Binod Kumar**, "A Unified Methodology For Hardware Obfuscation and IP Watermarking", VLSI Design and Test (**VDAT**) 2019, Springer Singapore.

($BC2$) Vineesh VS, **Binod Kumar** and Jay Adhaduk, "Identification of Effective Guidance Hints for Better Design Debugging by Formal methods", VLSI Design and Test (**VDAT**) 2019, Springer Singapore.

($BC3$) **Binod Kumar**, Kanad Basu, Ankit Jindal, Brajesh Pandey and Masahiro Fujita, "A Formal Perspective on Effective Post-silicon Debug and Trace Signal Selection", VLSI Design and Test (**VDAT**) 2017, Springer Singapore.

- **International Conferences**

($C1$) **Binod Kumar**, Akshay Kumar Jaiswal, Vineesh V S and Rushikesh Shinde, "Analyzing Hardware Security Properties of Processors through Model Checking", 33^{rd} International Conference on VLSI Design (**VLSID**) 2020, India

($C2$) Utsav Jana, **Binod Kumar**, Ankita Agarwal and Deepak Agrawal, "Concealing Test Compression Mechanisms from Security Attacks", International Test Conference (**ITC-India**) 2020, India

($C3$) **Binod Kumar**, Swapniel Thakur, Kanad Basu, Masahiro Fujita and Virendra Singh, "A Low Overhead Methodology for Validating Memory Consistency Models in Chip Multiprocessors", 33^{rd} International Conference on VLSI Design (**VLSID**) 2020, India

($C4$) **Binod Kumar**, Atul Kumar Bhosale, Masahiro Fujita and Virendra Singh, "Validating Multiprocessor Cache Coherence Mechanisms Under Diminished Observability", IEEE 28^{th} Asian Test Symposium (**ATS**), Kolkata, India, Dec 2019

($C5$) **Binod Kumar**, Masahiro Fujita and Virendra Singh, "A Methodology for SAT-based Electrical Error Debugging during Post-silicon Validation", 32^{nd} International Conference on VLSI Design (**VLSID**) 2019, New Delhi, Jan 2019

($C6$) Vineesh V S, **Binod Kumar**, Rushikesh Shinde, Akshay Kumar Jaiswal, Harsh Bhargava and Virendra Singh, "Orion: A Technique to Prune State Space Search Directions for Guidance-Based Formal Verification", IEEE 28^{th} Asian Test Symposium (**ATS**), Kolkata, India, Dec 2019

($C7$) **Binod Kumar**, Kanad Basu, and Virendra Singh, "A Technique for Electrical Error Localization with Learning Methods During Post-silicon Debugging", 10^{th} International Green and Sustainable Computing Conference (**IGSC**) 2018, Pittsburgh, USA, Oct 2018

($C8$) Ankit Jindal, **Binod Kumar**, Kanad Basu, and Masahiro Fujita, "ELURA: a methodology for post-silicon gate-level Error Localization Using Regression Analysis", 31^{st} International conference on VLSI Design (**VLSID**) 2018, Pune, Jan 2018

($C9$) Ankit Jindal, **Binod Kumar**, Masahiro Fujita and Virendra Singh " Silicon debug with maximally expanded internal observability using nearest neighbour algorithm", IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**) 2018, Hongkong, SAR, China, July 2018

($C10$) **Binod Kumar**, Ankit Jindal, Masahiro Fujita and Virendra Singh, "Post-silicon Observability Enhancement with Topology Based Trace Signal Selection", 18^{th} IEEE Latin American Test Symposium (**LATS**) 2017, Bogota, Colombia, March 2017

($C11$) **Binod Kumar**, Kanad Basu, Ankit Jindal, Masahiro Fujita, and Virendra Singh, "Improving post-silicon error detection with topological selection of trace signals", 25^{th} IEEE/IFIP International Conference on on Very Large Scale Integration (**VLSI-SoC**), Abu Dhabi, UAE, Oct 2017

($C12$) **Binod Kumar**, Ankit Jindal, Jaynarayan Tudu, Brajesh Pandey and Virendra Singh, "Revisiting Random Access Scan for Effective Enhancement of Post-silicon Observability", 23^{rd} IEEE International Symposium on On-Line Testing and Robust System Design (**IOLTS**) 2017, Thessaloniki, Greece, July 2017

($C13$) **Binod Kumar**, Ankit Jindal, Virendra Singh, and Masahiro Fujita, "A methodology for trace signal selection to improve error detection in post silicon validation", 30^{th} International conference on VLSI Design (**VLSID**) 2017, Hyderabad, Jan 2017

($C14$) **Binod Kumar**, Ankit Jindal and Virendra Singh, "A trace signal selection algorithm for improved post silicon debug", 14^{th} IEEE East-West Design and Test Symposium (**EWDTS**) 2016, Yerevan, Armenia, Oct 2016

($C15$) **Binod Kumar**, Ankit Jindal, Masahiro Fujita, and Virendra Singh, "Combining Restorability and Error Detection Ability for Effective Trace Signal Selection", 27^{th} ACM Great Lakes Symposium on VLSI (**GLSVLSI**) 2017, Alberta, Canada, May 2017

($C16$) Toral Shah, Anzhela Matrosova, **Binod Kumar**, Masahiro Fujita and Virendra Singh, "Testing Multiple Stuck-at Faults of ROBDD Based Combinational Circuit Design", 18^{th} IEEE Latin American Test Symposium (**LATS**) 2017, Bogota, Colombia, March 2017

($C17$) Nirmal Kumar Boran, Rameshwar Prasad Meghwal, Kuldeep Sharma, **Binod Kumar**, and Virendra Singh, "Performance modelling of heterogeneous ISA multicore architecture", 14^{th} IEEE East-West Design and Test Symposium (**EWDTS**) 2016, Yerevan, Armenia, Oct 2016

(*C*18) **Binod Kumar**, Boda Nehru, Brajesh Pandey, Jaynarayan T Tudu, and Virendra Singh, "A technique for low power, stuck-at fault diagnosable and reconfigurable scan architecture", 14^{th} IEEE East-West Design and Test Symposium (**EWDTS**) 2016, Yerevan, Armenia, Oct 2016

(*C*19) **Binod Kumar**, Boda Nehru, Brajesh Pandey and Jaynarayan Tudu, "Skip-Scan: A Methodology for Test Time Reduction", 20^{th} International Symposium on VLSI Design and Test (**VDAT**) 2016, Guwahati, India, May 2016

KEY COURSE PROJECTS/SEMINAR UNDERTAKEN/MENTORED (M.Tech. + Ph.D.)

- Design of a fault simulator (with fault dropping) for digital combinational circuits
- Automatic Test Pattern Generation (ATPG) for digital circuits to achieve specified fault coverage
- Design of an operational amplifier to achieve specified requirements of small-signal gain, unity gain frequency, voltage swing, gain and phase margin
- Development of congestion-aware routing algorithm of a group of signals under fixed wire-length budget
- Design of a 8 bit countdown timer & its layout and verification by post-layout simulation
- Design of RISC pipelined processor (in VHDL) with handling of data, memory and control hazards
- Design & post-synthesis optimization of a GCD calculator using Euclidean algorithm
- Static timing characterization of flip-flops using Ngspice
- Stack-based implementation of a computing unit in VHDL & testing by JTAG scan chain
- Design & post-synthesis simulation of a computing unit using Quartus Tool & DE0-Nano board
- Sequence detector, priority encoder and ALU design and their simulation-based verification
- TCAD simulation of 90 nm short channel MOSFET & its electrical characterization
- Simulation & electrical characterization of *pn* junction diode, MOS Capacitor & long channel MOS
- MTech. Seminar on introduction to HEMT compact modeling for high frequency RF applications
- Mentored one student for year-long Master's project on "State Retention for IoT Device Operating on Intermittent Energy"
- Mentored one student for half-semester R&D project on "Simplifying Design Verification with Hardware Description Language (HDL) Slicing"

PROFESSIONAL MEMBERSHIP & REVIEWER SERVICES

Member of ACM and IEEE
Served as reviewer for several IEEE TCAD and IEEE OpenAccess journal articles
Served as Program Committee member for Asian Test Symposium (ATS)-2020

COURSES (FOR TEACHING)

- Basic level:
  - Digital Systems/Circuits
  - VLSI Design
  - Microprocessors & Micro-controllers
  - Foundation of VLSI CAD
  - Computer Organization & Architecture
  - Analog Circuits
  - Introduction to Semiconductor Devices
- Advanced level:
  - SoC Verification & Test Techniques
  - Hardware Security Principles
  - System Simulation Methodologies
  - Applying ML in SOC Design & Verification
  - IoT Systems Design & Verification
  - Healthcare Diagnostics Systems

REFERENCES

- Prof. Virendra Singh
  Department of Electrical Engineering
  IIT Bombay, Powai, Mumbai
  Email:virendra@computer.org

- Prof. Masahiro Fujita
  VLSI Design and Education Center
  University of Tokyo, Tokyo, Japan
  Email:fujita@ee.t.u-tokyo.ac.jp

- Prof. Kanad Basu
  Department of Electrical and Computer Engg.
  University of Texas at Dallas, USA
  Email:kanad.basu@utdallas.edu

- Prof. Adit Singh
  Dept. of Electrical Engineering
  Auburn University, USA
  Email: adsingh@eng.auburn.edu

PERSONAL DETAILS

- Email-ID: binodkumar@ee.iitb.ac.in
- Alternative Email-ID: binod23.iitb@gmail.com
- Contact No. +91-8879049805
- DoB: 21/03/1992
- Father's Name: Mr. Bipin Kumar Singh
- Mother's Name: Mrs. Nilam Kumari
- Permanent Address: Govt. Qtr-3/25, AT+P.O- Kunjaban Township (KTS), Kunjaban, Agartala, Tripura (W)-799006
- Marital Status: Unmarried
- Languages Known: English, Hindi, Bengali (speaking only)