Voltage Reference:

The 1.65V reference is generated by a shunt diode(D1), the minimum working current is 1uA.

In the simulation, I use a similar 2.5V shunt diode which is available in build-in library. Then divide 2.5V to 1.65V reference by two resistors.

The shunt reference only sources current. In order to sink current, a follower(OP1) buffers the reference and output Vref2.5.

Vref1.65 is used as bias for non-inverting Schmitt comparator(OP2) and inverting Schmitt comparator(OP3).

The shunt diode(D1) is working at 1.5uA. Current of R2 & R3 is set to 1uA.

R1= (Vbatt – Vref) / (Ir2 + Id1)

= (7.5 – 2.5) / (1u + 1.5u) = 2Mohm

Vbatt sensing divider:

When Vbatt = (6V + 6.5V) /2 = 6.25V, R6 & R7 divided Vbatt to 1.65V. The divided Vbatt is buffered by OP4 and then feed into non-inverting Schmitt comparator(OP2) later Vref2.5 later.

The input resistance of non-inverting Schmitt comparator(OP2) paralleled by R7 may change the divider, so the follower(OP4) is implemented.

When Vbatt = (7.75V + 7.85V) /2 = 7.8V, R4 & R5 divided Vbatt to 1.65V. The divided Vbatt is feed into inverting Schmitt comparator(OP3) later.

Current of R4 & R6 are all set to 1uA.

Lower threshold (6V-6.5V) non-inverting Schmitt comparator:

OP2 is a non-inverting Schmitt comparator. Set Vss of OP3 0V. Set Vcc of OP3 3.3V.

The Schmitt window is calculated as:

Vschmitt-window = Vref1.65 +- (Vcc / 2)\*(R10 / R11) = 1.584V~1.716V

The corresponding Vbatt of the Schmitt window is 6V~6.5V

OP2 must have a very low input bias current, so that the bias current doesn’t affect the divider.

OP2 must be a rail-to-rail output.

In order to drive a PMOS and behave the right way logically, the output of OP2 is inverted by M1 and ‘1’ of ‘Input\_1’ is pulled up to Vbatt to fully close PMOS.

Higher threshold (7.75-7.85V) Schmitt comparator:

OP3 is an inverting Schmitt comparator. Set Vss of OP3 0V. Set Vcc of OP3 3.3V.

The Schmitt window is calculated as:

Vschmitt-window = Vref1.65 +- (Vcc / 2)\*(R8//R15 / (R8//R15 + R9)) = 1.62V~1.68V

The corresponding Vbatt of the Schmitt window is 7.75V~7.85V

OP3 must have a very low input bias current, so that the bias current doesn’t affect the divider.

OP3 must be a rail-to-rail output.

3.3V LDO:

Vbatt is regulated to 3.3V for OP-amps. The LDO should have low quiescent current.

Others:

If useing a Lithium Charge IC(e.g BQ2057), the body diode of the P-MOS will conduct all the time. It causes over charging. By using a PNP instead. In this case, the current & power consumption goes up.

Cost estimate (option1)

TLV8544 \*1: $0.3 \*1

ZXRE330ASA \*1: $0.3 \*1

NCP551SN50T1G \*1: $0.2 \*1

NMOS\*1: $0.1 \*1

Current estimate:

Op-amp 0.5uA \*4 = 2.0uA

Shunt diode 1.5uA

Divider resistors 1uA\*3 = 3uA

LDO Iq 1uA max

R8 & R9 1uA max

R10 & R11 1uA max

Ids of M1 1uA