REALTEK RTL8139C PCB LAYOUT GUIDE

1. Introduction

The Realtek RTL8139C is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

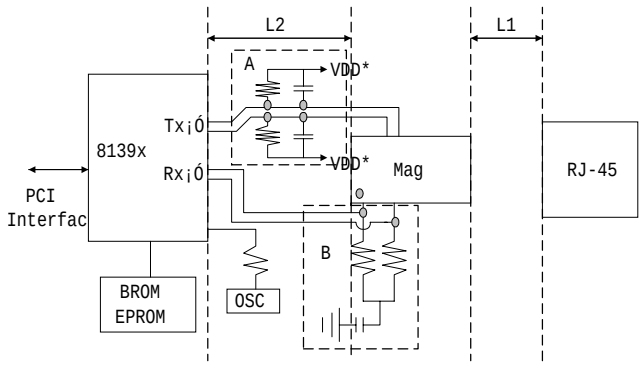
This guide is intended for the Realtek customer who will be designing a hardware system around the Realtek RTL8139C chips. It has the following goals:

(1) Make a noise-free, power-stable, environment that suitable for the RTL8139C.
(2) Reduce the possibility of EMI, EMC and their influence to the chip.
(3) Simplify the task of routing signal trace, so as to make a better circuit for the RTL8139C.

All information provided in this guide has been tested by Realtek systems engineers to be accurate and directly applicable to proper system designs using the RTL8139.

2. Placement

The following diagram and description cover an ideal placement situation.



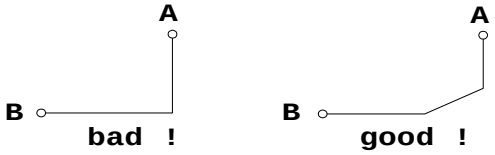
Component placement block diagram

1. Block B may be placed close to Mag, as the RTL8139C will sink current from Block A during Tx. When Rx is active, the RTL8139C will take a differential volt signal from Block B.
2. The distance from the RJ-45 to Mag. (L1) should be as short as possible.
3. RTSET of the RTL8139C pin 84 should be placed as close to the RTL8139C chip as possible and as far away as possible from the TX+/-, RX+/-, and clock signals.
4. The crystal should not be placed near I/O ports, board edges, or other high-frequency devices or traces (such as Tx , Rx and Power signals) or a magnetic field device (such as magnetic).
5. The outer shield of the crystal needs good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.
6. The magnetic device or devices with magnetic fields should be separated and mounted at 90° to each other. High Current devices should be placed as close to the power source as possible to reduce the trace length. Traces with high current will induce more EMI.
7. Termination Resistors: The pull high resistors and capacitors of Block A, above, need to be located close to the RTL8139C chip. The 2 receiving termination resistors (50Ω) of Block B may be placed close to Mag. For better impedance matching, these resistor/capacitor pairs should be chosen carefully.
8. The traces between the RTL8139C and Mag. (L2, above) should be as short as possible. However, for practical implementation convenience, the distance can be flexible, but should remain within a 10~12cm maximum length. It is important to keep the Tx± and Rx± signal traces symmetrical.
9. The signal trace length difference between Tx+ and Tx- (and Rx+ and Rx-) should be kept within 2 cm.
10. *VDD is 3.3V for the RTL8139C.

3. Trace Routing

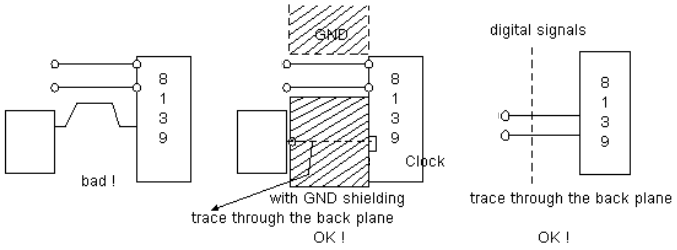
Good routing of traces can reduce propagation delay, cross-talk, and high-frequency noise. It will also improve the signal quality to the receiver and reduce the loss from transmit signals.

1. Avoid right angle signal traces:



2. It is important to avoid interference between digital signals (such as PCI signals, BROM, Flash or CLOCKs), Analog signals (Tx±, Rx±, RTSET traces) and Power traces. If it is necessary to cross digital signals with Analog/Power, do so at 90˚ angles.

3. The RTL8139C can use a 25M OSC clock as its reference clock. However, it may also use a 25M *crystal* as the reference clock source with just a slight circuit modification.



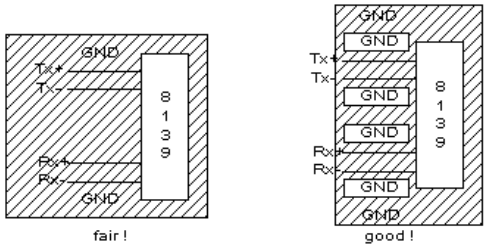
Using a 25M crystal.

4. The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. The clock and other high speed signal traces should be as short and wide as possible (compared with normal digital traces). It is better to have a ground plane under these traces, with, if possible, a GND plane around them.

5. The length of a signal trace should not exceed 1/20 of the highest harmonic (about 10^{th}) wavelength. For example, the 25M clock trace should not exceed 30cm and the 125M signal traces (Tx±, Rx±) should not exceed 12cm.

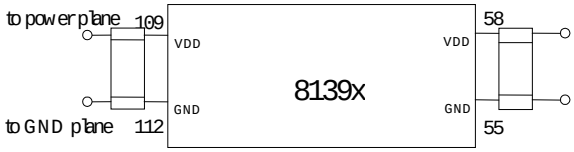
6. The Power signal traces (de-couple cap traces, power traces, grounding traces) should be short and wide. The VIAs of the de-couple capacitor should be larger in diameter.

7. Each cap should have a separated VIA to GND. The GND VIA should be within 0.2 inch. Avoid the following de-couple cap connection:



8. All analog power pins on the 8139C (pins 90, 96, 77) need to be de-coupled with a capacitor. The de-couple capacitors should be placed as close to the IC as possible and the traces should be short.

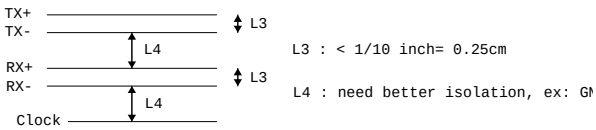
9. All digital power pins on the RTL8139C can be improved with a de-couple capacitor. This is especially true for pins 58 and 109. See the following diagram.



10. Ferrite Bead placement: The bead connected to pins 77, 90 and 96 should be as close to the RTL8139C as possible. Pin 77 must use a bead (100MHz/100Ω).

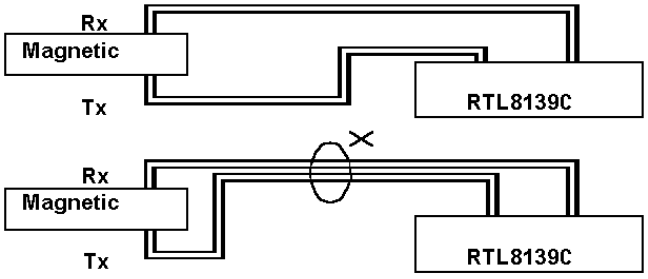
11. It is important that the Tx± and Rx± traces follow these guidelines:

a. Avoid signal loss on these traces.
b. Tx+ and Tx- should be as equal in length as possible.
c. Rx+ and Rx- should be as equal in length as possible.
d. The distance between Tx± and Rx±:



e. Rx± should not use a via. It is better if the Rx± traces remain on the component side.
f. Ferrite Beads should be as close to the chip pins as possible and have a rating of 100Ω@100MHz.

12. Keep the distance between the Tx and Rx signal pairs large, and decrease the portion of these two signal-pair traces which run parallel. In addition, Ground planes can be separated underneath the Tx and Rx signal pairs.

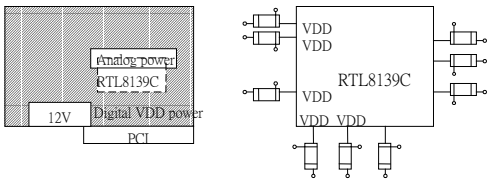


Separate Tx and Rx signal pairs

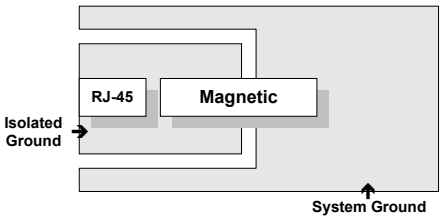
13. Magnetic: Any Magnetic with Tx/Rx turn ratios of 1:1/1:1 are suitable for the RTL8139C. Examples include Pulse PE68515/H1012, Valor ST6118, YCL 20PMT04, DELTA LF8221, BH16ST8515, TAIMIC HSIP-002.

4. Power and Ground Plane

1. 3.3V Power is used to support the RTL8139C, digital/PCI and other devices. Avoid using unnecessary power traces to the RTL8139C and keep these traces as short and wide as possible. If necessary, make good use of via. Keep the 3.3V power plane as a whole layer, and leave some space for the analog power plane.



Both the RJ-45 connector and the secondary side of the magnetic, which connects the RJ-45 connector, use their own isolated ground. No power and ground planes exist underneath this isolated area.



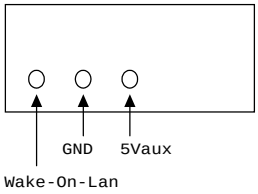
Isolate the RJ-45 connector ground from system ground

2. The digital ground plane can be separated from the analog ground plane. Partition of the GND plane needs experience and experimentation. The key point is to keep the analog ground return path about equal to the common GND. If necessary, the ground plane can remained unchanged, that is no partitioning at all.
3. For all partitions of the Power/GND plane, no right angles are recommend. This applies to the signal/power/bus traces as well.
4. Digital GND pins from the RTL8139C should use a via to the digital GND plane. Analog GND pins and Tx±/Rx± peripheral circuit GND pins should be connected to the analog GND plane.

Power/Ground Pins	**8139C**
Analog Power Pins	77,90,96
Digital Power Pins	1,12,25,35,46,58,59, 106,109,119
Analog GND Pins	74,80,85,93
Digital GND Pins	7,18,30,40,55,56,62, 111,112,113,124

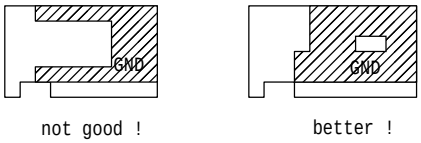
5. Special Design Notes

1. The GND side of the de-coupling capacitors at pins 58 and 109 must be kept as large as possible.
2. For EMI considerations, add two 0.1uF capacitors between system GND and chassis GND.
3. When implementing the Wake-On-LAN (WOL) or power management functions using a 5V (or 3.3V) auxiliary power supply, notice the 3-pin connector's pin-out and the capacitor connection at the input end of 5V-Vaux.



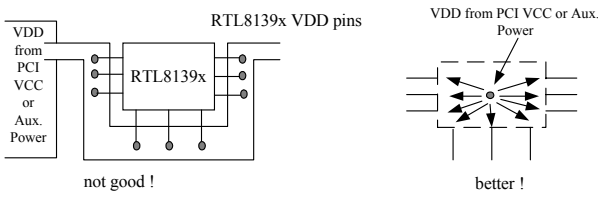
WOL Connector pin-out

4. For the WOL function, the 5V (or 3.3V) auxiliary power supply must provide at least 200mA current during the D3 cold/Power down mode.
5. The Schottky diode used on the WOL circuit should meet the following requirements:
   Rated current when on: at least 500mA
   Voltage drop when on: less than 0.3V
6. For better GND plane performance on 2-layer designs, it is recommended to keep the plane as large and uniform as possible. See example below.



Ground planes

7. For better power plane performance on 2-layer designs, it is recommended to use direct connections, rather than multiple smaller connections. See example below.



8. For better and more stable analog performance, refer to the following information:

a. The analog GND pins (74, 80, 84, 93) must maintain a good ground return path. This can be done by avoiding the use of a single ended ground, enlarging the analog GND plane, and by sending the analog circuit's return current back to the real GND (from PCI) as soon as possible. This is especially important in 2-layer designs.

b. If EMI is a problem during read/write from the PCI 33MHz interface, add some de-couple capacitors

(0.047uf, 22uf) between the system GND and the power planes.

c. During layout of the 25MHz OSC/crystal output to the RTL8139C, avoid coupling this signal to the adjustment power/GND traces. This can be done by making sure the traces do not run in parallel for longer distances.
d. When designing a LAN card, and including WOL functionality, the WOL connector on the card must match that used on the motherboard.
e. When using a 25Mhz crystal as the clock source, the specifications of the crystal are important. Please refer to the attached crystal specification. When using a crystal as specified two matching capacitors (27pf in the schematic) should be attached to the X1 and X2 pins.
f. When using an oscillator as the clock source (25Mhz), avoid attaching any capacitors to the clock trace.

6. RTL8139C(L) Issues:

1. Note that pin 85 is GND, pin 84 is RTSET.
2. All analog power pins (pins 77, 90, 96) need a ferrite bead and these pins should be de-coupled as the schematic file suggests. For pin 77, these beads should be placed as close to the RTL8139C as possible.
3. No GND plane partition is recommended. Please keep the GND plane as large and uniform as possible.
4. When using a regulator to perform the 5V → 3.3V conversion, the rated current of this regulator should be at least 300mA.
5. When using a transistor amplifier to perform the 5V → 3.3V conversion, the rated current and current gain should be considered so that the output can sustain a stable 3.3V source. Special attention should be paid on the effective current gain on this working point.
6. The capacitor parallel to the pull high termination (50 ohm) can be changed to suit different kinds of transformers of different inductance.
7. The center tape of the transmit pair of transformer needs to be pulled high, as noted in the schematic files.

Realtek Semiconductor Corp.

Headquarters
No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel : 886-3-5780211 Fax : 886-3-5776047
WWW: www.realtek.com.tw