

Q3

```
module signedmultiplier(output reg[7:0]out,input[3:0] a, b);
reg q;
reg [3:0]A;
reg [3:0]B;
always@(a,b)
begin
q=a[3];
out=b[3];
if(a[3]==1'b1)
begin
A[3]=a[3]^1'b1;
A[2]=a[2]^1'b1;
A[1]=a[1]^1'b1;
A[0]=a[0]^1'b1;
A=A+1'b1;
end
else
begin
A[3]=a[3];
A[2]=a[2];
A[1]=a[1];
A[0]=a[0];
end

if(b[3]==1'b1)
begin
B[3]=b[3]^1'b1;
B[2]=b[2]^1'b1;
B[1]=b[1]^1'b1;
B[0]=b[0]^1'b1;
```

```
B=B+1'b1;  
end  
else  
begin  
B[3]=b[3];  
B[2]=b[2];  
B[1]=b[1];  
B[0]=b[0];  
end  
end
```

```
reg [7:0] r;  
reg[2:0] i;  
always @(a,b)  
begin  
r=0;  
for(i=0;i<4;i=i+1)  
begin  
if(B[i]==1'b1)  
begin  
r = r+(A<<i);  
end  
end  
end
```

```
always@(a,b)  
begin  
if(a[3]==b[3])  
begin  
out[7]=r[7]^1'b0;  
out[6]=r[6]^1'b0;  
out[5]=r[5]^1'b0;  
out[4]=r[4]^1'b0;  
out[3]=r[3]^1'b0;
```

```
out[2]=r[2]^1'b0;  
out[1]=r[1]^1'b0;  
out[0]=r[0]^1'b0;
```

```
end  
else  
begin  
out[7]=r[7]^1'b1;  
out[6]=r[6]^1'b1;  
out[5]=r[5]^1'b1;  
out[4]=r[4]^1'b1;  
out[3]=r[3]^1'b1;  
out[2]=r[2]^1'b1;  
out[1]=r[1]^1'b1;  
out[0]=r[0]^1'b1;  
out=out+1'b1;
```

```
end  
end  
endmodule
```

TEST BENCH

```
module tb;  
wire [7:0]p;  
reg [3:0]a;  
reg [3:0]b;  
integer i;  
integer j;  
signedmultiplier M(p,a,b);  
initial  
begin  
for(i=0;i<16;i=i+1)
```

```
begin
for(j=0;j<16;j=j+1)
begin
#20
a=$random();
b=$random();
#20;
end
end
end
endmodule
```