8-bit register

```
module Q4a (D,clk,clr,pre,Q,Qnot);
parameter n=8;
input [n-1:0] D;
input clk,clr,pre;
output reg [n-1:0]Q,Qnot;
always @(negedge clr,negedge pre,posedge clk)
begin
if(!clr)
begin
if(!pre)
begin
Q<=1'bx;
Qnot=1'bx;
end
else
begin
Q<=0;
Qnot<=1;
end
end
else
begin
if(!pre)
begin
Q<=1;
Qnot<=0;
end
else
begin
Q<=D;
Qnot<=!D;
end
end
end
endmodule
```

test bench

```
module test;
reg [7:0]D;
reg  clk,clr,pre;
wire  reg [7:0]Q
wire Qnot;
Q4a ins( D,clk,clr,pre,Q,Qnot);
initial begin
D={8'b00000000};
repeat(100)begin
#10 D=D+{8'b00000001};
clk=$random();
clr=$random();pre=$random();
```

```
end
end
endmodule
```

8-bit register

```
module Q4b (D,clk,clr,pre,Q,Qnot);
parameter n=16;
input [n-1:0] D;
input clk,clr,pre;
output reg [n-1:0]Q,Qnot;

always @(negedge clr,negedge pre,posedge clk)
        begin
        if(!clr)
        begin
        if(!pre)
        begin
        Q<=1'bx;
        Qnot=1'bx;
        end
        else
        begin
        Q<=0;
        Qnot<=1;
        end
        end
        else
        begin
        if(!pre)
        begin
        Q<=1;
        Qnot<=0;
        end
        else
        begin
        Q<=D;
        Qnot<=!D;
        end
        end
        end
endmodule
```

test bench

```
module test;
reg [15:0]D;
reg  clk,clr,pre;
wire  reg [15:0]Q
wire Qnot;
Q4a ins( D,clk,clr,pre,Q,Qnot);
initial begin
```

```
D={8'b0000000000000000};
repeat(100)begin
#10 D=D+{8'b0000000000000001};
clk=$random();
clr=$random();pre=$random();
end
end
endmodule
```