BINSHADH BSHEER B210517CS Q2

Unclocked S-R latch

gate lavel

```
module assg3(output q,qn,input s,r);
nor n1(qn,s,q);
nor n2(q,r,qn);
endmodule
```

dataflow

```
module assg3(output q,qn,input s,r);
assign qn=~(s|q),q=~(qn|r);
endmodule
```

behavioural

```
module assg3(output reg q,qn,input s,r);
always@(s,r,q,qn)begin
qn<=~(q|s);
q<=~(qn|r);
end
endmodule
```

test_bench

```
module assg3_tb;
reg s,r;
wire q,qn;
assg3 ins(q,qn,s,r);
initial begin
#5 s=1; r=0;
#5 s=0;r=0;

#5 s=0;r=1;
#5 s=0;r=0;
#5 s=1;r=1;
#5 s=0;r=0;
#5 ;
end
endmodule
```

clocked sr latch

dataflow

```
module assg3(output q,qn,input s,r,e);
wire w1,w2;
```

```
assign w1=s&e,w2=r&e;
assign q=~(w2|qn),
qn=~(w1|q);
endmodule
```

gate lavel

```
module assg3(output q,qn,input s,r,e);
wire w1,w2;
and (w1,s,e);
and(w2,r,e);
nor(q,w2,qn);
nor(qn,w1,q);
endmodule
```

behavioural

```
module assg3(output reg q,qn,input s,r,e);
reg w1,w2;
always@(q,qn,s,r,e)
begin
 w1=s&e;w2=r&e;
 q<=~(w2|qn);
qn<=~(w1|q);
end
endmodule
```

test_bench

```
module assg3_tb;
reg s,r,e;
wire q,qn;
assg3 ins(q,qn,s,r,e);
initial begin
#5 e=1'b1;s=1'b1;r=1'b0;
#5 e=1'b1;s=1'b1;r=1'b1;
#5 e=1'b1;s=1'b0;r=1'b0;
#5 e=1'b1;s=1'b0;r=1'b1;
#5 e=1'b1;s=1'b0;r=1'b0;
#5 ;
end
endmodule
```