B210517CS BINSHADH BASHEER Q3

Clocked D latch with asynchronous preset and clear.

```
module assg3(input d,pre,set,e,output reg q1,q2);
always @(*)
begin
if(pre==1'b1)
begin
q1=1'b1;
q2=~q1;
end
else if(set==1'b1)
begin
q1=1'b0;
q2=~q1;
end
else if(d==1'b0&&e==1'b1)
begin
q1=1'b0;
q2=~q1;
end
else if(d==1'b1&&e==1'b1)
begin
q1=1'b1;
q2=~q1;
end
end
endmodule
```

test bench

```
module tb;
reg a,b,c,d;
wire q,w;
assg3 f(d,b,c,a,q,w);
initial begin
a=0;b=0;c=1;d=0;
#10 a=0;b=0;c=0;d=0;
#10 a=0;b=0;c=0;d=1;
#10 a=0;b=0;c=1;d=0;
#10 a=0;b=0;c=1;d=1;
#10 a=0;b=1;c=0;d=0;
#10 a=0;b=1;c=0;d=1;
//#10 a=0;b=1;c=1;d=0;
//#10 a=0;b=1;c=1;d=1;
#10 a=1;b=0;c=0;d=0;
#10 a=1;b=0;c=0;d=1;
#10 a=1;b=0;c=1;d=0;
#10 a=1;b=0;c=1;d=1;
#10 a=1;b=1;c=0;d=0;
```

```
#10 a=1;b=1;c=0;d=1;
//#10 a=1;b=1;c=1;d=0;
//#10 a=1;b=1;c=1;d=1;
end
endmodule
```

Clocked D latch with synchronous preset and clear.

```
module assg3(input d,pre,set,e,output reg q1,q2);
always @(*)
begin
if(pre==1'b1&&e==1'b1)
begin
q1=1'b1;
q2=~q1;
end
else if(set==1'b1&&e==1'b1)
begin
q1=1'b0;
q2=~q1;
end
else if(d==1'b0&&e==1'b1)
begin
q1=1'b0;
q2=~q1;
end
else if(d==1'b1&&e==1'b1)
begin
q1=1'b1;
q2=~q1;
end
end
endmodule
```

test bench

```
module tb;
reg a,b,c,d;
wire q,w;
assg3 f(d,b,c,a,q,w);
initial begin
a=1;b=1;c=0;d=0;
#10 a=0;b=0;c=0;d=0;
#10 a=0;b=0;c=0;d=1;
#10 a=0;b=0;c=1;d=0;
#10 a=0;b=0;c=1;d=1;
#10 a=0;b=1;c=0;d=0;
#10 a=0;b=1;c=0;d=1;
//#10 a=0;b=1;c=1;d=0;
```

```
//#10 a=0;b=1;c=1;d=1;
#10 a=1;b=0;c=0;d=0;
#10 a=1;b=0;c=0;d=1;
#10 a=1;b=0;c=1;d=0;
#10 a=1;b=0;c=1;d=1;
#10 a=1;b=1;c=0;d=0;
#10 a=1;b=1;c=0;d=1;
//#10 a=1;b=1;c=1;d=0;
//#10 a=1;b=1;c=1;d=1;
end
endmodule
```

D flip-flop with synchronous preset and clear.

```
 module dff(output reg q,input d,clk,sclr,spre);
always@(posedge clk )begin
if(sclr)
q<=1'b0;
else if(spre )
q<=1'b1;
else
q<=d;
end
endmodule
```

test bench

```
 module test;
reg  d,clk,sclr,spre;
wire q;
dff ins(q, d,clk,sclr,spre);
initial begin
{q, d,clk,sclr,spre}={5'b00000};
repeat(32)begin
#10 {q, d,clk,sclr,spre}={q, d,clk,sclr,spre}+{5'b00001};
end
end
endmodule
```

D flip-flop with asynchronous preset and clear

```
module dff(output reg q,input d,clk,aclr);
always@(posedge clk,posedge aclr )begin
if(aclr)
q<=1'b0;
else
q<=d;
end
endmodule
```

test bench

```
 module test;
reg  d,clk,aclr;
wire q;
dff ins(q, d,clk,aclr);
initial begin
{q, d,clk,aclr}={5'b0000};
repeat(32)begin
#10 {q, d,clk,aclr}={q, d,clk,aclr}+{5'b0001};
end
end
endmodule
```