BINSHADH BASHEER B210517CS

Q1

```
module conv(input [3:0] a,b,input clk,shift,output reg[3:0] d,output reg c);
reg [3:0] rg1, rg2;
reg w1,w2;
integer i;
initial
begin
i=1'b0;
c=1'b0;
end
always@(posedge clk)
begin
if(!shift)
begin
rg1<=a;
rg2<=b;
end
else
begin
w1=rg1[0];
w2=rg2[0];
rg1<={1'b0,rg1[3],rg1[2],rg1[1]};
rg2<={1'b0,rg2[3],rg2[2],rg2[1]};
{c,d[i]}=w1-w2-c;
i=i+1;
end
end
endmodule
```

TEST BENCH

```
module test;
wire [3:0]d;
wire c;
reg [3:0]a,b;
reg clk,shift;
conv ins(a,b,clk,shift,d,c);
initial begin
clk=1’b1;
shift=1’b0;
```

```
a=4’b0011;b=4’b1001;
#10 a=4’b0011; b=4’b1111;

#10 a=4’b1011;b=4’b1001;

#10 a=4’b0011;b=4’b1001;
end
endmodule
```